

PRELIMINARY
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 Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS
M37920S4CGP

16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37920S4CGP is a single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in 100-pin plastic molded QFP. This microcomputer supports the 7900 Series instruction set, which are enhanced and expanded instruction set and are upper-compatible with the 7700/7751 Series instruction set.

The CPU of this microcomputer is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Also, the bus interface unit of this microcomputer enhance the memory access efficiency to execute instructions fast. This microcomputer include the 4-channel DMA controller and the DRAM controller with enhanced fast page mode. Therefore, this microcomputer are suitable for office, business, and industrial equipment controller that require fast processing of large data.

- Instruction execution time
 The fastest instruction at 20 MHz frequency 50 ns
- Single power supply 5 V ± 0.5 V
- Interrupts 6 external sources, 17 internal sources, 7 levels
- Multi-functional 16-bit timer 5 + 3
- Serial I/O (UART or Clock synchronous) 2
- 10-bit A-D converter 4-channel inputs
- DMA controller 4-channels
- DRAM controller
- Real-time output
 4 bits × 2 channels, or 6 bits × 1 channel + 2 bits × 1 channel
- 12-bit watchdog timer
- Programmable input/output (ports P2–P9, P12) 49

DISTINCTIVE FEATURES

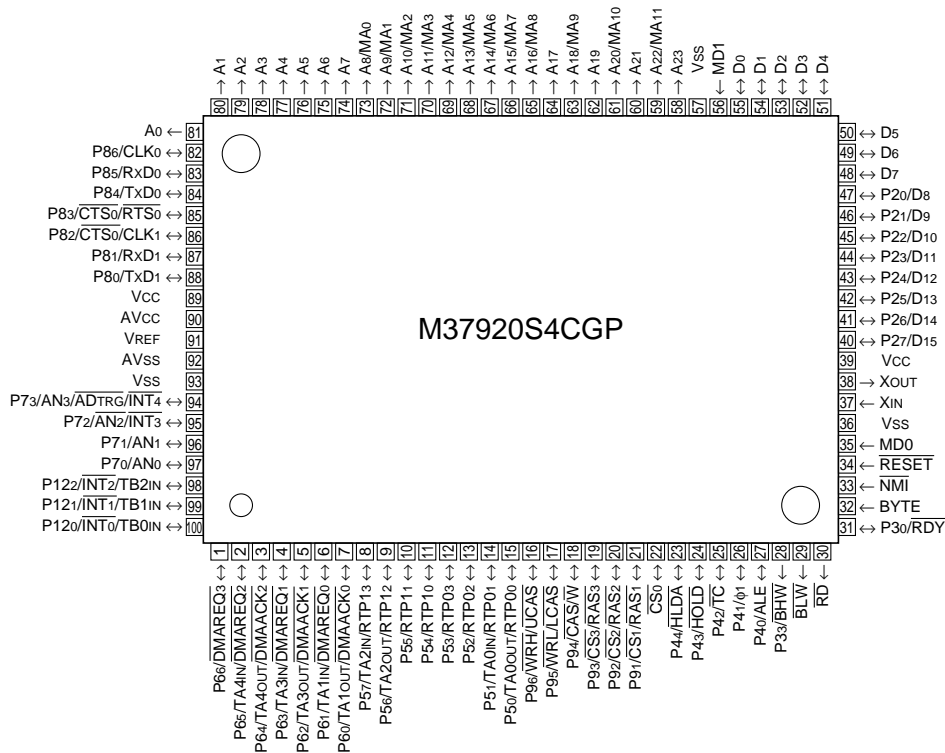
<Microcomputer mode>

- Number of basic machine instructions 203
- Memory
 RAM 2048 bytes
 ROM External

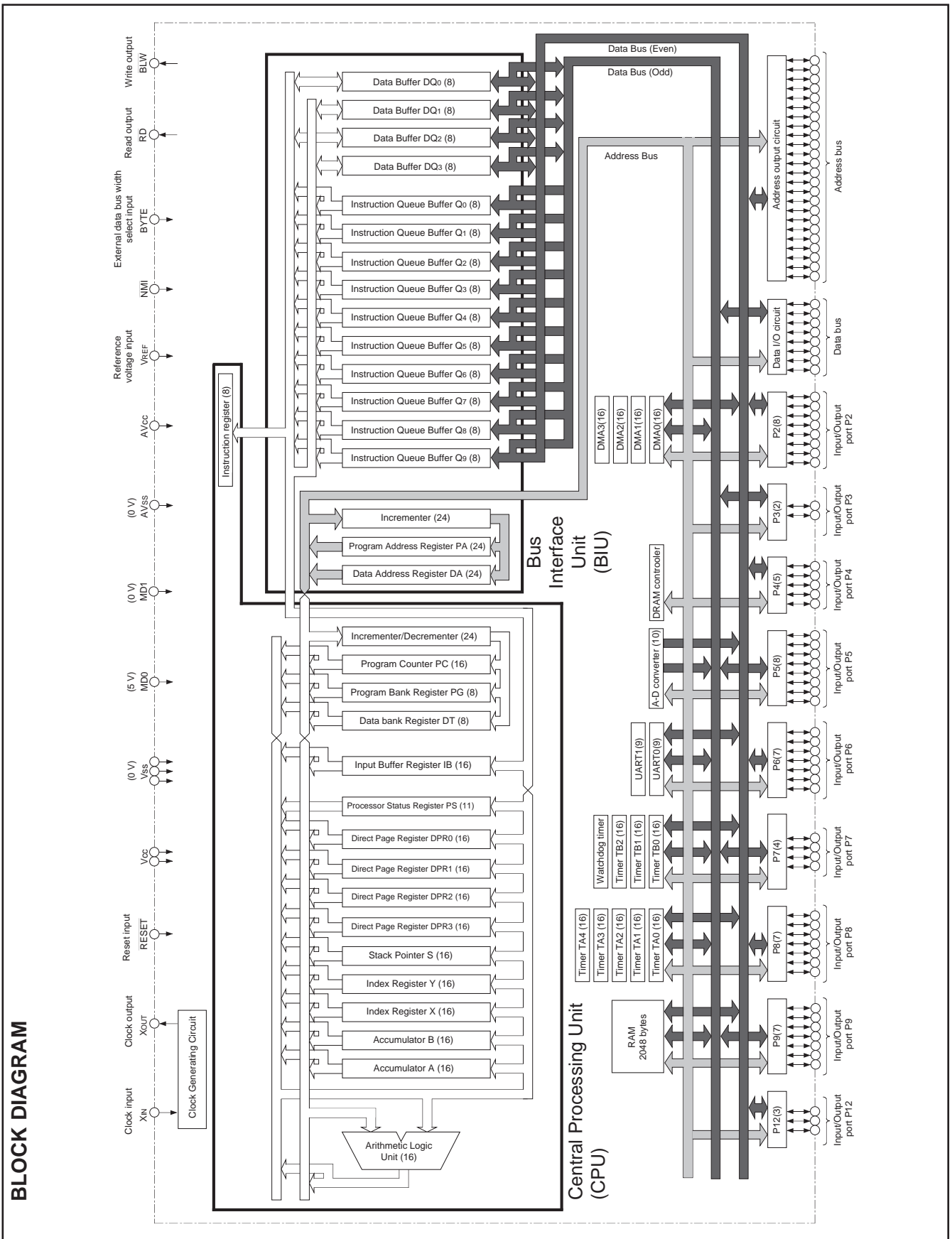
APPLICATION

Telecommunications equipment such as copiers, printers, typewriters, facsimiles, optical disk drives, HDD, mobile radio communication equipment, ISDN terminals
 Control devices for office automation equipment such as personal computers

M37920S4CGP PIN CONFIGURATION (TOP VIEW)



Outline 100P6S-A



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FUNCTIONS (Microcomputer mode)

| Parameter | | Functions |
|--|--------------------------------|--|
| Number of basic machine instructions | | 203 |
| Instruction execution time | | 50 ns (the fastest instruction at $f(X_{IN}) = 20$ MHz) |
| External clock input frequency $f(X_{IN})$ | | 20 MHz (Max.) |
| Memory size | ROM | External |
| | RAM | 2048 bytes |
| Programmable input/output ports | P2, P5 | 8-bit X 2 |
| | P3 | 2-bit X 1 |
| | P4 | 5-bit X 1 |
| | P6, P8 | 7-bit X 2 |
| | P7 | 4-bit X 1 |
| | P9 | 6-bit X 1 |
| | P12 | 3-bit X 1 |
| Multi-functional timers | TA0–TA4 | 16-bit X 5 |
| | TB0–TB2 | 16-bit X 3 |
| Serial I/O | UART0 and UART1 | (UART or Clock synchronous serial I/O) X 2 |
| A-D converter | | 10-bit successive approximation method X 1 (4 channels) |
| Watchdog timer | | 12-bit X 1 |
| DMA controller | | 4 channels Maximum transfer rate 20 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 1-bus cycle transfer) 10 Mbytes/sec. (at $f(X_{IN}) = 20$ MHz, 0 wait, 2-bus cycles transfer) |
| DRAM controller | | 1 channel Supports fast page access mode. Incorporates 8-bit refresh timer. Supports \overline{CAS} before \overline{RAS} refresh method or self refresh method. |
| Chip-select wait control | | Chip select area X 4 (\overline{CS}_0 – \overline{CS}_3). A wait number and bus width can be set for each chip select area. |
| Real-time output | | 4 bits X 2 channels; or 6 bits X 1 channel + 2 bits X 1 channel |
| Interrupts | | 6 external types, 17 internal types. Each interrupt except \overline{NMI} can be set to a priority level within the range of 0–7 by software. |
| Clock generating circuit | | Built-in (externally connected to a ceramic resonator or quartz crystal resonator). |
| Power supply voltage | | 5 V \pm 10 % |
| Power dissipation | | 135 mW (at $f(X_{IN}) = 20$ MHz, typ.) |
| Ports' input/output characteristics | Input/Output withstand voltage | 5 V |
| | Output current | 5 mA |
| Memory expansion | | Up to 16 Mbytes. Note that bank FF16 is a reserved area. |
| Operating temperature range | | –20 to 85 °C |
| Device structure | | CMOS high-performance silicon gate process |
| Package | | 100-pin plastic molded QFP |

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PIN DESCRIPTION (Microcomputer mode)

| Pin | Name | Input/ Output | Functions |
|--|---------------------------------------|--|---|
| Vcc, Vss | Power supply input | — | Apply 5 V±10 % to Vcc, and 0 V to Vss. |
| MD0 | MD0 | Input | This pin controls the processor mode. Connect this pin to Vcc. |
| MD1 | MD1 | Input | Connect this pin to Vss. |
| $\overline{\text{RESET}}$ | Reset input | Input | The microcomputer is reset when "L" level is applied to this pin. |
| XIN | Clock input | Input | These are input and output pins of the internal clock generating circuit. Connect a ceramic or quartz- crystal resonator between the XIN and XOUT pins. When an external clock is used, the clock source should be connected to the XIN pin, and the XOUT pin should be left open. |
| XOUT | Clock output | Output | |
| BYTE | External data bus width select input | Input | This pin determines whether the external data bus has an 8-bit width or 16-bit width for the memory expansion mode or microprocessor mode. The width is 16 bits when "L" signal is input, and 8 bits when "H" signal is input. |
| AVcc, AVss | Analog power supply input | — | Power supply input pin for the A-D converter. Connect AVcc to Vcc, and AVss to Vss externally. |
| VREF | Reference voltage input | Input | This is the reference voltage input pin for the A-D converter. |
| A0–A7 | Low-order address | Output | The low-order 8 bits of address (A0–A7) are output. |
| A8–A15/ MA0–MA7 | Middle-order address/ DRAM address | Output | The middle-order 8 bits of address (A8–A15) are input/output. While DRAM space is accessed, multiplexed address (MA0–MA7) is output. |
| A16–A23/ MA8–MA11 | High-order address/ DRAM address | Output | The high-order 8 bits of address (A16–A23) are output. While DRAM space is accessed, multiplexed address (MA8–MA11) is output. |
| D0–D7 | Low-order data | I/O | The low-order 8 bits of data (D0–D7) are input/output. |
| P20/D8– P27/D15 | I/O port P2/ High-order data | I/O | <ul style="list-style-type: none"> ■ When 8-bit external data bus is used (BYTE = "H" level) Port P2 is an 8-bit I/O port. ■ When 16-bit external data bus is used (BYTE = "L" level) The high-order 8 bits (D8–D15) are input/output. |
| P30/ $\overline{\text{RDY}}$, $\overline{\text{RD}}$, $\overline{\text{BLW}}$, P33/ $\overline{\text{BHW}}$ | Memory control signal I/O | Input Output Output Output | <p>While the input level at pin $\overline{\text{RDY}}$ is "L", the microcomputer is placed in the ready state. While pin $\overline{\text{RD}}$ is at "L" level, the microcomputer reads out data and instruction codes. Also, pin $\overline{\text{RDY}}$ can function as a programmable I/O port pin (P30) by software.</p> <ul style="list-style-type: none"> ■ When 8-bit external data bus is used (BYTE = "H" level) While pin $\overline{\text{BLW}}$ is at "L" level, the microcomputer writes data. ■ When 16-bit external data bus is used (BYTE = "L" level) While pin $\overline{\text{BLW}}$ is at "L" level, the microcomputer writes data into an even-numbered address. While pin $\overline{\text{BHW}}$ is at "L" level, the microcomputer writes data into an odd-numbered address. |
| P40/ALE, P41/ ϕ_1 , P42/ $\overline{\text{TC}}$, P43/ $\overline{\text{HOLD}}$, P44/ $\overline{\text{HLDA}}$ | I/O port P4 | Output Output I/O Input Output | Signal ALE is used to latch an address. ϕ_1 has the same period as internal clock ϕ . Pin P42 functions as a programmable I/O port pin. While the input level at pin $\overline{\text{HOLD}}$ is at "L" level, the microcomputer is placed in the hold state. Signal $\overline{\text{HLDA}}$ is used to inform the external that the microcomputer enters the hold state. By software, pin ALE, clock ϕ_1 output pin, and pins $\overline{\text{HOLD}}$, $\overline{\text{HLDA}}$ function as programmable I/O port pins (P40, P41, P43, P44). Pin P42 also functions as pin $\overline{\text{TC}}$. |
| P50–P57 | I/O port P5 | I/O | Port P5 is an 8-bit I/O port. These pins also function as I/O pins for timers A0, A2, and pulse output pins for the real-time output. |
| P60–P66 | I/O port P6 | I/O | Port P6 is a 7-bit I/O port. These pins also function as I/O pins for timers A1, A3, A4, input pins for DMA requests, and output pins for DMA acknowledge signals. |

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| Pin | Name | Input/ Output | Functions |
|--------------------------|------------------------|------------------|--|
| P70–P73 | I/O port P7 | I/O | Port P7 is a 4-bit I/O port. P72 and P73 also function as input pins for $\overline{\text{INT}}_3$ and $\overline{\text{INT}}_4$. According to the software setting, these pins also function as input pins for the A-D converter. |
| P80–P86 | I/O port P8 | I/O | Port P8 is a 7-bit I/O port. These pins also function as I/O pins for UART0, UART1. |
| $\overline{\text{CS}}_0$ | Chip-select output | Output | This is an output pin for $\overline{\text{CS}}_0$. |
| P91–P96 | I/O port P9 | I/O | Port P9 is a 6-bit I/O port. According to the software setting, P91–P93 also function as chip select output pins. While DRAM space is selected, P94–P96 function as output pins for DRAM control signals. |
| P120–P122 | I/O port P12 | I/O | Port P12 is a 3-bit I/O port. These pins also function as input pins for $\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, $\overline{\text{INT}}_2$. According to software setting, these pins also function as input pins for timers B0–B2. |
| $\overline{\text{NMI}}$ | Non-maskable interrupt | Input | This pin is for a non-maskable interrupt. |

BASIC FUNCTION BLOCKS

The M37920S4CGP is the same functions as the M37920F8CGP except for the following.

Therefore, refer to the datasheet of the M37920F8CGP.

- The M37920S4CGP does not include the internal flash memory.
- The M37920S4CGP operates only in the microprocessor mode.
- The M37920S4CGP does not have the flash memory control register (address 9E16).
- Some of programmable I/O ports of the M37920S4CGP differ from those of the M37920FGCGP.

MEMORY

Figure 1 shows the memory map.

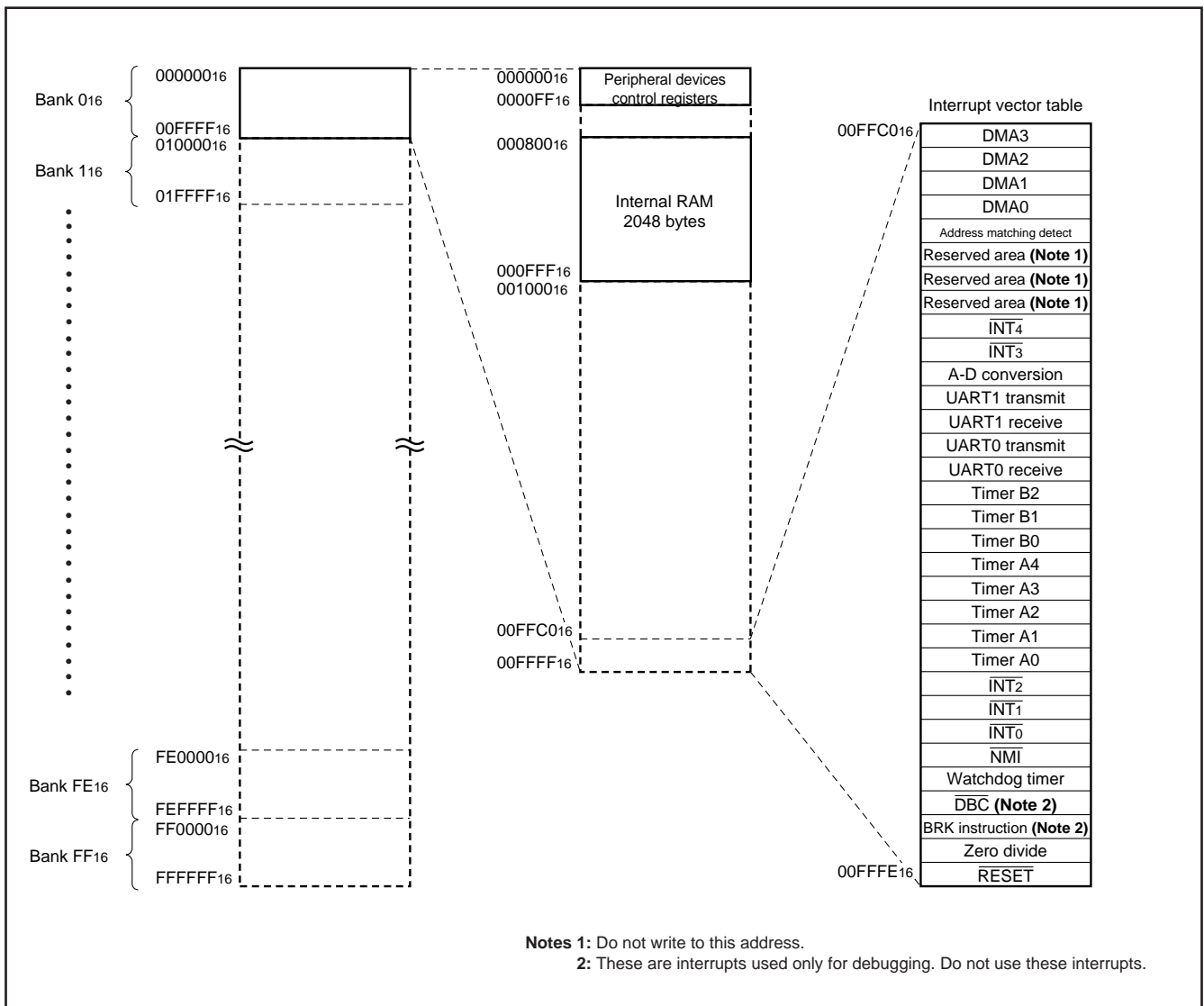


Fig. 1 Memory map

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| Address (Hexadecimal notation) | Address (Hexadecimal notation) |
|--------------------------------|---|
| 000000 ¹⁶ | Reserved area (Note 1) |
| 000001 ¹⁶ | Reserved area (Note 1) |
| 000002 ¹⁶ | [Port P0 register] (Note 2) |
| 000003 ¹⁶ | [Port P1 register] (Note 2) |
| 000004 ¹⁶ | [Port P0 direction register] (Note 2) |
| 000005 ¹⁶ | [Port P1 direction register] (Note 2) |
| 000006 ¹⁶ | Port P2 register |
| 000007 ¹⁶ | Port P3 register |
| 000008 ¹⁶ | Port P2 direction register |
| 000009 ¹⁶ | Port P3 direction register |
| 00000A ¹⁶ | Port P4 register |
| 00000B ¹⁶ | Port P5 register |
| 00000C ¹⁶ | Port P4 direction register |
| 00000D ¹⁶ | Port P5 direction register |
| 00000E ¹⁶ | Port P6 register |
| 00000F ¹⁶ | Port P7 register |
| 000010 ¹⁶ | Port P6 direction register |
| 000011 ¹⁶ | Port P7 direction register |
| 000012 ¹⁶ | Port P8 register |
| 000013 ¹⁶ | Port P9 register |
| 000014 ¹⁶ | Port P8 direction register |
| 000015 ¹⁶ | Port P9 direction register |
| 000016 ¹⁶ | [Port P10 register] (Note 2) |
| 000017 ¹⁶ | [Port P11 register] (Note 2) |
| 000018 ¹⁶ | [Port P10 direction register] (Note 2) |
| 000019 ¹⁶ | [Port P11 direction register] (Note 2) |
| 00001A ¹⁶ | Port P12 register |
| 00001B ¹⁶ | |
| 00001C ¹⁶ | Port P12 direction register |
| 00001D ¹⁶ | |
| 00001E ¹⁶ | A-D control register 0 |
| 00001F ¹⁶ | A-D control register 1 |
| 000020 ¹⁶ | A-D register 0 |
| 000021 ¹⁶ | |
| 000022 ¹⁶ | A-D register 1 |
| 000023 ¹⁶ | |
| 000024 ¹⁶ | A-D register 2 |
| 000025 ¹⁶ | |
| 000026 ¹⁶ | A-D register 3 |
| 000027 ¹⁶ | |
| 000028 ¹⁶ | |
| 000029 ¹⁶ | |
| 00002A ¹⁶ | |
| 00002B ¹⁶ | |
| 00002C ¹⁶ | |
| 00002D ¹⁶ | |
| 00002E ¹⁶ | |
| 00002F ¹⁶ | |
| 000030 ¹⁶ | UART0 transmit/receive mode register |
| 000031 ¹⁶ | UART0 baud rate register (BRG0) |
| 000032 ¹⁶ | UART0 transmit buffer register |
| 000033 ¹⁶ | |
| 000034 ¹⁶ | UART0 transmit/receive control register 0 |
| 000035 ¹⁶ | UART0 transmit/receive control register 1 |
| 000036 ¹⁶ | |
| 000037 ¹⁶ | UART0 receive buffer register |
| 000038 ¹⁶ | |
| 000039 ¹⁶ | UART1 transmit/receive mode register |
| 00003A ¹⁶ | UART1 baud rate register (BRG1) |
| 00003B ¹⁶ | UART1 transmit buffer register |
| 00003C ¹⁶ | |
| 00003D ¹⁶ | UART1 transmit/receive control register 0 |
| 00003E ¹⁶ | UART1 transmit/receive control register 1 |
| 00003F ¹⁶ | UART1 receive buffer register |
| 000040 ¹⁶ | Count start register |
| 000041 ¹⁶ | |
| 000042 ¹⁶ | One-shot start register |
| 000043 ¹⁶ | |
| 000044 ¹⁶ | Up-down register |
| 000045 ¹⁶ | Timer A clock division select register |
| 000046 ¹⁶ | Timer A0 register |
| 000047 ¹⁶ | |
| 000048 ¹⁶ | Timer A1 register |
| 000049 ¹⁶ | |
| 00004A ¹⁶ | Timer A2 register |
| 00004B ¹⁶ | |
| 00004C ¹⁶ | Timer A3 register |
| 00004D ¹⁶ | |
| 00004E ¹⁶ | Timer A4 register |
| 00004F ¹⁶ | |
| 000050 ¹⁶ | Timer B0 register |
| 000051 ¹⁶ | |
| 000052 ¹⁶ | Timer B1 register |
| 000053 ¹⁶ | |
| 000054 ¹⁶ | Timer B2 register |
| 000055 ¹⁶ | |
| 000056 ¹⁶ | Timer A0 mode register |
| 000057 ¹⁶ | Timer A1 mode register |
| 000058 ¹⁶ | Timer A2 mode register |
| 000059 ¹⁶ | Timer A3 mode register |
| 00005A ¹⁶ | Timer A4 mode register |
| 00005B ¹⁶ | Timer B0 mode register |
| 00005C ¹⁶ | Timer B1 mode register |
| 00005D ¹⁶ | Timer B2 mode register |
| 00005E ¹⁶ | Processor mode register 0 |
| 00005F ¹⁶ | Processor mode register 1 |
| 000060 ¹⁶ | Watchdog timer register |
| 000061 ¹⁶ | Watchdog timer frequency select register |
| 000062 ¹⁶ | Particular function select register 0 |
| 000063 ¹⁶ | Particular function select register 1 |
| 000064 ¹⁶ | Particular function select register 2 |
| 000065 ¹⁶ | Reserved area (Note 1) |
| 000066 ¹⁶ | Debug control register 0 |
| 000067 ¹⁶ | Debug control register 1 |
| 000068 ¹⁶ | |
| 000069 ¹⁶ | Address comparison register 0 |
| 00006A ¹⁶ | |
| 00006B ¹⁶ | |
| 00006C ¹⁶ | Address comparison register 1 |
| 00006D ¹⁶ | |
| 00006E ¹⁶ | INT ₃ interrupt control register |
| 00006F ¹⁶ | INT ₄ interrupt control register |
| 000070 ¹⁶ | A-D conversion interrupt control register |
| 000071 ¹⁶ | UART0 transmit interrupt control register |
| 000072 ¹⁶ | UART0 receive interrupt control register |
| 000073 ¹⁶ | UART1 transmit interrupt control register |
| 000074 ¹⁶ | UART1 receive interrupt control register |
| 000075 ¹⁶ | Timer A0 interrupt control register |
| 000076 ¹⁶ | Timer A1 interrupt control register |
| 000077 ¹⁶ | Timer A2 interrupt control register |
| 000078 ¹⁶ | Timer A3 interrupt control register |
| 000079 ¹⁶ | Timer A4 interrupt control register |
| 00007A ¹⁶ | Timer B0 interrupt control register |
| 00007B ¹⁶ | Timer B1 interrupt control register |
| 00007C ¹⁶ | Timer B2 interrupt control register |
| 00007D ¹⁶ | INT ₀ interrupt control register |
| 00007E ¹⁶ | INT ₁ interrupt control register |
| 00007F ¹⁶ | INT ₂ interrupt control register |

Notes 1: Do not read/write to this address.

2: These registers are used in the bus fixation of the power saving function. For details, refer to the section on the power saving function of the M37920F8CGP datasheet.

Fig. 2 Location of peripheral devices' control registers (1)

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| Address (Hexadecimal notation) | | Address (Hexadecimal notation) | |
|--------------------------------|---|--------------------------------|----------------------------------|
| 000080 ¹⁶ | CS ₀ control register L | 0000C0 ¹⁶ | Source address register 0 L |
| 000081 ¹⁶ | CS ₀ control register H | 0000C1 ¹⁶ | Source address register 0 M |
| 000082 ¹⁶ | CS ₁ control register L | 0000C2 ¹⁶ | Source address register 0 H |
| 000083 ¹⁶ | CS ₁ control register H | 0000C3 ¹⁶ | |
| 000084 ¹⁶ | CS ₂ control register L | 0000C4 ¹⁶ | Destination address register 0 L |
| 000085 ¹⁶ | CS ₂ control register H | 0000C5 ¹⁶ | Destination address register 0 M |
| 000086 ¹⁶ | CS ₃ control register L | 0000C6 ¹⁶ | Destination address register 0 H |
| 000087 ¹⁶ | CS ₃ control register H | 0000C7 ¹⁶ | |
| 000088 ¹⁶ | | 0000C8 ¹⁶ | Transfer counter register 0 L |
| 000089 ¹⁶ | | 0000C9 ¹⁶ | Transfer counter register 0 M |
| 00008A ¹⁶ | Area CS ₀ start address register | 0000CA ¹⁶ | Transfer counter register 0 H |
| 00008B ¹⁶ | | 0000CB ¹⁶ | |
| 00008C ¹⁶ | Area CS ₁ start address register | 0000CC ¹⁶ | DMA0 mode register L |
| 00008D ¹⁶ | | 0000CD ¹⁶ | DMA0 mode register H |
| 00008E ¹⁶ | Area CS ₂ start address register | 0000CE ¹⁶ | DMA0 control register |
| 00008F ¹⁶ | | 0000CF ¹⁶ | |
| 000090 ¹⁶ | Area CS ₃ start address register | 0000D0 ¹⁶ | Source address register 1 L |
| 000091 ¹⁶ | | 0000D1 ¹⁶ | Source address register 1 M |
| 000092 ¹⁶ | | 0000D2 ¹⁶ | Source address register 1 H |
| 000093 ¹⁶ | | 0000D3 ¹⁶ | |
| 000094 ¹⁶ | | 0000D4 ¹⁶ | Destination address register 1 L |
| 000095 ¹⁶ | | 0000D5 ¹⁶ | Destination address register 1 M |
| 000096 ¹⁶ | | 0000D6 ¹⁶ | Destination address register 1 H |
| 000097 ¹⁶ | | 0000D7 ¹⁶ | |
| 000098 ¹⁶ | | 0000D8 ¹⁶ | Transfer counter register 1 L |
| 000099 ¹⁶ | | 0000D9 ¹⁶ | Transfer counter register 1 M |
| 00009A ¹⁶ | | 0000DA ¹⁶ | Transfer counter register 1 H |
| 00009B ¹⁶ | | 0000DB ¹⁶ | |
| 00009C ¹⁶ | Reserved area (Note 1) | 0000DC ¹⁶ | DMA1 mode register L |
| 00009D ¹⁶ | Reserved area (Note 1) | 0000DD ¹⁶ | DMA1 mode register H |
| 00009E ¹⁶ | Reserved area (Note 1) | 0000DE ¹⁶ | DMA1 control register |
| 00009F ¹⁶ | | 0000DF ¹⁶ | |
| 0000A0 ¹⁶ | Real-time output control register | 0000E0 ¹⁶ | Source address register 2 L |
| 0000A1 ¹⁶ | | 0000E1 ¹⁶ | Source address register 2 M |
| 0000A2 ¹⁶ | Pulse output data register 0 | 0000E2 ¹⁶ | Source address register 2 H |
| 0000A3 ¹⁶ | | 0000E3 ¹⁶ | |
| 0000A4 ¹⁶ | Pulse output data register 1 | 0000E4 ¹⁶ | Destination address register 2 L |
| 0000A5 ¹⁶ | | 0000E5 ¹⁶ | Destination address register 2 M |
| 0000A6 ¹⁶ | Reserved area (Note 1) | 0000E6 ¹⁶ | Destination address register 2 H |
| 0000A7 ¹⁶ | | 0000E7 ¹⁶ | |
| 0000A8 ¹⁶ | DRAM control register | 0000E8 ¹⁶ | Transfer counter register 2 L |
| 0000A9 ¹⁶ | Refresh timer | 0000E9 ¹⁶ | Transfer counter register 2 M |
| 0000AA ¹⁶ | | 0000EA ¹⁶ | Transfer counter register 2 H |
| 0000AB ¹⁶ | | 0000EB ¹⁶ | |
| 0000AC ¹⁶ | CTS/RTS separate select register | 0000EC ¹⁶ | DMA2 mode register L |
| 0000AD ¹⁶ | | 0000ED ¹⁶ | DMA2 mode register H |
| 0000AE ¹⁶ | | 0000EE ¹⁶ | DMA2 control register |
| 0000AF ¹⁶ | | 0000EF ¹⁶ | |
| 0000B0 ¹⁶ | DMAC control register L | 0000F0 ¹⁶ | Source address register 3 L |
| 0000B1 ¹⁶ | DMAC control register H | 0000F1 ¹⁶ | Source address register 3 M |
| 0000B2 ¹⁶ | DMA0 interrupt control register | 0000F2 ¹⁶ | Source address register 3 H |
| 0000B3 ¹⁶ | DMA1 interrupt control register | 0000F3 ¹⁶ | |
| 0000B4 ¹⁶ | DMA2 interrupt control register | 0000F4 ¹⁶ | Destination address register 3 L |
| 0000B5 ¹⁶ | DMA3 interrupt control register | 0000F5 ¹⁶ | Destination address register 3 M |
| 0000B6 ¹⁶ | | 0000F6 ¹⁶ | Destination address register 3 H |
| 0000B7 ¹⁶ | | 0000F7 ¹⁶ | |
| 0000B8 ¹⁶ | | 0000F8 ¹⁶ | Transfer counter register 3 L |
| 0000B9 ¹⁶ | | 0000F9 ¹⁶ | Transfer counter register 3 M |
| 0000BA ¹⁶ | | 0000FA ¹⁶ | Transfer counter register 3 H |
| 0000BB ¹⁶ | | 0000FB ¹⁶ | |
| 0000BC ¹⁶ | Reserved area (Note 1) | 0000FC ¹⁶ | DMA3 mode register L |
| 0000BD ¹⁶ | Reserved area (Note 1) | 0000FD ¹⁶ | DMA3 mode register H |
| 0000BE ¹⁶ | Reserved area (Note 1) | 0000FE ¹⁶ | DMA3 control register |
| 0000BF ¹⁶ | Reserved area (Note 1) | 0000FF ¹⁶ | |

Note 1: Do not read/write to this address.

Fig. 3 Location of peripheral devices' control registers (2)

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Processor mode

The M37920S4CGP operates only in the microprocessor mode exclusive for the external ROM. Be sure to fix the level at pin MD0 to Vcc and the level at pin MD1 to Vss. Also, be sure to fix bits 1, 0 at address 5E16 (the processor mode register 0) to "1" and "0", respectively.

Microprocessor mode

When the microcomputer starts its operation after reset with the level at pin MD0 = Vcc level (5 V), the microcomputer is placed in the microprocessor mode.

Table 1. Relationship between pins MD0, MD1 and processor mode

| Pin MD0 | Pin MD1 | Processor mode |
|--------------------|--------------------|--|
| Vcc level (5 V) | Vss level (5 V) | After reset, the microcomputer starts its operation in the microprocessor mode. (Be sure to pin MD0 to Vcc level.) |

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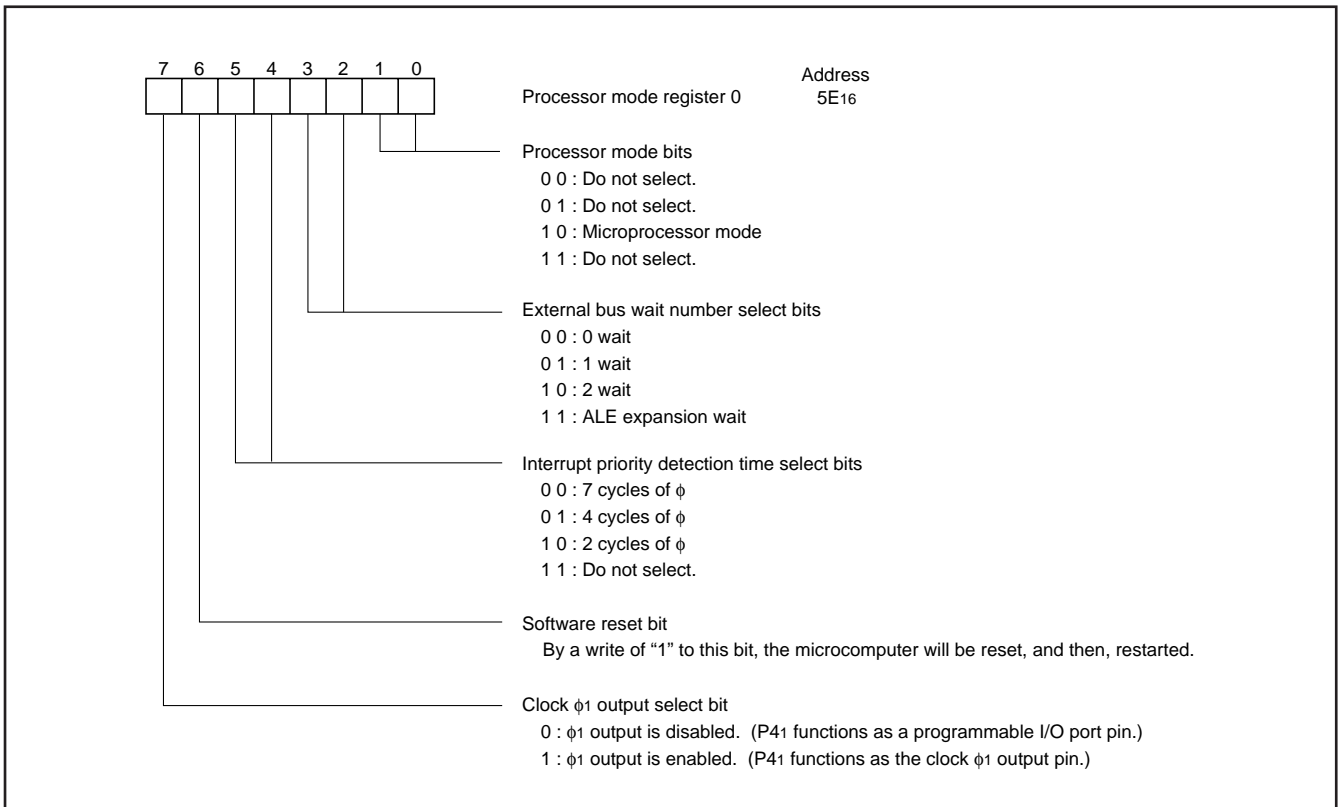


Fig. 4 Processor mode register 0's bit configuration

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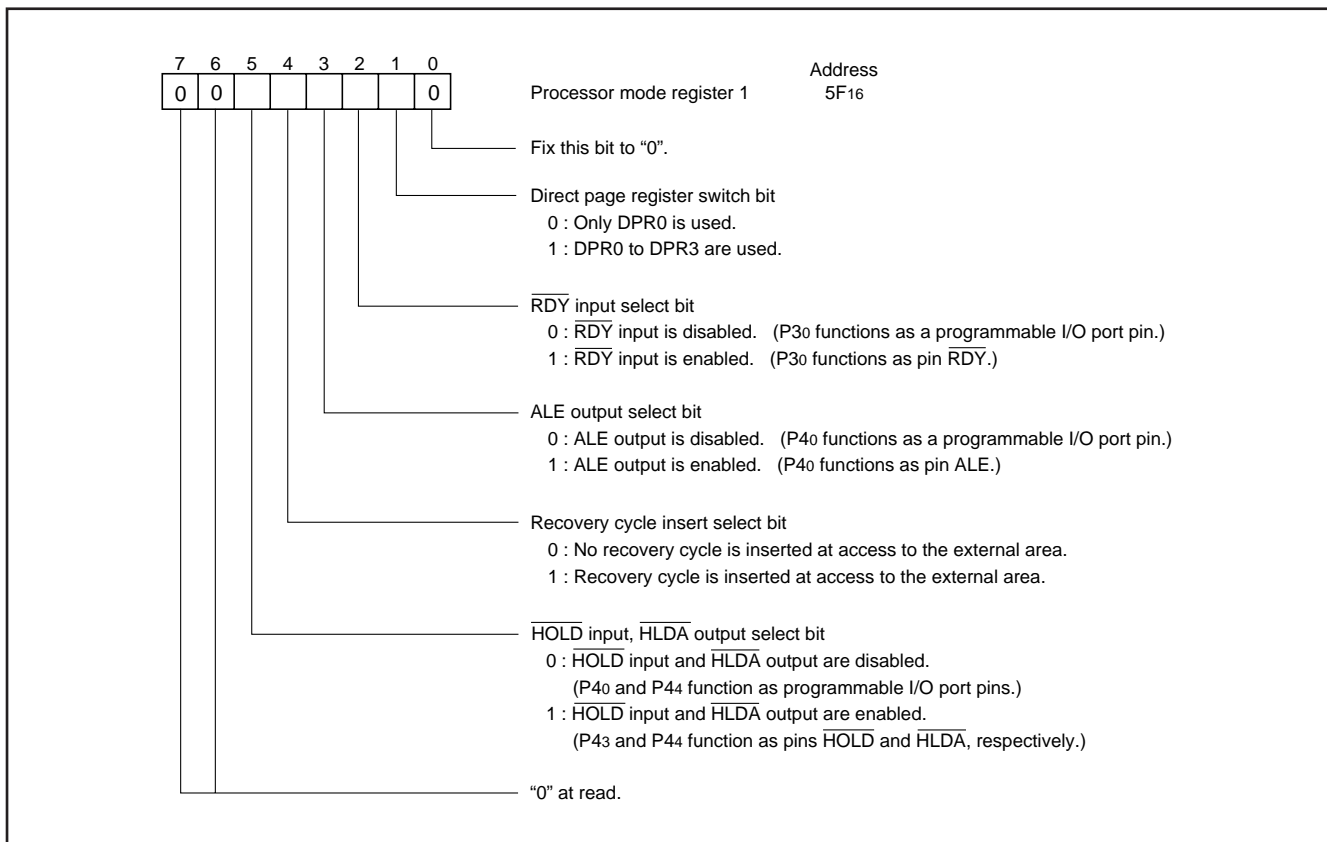


Fig. 5 Processor mode register 1's bit configuration

| | Address | | Address | |
|--|------------------------|------------------|--|--|
| Port P0 direction register | (04 ₁₆)... | 00 ₁₆ | Processor mode register 0 | (5E ₁₆)... <small>Note 2</small> 0 0 0 1 0 <small>Note 2</small> 0 |
| Port P1 direction register | (05 ₁₆)... | 00 ₁₆ | Processor mode register 1 | (5F ₁₆)... 0 0 (Note 2) 0 0 |
| Port P2 direction register | (08 ₁₆)... | 00 ₁₆ | Watchdog timer | (60 ₁₆)... FFF ₁₆ |
| Port P3 direction register | (09 ₁₆)... | XXXXXXXX0000 | Watchdog timer frequency select register | (61 ₁₆)... XXXXXXXX0 |
| Port P4 direction register | (0C ₁₆)... | XXXXXXXX0000 | Particular function select register 0 | (62 ₁₆)... XXXXXXXX00 |
| Port P5 direction register | (0D ₁₆)... | 00 ₁₆ | Particular function select register 1 | (63 ₁₆)... XXXXXXX00 (Note 3) |
| Port P6 direction register | (10 ₁₆)... | X0000000 | Debug control register 0 | (66 ₁₆)... 1 (Note 3) |
| Port P7 direction register | (11 ₁₆)... | XXXXXXXX0000 | Debug control register 1 | (67 ₁₆)... 000 <small>Note 3</small> 000 <small>Note 3</small> |
| Port P8 direction register | (14 ₁₆)... | X0000000 | $\overline{\text{INT}}_3$ interrupt control register | (6E ₁₆)... XXXXXXX000 |
| Port P9 direction register | (15 ₁₆)... | X0000000 | $\overline{\text{INT}}_4$ interrupt control register | (6F ₁₆)... XXXXXXX000 |
| Port P10 direction register | (18 ₁₆)... | 00 ₁₆ | A-D conversion interrupt control register | (70 ₁₆)... XXXXXXX?000 |
| Port P11 direction register | (19 ₁₆)... | 00 ₁₆ | UART 0 transmit interrupt control register | (71 ₁₆)... XXXXXXX000 |
| Port P12 direction register | (1C ₁₆)... | XXXXXXXX000 | UART 0 receive interrupt control register | (72 ₁₆)... XXXXXXX000 |
| A-D control register 0 | (1E ₁₆)... | 00000??? | UART 1 transmit interrupt control register | (73 ₁₆)... XXXXXXX000 |
| A-D control register 1 | (1F ₁₆)... | X0000001 | UART 1 receive interrupt control register | (74 ₁₆)... XXXXXXX000 |
| UART 0 Transmit/Receive mode register | (30 ₁₆)... | 00 ₁₆ | Timer A0 interrupt control register | (75 ₁₆)... XXXXXXX000 |
| UART 1 Transmit/Receive mode register | (38 ₁₆)... | 00 ₁₆ | Timer A1 interrupt control register | (76 ₁₆)... XXXXXXX000 |
| UART 0 Transmit/Receive control register 0 | (34 ₁₆)... | 00001000 | Timer A2 interrupt control register | (77 ₁₆)... XXXXXXX000 |
| UART 1 Transmit/Receive control register 0 | (3C ₁₆)... | 00001000 | Timer A3 interrupt control register | (78 ₁₆)... XXXXXXX000 |
| UART 0 Transmit/Receive control register 1 | (35 ₁₆)... | 00000010 | Timer A4 interrupt control register | (79 ₁₆)... XXXXXXX000 |
| UART 1 Transmit/Receive control register 1 | (3D ₁₆)... | 00000010 | Timer B0 interrupt control register | (7A ₁₆)... XXXXXXX000 |
| Count start register | (40 ₁₆)... | 00 ₁₆ | Timer B1 interrupt control register | (7B ₁₆)... XXXXXXX000 |
| One-shot start register | (42 ₁₆)... | 0XXXX000 | Timer B2 interrupt control register | (7C ₁₆)... XXXXXXX000 |
| Up-down register | (44 ₁₆)... | 00000000 | $\overline{\text{INT}}_0$ interrupt control register | (7D ₁₆)... XX000000 |
| Timer A clock division select register | (45 ₁₆)... | XXXXXXXX00 | $\overline{\text{INT}}_1$ interrupt control register | (7E ₁₆)... XX000000 |
| Timer A0 mode register | (56 ₁₆)... | 00 ₁₆ | $\overline{\text{INT}}_2$ interrupt control register | (7F ₁₆)... XX000000 |
| Timer A1 mode register | (57 ₁₆)... | 00 ₁₆ | Processor status register PS | 000??0001?? |
| Timer A2 mode register | (58 ₁₆)... | 00 ₁₆ | Program bank register PG | 00 ₁₆ |
| Timer A3 mode register | (59 ₁₆)... | 00 ₁₆ | Program counter PC _H | Contents at address FFFF ₁₆ |
| Timer A4 mode register | (5A ₁₆)... | 00 ₁₆ | Program counter PC _L | Contents at address FFFE ₁₆ |
| Timer B0 mode register | (5B ₁₆)... | 00?X0000 | Direct page registers DPR0 to DPR3 | 0000 ₁₆ |
| Timer B1 mode register | (5C ₁₆)... | 00?X0000 | Data bank register DT | 00 ₁₆ |
| Timer B2 mode register | (5D ₁₆)... | 00?X0000 | Stack pointer | FFF ₁₆ |

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.
2: The status just after reset depends on the voltage level applied to pin MD0.
3: At power-on reset, these bits are clear to "0". At hardware or software reset, on the other hand, these bits retain the state just before reset.

Fig. 6 Microcomputer internal status just after reset (1)

| | | | | | | | | | | | | | | | | | | | |
|--|--|--------|---|---|--------|---|--------|---|---|---------------------------------|--|---|---|---|---|---|---|---|---|
| \overline{CS}_0 control register L | Address (80 ₁₆)... <table border="1"><tr><td>Note 2</td><td>1</td><td>0</td><td>X</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table> | Note 2 | 1 | 0 | X | 0 | Note 3 | 1 | 0 | DMA0 interrupt control register | Address (B2 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | X | X | X | X | 0 | 0 | 0 | 0 |
| Note 2 | 1 | 0 | X | 0 | Note 3 | 1 | 0 | | | | | | | | | | | | |
| X | X | X | X | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_0 control register H | (81 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr></table> | X | X | X | X | X | 0 | 0 | 1 | DMA1 interrupt control register | (B3 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | X | X | X | X | 0 | 0 | 0 | 0 |
| X | X | X | X | X | 0 | 0 | 1 | | | | | | | | | | | | |
| X | X | X | X | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_1 control register L | (82 ₁₆)... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table> | 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | DMA2 interrupt control register | (B4 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | X | X | X | X | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | | | | | | | | | | | | |
| X | X | X | X | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_1 control register H | (83 ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | X | X | X | X | 0 | 0 | 0 | DMA3 interrupt control register | (B5 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | X | X | X | X | 0 | 0 | 0 | 0 |
| 0 | X | X | X | X | 0 | 0 | 0 | | | | | | | | | | | | |
| X | X | X | X | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_2 control register L | (84 ₁₆)... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table> | 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | DMA0 mode register L | (CC ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_2 control register H | (85 ₁₆)... <table border="1"><tr><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | X | X | X | X | 0 | 0 | 0 | DMA0 mode register H | (CD ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | X | X | X | X | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_3 control register L | (86 ₁₆)... <table border="1"><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>Note 3</td><td>1</td><td>0</td></tr></table> | 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | DMA0 control register | (CE ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | Note 3 | 1 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| \overline{CS}_3 control register H | (87 ₁₆)... <table border="1"><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>0</td></tr></table> | X | X | X | X | X | 0 | 0 | 0 | DMA1 mode register L | (DC ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| X | X | X | X | X | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| Area \overline{CS}_0 start address register | (8A ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | DMA1 mode register H | (DD ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| Area \overline{CS}_1 start address register | (8C ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA1 control register | (DE ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| Area \overline{CS}_2 start address register | (8E ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA2 mode register L | (EC ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| Area \overline{CS}_3 start address register | (90 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA2 mode register H | (ED ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| Real-time output control register | (A0 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA2 control register | (EE ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| DRAM control register | (A8 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA3 mode register L | (FC ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| $\overline{CTS}/\overline{RTS}$ separate select register | (AC ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA3 mode register H | (FD ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| DMAC control register L | (B0 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DMA3 control register | (FE ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |
| DMAC control register H | (B1 ₁₆)... <table border="1"><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table> | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | | | | | | | | |

Notes 1: The contents of the other registers and RAM are undefined at reset and must be initialized by software.
2: The status just after reset depends on the voltage level applied to pin MD0.
3: While V_{SS} level voltage is applied to pin BYTE, these bits are "0". While V_{CC} level voltage is applied to pin BYTE, on the other hand, these bits are "1".

Fig. 7 Microcomputer internal registers' status just after reset (2)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

INPUT/OUTPUT PINS

Each of ports P3 to P9 and P12 has an direction register, and each bit can be programmed for input or output. A pin becomes an output pin when the corresponding bit of direction register is "1", and an input pin when it is "0".

When a pin is programmed as an output pin, the data written to its port latch is output to the output pin. When a pin is programmed as an output pin, the contents of the port latch are read out instead of the value of the pin. Accordingly, a previously output value can be read out correctly even when the output "H" voltage is lowered or the output "L" voltage is raised, owing to an external load, etc.

A pin programmed as an input pin is placed in the floating state, and the value input to the pin can be read out correctly. When a pin is programmed as an input pin, the data can be written only in the port latch, and the pin remains floating.

Each of Figures 8 and 9 shows the block diagram for each port pin.

Table 2. Correspondence between external buses, bus control signals, and programmable I/O port pins

| External buses, Bus control signals | Standby state select bit | |
|--|---|---|
| | 0 | 1 |
| A0 to A7, A8 to A15, A16 to A23 | A0 to A7, A8 to A15, A16 to A23 | P100 to P107 (Note 2), P110 to P117 (Note 2), P00 to P07 (Note 2) |
| D0 to D7, D8 to D15 | D0 to D7, D8 to D15 (Note 1) | P10 to P17 (Note 2), P20 to P27 |
| \overline{RD} , \overline{BLW} , \overline{BHW} | \overline{RD} , \overline{BLW} , \overline{BHW} (Note 1) | P31, P32 (Note 2), P33 |
| $\overline{CS0}$ | $\overline{CS0}$ | P90 (Note 2) |

Notes 1: When the external data bus width = 8 bits (BYTE = VCC level), this becomes a programmable I/O port pin, regardless of the standby state select bit's contents.

2: Pin functions of port pins P0, P1, P31, P32, P90, P10, P11 are not shown in the pin configuration. However, relationship with corresponding bus signals and ports is listed in Table 2. For the addresses of these port's registers and direction registers, refer to the location of the peripheral devices' control registers (Figures 2 and 3).

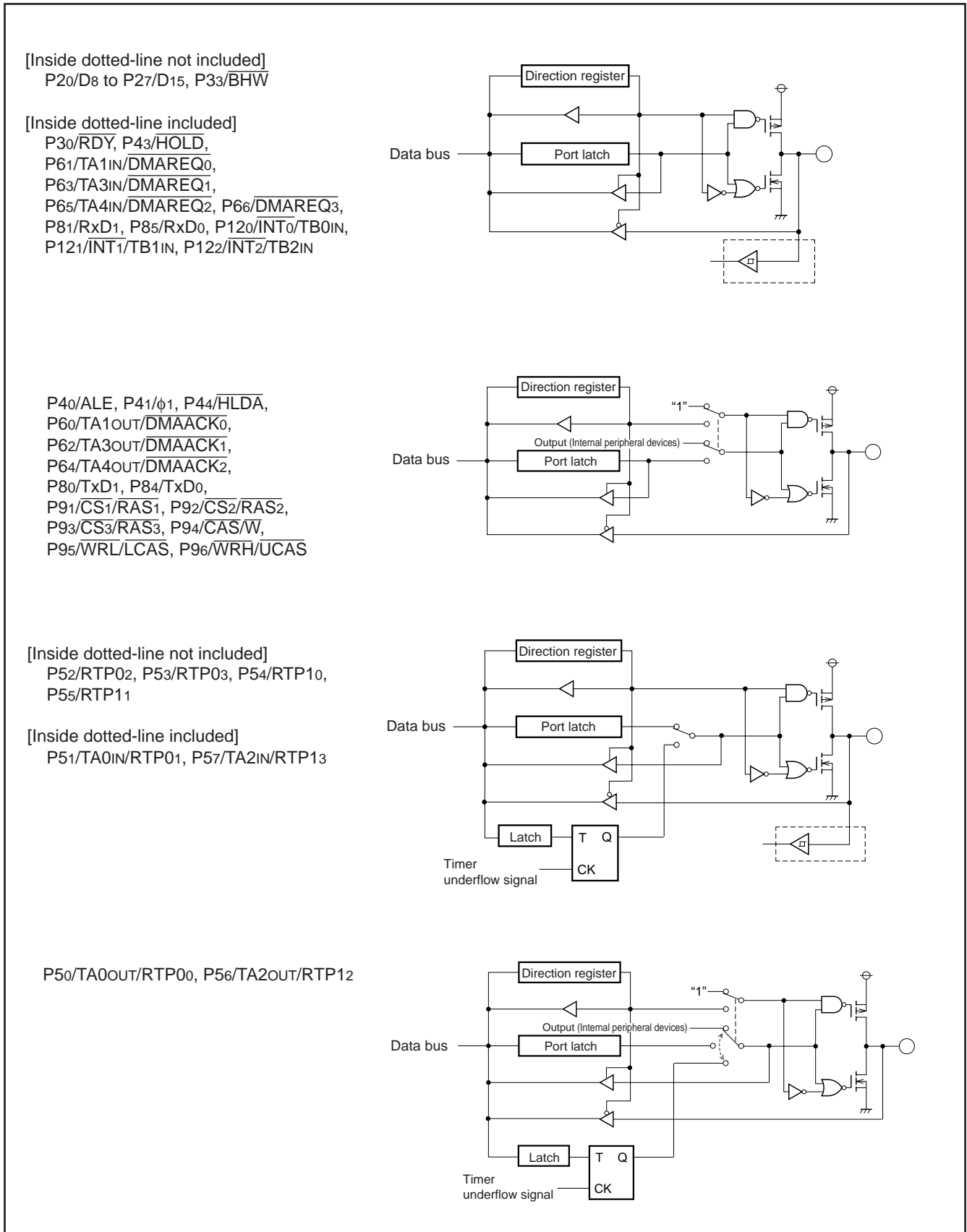


Fig. 8 Block diagram for each port pin (1)

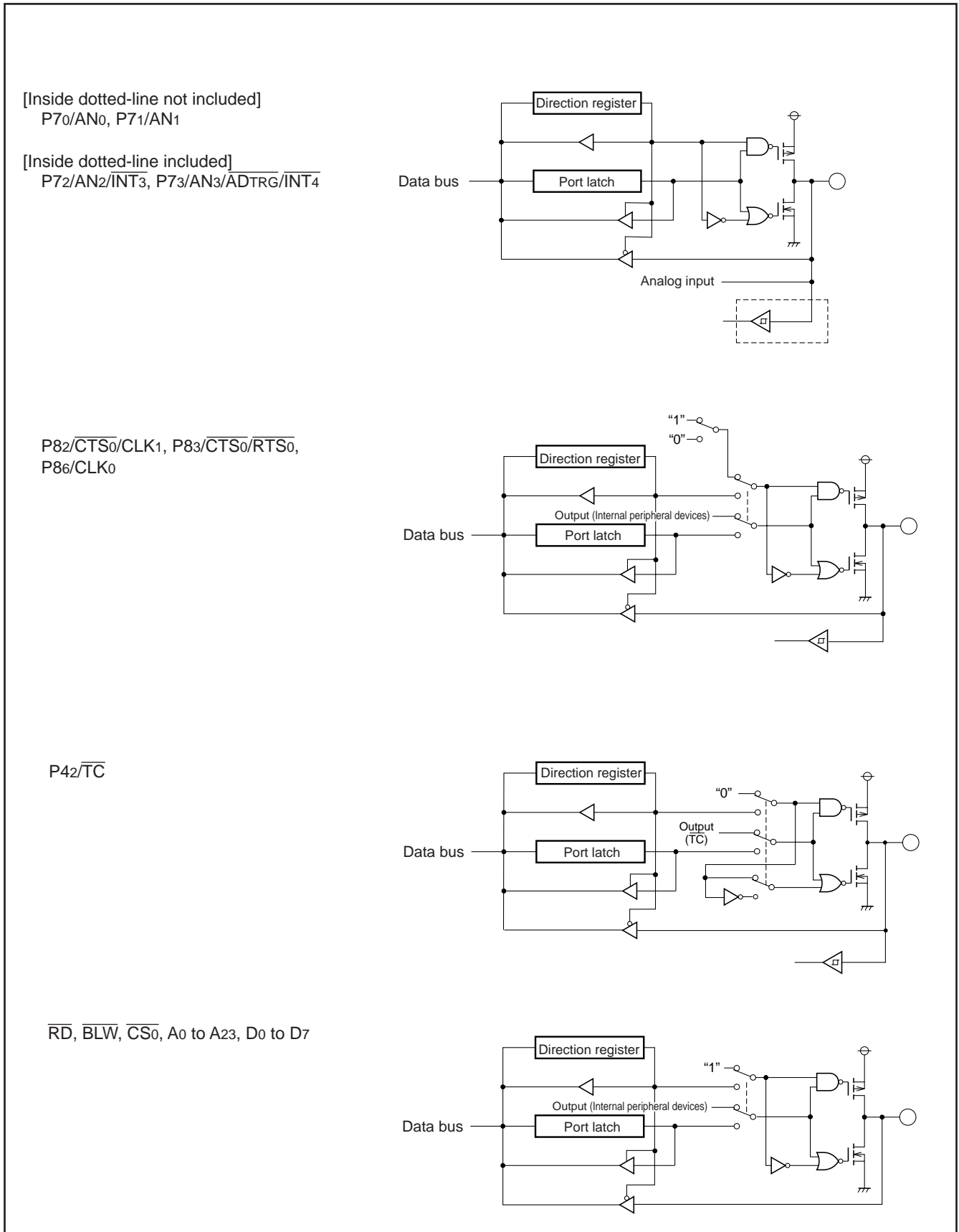


Fig. 9 Block diagram for each port pin (2)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Ratings | Unit |
|--------|--|-----------------|------|
| VCC | Power source voltage | -0.3 to 6.5 | V |
| AVCC | Analog power source voltage | -0.3 to 6.5 | V |
| Vi | Input voltage D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ , VREF, XIN, RESET, BYTE, MD0, MD1, NMI | -0.3 to Vcc+0.3 | V |
| Vo | Output voltage A ₀ -A ₂₃ , RD, BLW, BHW/P ₃₃ , CS ₀ , D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ , XOUT | -0.3 to Vcc+0.3 | V |
| Pd | Power dissipation | 300 | mW |
| Topr | Operating temperature | -20 to 85 | °C |
| Tstg | Storage temperature | -40 to 150 | °C |

RECOMMENDED OPERATING CONDITIONS (Vcc = 5 V, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------|--|--------|------|---------|------|
| | | Min. | Typ. | Max. | |
| VCC | Power source voltage | 4.5 | 5 | 5.5 | V |
| AVCC | Analog power source voltage | | Vcc | | V |
| VSS | Power source voltage | | 0 | | V |
| AVSS | Analog power source voltage | | 0 | | V |
| VIH | High-level input voltage P ₂₀ -P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ , XIN, RESET, BYTE, MD0, MD1, NMI | 0.8VCC | | Vcc | V |
| VIH | High-level input voltage D ₀ -D ₇ , D ₈ -D ₁₅ | 0.5VCC | | Vcc | V |
| VIL | Low-level input voltage P ₂₀ -P ₂₇ , P ₃₀ , P ₃₃ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ , XIN, RESET, BYTE, MD0, MD1, NMI | 0 | | 0.2Vcc | V |
| VIL | Low-level input voltage D ₀ -D ₇ , D ₈ -D ₁₅ | 0 | | 0.16Vcc | V |
| IOH (peak) | High-level peak output current A ₀ -A ₂₃ , RD, BLW, BHW/P ₃₃ , CS ₀ , D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ | | | -10 | mA |
| IOH (avg) | High-level average output current A ₀ -A ₂₃ , RD, BLW, BHW/P ₃₃ , CS ₀ , D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ | | | -5 | mA |
| IOL (peak) | Low-level peak output current A ₀ -A ₂₃ , RD, BLW, BHW/P ₃₃ , CS ₀ , D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ | | | 10 | mA |
| IOL (avg) | Low-level average output current A ₀ -A ₂₃ , RD, BLW, BHW/P ₃₃ , CS ₀ , D ₀ -D ₇ , D ₈ /P ₂₀ -D ₁₅ /P ₂₇ , P ₃₀ , P ₄₀ -P ₄₄ , P ₅₀ -P ₅₇ , P ₆₀ -P ₆₆ , P ₇₀ -P ₇₃ , P ₈₀ -P ₈₆ , P ₉₁ -P ₉₆ , P ₁₂₀ -P ₁₂₂ | | | 5 | mA |
| f(XIN) | External clock input frequency | | | 20 | MHz |

Notes 1: Average output current is the average value of an interval of 100 ms.

2: The sum of IOL(peak) for A₀-A₂₃, D₀-D₇, D₈/P₂₀-D₁₅/P₂₇, ports P₈₀-P₈₆ must be 80 mA or less, the sum of IOH(peak) for A₀-A₂₃, D₀-D₇, D₈/P₂₀-D₁₅/P₂₇, ports P₈₀-P₈₆ must be 80 mA or less, the sum of IOL(peak) for ports P₃₀, RD, BLW, BHW/P₃₃, CS₀, P₄₀-P₄₄, P₅₀-P₅₇, P₆₀-P₆₆, P₇₀-P₇₃, P₉₁-P₉₆, P₁₂₀-P₁₂₂ must be 80 mA or less, the sum of IOH(peak) for P₃₀, RD, BLW, BHW/P₃₃, CS₀, P₄₀-P₄₄, P₅₀-P₅₇, P₆₀-P₆₆, P₇₀-P₇₃, P₉₁-P₉₆, P₁₂₀-P₁₂₂ must be 80 mA or less.

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|----------|--|---|-----------------------------------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| VOH | High-level output voltage A0–A23, \overline{CS}_0 , D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122 | IOH = –10 mA | 3 | | | V |
| VOH | High-level output voltage A0–A23, \overline{CS}_0 , D0–D7, D8/P20–D15/P27, P40, P44, P91–P93 | IOH = –400 μA | 4.7 | | | V |
| VOH | High-level output voltage \overline{RD} , \overline{BLW} , \overline{BHW} /P33, P94/CAS \overline{W} , P95/WRL/LCAS, P96/WRH/UCAS | IOH = –10 mA | 3.4 | | | V |
| | | IOH = –400 μA | 4.8 | | | |
| VOL | Low-level output voltage A0–A23, \overline{CS}_0 , D0–D7, D8/P20–D15/P27, P30, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P93, P120–P122 | IOL = 10 mA | | | 2 | V |
| VOL | Low-level output voltage A0–A23, \overline{CS}_0 , D0–D7, D8/P20–D15/P27, P40, P44, P91–P93 | IOL = 2 mA | | | 0.45 | V |
| VOL | Low-level output voltage \overline{RD} , \overline{BLW} , \overline{BHW} /P33, P94/CAS \overline{W} , P95/WRL/LCAS, P96/WRH/UCAS | IOL = 10 mA | | | 1.6 | V |
| | | IOL = 2 mA | | | 0.4 | |
| VT+ –VT– | Hysteresis TA0IN–TA4IN, TB0IN–TB2IN, \overline{INT}_0 – \overline{INT}_4 , \overline{DMAREQ}_0 – \overline{DMAREQ}_3 , ADTRG, CTS0, CLK0, CLK1, NMI, RDY, HOLD, RxD0, RxD1 | | 0.4 | | 1 | V |
| VT+ –VT– | Hysteresis \overline{RESET} | | 0.5 | | 1.5 | V |
| VT+ –VT– | Hysteresis XIN | | 0.1 | | 0.3 | V |
| IiH | High-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, \overline{RESET} , BYTE, MD0, MD1, NMI | VI = 5.0 V | | | 5 | μA |
| IiL | Low-level input current D0–D7, D8/P20–D15/P27, P30, P33, P40–P44, P50–P57, P60–P66, P70–P73, P80–P86, P91–P96, P120–P122, XIN, \overline{RESET} , BYTE, MD0, MD1, NMI | VI = 0 V | | | –5 | μA |
| VRAM | RAM hold voltage | When clock is stopped. | 2 | | | V |
| ICC | Power source current | At reset in micro-processor mode, output-only pins are open, and the other pins are connected to Vss. | f(XIN) = 20 MHz. | 25 | 50 | mA |
| | | | Ta = 25 °C when clock is stopped. | | 1 | |
| | | | Ta = 80 °C when clock is stopped. | | 20 | |

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

A-D CONVERTER CHARACTERISTICS

(VCC = AVCC = 5 V ± 10 %, VSS = AVSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | Unit |
|---------|----------------------|-----------------|------------------------|-------------|------|
| | | | Min. | Max. | |
| ————— | Resolution | VREF = VCC | | 10 | Bits |
| ————— | Absolute accuracy | VREF = VCC | 10-bit resolution mode | ± 3 | LSB |
| | | | 8-bit resolution mode | ± 2 | LSB |
| RLADDER | Ladder resistance | VREF = VCC | 5 | | kΩ |
| tCONV | Conversion time | f(XIN) ≤ 20 MHz | 10-bit resolution mode | 5.9 | μs |
| | | | 8-bit resolution mode | 2.45 (Note) | |
| VREF | Reference voltage | ————— | 2.7 | VCC | V |
| VIA | Analog input voltage | ————— | 0 | VREF | V |

Note: This is applied when A-D conversion frequency (φAD) = f1(φ).

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

PERIPHERAL DEVICE INPUT/OUTPUT TIMING

(VCC = 5 V ± 10 %, VSS = 0 V, Ta = -20 to 85 °C, f(XIN) = 20 MHz unless otherwise noted)

* For limits depending on f(XIN), their calculation formulas are shown below. Also, the values at f(XIN) = 20 MHz are shown in ().

Timer A input (Count input in event counter mode)

| Symbol | Parameter | Limits | | Unit |
|---------|------------------------------------|--------|------|------|
| | | Min. | Max. | |
| tc(TA) | TAiIN input cycle time | 80 | | ns |
| tw(TAH) | TAiIN input high-level pulse width | 40 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | 40 | | ns |

Timer A input (Gating input in timer mode)

| Symbol | Parameter | | Limits | | Unit |
|---------|------------------------------------|-----------------|---------------------------------------|------|------|
| | | | Min. | Max. | |
| tc(TA) | TAiIN input cycle time | f(XIN) ≤ 20 MHz | $\frac{16 \times 10^9}{f(XIN)}$ (800) | | ns |
| tw(TAH) | TAiIN input high-level pulse width | f(XIN) ≤ 20 MHz | $\frac{8 \times 10^9}{f(XIN)}$ (400) | | ns |
| tw(TAL) | TAiIN input low-level pulse width | f(XIN) ≤ 20 MHz | $\frac{8 \times 10^9}{f(XIN)}$ (400) | | ns |

Note : The TAiIN input cycle time requires 4 or more cycles of a count source. The TAiIN input high-level pulse width and the TAiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f2 at f(XIN) ≤ 20 MHz.

Timer A input (External trigger input in one-shot pulse mode)

| Symbol | Parameter | | Limits | | Unit |
|---------|------------------------------------|-----------------|--------------------------------------|------|------|
| | | | Min. | Max. | |
| tc(TA) | TAiIN input cycle time | f(XIN) ≤ 20 MHz | $\frac{8 \times 10^9}{f(XIN)}$ (400) | | ns |
| tw(TAH) | TAiIN input high-level pulse width | | 80 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | | 80 | | ns |

Timer A input (External trigger input in pulse width modulation mode)

| Symbol | Parameter | Limits | | Unit |
|---------|------------------------------------|--------|------|------|
| | | Min. | Max. | |
| tw(TAH) | TAiIN input high-level pulse width | 80 | | ns |
| tw(TAL) | TAiIN input low-level pulse width | 80 | | ns |

Timer A input (Up-down input and Count input in event counter mode)

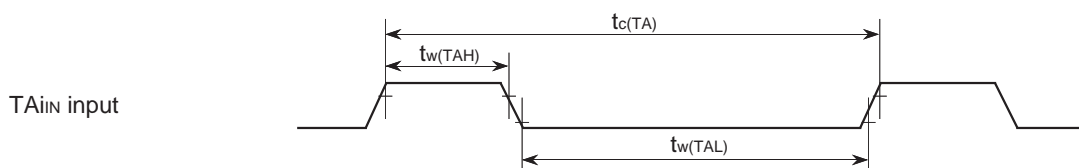
| Symbol | Parameter | Limits | | Unit |
|-------------|-------------------------------------|--------|------|------|
| | | Min. | Max. | |
| tc(UP) | TAiOUT input cycle time | 2000 | | ns |
| tw(UPH) | TAiOUT input high-level pulse width | 1000 | | ns |
| tw(UPL) | TAiOUT input low-level pulse width | 1000 | | ns |
| tsu(UP-TIN) | TAiOUT input setup time | 400 | | ns |
| th(TIN-UP) | TAiOUT input hold time | 400 | | ns |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

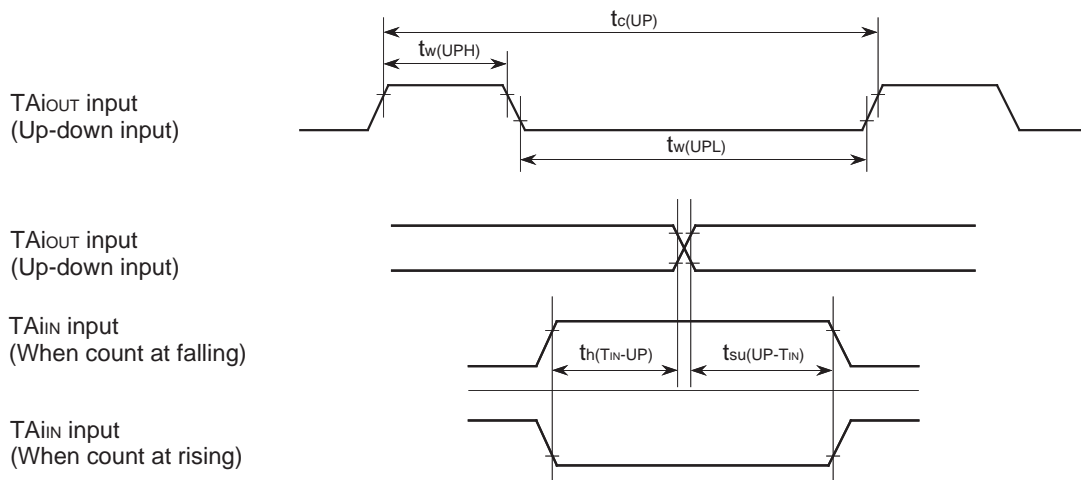
Timer A input (Two-phase pulse input in event counter mode)

| Symbol | Parameter | Limits | | Unit |
|------------------------|-------------------------|--------|------|------|
| | | Min. | Max. | |
| $t_{c(TA)}$ | TAiIN input cycle time | 800 | | ns |
| $t_{su(TAjIN-TAjOUT)}$ | TAjIN input setup time | 200 | | ns |
| $t_{su(TAjOUT-TAjIN)}$ | TAjOUT input setup time | 200 | | ns |

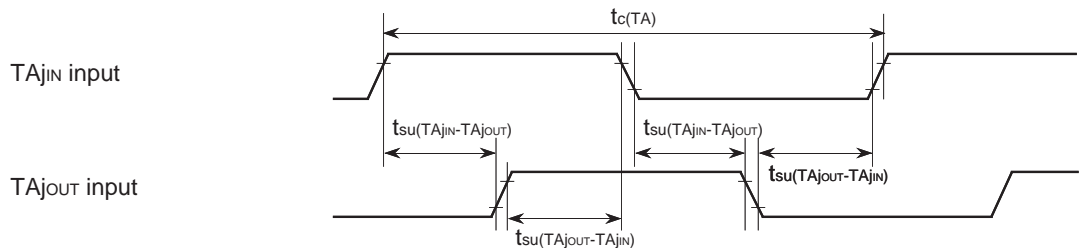
- Gating input in timer mode
- Count input in event counter mode
- External trigger input in one-shot pulse mode
- External trigger input in pulse width modulation mode



- Up-down input and Count input in event counter mode



- Two-phase pulse input in event counter mode



Test conditions

- Vcc = 5 V ± 10 %, Ta = -20 to 85 °C
- Input timing voltage : VIL = 1.0 V, VIH = 4.0 V

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timer B input (Count input in event counter mode)

| Symbol | Parameter | Limits | | Unit |
|----------------------|--|--------|------|------|
| | | Min. | Max. | |
| t _c (TB) | TBiIN input cycle time (one edge count) | 80 | | ns |
| t _w (TBH) | TBiIN input high-level pulse width (one edge count) | 40 | | ns |
| t _w (TBL) | TBiIN input low-level pulse width (one edge count) | 40 | | ns |
| t _c (TB) | TBiIN input cycle time (both edge count) | 160 | | ns |
| t _w (TBH) | TBiIN input high-level pulse width (both edge count) | 80 | | ns |
| t _w (TBL) | TBiIN input low-level pulse width (both edge count) | 80 | | ns |

Timer B input (Pulse period measurement mode)

| Symbol | Parameter | | Limits | | Unit |
|----------------------|------------------------------------|------------------------------|--|------|------|
| | | | Min. | Max. | |
| t _c (TB) | TBiIN input cycle time | f(X _{IN}) ≤ 20 MHz | $\frac{16 \times 10^9}{f(X_{IN})}$ (800) | | ns |
| t _w (TBH) | TBiIN input high-level pulse width | f(X _{IN}) ≤ 20 MHz | $\frac{8 \times 10^9}{f(X_{IN})}$ (400) | | ns |
| t _w (TBL) | TBiIN input low-level pulse width | f(X _{IN}) ≤ 20 MHz | $\frac{8 \times 10^9}{f(X_{IN})}$ (400) | | ns |

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at f(X_{IN}) ≤ 20 MHz.

Timer B input (Pulse width measurement mode)

| Symbol | Parameter | | Limits | | Unit |
|----------------------|------------------------------------|------------------------------|--|------|------|
| | | | Min. | Max. | |
| t _c (TB) | TBiIN input cycle time | f(X _{IN}) ≤ 20 MHz | $\frac{16 \times 10^9}{f(X_{IN})}$ (800) | | ns |
| t _w (TBH) | TBiIN input high-level pulse width | f(X _{IN}) ≤ 20 MHz | $\frac{8 \times 10^9}{f(X_{IN})}$ (400) | | ns |
| t _w (TBL) | TBiIN input low-level pulse width | f(X _{IN}) ≤ 20 MHz | $\frac{8 \times 10^9}{f(X_{IN})}$ (400) | | ns |

Note: The TBiIN input cycle time requires 4 or more cycles of a count source. The TBiIN input high-level pulse width and the TBiIN input low-level pulse width respectively require 2 or more cycles of a count source. The limits in this table are applied when the count source = f₂ at f(X_{IN}) ≤ 20 MHz.

A-D trigger input

| Symbol | Parameter | Limits | | Unit |
|----------------------|--|--------|------|------|
| | | Min. | Max. | |
| t _c (AD) | ADTRG input cycle time (minimum allowable trigger) | 1000 | | ns |
| t _w (ADL) | ADTRG input low-level pulse width | 125 | | ns |

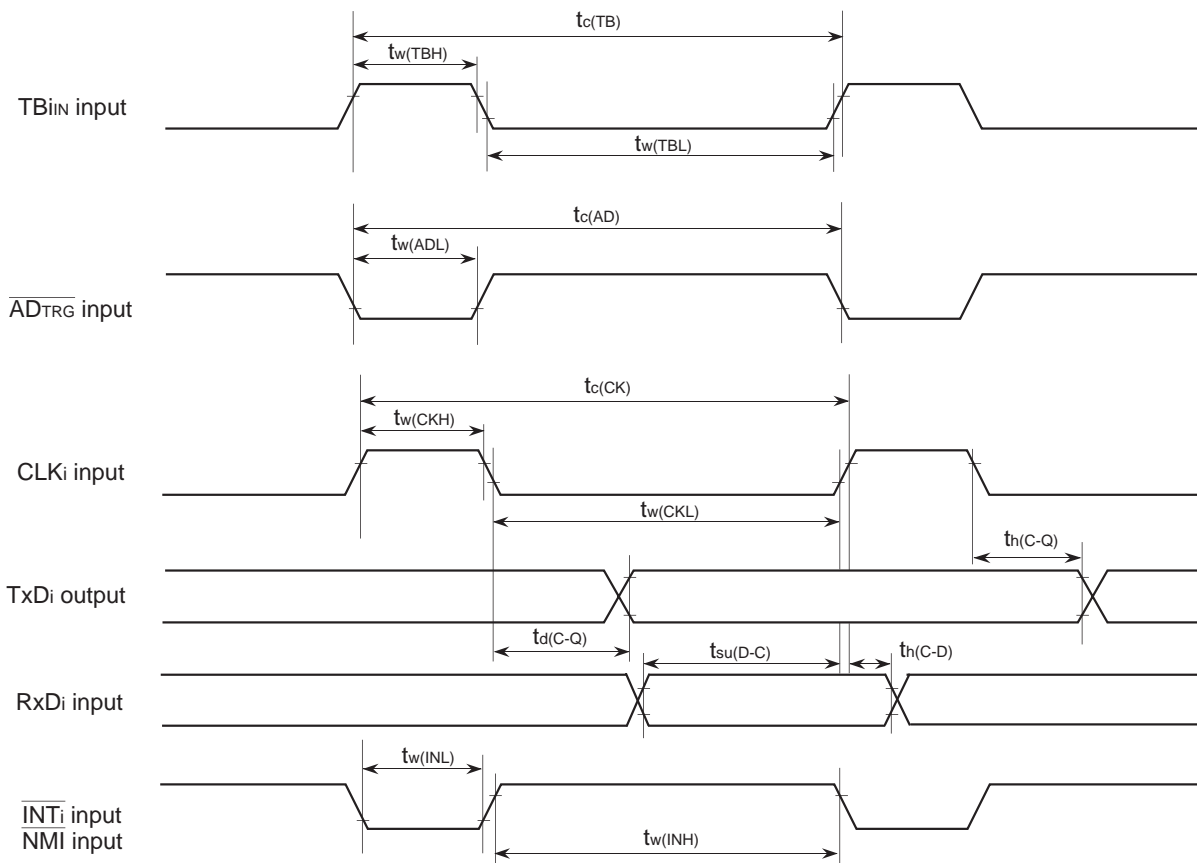
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Serial I/O

| Symbol | Parameter | Limits | | Unit |
|----------------------|-----------------------------------|--------|------|------|
| | | Min. | Max. | |
| $t_c(\text{CK})$ | CLKi input cycle time | 200 | | ns |
| $t_w(\text{CKH})$ | CLKi input high-level pulse width | 100 | | ns |
| $t_w(\text{CKL})$ | CLKi input low-level pulse width | 100 | | ns |
| $t_d(\text{C-Q})$ | TxDi output delay time | | 80 | ns |
| $t_h(\text{C-Q})$ | TxDi hold time | 0 | | ns |
| $t_{su}(\text{D-C})$ | RxDi input setup time | 20 | | ns |
| $t_h(\text{C-D})$ | RxDi input hold time | 90 | | ns |

External interrupt ($\overline{\text{INT}}_i$) input, $\overline{\text{NMI}}$ input

| Symbol | Parameter | Limits | | Unit |
|-------------------|---|--------|------|------|
| | | Min. | Max. | |
| $t_w(\text{INH})$ | $\overline{\text{INT}}_i$ input/ $\overline{\text{NMI}}$ input high-level pulse width | 250 | | ns |
| $t_w(\text{INL})$ | $\overline{\text{INT}}_i$ input/ $\overline{\text{NMI}}$ input low-level pulse width | 250 | | ns |



Test conditions

- $V_{CC} = 5 \text{ V} \pm 10 \%$, $T_a = -20 \text{ to } 85 \text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0 \text{ V}$, $V_{IH} = 4.0 \text{ V}$
- Output timing voltage : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

READY, HOLD TIMING

Timing requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|-----------------------|------------------------------------|--------|------|------|
| | | Min. | Max. | |
| $t_{su}(RDY-\phi 1)$ | \overline{RDY} input setup time | 40 | | ns |
| $t_{su}(HOLD-\phi 1)$ | \overline{HOLD} input setup time | 40 | | ns |
| $t_{h}(\phi 1-RDY)$ | \overline{RDY} input hold time | 0 | | ns |
| $t_{h}(\phi 1-HOLD)$ | \overline{HOLD} input hold time | 0 | | ns |

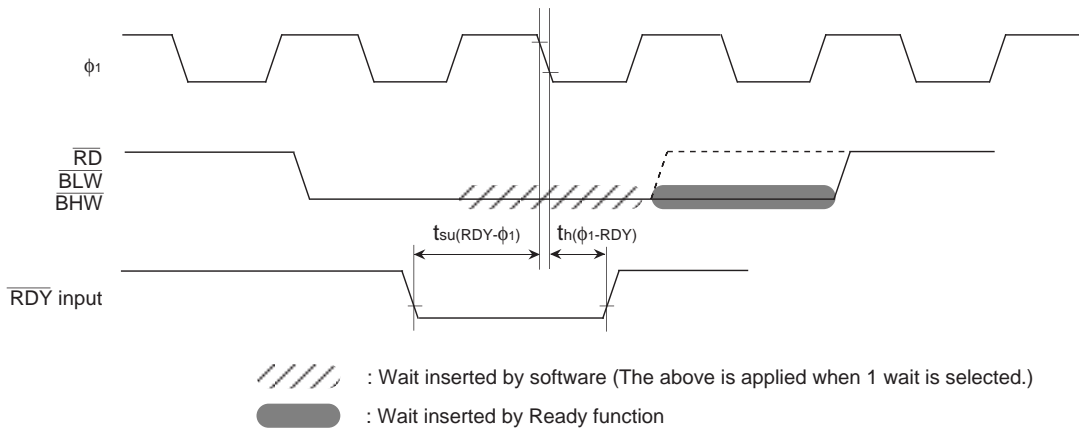
Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|-----------------------|--|-------------------|------|------|
| | | Min. | Max. | |
| $t_d(\phi 1-HLDAL)$ | \overline{HLDAL} output delay time | | 20 | ns |
| $t_d(RDH-HLDAL)$ | \overline{HLDAL} low-level output delay time after read | $t_c - 15$ (Note) | | ns |
| $t_d(BXWH-HLDAL)$ | \overline{HLDAL} low-level output delay time after write | $t_c - 15$ (Note) | | ns |
| $t_{pxz}(HLDAL-RDZ)$ | Floating start delay time | -15 | 10 | ns |
| $t_{pxz}(HLDAL-BXWZ)$ | Floating start delay time | -15 | 10 | ns |
| $t_{pxz}(HLDAL-CSIZ)$ | Floating start delay time | -15 | 10 | ns |
| $t_{pxz}(HLDAL-ALEZ)$ | Floating start delay time | -15 | 10 | ns |
| $t_{pxz}(HLDAL-AZ)$ | Floating start delay time | -15 | 10 | ns |
| $t_{pzx}(HLDAL-RDZ)$ | Floating release delay time | 0 | | ns |
| $t_{pzx}(HLDAL-BXWZ)$ | Floating release delay time | 0 | | ns |
| $t_{pzx}(HLDAL-CSIZ)$ | Floating release delay time | 0 | | ns |
| $t_{pzx}(HLDAL-ALEZ)$ | Floating release delay time | 0 | | ns |
| $t_{pzx}(HLDAL-AZ)$ | Floating release delay time | 0 | | ns |

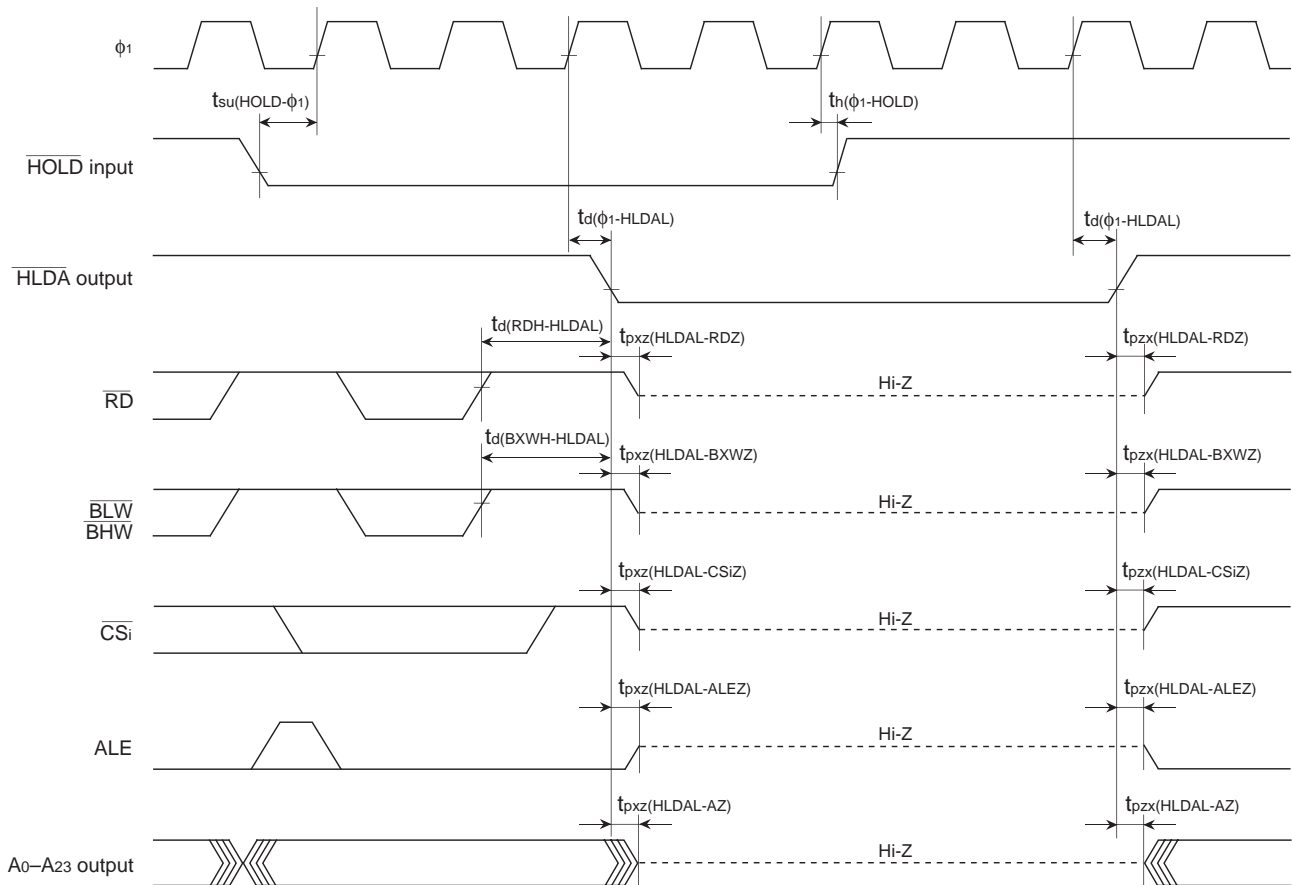
Note: $t_c = 1/f(X_{IN})$.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

RDY input



HOLD input



Test conditions

- $V_{CC} = 5 \text{ V} \pm 10 \%$, $T_a = -20 \text{ to } 85 \text{ }^\circ\text{C}$
- RDY input, HOLD input : $V_{IL} = 1.0 \text{ V}$, $V_{IH} = 4.0 \text{ V}$
- HLDA output : $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 2.0 \text{ V}$, $C_L = 50 \text{ pF}$

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

External bus timing

For limits depending on $f(X_{IN})$, their calculation formulas are shown below.

$W = 0$ (0 wait)

$W = 1$ (1 wait)

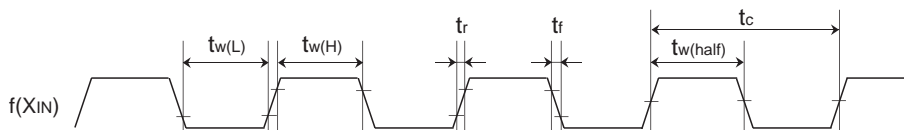
$W = 2$ (2 wait)

$t_c = 1/f(X_{IN})$.

Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20$ to $85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | | | Unit |
|------------------------|--|-----------------------------|---------------------|-------------------------------------|---------------|------|
| | | When 0/1/2 wait is selected | | When ALE expansion wait is selected | | |
| | | Min. | Max. | Min. | Max. | |
| t_c | External clock input cycle time | 50 | | 50 | | ns |
| $t_{w(\text{half})}$ | External clock input pulse width with half input-voltage | $0.45t_c$ | $0.55t_c$ | $0.45t_c$ | $0.55t_c$ | ns |
| $t_{w(\text{H})}$ | External clock input high-level pulse width | $0.5t_c - 8$ | | $0.5t_c - 8$ | | ns |
| $t_{w(\text{L})}$ | External clock input low-level pulse width | $0.5t_c - 8$ | | $0.5t_c - 8$ | | ns |
| t_r | External clock input rise time | | 8 | | 8 | ns |
| t_f | External clock input fall time | | 8 | | 8 | ns |
| $t_{a(\text{A-D})}$ | Address access time | | $(2 + W)t_c - 45$ | | $4t_c - 45$ | ns |
| $t_{a(\text{CSIL-D})}$ | Chip select access time | | $(1.5 + W)t_c - 35$ | | $3.5t_c - 35$ | ns |
| $t_{a(\text{RDL-D})}$ | Read access time | | $(1 + W)t_c - 30$ | | $2t_c - 30$ | ns |
| $t_{su(\text{D-RDL})}$ | Read data setup time | 15 | | 15 | | ns |
| $t_{h(\text{RDH-D})}$ | Data input hold time after read | 0 | | 0 | | ns |
| $t_{a(\text{BA-D})}$ | Address access time at burst ROM access | | $(1 + W)t_c - 35$ | | $2t_c - 35$ | ns |
| $t_{h(\text{BA-D})}$ | Data hold time after address at burst ROM access | 0 | | 0 | | ns |

External clock input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$ ($t_{w(\text{H})}$, $t_{w(\text{L})}$, t_r , t_f)
- Input timing voltage : 2.5 V (t_c , $t_{w(\text{half})}$)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20$ to $85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

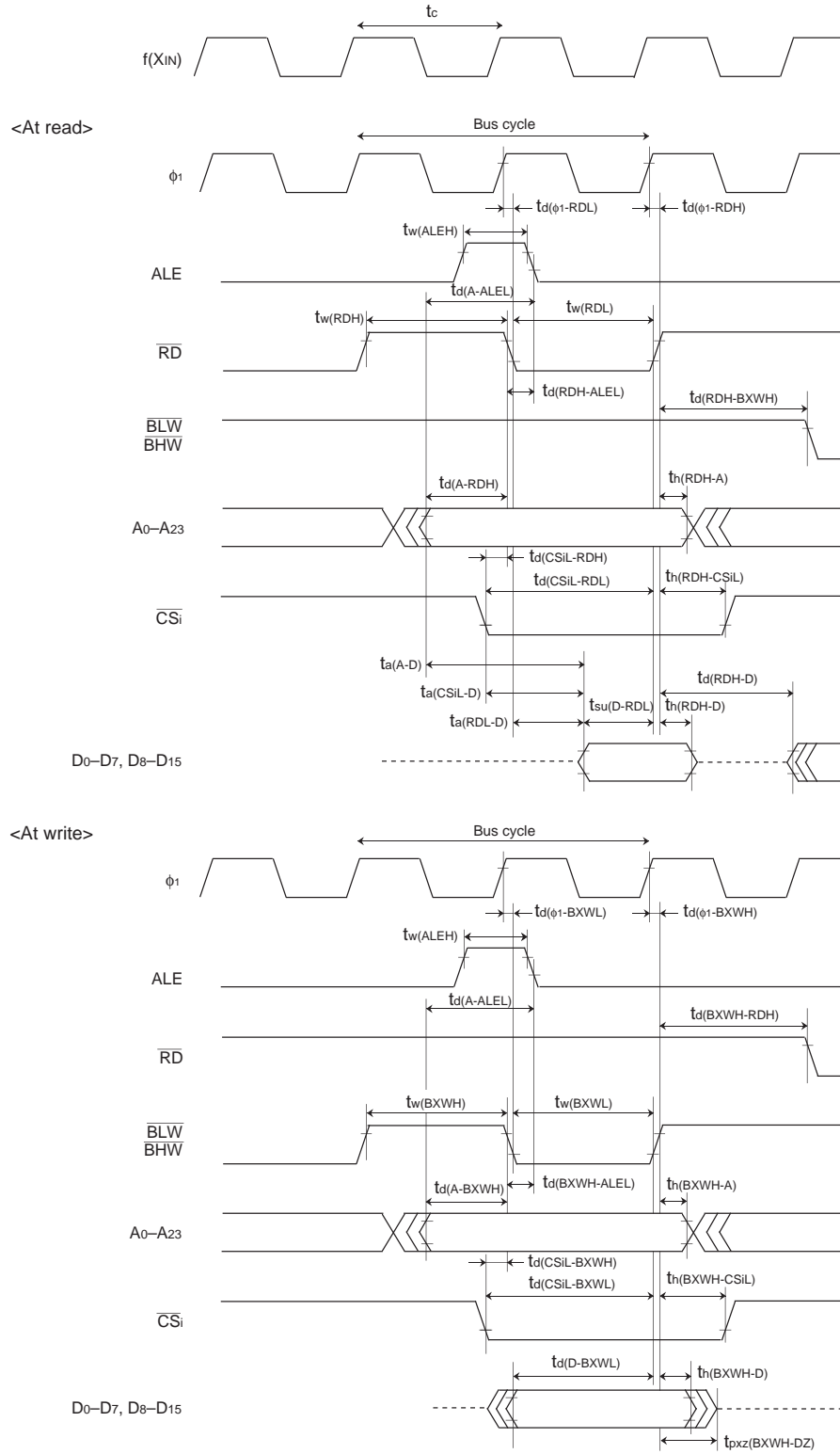
| Symbol | Parameter | Limits | | | | Unit |
|-----------------------------|--|-----------------------------|------|-------------------------------------|------|------|
| | | When 0/1/2 wait is selected | | When ALE expansion wait is selected | | |
| | | Min. | Max. | Min. | Max. | |
| $t_{d(\phi 1\text{-RDL})}$ | Read low-level output delay time | -10 | 15 | -10 | 15 | ns |
| $t_{d(\phi 1\text{-RDH})}$ | Read high-level output delay time | -10 | 10 | -10 | 10 | ns |
| $t_{d(\phi 1\text{-BXWL})}$ | Write low-level output delay time | -10 | 15 | -10 | 15 | ns |
| $t_{d(\phi 1\text{-BXWH})}$ | Write high-level output delay time | -10 | 10 | -10 | 10 | ns |
| $t_w(\text{ALEH})$ | ALE pulse width | 0.5tc - 20 | | tc - 20 | | ns |
| $t_d(\text{A-ALE})$ | ALE completion delay time after address stabilization | tc - 30 | | 1.5tc - 30 | | ns |
| $t_w(\text{RDL})$ | Read output pulse width | $(1 + W)tc - 15$ | | 2tc - 15 | | ns |
| $t_w(\text{RDH})$ | Read output high-level width (Note 1) | tc - 15 | | 2tc - 15 | | ns |
| $t_d(\text{RDH-BXWH})$ | Write disable valid time after read (Note 2) | tc - 15 | | tc - 15 | | ns |
| $t_d(\text{A-RDH})$ | Address valid time before read | tc - 30 | | 2tc - 30 | | ns |
| $t_h(\text{RDH-A})$ | Address hold time after read (Note 3) | 8 | | 8 | | ns |
| $t_d(\text{RDH-ALE})$ | ALE completion delay time after read start | 20 | | | | ns |
| $t_d(\text{ALEL-RDH})$ | Read disable valid time after ALE completion | | | 0.5tc - 20 | | ns |
| $t_d(\text{CSiL-RDH})$ | Chip select valid time before read | 0.5tc - 20 | | 1.5tc - 20 | | ns |
| $t_d(\text{CSiL-RDL})$ | Chip select output valid time before read completion | $(1.5 + W)tc - 20$ | | 3.5tc - 20 | | ns |
| $t_h(\text{RDH-CSiL})$ | Chip select hold time after read | 0.5tc - 20 | | 0.5tc - 20 | | ns |
| $t_d(\text{RDH-D})$ | Next write cycle data output delay time after read (Note 2) | tc - 15 | | tc - 15 | | ns |
| $t_w(\text{BXWL})$ | Write output pulse width | $(1 + W)tc - 15$ | | 2tc - 15 | | ns |
| $t_w(\text{BXWH})$ | Write output high-level width (Note 1) | tc - 15 | | 2tc - 15 | | ns |
| $t_d(\text{BXWH-RDH})$ | Read disable valid time after write (Note 2) | tc - 15 | | tc - 15 | | ns |
| $t_d(\text{A-BXWH})$ | Address valid time before write | tc - 30 | | 2tc-30 | | ns |
| $t_h(\text{BXWH-A})$ | Address hold time after write (Note 3) | 8 | | 8 | | ns |
| $t_d(\text{BXWH-ALE})$ | ALE completion delay time after write start | 20 | | | | ns |
| $t_d(\text{ALEL-BXWH})$ | Write disable valid time after ALE completion | | | 0.5tc - 20 | | ns |
| $t_d(\text{CSiL-BXWH})$ | Chip select valid time before write | 0.5tc - 20 | | 1.5tc - 20 | | ns |
| $t_d(\text{CSiL-BXWL})$ | Chip select output valid time before write completion | $(1.5 + W)tc - 20$ | | 3.5tc - 20 | | ns |
| $t_h(\text{BXWH-CSiL})$ | Chip select hold time after write | 0.5tc - 20 | | 0.5tc - 20 | | ns |
| $t_d(\text{D-BXWL})$ | Data output valid time before write completion | $(1 + W)tc - 20$ | | 2tc - 20 | | ns |
| $t_h(\text{BXWH-D})$ | Data hold time after write | 0.5tc - 10 | | 0.5tc - 10 | | ns |
| $t_{pxz}(\text{BXWH-DZ})$ | Floating start delay time after write | | | 0.5tc + 10 | | ns |

Notes 1: When the bus cycle just before this parameter is for the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).

2: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns).

3: When accessing the area where the recovery cycle insertion is selected, this parameter is extended by tc (ns). However, except for the case at instruction prefetch.

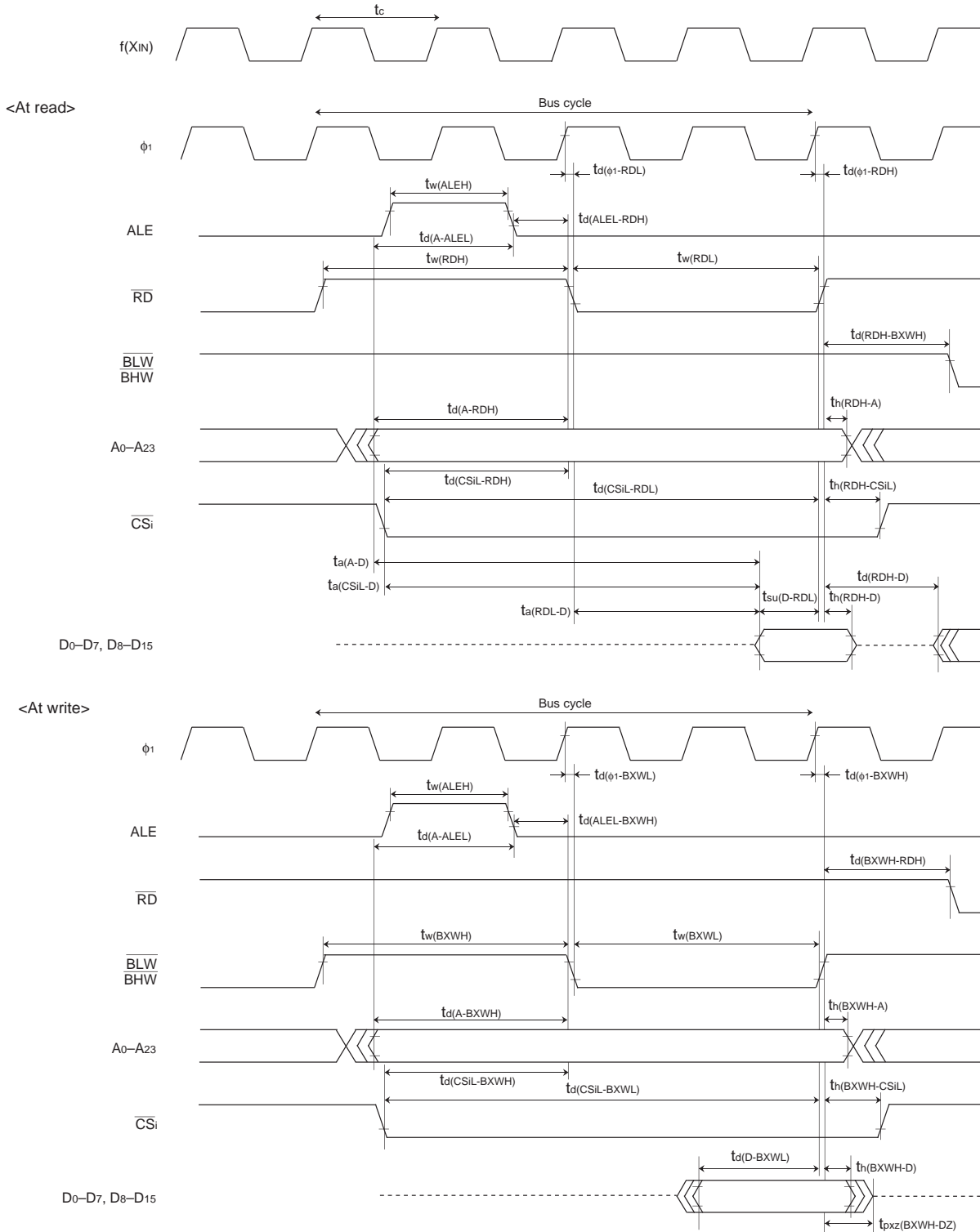
Normal access: 0/1/2 wait



Test conditions

- $V_{cc} = 5\text{ V} \pm 10\%$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{\text{CSi}}$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{\text{CSi}}$)

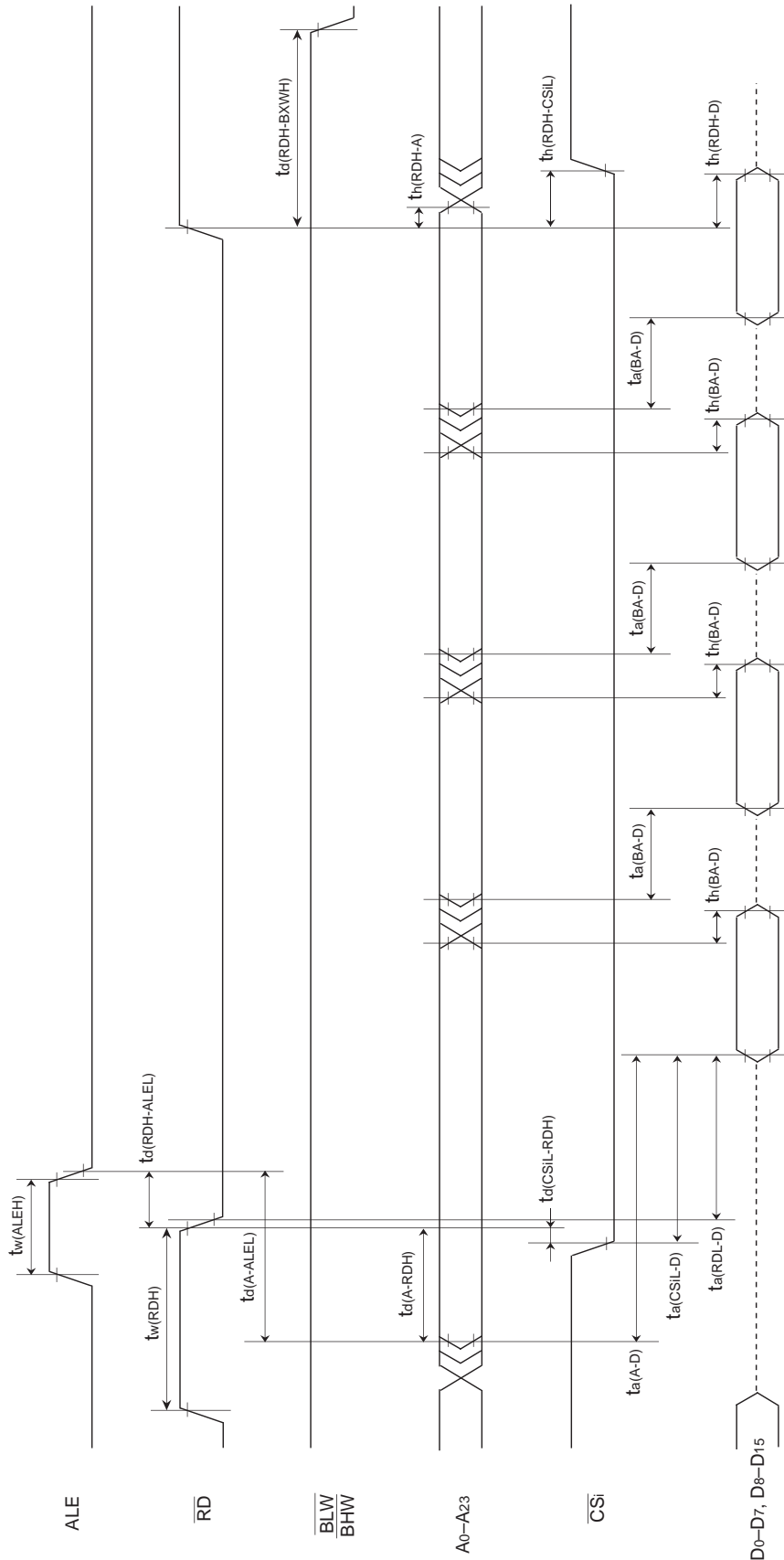
Normal access : ALE extension wait



Test conditions

- $V_{CC} = 5V \pm 10\%$, $T_a = -20$ to $85^\circ C$
- Input timing voltage : $V_{IL} = 0.8V$, $V_{IH} = 2.5V$
- Output timing voltage : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$, $C_L = 15 pF$ (\overline{CSi})
- Output timing voltage : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$, $C_L = 50 pF$ (except for \overline{CSi})

Burst ROM access : 0/1/2 wait at instruction prefetch



- Test conditions
- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
 - Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ (CSi)
 - Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for CSi)

PRELIMINARY
Notice: This is not a final specification.
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DRAM access

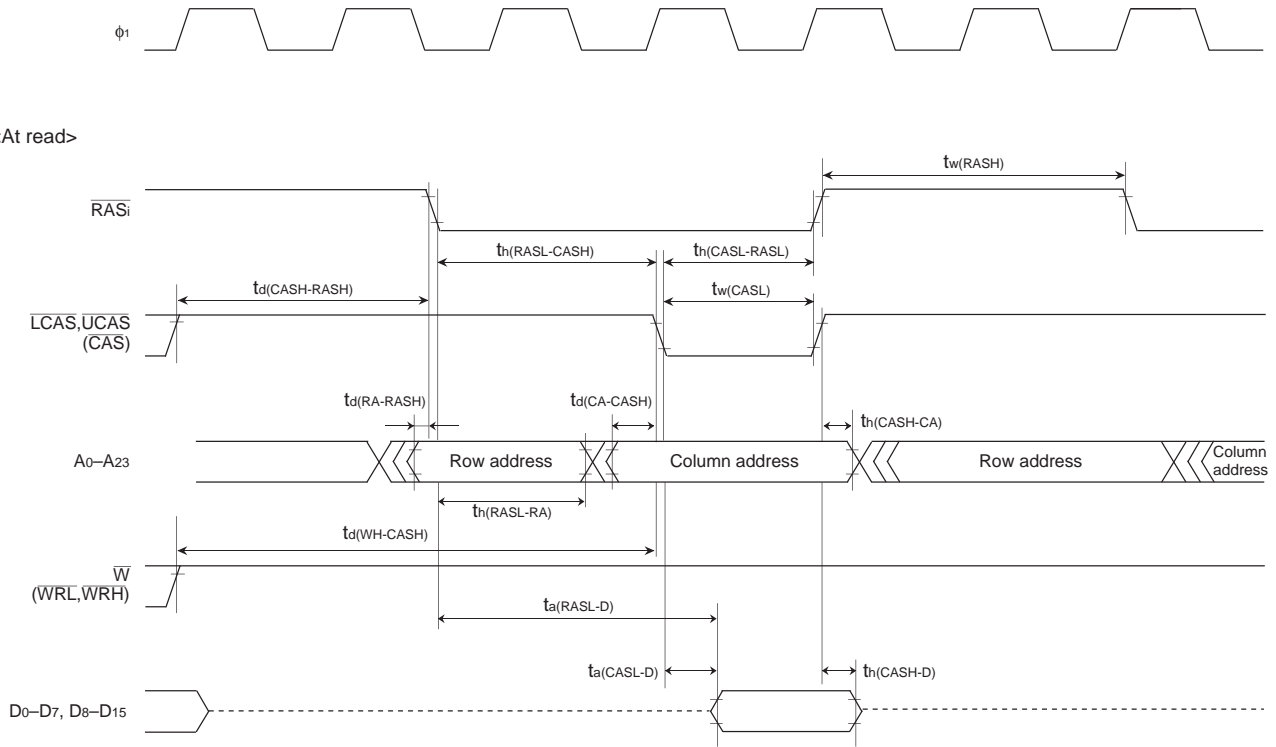
Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|----------------------|--|--------|---------------|------|
| | | Min. | Max. | |
| $t_a(\text{RASL-D})$ | $\overline{\text{RAS}}$ access time | | $2.5t_c - 35$ | ns |
| $t_a(\text{CASL-D})$ | $\overline{\text{CAS}}$ access time | | $t_c - 30$ | ns |
| $t_h(\text{CASH-D})$ | Data input hold time after $\overline{\text{CAS}}$ | 0 | | ns |

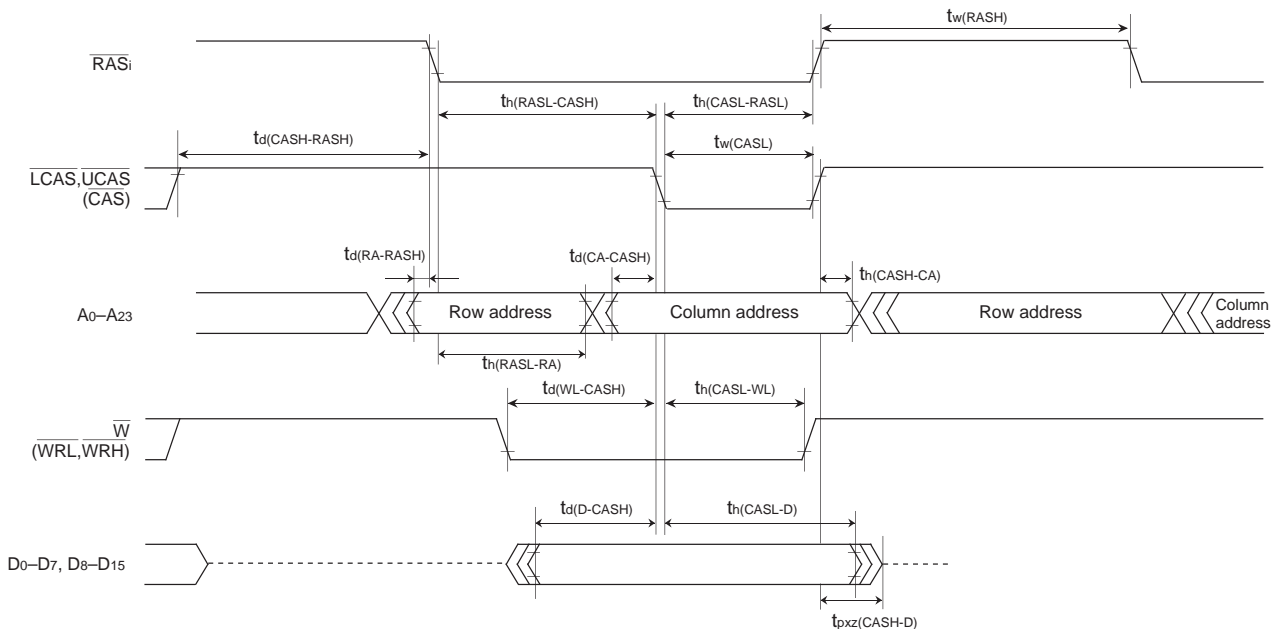
Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|--------------------------|--|---------------|---------------|------|
| | | Min. | Max. | |
| $t_w(\text{RASH})$ | $\overline{\text{RAS}}$ high-level pulse width | $1.5t_c - 20$ | | ns |
| $t_d(\text{CASH-RASH})$ | $\overline{\text{CAS}}$ high-level valid time before $\overline{\text{RAS}}$ | $1.5t_c - 20$ | | ns |
| $t_h(\text{RASL-CASH})$ | $\overline{\text{CAS}}$ high-level hold time after $\overline{\text{RAS}}$'s low level | $1.5t_c - 20$ | | ns |
| $t_h(\text{CASL-RASL})$ | $\overline{\text{RAS}}$ hold time after $\overline{\text{CAS}}$'s low level | $t_c - 15$ | | ns |
| $t_w(\text{CASL})$ | $\overline{\text{CAS}}$ low-level pulse width | $t_c - 15$ | | ns |
| $t_d(\text{RA-RASH})$ | Row address valid time before $\overline{\text{RAS}}$ | $0.5t_c - 25$ | | ns |
| $t_h(\text{RASL-RA})$ | Row address hold time after $\overline{\text{RAS}}$'s low level | $t_c - 40$ | | ns |
| $t_d(\text{CA-CASH})$ | Column address valid time before $\overline{\text{CAS}}$ | $0.5t_c - 20$ | | ns |
| $t_h(\text{CASH-CA})$ | Column address hold time after $\overline{\text{CAS}}$'s high level | 0 | | ns |
| $t_d(\text{WH-CASH})$ | $\overline{\text{W}}$ high-level valid time before $\overline{\text{CAS}}$ | $3t_c - 15$ | | ns |
| $t_d(\text{WL-CASH})$ | $\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$ | $t_c - 15$ | | ns |
| $t_h(\text{CASL-WL})$ | $\overline{\text{W}}$ hold time after $\overline{\text{CAS}}$'s low level | $t_c - 15$ | | ns |
| $t_d(\text{D-CASH})$ | Data output valid time before $\overline{\text{CAS}}$ | $t_c - 20$ | | ns |
| $t_h(\text{CASL-D})$ | Data output hold time after $\overline{\text{CAS}}$'s low level | $1.5t_c - 15$ | | ns |
| $t_{pxz}(\text{CASH-D})$ | Floating start delay time after $\overline{\text{CAS}}$ | $0.5t_c + 10$ | | ns |
| $t_d(\text{CAF-CASH})$ | Column address valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected) | $t_c - 40$ | | ns |
| $t_d(\text{WFL-CASH})$ | $\overline{\text{W}}$ low-level valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected) | $0.5t_c - 20$ | | ns |
| $t_d(\text{DF-CASH})$ | Data output valid time before $\overline{\text{CAS}}$ (When fast page access ON is selected) | $0.5t_c - 20$ | | ns |
| $t_{pxz}(\text{WH-D})$ | Floating start delay time after write | | $0.5t_c + 10$ | ns |

DRAM access : fast page access = OFF



<At write>

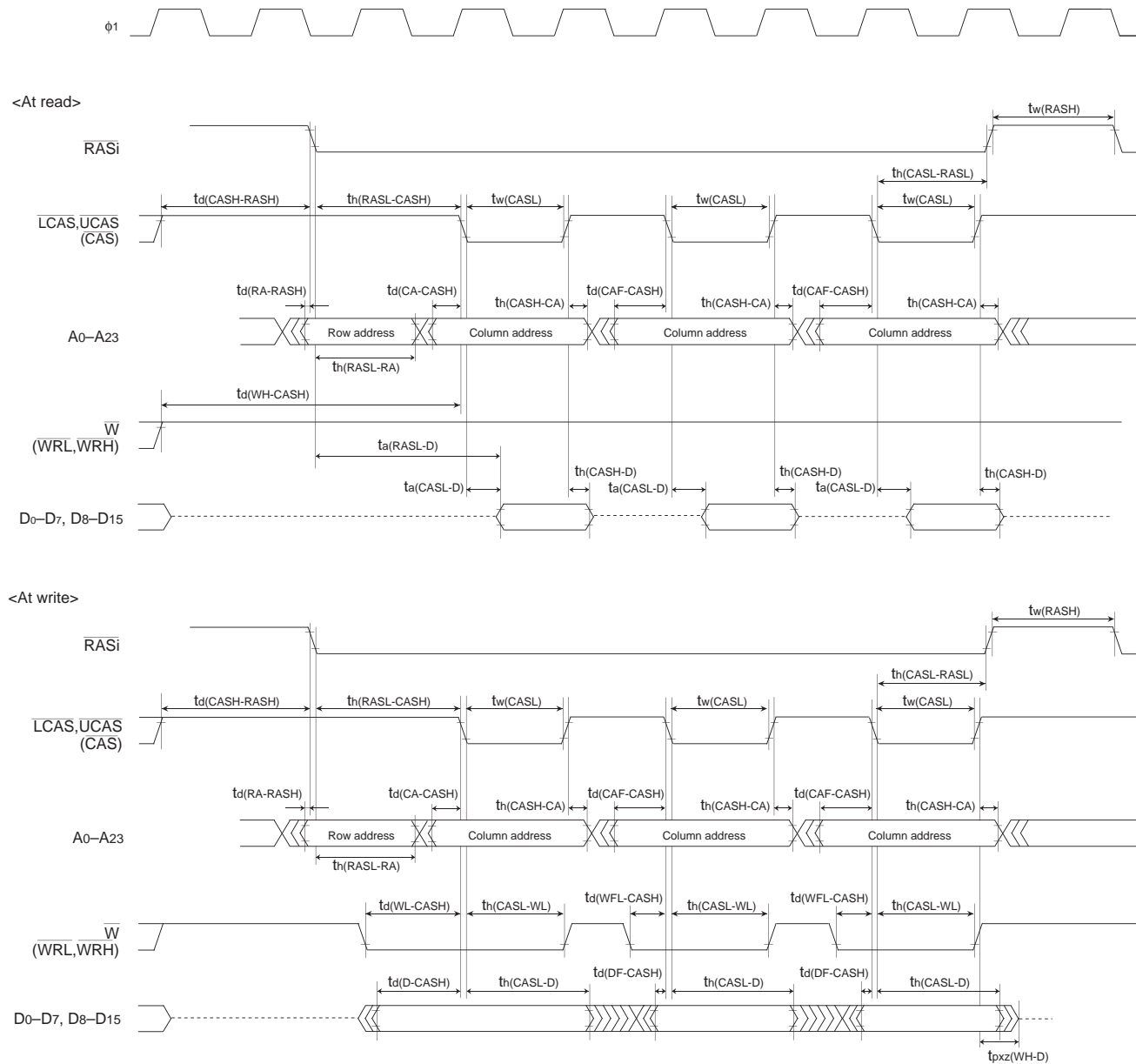


Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{\text{RAS}}_i$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{\text{RAS}}_i$)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DRAM access : fast page access = ON



Test conditions
 • $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0$ to $70\text{ }^\circ\text{C}$
 • Input timing voltage : $V_{IL} = 0.8\text{ V}$, $V_{IH} = 2.5\text{ V}$
 • Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ (\overline{RAS}_i)
 • Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for \overline{RAS}_i)

PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

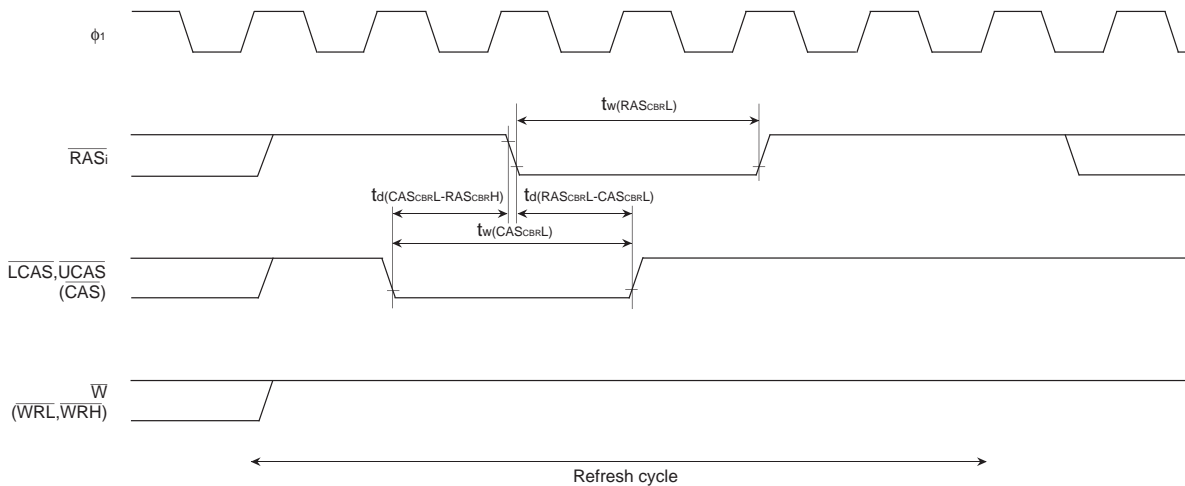
DRAM refresh

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

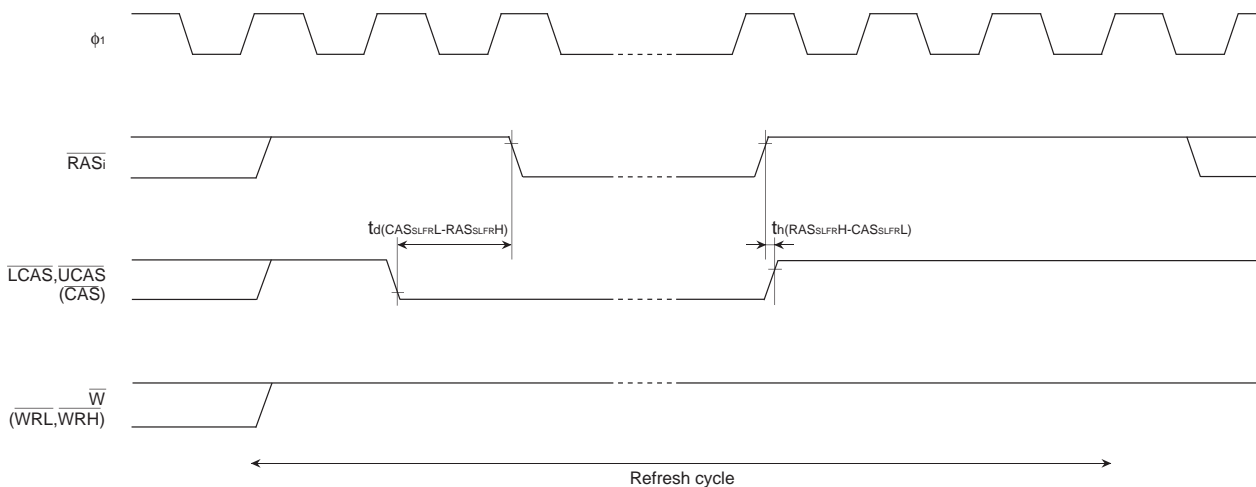
| Symbol | Parameter | Limits | | Unit |
|--|--|-------------|------|------|
| | | Min. | Max. | |
| $t_w(\overline{\text{RAS}}_{\text{CBRL}})$ | $\overline{\text{RAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) | $2t_c - 15$ | | ns |
| $t_w(\overline{\text{CAS}}_{\text{CBRL}})$ | $\overline{\text{CAS}}$ low-level pulse width (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) | $2t_c - 15$ | | ns |
| $t_d(\overline{\text{CAS}}_{\text{CBRL}} - \overline{\text{RAS}}_{\text{CBRL}})$ | $\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$'s low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) | $t_c - 15$ | | ns |
| $t_d(\overline{\text{RAS}}_{\text{CBRL}} - \overline{\text{CAS}}_{\text{CBRL}})$ | $\overline{\text{CAS}}$ low-level valid time after $\overline{\text{RAS}}$'s low level start (At $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) | $t_c - 15$ | | ns |
| $t_d(\overline{\text{CAS}}_{\text{SLFRH}} - \overline{\text{RAS}}_{\text{SLFRH}})$ | $\overline{\text{RAS}}$ high-level valid time after $\overline{\text{CAS}}$'s low level start (At self refresh) | $t_c - 15$ | | ns |
| $t_h(\overline{\text{RAS}}_{\text{SLFRH}} - \overline{\text{CAS}}_{\text{SLFRL}})$ | $\overline{\text{CAS}}$ low-level hold time after $\overline{\text{RAS}}$'s high level (At self refresh) | -15 | 15 | ns |

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DRAM refresh : $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh



DRAM refresh : self refresh



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = 0\text{ to }70\text{ }^\circ\text{C}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 15\text{ pF}$ ($\overline{\text{RAS}}_i$)
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$ (except for $\overline{\text{RAS}}_i$)

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

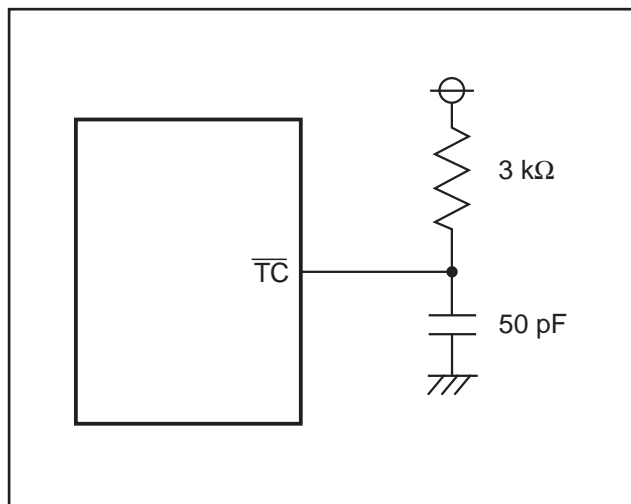
DMA transfer timing

Timing Requirements ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

| Symbol | Parameter | Limits | | Unit |
|---------------------------|---|------------|------|------|
| | | Min. | Max. | |
| $t_{su}(TC_{INL}-\phi_1)$ | \overline{TC} input setup time | 40 | | ns |
| $t_w(TC_{INL})$ | \overline{TC} input pulse width | $t_c + 20$ | | ns |
| $t_{su}(DRQL-\phi_1)$ | \overline{DMAREQ}_i input setup time | 40 | | ns |
| $t_w(DRQL)$ | \overline{DMAREQ}_i input pulse width | t_c | | ns |

Switching characteristics ($V_{CC} = 5\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $T_a = -20\text{ to }85\text{ }^\circ\text{C}$, $f(X_{IN}) = 20\text{ MHz}$, unless otherwise noted)

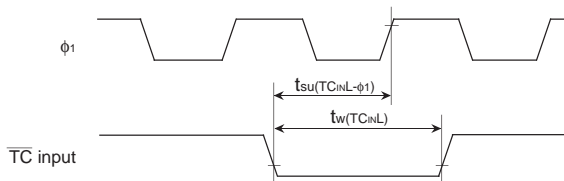
| Symbol | Parameter | Limits | | Unit |
|--------------------|--|---------------|------|------|
| | | Min. | Max. | |
| $t_w(TCL)$ | \overline{TC} output pulse width | $t_c - 20$ | | ns |
| $t_d(RDH-TCL)$ | \overline{TC} output start delay time after read | $t_c - 15$ | | ns |
| $t_d(BXWH-TCL)$ | \overline{TC} output start delay time after write | $t_c - 15$ | | ns |
| $t_d(TCL-DMAACKL)$ | \overline{DMAACK} low-level output valid time after \overline{TC} output start | $2.5t_c - 20$ | | ns |



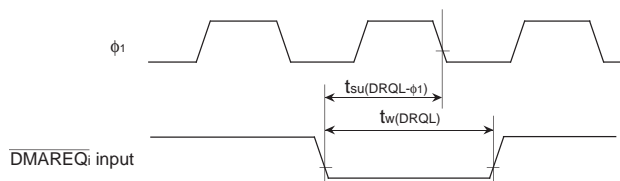
Test circuit for \overline{TC} output

PRELIMINARY
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● \overline{TC} input



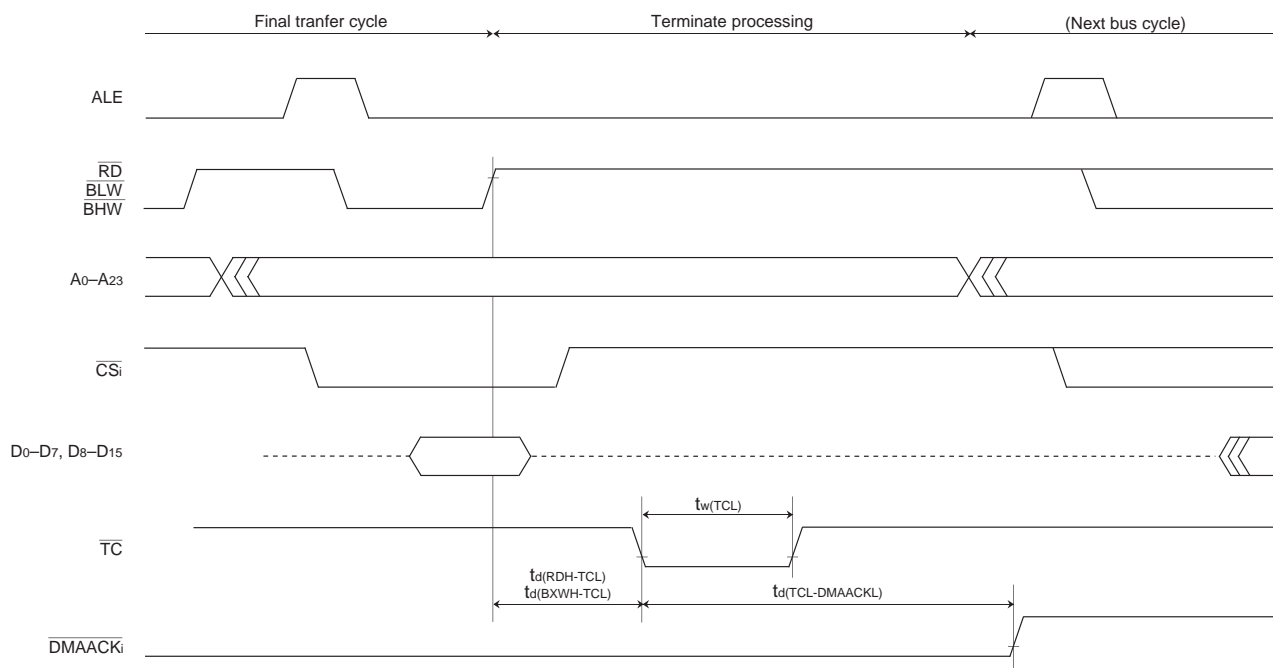
● \overline{DMAREQ}_i input



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- Input timing voltage : $V_{IL} = 1.0\text{ V}$, $V_{IH} = 4.0\text{ V}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$

● Transfer terminate timing



Test conditions

- $V_{CC} = 5\text{ V} \pm 10\%$, $T_a = -20$ to $85\text{ }^\circ\text{C}$
- Output timing voltage : $V_{OL} = 0.8\text{ V}$, $V_{OH} = 2.0\text{ V}$, $C_L = 50\text{ pF}$

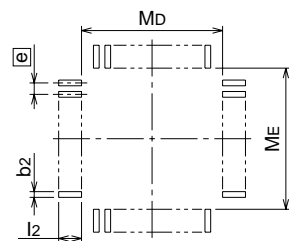
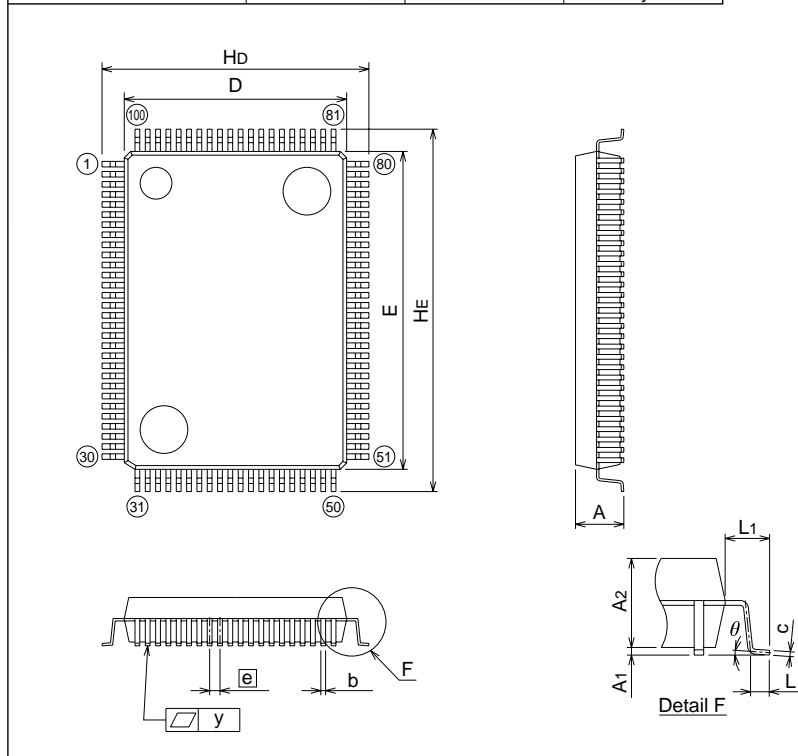
PRELIMINARY
 Notice: This is not a final specification.
 Some parametric limits are subject to change.

PACKAGE OUTLINE

100P6S-A

Plastic 100pin 14X20mm body QFP

| | | | |
|--------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| QFP100-P-1420-0.65 | — | 1.58 | Alloy 42 |



Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|------|------|
| | Min | Nom | Max |
| A | — | — | 3.05 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | — | 2.8 | — |
| b | 0.25 | 0.3 | 0.4 |
| c | 0.13 | 0.15 | 0.2 |
| D | 13.8 | 14.0 | 14.2 |
| E | 19.8 | 20.0 | 20.2 |
| e | — | 0.65 | — |
| Hd | 16.5 | 16.8 | 17.1 |
| HE | 22.5 | 22.8 | 23.1 |
| L | 0.4 | 0.6 | 0.8 |
| L1 | — | 1.4 | — |
| y | — | — | 0.1 |
| θ | 0° | — | 10° |
| b2 | — | 0.35 | — |
| l2 | 1.3 | — | — |
| MD | — | 14.6 | — |
| ME | — | 20.6 | — |

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REVISION DESCRIPTION LIST

M37920S4CGP Datasheet

| Rev. No. | Revision Description | Rev. date |
|----------|----------------------|-----------|
| 1.00 | First Edition | 990916 |
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