38B7 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38B7 group is the 8-bit microcomputer based on the 740 family core technology.

The 38B7 group has six 8-bit timers, one 16-bit timer, a fluorescent display automatic display circuit, 16-channel 10-bit A-D converter, a serial I/O with automatic transfer function, which are available for controlling musical instruments and household appliances.

The 38B7 group has variations of internal memory type. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 38B7 group, refer to the section on group expansion.

Built-in pull-down resistors connected to high-breakdown voltage ports are available by specifying with the mask option in the mask ROM version. For the details, refer to the section on the mask option of pull-down resistor.

FEATURES

<Microcomputer mode>

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.48 µs
  (at 4.19 MHz oscillation frequency)
- Memory size
  ROM ..... 60K bytes
  RAM ..... 2048 bytes
- Programmable input/output ports 75
- High-breakdown-voltage output ports 52
- Software pull-up resistors. (Ports $P6_4$ to $P6_7$, P7, $P8_0$ to $P8_3$, P9, PA, PB)
- Interrupts ..... 22 sources, 16 vectors
- Timers ..... 8-bit × 6, 16-bit × 1
- Serial I/O1 (Clock-synchronized) ..... 8-bit × 1
  (max. 256-byte automatic transfer function)
- Serial I/O2 (UART or Clock-synchronized) ..... 8-bit × 1
- Serial I/O3 (Clock-synchronized) ..... 8-bit × 1
- PWM ..... 14-bit × 1
  8-bit × 1 (also functions as timer 6)
- A-D converter ..... 10-bit × 16 channels
- D-A converter ..... 1 channel
- Fluorescent display function ..... Total 56 control pins
- Interrupt interval determination function 1
  (Serviceable even in low-speed mode)
- Watchdog timer ..... 16-bit × 1
- Buzzer output 1
- Two clock generating circuits
  Main clock (X_{IN}–X_{OUT}) ..... Internal feedback resistor
  Sub-clock (X_{CIN}–X_{COUT}) ..... Without internal feedback resistor
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode ..... 4.0 to 5.5 V
  (at 4.19 MHz oscillation frequency and high-speed selected)
  In middle-speed mode ..... 2.7 to 5.5 V (*)
  (at 4.19 MHz oscillation frequency and middle-speed selected)
  In low-speed mode ..... 2.7 to 5.5 V (*)
  (at 32 kHz oscillation frequency)
  (*: 4.0 to 5.5 V for Flash memory version)
- Power dissipation
  In high-speed mode ..... 35 mW
  (at 4.19 MHz oscillation frequency)
  In low-speed mode ..... 60 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... –20 to 85 °C

<Flash memory mode>

- Supply voltage ..... V_{CC} = 5 V ± 10 %
- Program/Erase voltage ..... V_{PP} = 11.7 to 12.6 V
- Programming method ..... Programming in unit of byte
- Erasing method
  Batch erasing ..... Parallel/Serial I/O mode
  Block erasing ..... CPU reprogramming mode
- Program/Erase control by software command
- Number of times for programming/erasing 100
- Operating temperature range (at programming/erasing)
  ..... Normal temperature

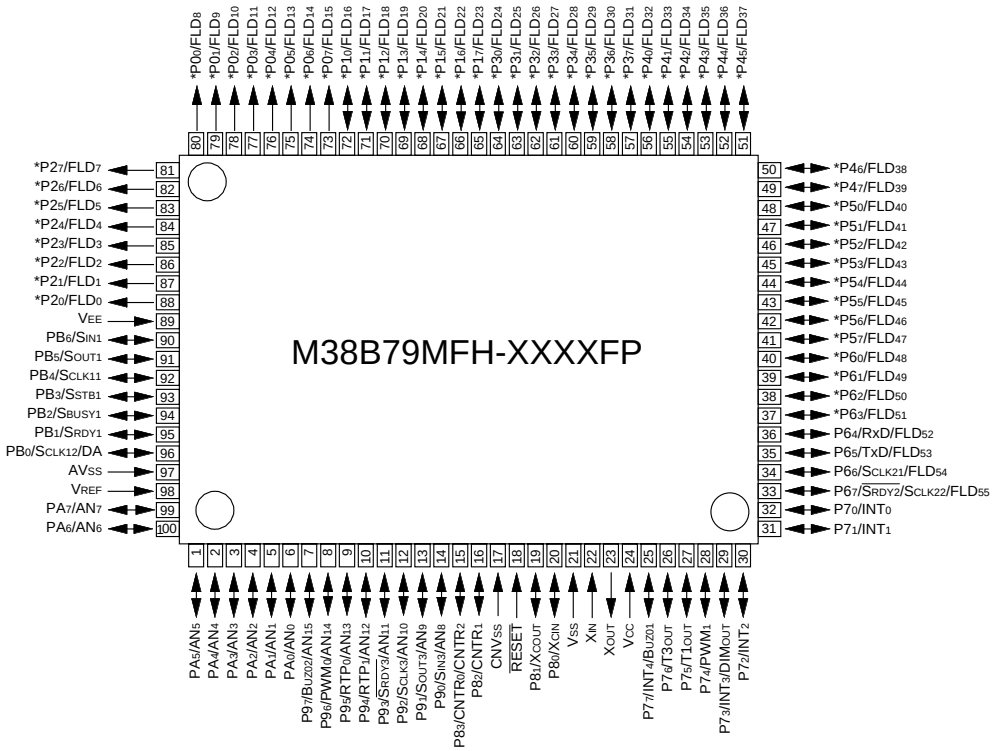
■Notes

1. The flash memory version cannot be used for application embedded in the MCU card.
2. Power source voltage Vcc of the flash memory version is 4.0 to 5.5 V.

APPLICATION

Musical instruments, VCR, household appliances, etc.

PIN CONFIGURATION (TOP VIEW)



*High-breakdown-voltage output port: Totaling 52

Package type: 100P6S-A

Fig. 1 Pin configuration of M38B79MFH-XXXXFP

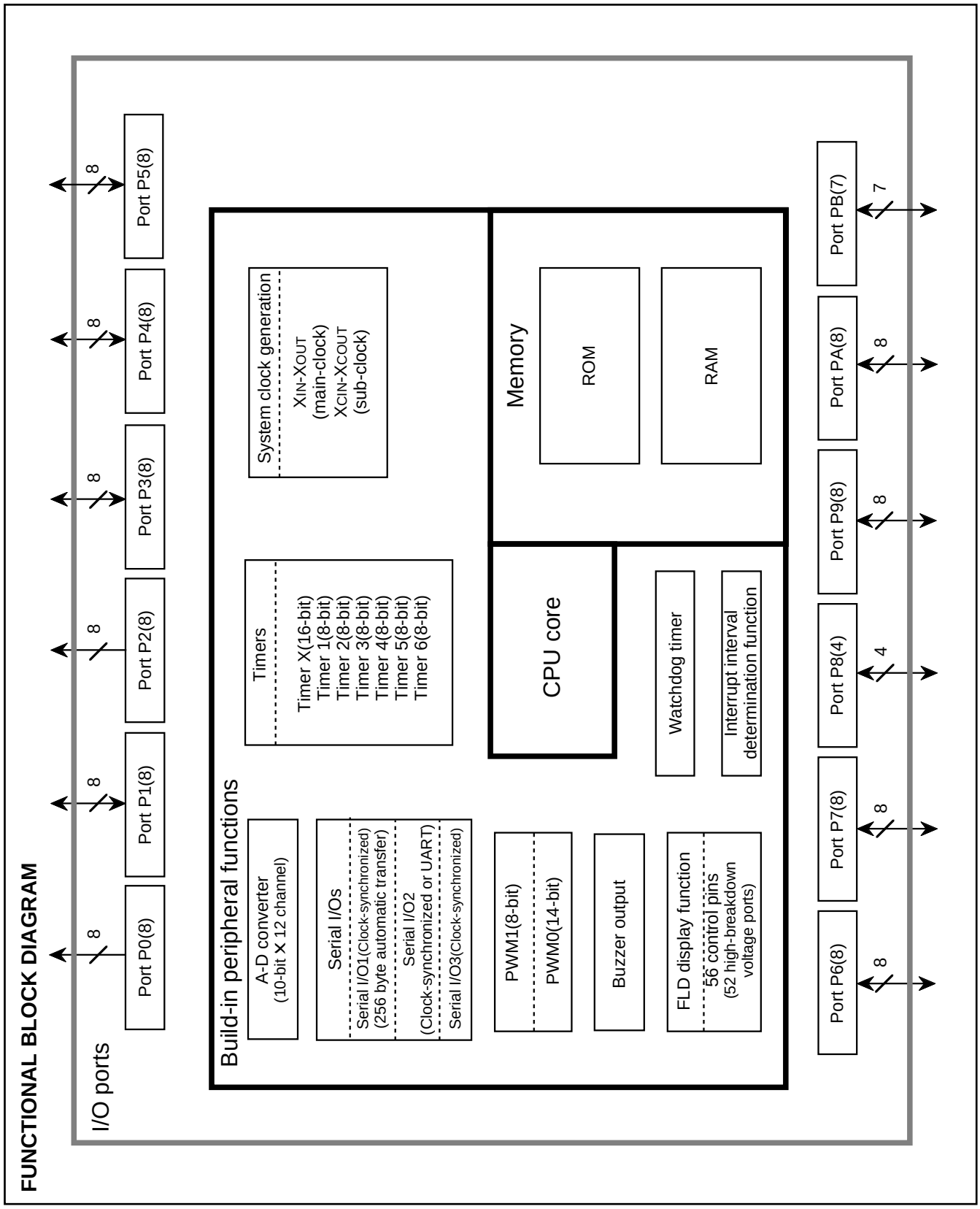


Fig. 2 Functional block diagram

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 4.0–5.5 V to V_{CC}, and 0 V to V_{SS}.	
CNV_{SS}	CNV_{SS}	• Connect to V_{SS}. • VPP power input pin in flash memory mode.	
V_{EE}	Pull-down power source	• Apply voltage supplied to pull-down resistors of ports P0, P1, P2 and P3.	
V_{REF}	Reference voltage	• Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	• Analog power source input pin for A-D converter. • Connect to V_{SS}.	
$\overline{RESET}$	Reset input	• Reset input pin for active “L”.	
X_{IN}	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between X_{IN} pin and X_{OUT} pin. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. • When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • The clock is used as the oscillating source of system clock.	
X_{OUT}	Clock output		
$P0_0/FLD_8$–$P0_7/FLD_{15}$	Output port P0	• 8-bit output port. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is built in between port P0 and the V_{EE} pin. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P1_0/FLD_{16}$–$P1_7/FLD_{23}$	I/O port P1	• 8-bit I/O port. • I/O direction register allows each pin to be individually programmed as either input or output. • At reset, this port is set to input mode. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is built in between port P1 and the V_{EE} pin. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P2_0/FLD_0$–$P2_7/FLD_7$	Output port P2	• 8-bit output port with the same function as port P0. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is built in between port P2 and the V_{EE} pin. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P3_0/FLD_{24}$–$P3_7/FLD_{31}$	I/O port P3	• 8-bit I/O port with the same function as port P1. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is built in between port P3 and the V_{EE} pin. • At reset, this port is set to V_{EE} level.	• FLD automatic display pins
$P4_0/FLD_{32}$–$P4_7/FLD_{39}$	I/O port P4	• 8-bit I/O port with the same function as port P1. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is not built in between port P4 and the V_{EE} pin.	• FLD automatic display pins
$P5_0/FLD_{40}$–$P5_7/FLD_{47}$	I/O port P5	• 8-bit I/O port with the same function as port P1. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is not built in between port P5 and the V_{EE} pin.	• FLD automatic display pins
$P6_0/FLD_{48}$–$P6_3/FLD_{51}$	I/O port P6	• 4-bit I/O port with the same function as port P1. • Low-voltage input level. • High-breakdown-voltage P-channel open-drain output structure. • A pull-down resistor is not built in between port P6 and the V_{EE} pin.	• FLD automatic display pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P64/RxD/FLD52, P65/TxD/FLD53, P66/SCLK21/FLD54, P67/$\overline{\text{SRDY2}}$/SCLK22/FLD55,	I/O port P6	• 4-bit I/O port . • Low-voltage input level for input ports. • CMOS compatible input level for RxD, SCLK21, SCLK22. • CMOS 3-state output structure.	• FLD automatic display pins • Serial I/O2 function pins
P70/INT0, P71/INT1, P72/INT2,	I/O port P7	• 8-bit I/O port. • CMOS compatible input level. • CMOS 3-state output structure.	• Interrupt input pins
P73/INT3/DIMOUT,			• Interrupt input pin • Dimmer signal output pin
P74/PWM1			• PWM output pin
P75/T1OUT, P76/T3OUT,			• Timer output pins
P77/INT4/BUZ01			• Interrupt input pin • Buzzer output pin
P80/XCIN, P81/XCOUT	I/O port P8	• 4-bit I/O port with the same function as port P7. • CMOS compatible input level. • CMOS 3-state output structure.	• I/O pins for sub-clock generating circuit (connect a ceramic resonator or a quarts-crystal oscillator)
P82/CNTR1, P83/CNTR0/CNTR2			• Timer input pin • Timer I/O pin
P90/SIN3/AN8, P91/SOUT3/AN9, P92/SCLK3/AN10, P93/$\overline{\text{SRDY3}}$/AN11,	I/O port P9	• 8-bit I/O port with the same function as port P7. • CMOS compatible input level. • CMOS 3-state output structure.	• Serial I/O3 function pins • A-D converter input pins
P94/RTP1/AN12, P95/RTP0/AN13			• Real time port output pins • A-D converter input pins
P96/PWM0/AN14			• 14-bit PWM output pin • A-D converter input pin
P97/BUZ02/AN15			• Buzzer output pin • A-D converter input pin
PA0/AN0–PA7/AN7	I/O port PA	• 8-bit I/O port with the same function as port P7. • CMOS compatible input level. • CMOS 3-state output structure.	• A-D converter input pin
PB0/SCLK12/DA	I/O port PB	• 7-bit I/O port with the same function as port P7. • CMOS compatible input level. • CMOS 3-state output structure.	• Serial I/O1 function pin • D-A converter output pin
PB1/SRDY1, PB2/SBUSY1, PB3/SSTB1, PB4/SCLK11, PB5/SOUT1, PB6/SIN1			• Serial I/O1 function pins

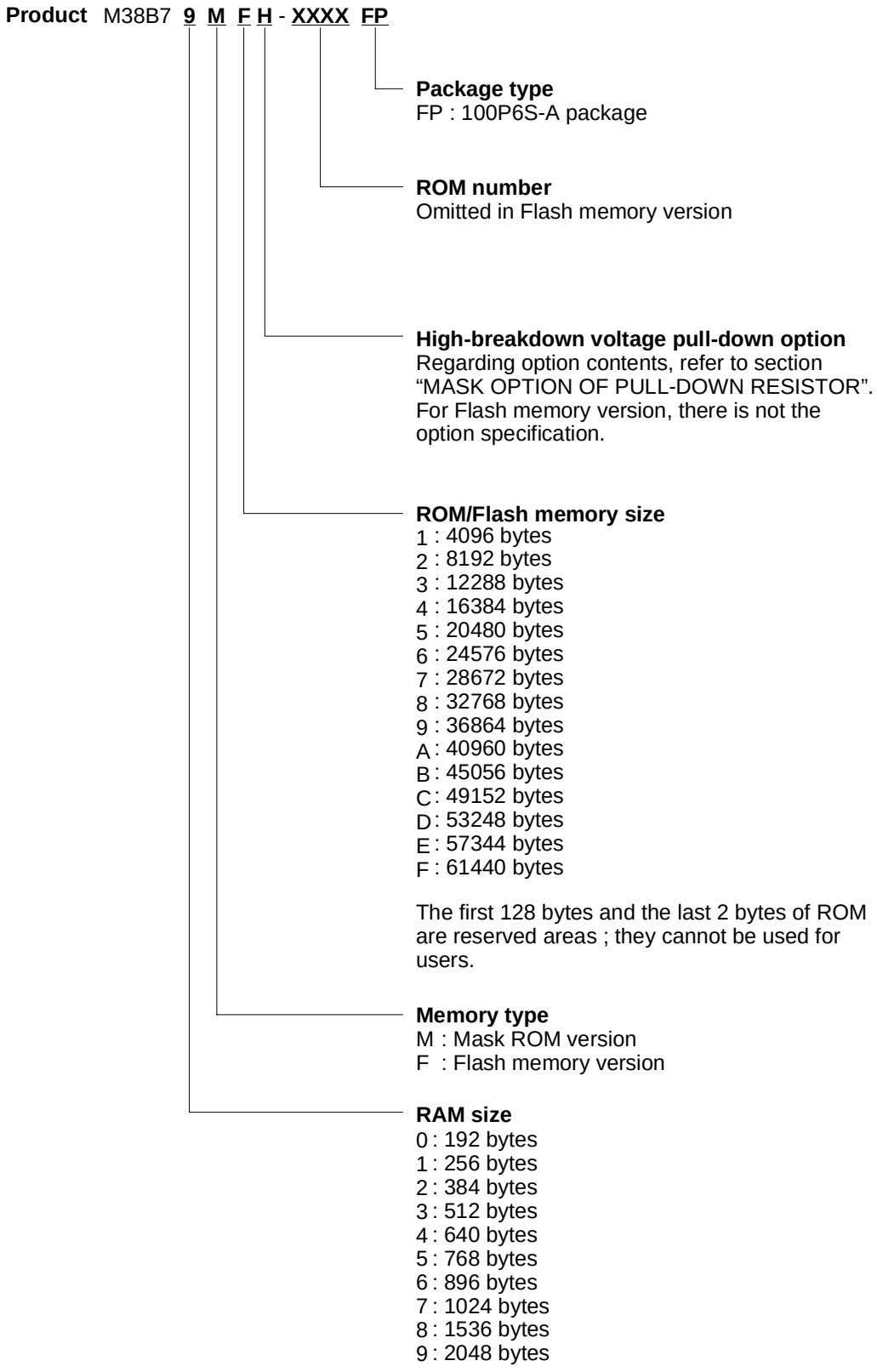


Fig. 3 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 38B7 group as follows.

Memory Type

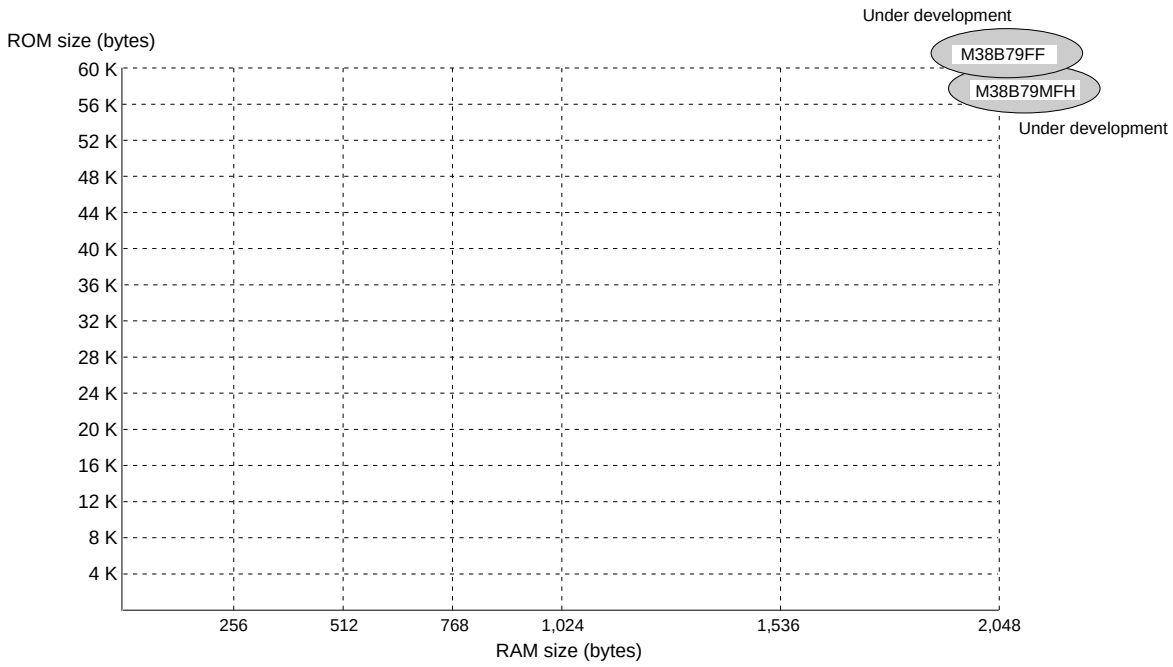
Support for Mask ROM and Flash memory versions.

Memory Size

Flash memory size ..... 60K bytes
Mask ROM size ..... 60K bytes
RAM size ..... 2048 bytes

Package

100P6S-A ..... 0.65 mm-pitch plastic molded QFP



Note : Products under development: the development schedule and specifications may be revised without notice.

Fig. 4 Memory expansion plan

Currently supported products are listed below.

Table 3 List of supported products **As of Mar. 2000**

Product	ROM size (bytes) ROM size for User ( )	RAM size (bytes)	Package	Remarks
M38B79MFH-XXXXFP	61440	2048	100P6S-A	Mask ROM version
M38B79FFFP	(61310)			Flash memory version

FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The 38B7 group uses the standard 740 Family instruction set. Refer to the table of 740 Series addressing modes and machine instructions or the 740 Series Software Manual for details on the instruction set.

Machine-resident 740 Series instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

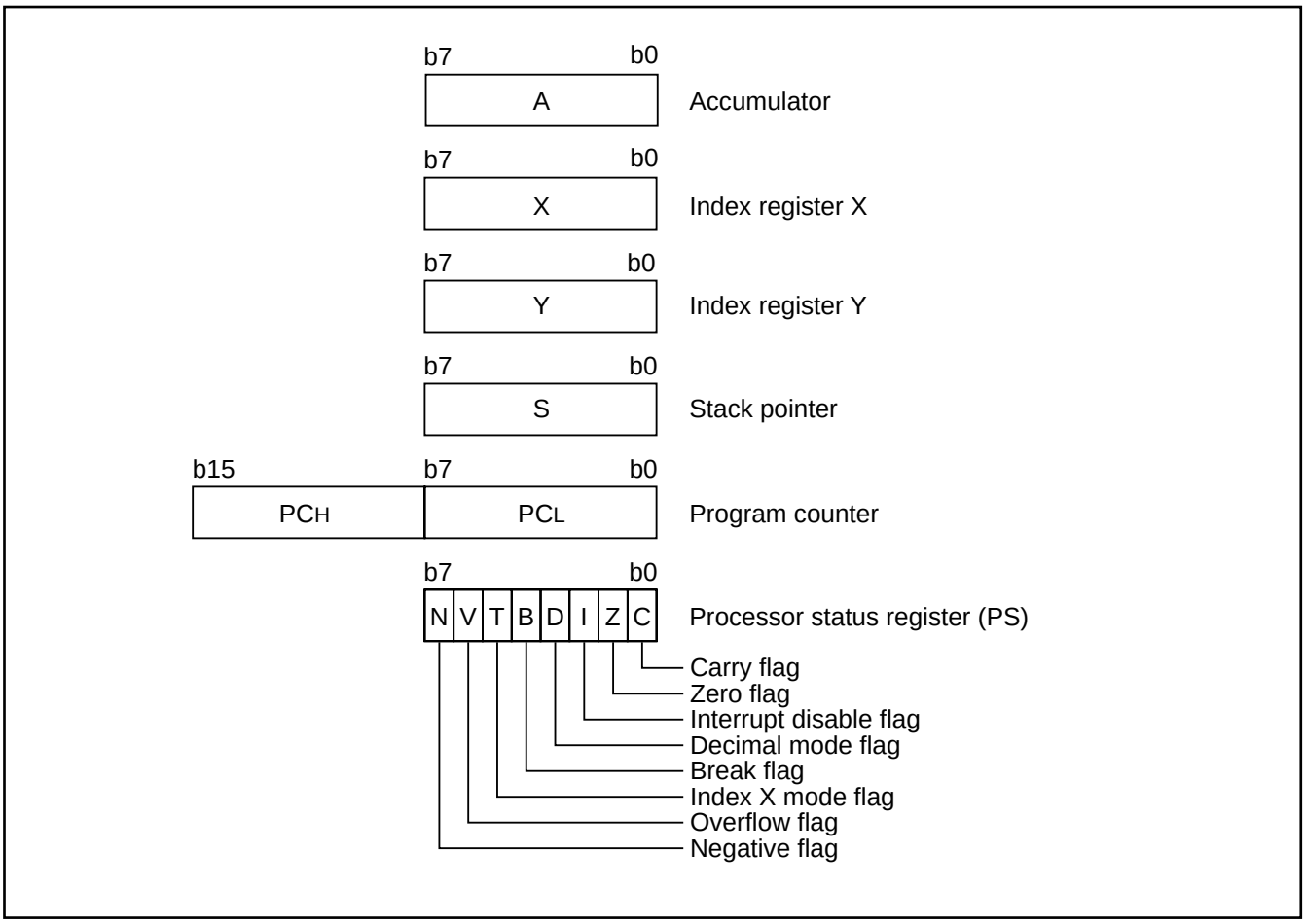


Fig. 5 740 Family CPU register structure

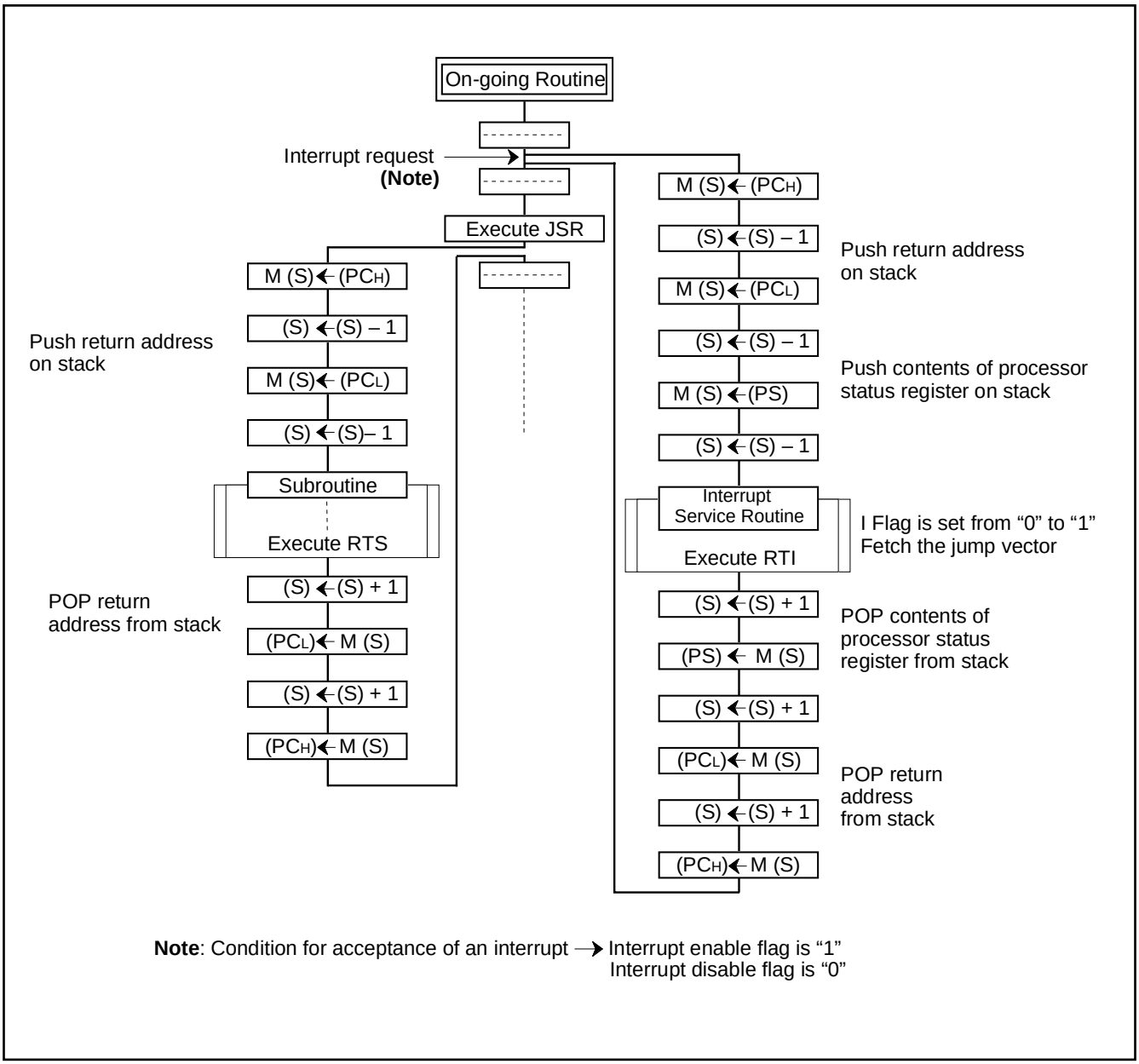


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit etc.
The CPU mode register is allocated at address 003B16.

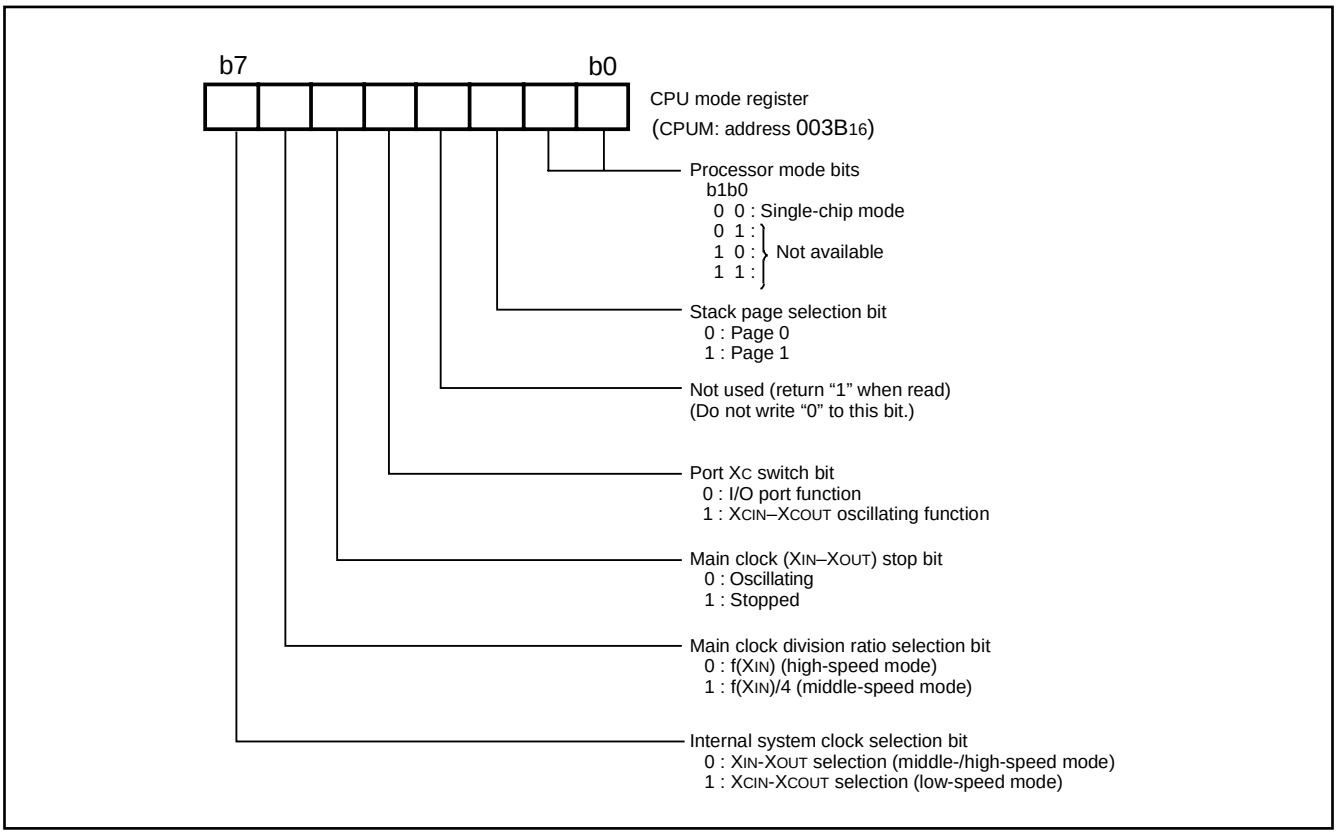


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area contains control registers for I/O ports, timers and other functions.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing, and the other areas are user areas for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

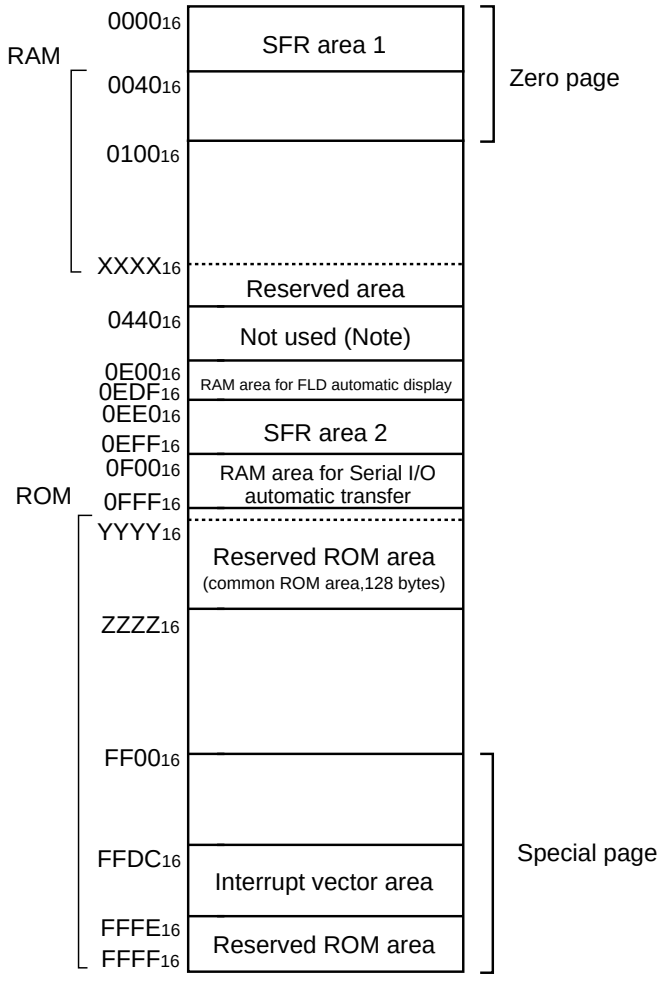
The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (byte)	Address XXXX16
192	00FF16
256	013F16
384	01BF16
512	023F16
640	02BF16
768	033F16
896	03BF16
1024	043F16
1536	063F16
2048	083F16

ROM area

ROM size (byte)	Address YYYY16	Address ZZZZ16
4096	F00016	F08016
8192	E00016	E08016
12288	D00016	D08016
16384	C00016	C08016
20480	B00016	B08016
24576	A00016	A08016
28672	900016	908016
32768	800016	808016
36864	700016	708016
40960	600016	608016
45056	500016	508016
49152	400016	408016
53248	300016	308016
57344	200016	208016
61440	100016	108016



Note: When 1024 bytes or more are used as RAM area, this area can be used.

Fig. 8 Memory map diagram

0000₁₆	Port P0 (P0)
0001₁₆	
0002₁₆	Port P1 (P1)
0003₁₆	Port P1 direction register (P1D)
0004₁₆	Port P2 (P2)
0005₁₆	
0006₁₆	Port P3 (P3)
0007₁₆	Port P3 direction register (P3D)
0008₁₆	Port P4 (P4)
0009₁₆	Port P4 direction register (P4D)
000A₁₆	Port P5 (P5)
000B₁₆	Port P5 direction register (P5D)
000C₁₆	Port P6 (P6)
000D₁₆	Port P6 direction register (P6D)
000E₁₆	Port P7 (P7)
000F₁₆	Port P7 direction register (P7D)
0010₁₆	Port P8 (P8)
0011₁₆	Port P8 direction register (P8D)
0012₁₆	Port P9 (P9)
0013₁₆	Port P9 direction register (P9D)
0014₁₆	Port PA (PA)
0015₁₆	Port PA direction register (PAD)
0016₁₆	Port PB (PB)
0017₁₆	Port PB direction register (PBD)
0018₁₆	Serial I/O1 automatic transfer data pointer (SIO1DP)
0019₁₆	Serial I/O1 control register 1 (SIO1CON1)
001A₁₆	Serial I/O1 control register 2 (SIO1CON2)
001B₁₆	Serial I/O1 register/Transfer counter (SIO1)
001C₁₆	Serial I/O1 control register 3 (SIO1CON3)
001D₁₆	Serial I/O2 control register (SIO2CON)
001E₁₆	Serial I/O2 status register (SIO2STS)
001F₁₆	Serial I/O2 transmit/receive buffer register (TB/RB)

0020₁₆	Timer 1 (T1)
0021₁₆	Timer 2 (T2)
0022₁₆	Timer 3 (T3)
0023₁₆	Timer 4 (T4)
0024₁₆	Timer 5 (T5)
0025₁₆	Timer 6 (T6)
0026₁₆	PWM control register (PWMCON)
0027₁₆	Timer 6 PWM register (T6PWM)
0028₁₆	Timer 12 mode register (T12M)
0029₁₆	Timer 34 mode register (T34M)
002A₁₆	Timer 56 mode register (T56M)
002B₁₆	D-A conversion register (DA)
002C₁₆	Timer X (low-order) (TXL)
002D₁₆	Timer X (high-order) (TXH)
002E₁₆	Timer X mode register 1 (TXM1)
002F₁₆	Timer X mode register 2 (TXM2)
0030₁₆	Interrupt interval determination register (IID)
0031₁₆	Interrupt interval determination control register (IIDCON)
0032₁₆	AD/DA control register (ADCON)
0033₁₆	A-D conversion register (low-order) (ADL)
0034₁₆	A-D conversion register (high-order) (ADH)
0035₁₆	PWM register (high-order) (PWMH)
0036₁₆	PWM register (low-order) (PWML)
0037₁₆	Baud rate generator (BRG)
0038₁₆	UART control register (UARTCON)
0039₁₆	Interrupt source switch register (IFR)
003A₁₆	Interrupt edge selection register (INTEDGE)
003B₁₆	CPU mode register (CPUM)
003C₁₆	Interrupt request register 1(IREQ1)
003D₁₆	Interrupt request register 2(IREQ2)
003E₁₆	Interrupt control register 1(ICON1)
003F₁₆	Interrupt control register 2(ICON2)

0EEC₁₆	Serial I/O3 control register (SIO3CON)
0EED₁₆	Serial I/O3 register (SIO3)
0EEE₁₆	Watchdog timer control register (WDTCON)
0EEF₁₆	Pull-up control register 3 (PULL3)
0EF0₁₆	Pull-up control register 1 (PULL1)
0EF1₁₆	Pull-up control register 2 (PULL2)
0EF2₁₆	Port P0 digit output set switch register (P0DOR)
0EF3₁₆	Port P2 digit output set switch register (P2DOR)
0EF4₁₆	FLDC mode register (FLDM)
0EF5₁₆	Tdisp time set register (TDISP)

0EF6₁₆	Toff1 time set register (TOFF1)	
0EF7₁₆	Toff2 time set register (TOFF2)	
0EF8₁₆	FLD data pointer (FLDDP)	
0EF9₁₆	Port P4 FLD/Port switch register (P4FPR)	
0EFA₁₆	Port P5 FLD/Port switch register (P5FPR)	
0EFB₁₆	Port P6 FLD/Port switch register (P6FPR)	
0EFC₁₆	FLD output control register (FLDCON)	
0EFD₁₆	Buzzer output control register (BUZCON)	
0EFE₁₆	Flash memory control register (FCON)	**(Note)**
0EFF₁₆	Flash command register (FCMD)	**(Note)**

Note: Flash memory version only.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS
[Direction Registers] PiD

The 38B7 group has 75 programmable I/O pins arranged in ten individual I/O ports (P1, P3, P4, P5, P6, P7, P8, P9, PA and PB). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that pin, that pin becomes an output pin. If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input (the bit corresponding to that pin must be set to "0") are floating and the value of that pin can be read. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[High-Breakdown-Voltage Output Ports]

The 38B7 group has seven ports with high-breakdown-voltage pins (ports P0 to P5 and $P6_0$–$P6_3$). The high-breakdown-voltage ports have P-channel open-drain output with Vcc – 45 V of breakdown voltage. Each pin in ports P0 to P3 has an internal pull-down resistor connected to VEE. At reset, the P-channel output transistor of each port latch is turned off, so that it goes to VEE level ("L") by the pull-down resistor.

Writing "1" (weak drivability) to bit 7 of the FLDC mode register (address $0EF4_{16}$) shows the rising transition of the output transistors for reducing transient noise. At reset, bit 7 of the FLDC mode register is set to "0" (strong drivability).

[Pull-up Control Register] PULL

Ports $P6_4$–$P6_7$, P7, $P8_0$–$P8_3$, P9, PA and PB have built-in programmable pull-up resistors. The pull-up resistors are valid only in the case that the each control bit is set to "1" and the corresponding port direction registers are set to input mode.

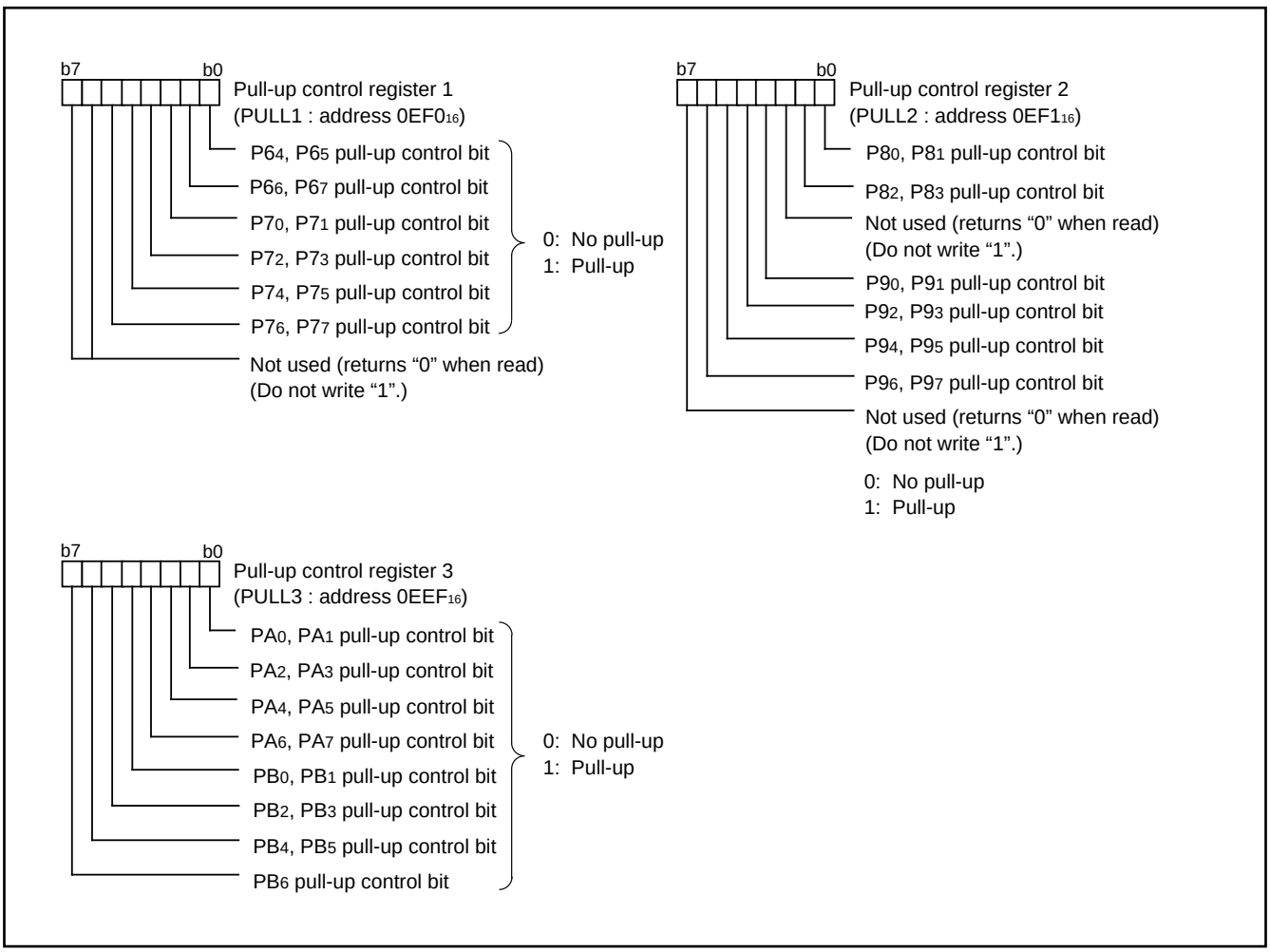


Fig. 10 Structure of pull-up control registers (PULL1, PULL2 and PULL3)

Table 6 List of I/O port functions (1)

Pin	Nama	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P00/FLD8– P07/FLD15	Port P0	Output	High-breakdown voltage P-channel open-drain output with pull-down resistor	FLD automatic display function	FLDC mode register P0 digit output set switch register	(1)
P10/FLD16– P17/FLD23	Port P1	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(2)
P20/FLD0– P27/FLD7	Port P2	Output	High-breakdown voltage P-channel open-drain output with pull-down resistor		FLDC mode register P2 digit output set switch register	(1)
P30/FLD24– P37/FLD31	Port P3	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output with pull-down resistor		FLDC mode register	(2)
P40/FLD32– P47/FLD39	Port P4	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output		FLDC mode register Port P4 FLD/Port switch register	(2)
P50/FLD40– P57/FLD47	Port P5	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output		FLDC mode register Port P5 FLD/Port switch register	(2)
P60/FLD48– P63/FLD51	Port P6	Input/output, individual bits	Low-voltage input level High-breakdown voltage P-channel open-drain output		FLDC mode register Port P6 FLD/Port switch register	(2)
P64/RxD/ FLD52			Low-voltage input level (port input) CMOS compatible input level (RxD, SCLK21, SCLK22) CMOS 3-state output	FLD automatic display function Serial I/O2 function I/O	FLDC mode register Serial I/O2 control register UART control register	(3)
P65/TxD/ FLD53, P66/SCLK21/ FLD54						(4)
P67/$\overline{\text{SRDY2}}$/ SCLK22/ FLD55						(5)
P70/INT0, P71/INT1	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrput input	Interrupt edge selection register	(6)
P72/INT2					Interrupt edge selection register Interrupt interval determination control register	
P73/INT3/ DIMOUT				External interrput input Dimmer signal output	Interrupt edge selection register FLD output control register	(7)
P74/PWM1				PWM output	Timer 56 mode register	(8)
P75/T1OUT				Timer output	Timer 12 mode register	
P76/T3OUT				Timer output	Timer 34 mode register	
P77/INT4/ BUZ01				Buzzer output External interrput input	Buzzer output control register Interrupt edge selection register	(9)
P80/XCIN	Port P8	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	CPU mode register	(10)
P81/XCOUT						(11)
P82/CNTR1				External count input	Interrupt edge selection register	(6)
P83/CNTR0/ CNTR2						(12)

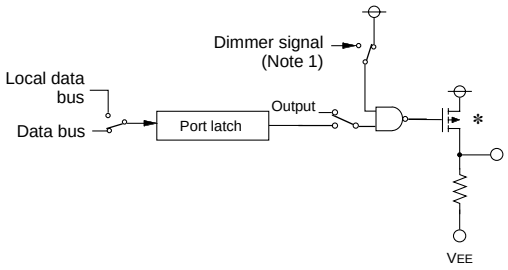
Table 7 List of I/O port functions (2)

Pin	Nama	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P90/SIN3/ AN8	Port P9	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O3 function I/O A-D conversion input	Serial I/O3 control register AD/DA control register	(6)
P91/SOUT3/ AN9,						(13)
P92/SCLK3/ AN10						
P93/$\overline{\text{SRDY3}}$/ AN11						(14)
P94/RTP1/ AN12,				Real time port output A-D conversion input	Timer X mode register 2 AD/DA control register	(15)
P95/RTP0/ AN13						
P96/PWM0/ AN14				PWM output A-D conversion input	PWM control register AD/DA control register	(16)
P97/BUZ02/ AN15				Buzzer output A-D conversion input	Buzzer output control register AD/DA control register	(16)
PA0/AN0– PA7/AN7	Port PA	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	AD/DA control register	(17)
PB0/SCLK12/ DA	Port PB	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O D-A conversion output	Serial I/O1 control registers 1, 2 AD/DA control register	(18)
PB1/SRDY1				Serial I/O1 function I/O	Serial I/O1 control registers 1, 2	(19)
PB2/SBUSY1						(18)
PB3/SSTB1						(20)
PB4/SCLK11						(21)
PB5/SOUT1						
PB6/SIN1						(6)

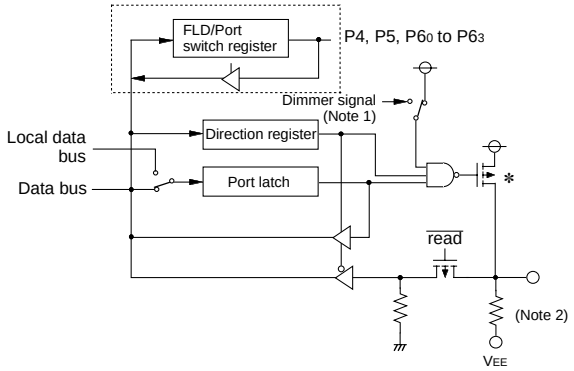
Notes 1 : How to use double-function ports as function I/O ports, refer to the applicable sections.

2 : Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

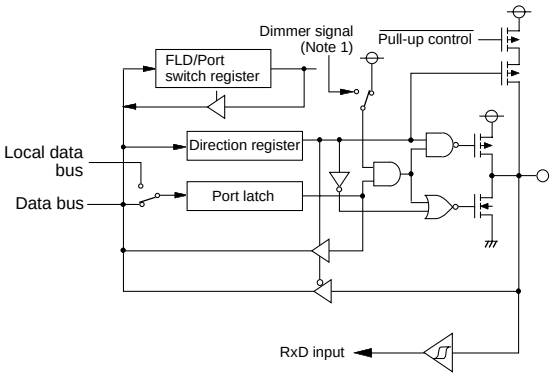
(1) Ports P0, P2



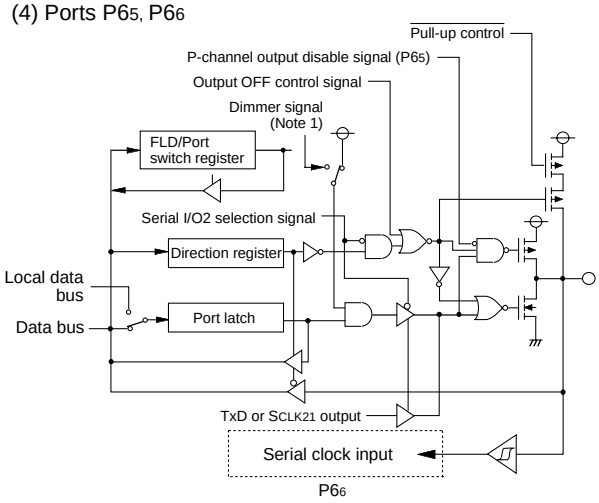
(2) Ports P1, P3, P4, P5, P6$_0$ to P6$_3$



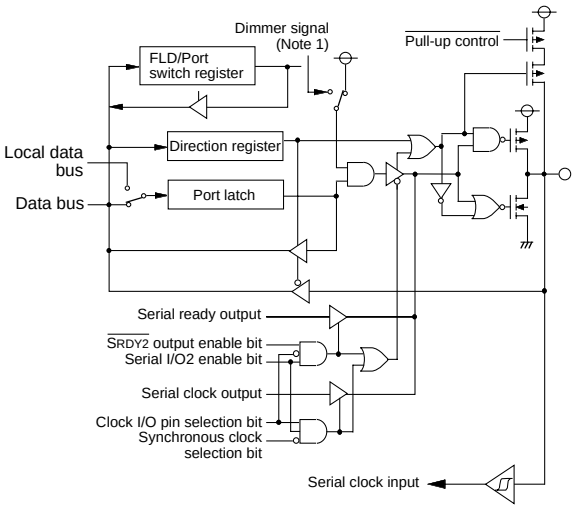
(3) Port P6$_4$



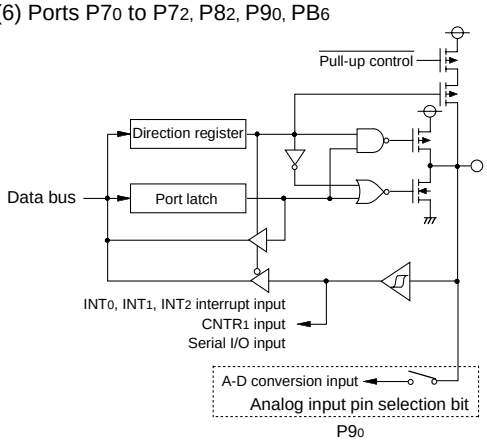
(4) Ports P6$_5$, P6$_6$



(5) Port P6$_7$



(6) Ports P7$_0$ to P7$_2$, P8$_2$, P9$_0$, PB$_6$



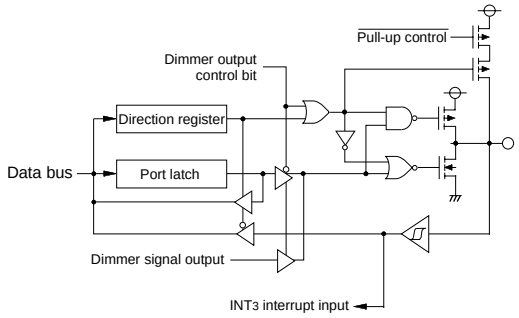
* High-breakdown-voltage P-channel transistor

Notes 1: The dimmer signal sets the Toff timing.

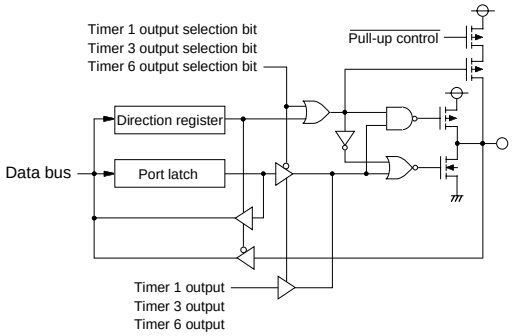
2: A pull-down resistor is not built in to ports P4, P5 and P6$_0$ to P6$_3$.

Fig. 11 Port block diagram (1)

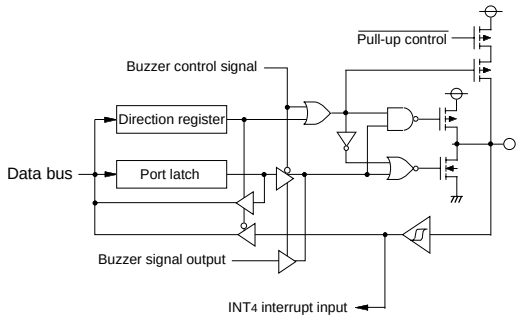
(7) Port P7$_3$



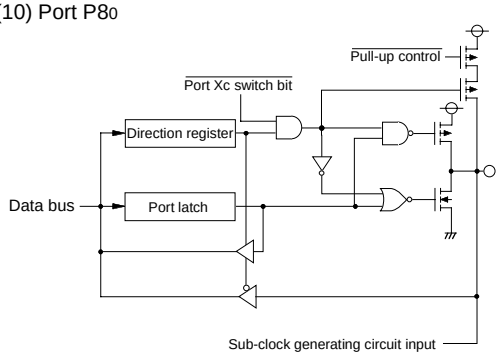
(8) Ports P7$_4$ to P7$_6$



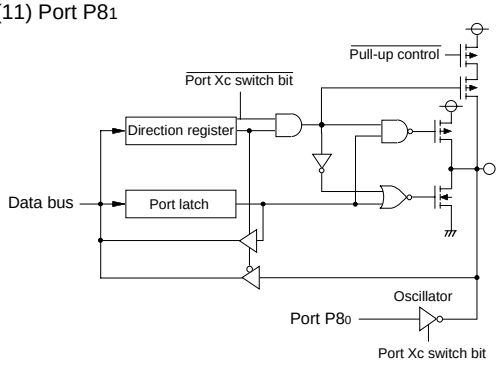
(9) Port P7$_7$



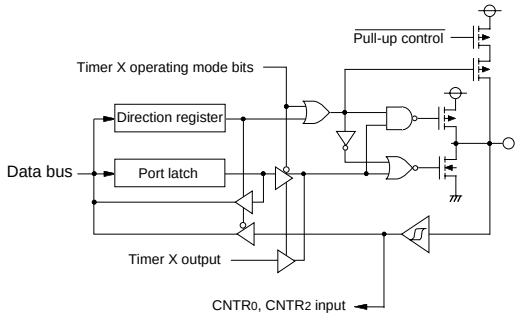
(10) Port P8$_0$



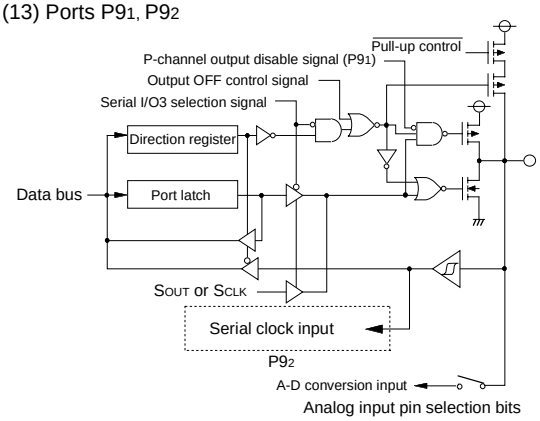
(11) Port P8$_1$



(12) Port P8$_3$



(13) Ports P9$_1$, P9$_2$



(14) Port P9$_3$

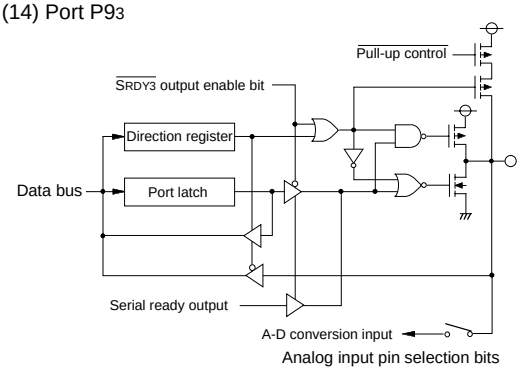


Fig. 12 Port block diagram (2)

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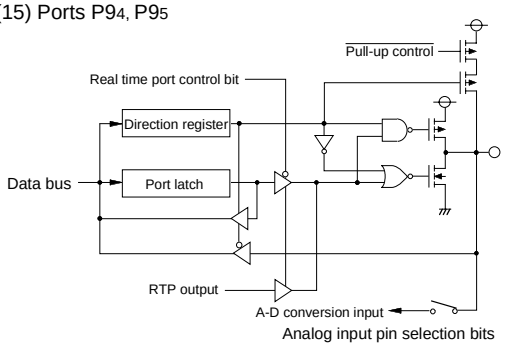
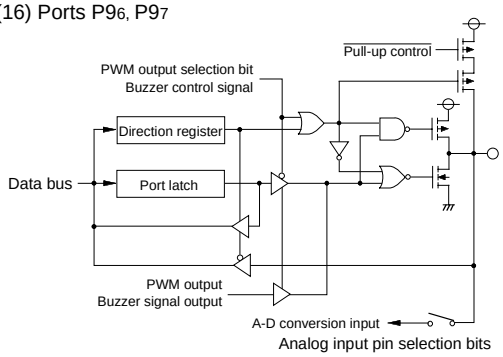
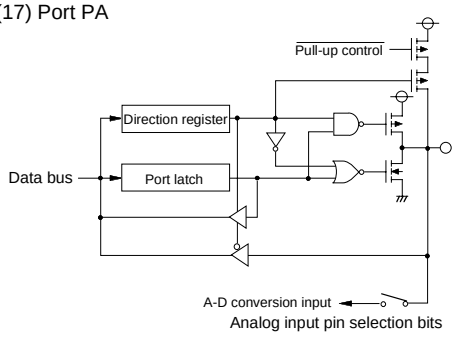
(15) Ports P9$_4$, P9$_5$



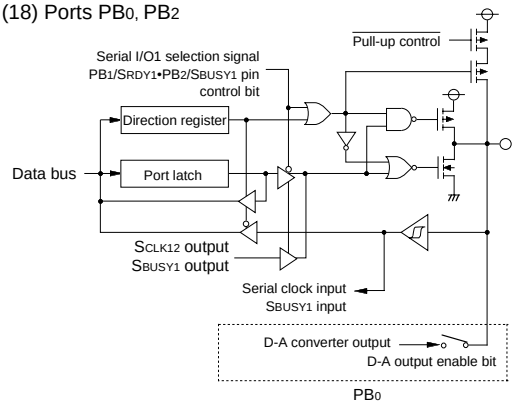
(16) Ports P9$_6$, P9$_7$



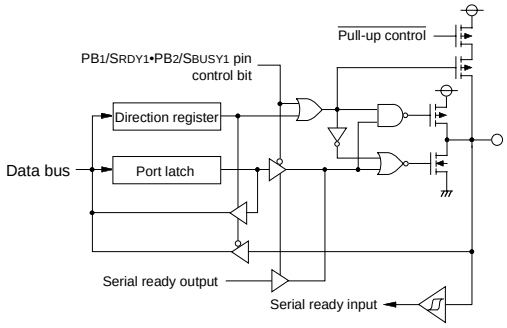
(17) Port PA



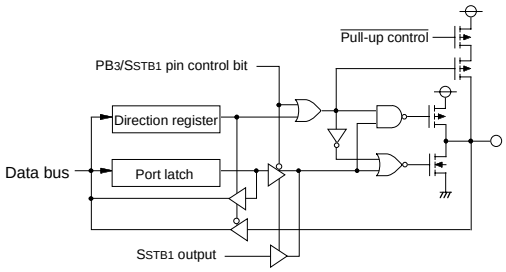
(18) Ports PB$_0$, PB$_2$



(19) Port PB$_1$



(20) Port PB$_3$



(21) Ports PB$_4$, PB$_5$

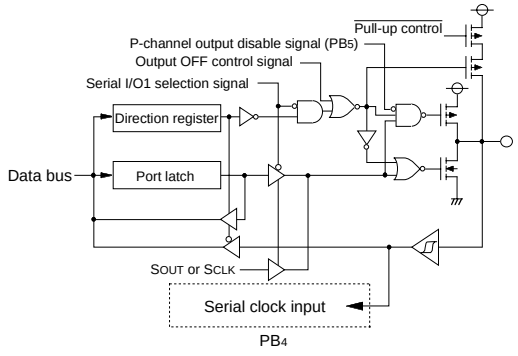


Fig. 13 Port block diagram (3)

INTERRUPTS

Interrupts occur by twenty two sources: five external, sixteen internal, and one software.

Interrupt Control

Each interrupt except the BRK instruction interrupt has both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0.” Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occur at the same time, the interrupt with highest priority is accepted first.

Interrupt Operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Interrupt Source Selection

Any of the following interrupt sources can be selected by the interrupt source switch register (address 0039_{16}).

1. INT_1 or Serial I/O3
2. INT_3 or Serial I/O2 transmit
3. INT_4 or A-D conversion

■Note

When the active edge of an external interrupt (INT_0–INT_4) is set or when switching interrupt sources in the same vector address, the corresponding interrupt request bit may also be set. Therefore, please take following sequence:

(1) Disable the external interrupt which is selected.
(2) Change the active edge in interrupt edge selection register
(3) Clear the set interrupt request bit to “0.”
(4) Enable the external interrupt which is selected.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable) Valid when INT1 interrupt is selected
Serial I/O3				At completion of data transfer	Valid when serial I/O3 is selected
INT2	4	FFF716	FFF616	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
Remote control/ counter overflow				At 8-bit counter overflow	Valid when interrupt interval determination is operating
Serial I/O1	5	FFF516	FFF416	At completion of data transfer	Valid when serial I/O ordinary mode is selected
Serial I/O auto-matic transfer				At completion of the last data transfer	Valid when serial I/O automatic transfer mode is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer 1	7	FFF116	FFF016	At timer 1 underflow	
Timer 2	8	FFEF16	FFEE16	At timer 2 underflow	STP release timer underflow
Timer 3	9	FFED16	FFEC16	At timer 3 underflow	
Timer 4	10	FFEB16	FFEA16	At timer 4 underflow	
Timer 5	11	FFE916	FFE816	At timer 5 underflow	
Timer 6	12	FFE716	FFE616	At timer 6 underflow	
Serial I/O2 receive	13	FFE516	FFE416	At completion of serial I/O2 data receive	
INT3	14	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable) Valid when INT3 interrupt is selected
Serial I/O2 transmit				At completion of serial I/O2 data transmit	
INT4	15	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable) Valid when INT4 interrupt is selected
A-D conversion				At completion of A-D conversion	Valid when A-D conversion is selected
FLD blanking	16	FFDF16	FFDE16	At falling edge of the last timing immediately before blanking period starts	Valid when FLD blanking interrupt is selected
FLD digit				At rising edge of digit (each timing)	Valid when FLD digit interrupt is selected
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

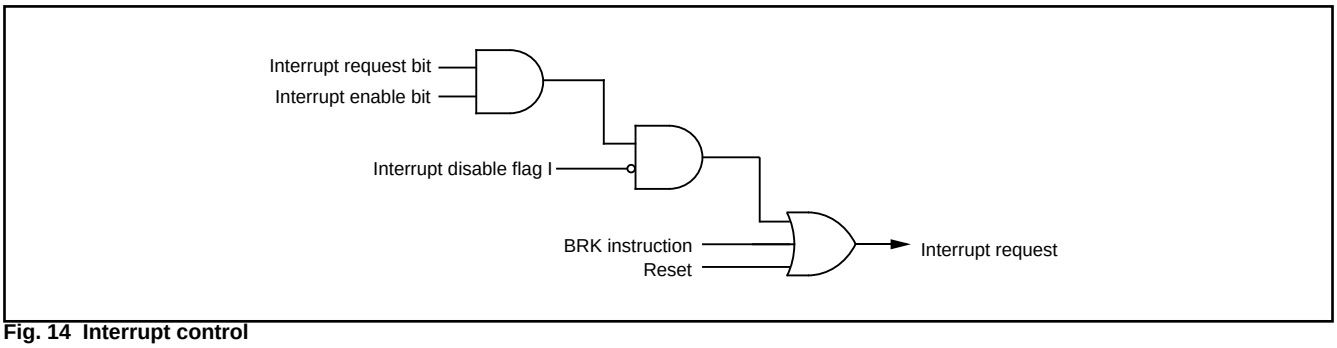


Fig. 14 Interrupt control

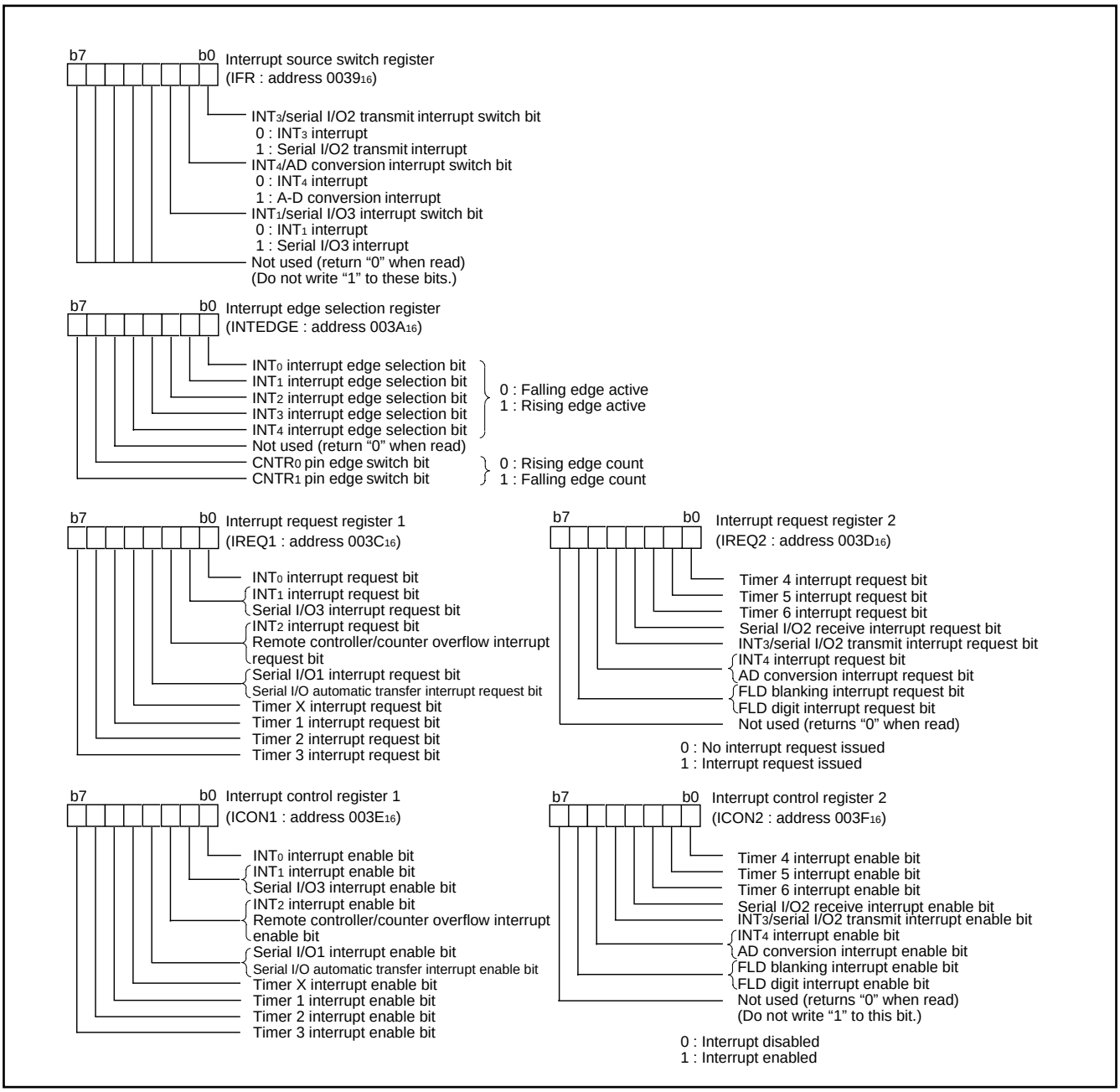


Fig. 15 Structure of interrupt related registers

TIMERS
8-Bit Timer

The 38B7 group has six built-in 8-bit timers : Timer 1, Timer 2, Timer 3, Timer 4, Timer 5, and Timer 6.

Each timer has the 8-bit timer latch. All timers are down-counters. When the timer reaches "00_{16}", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

The count can be stopped by setting the stop bit of each timer to "1". The internal system clock can be set to either the high-speed mode or low-speed mode with the CPU mode register. At the same time, the timer internal count source is switched to either f(X_{IN}) or f(X_{CIN}).

●Timer 1, Timer 2

The count sources of timer 1 and timer 2 can be selected by setting the timer 12 mode register. A rectangular waveform of timer 1 underflow signal divided by 2 can be output from the $P7_5$/$T1_{OUT}$ pin. The active edge of the external clock $CNTR_0$ can be switched with the bit 6 of the interrupt edge selection register.

At reset or when executing the STP instruction, all bits of the timer 12 mode register are cleared to "0", timer 1 is set to "FF_{16}", and timer 2 is set to "01_{16}".

●Timer 3, Timer 4

The count sources of timer 3 and timer 4 can be selected by setting the timer 34 mode register. A rectangular waveform of timer 3 underflow signal divided by 2 can be output from the $P7_6$/$T3_{OUT}$ pin. The active edge of the external clock $CNTR_1$ can be switched with the bit 7 of the interrupt edge selection register.

●Timer 5, Timer 6

The count sources of timer 5 and timer 6 can be selected by setting the timer 56 mode register. A rectangular waveform of timer 6 underflow signal divided by 2 can be output from the $P7_4$/PWM_1 pin.

●Timer 6 PWM_1 Mode

Timer 6 can output a PWM rectangular waveform with "H" duty cycle n/(n+m) from the $P7_4$/PWM_1 pin by setting the timer 56 mode register (refer to Figure 18). The n is the value set in timer 6 latch (address 0025_{16}) and m is the value in the timer 6 PWM register (address 0027_{16}). If n is "0," the PWM output is "L", if m is "0", the PWM output is "H" (n = 0 is prior than m = 0). In the PWM mode, interrupts occur at the rising edge of the PWM output.

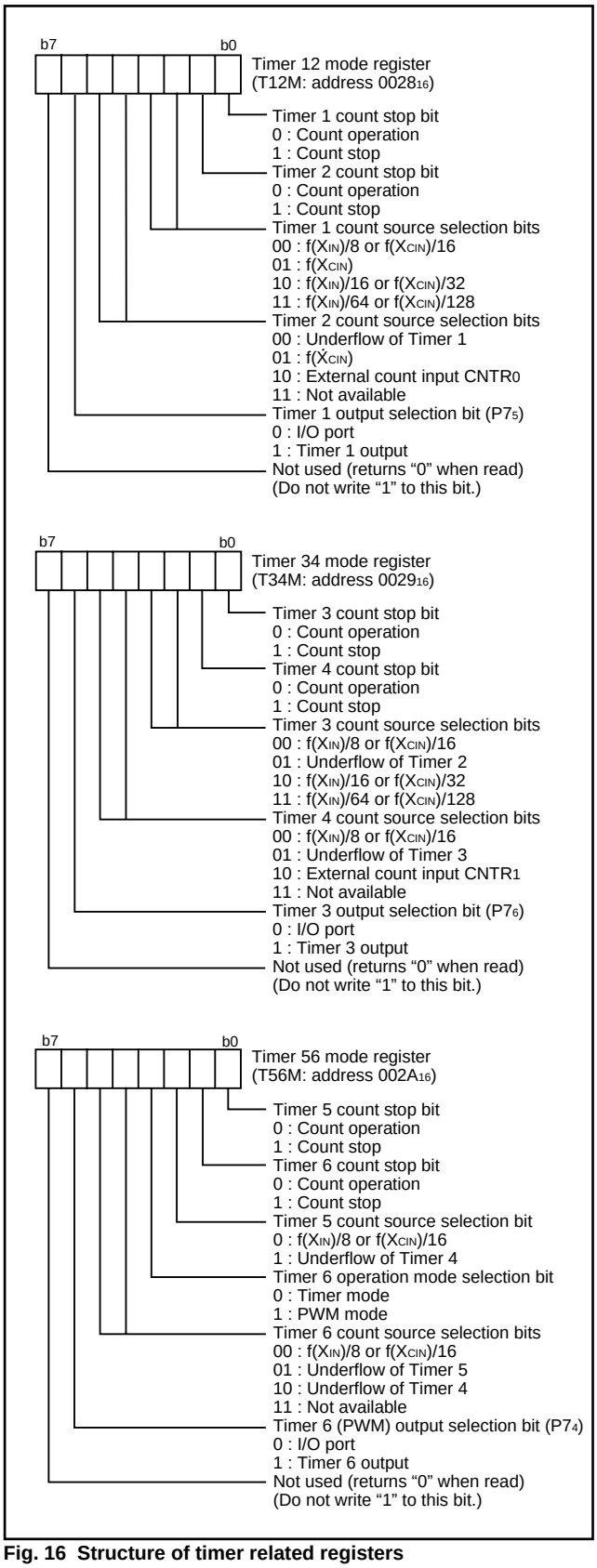


Fig. 16 Structure of timer related registers

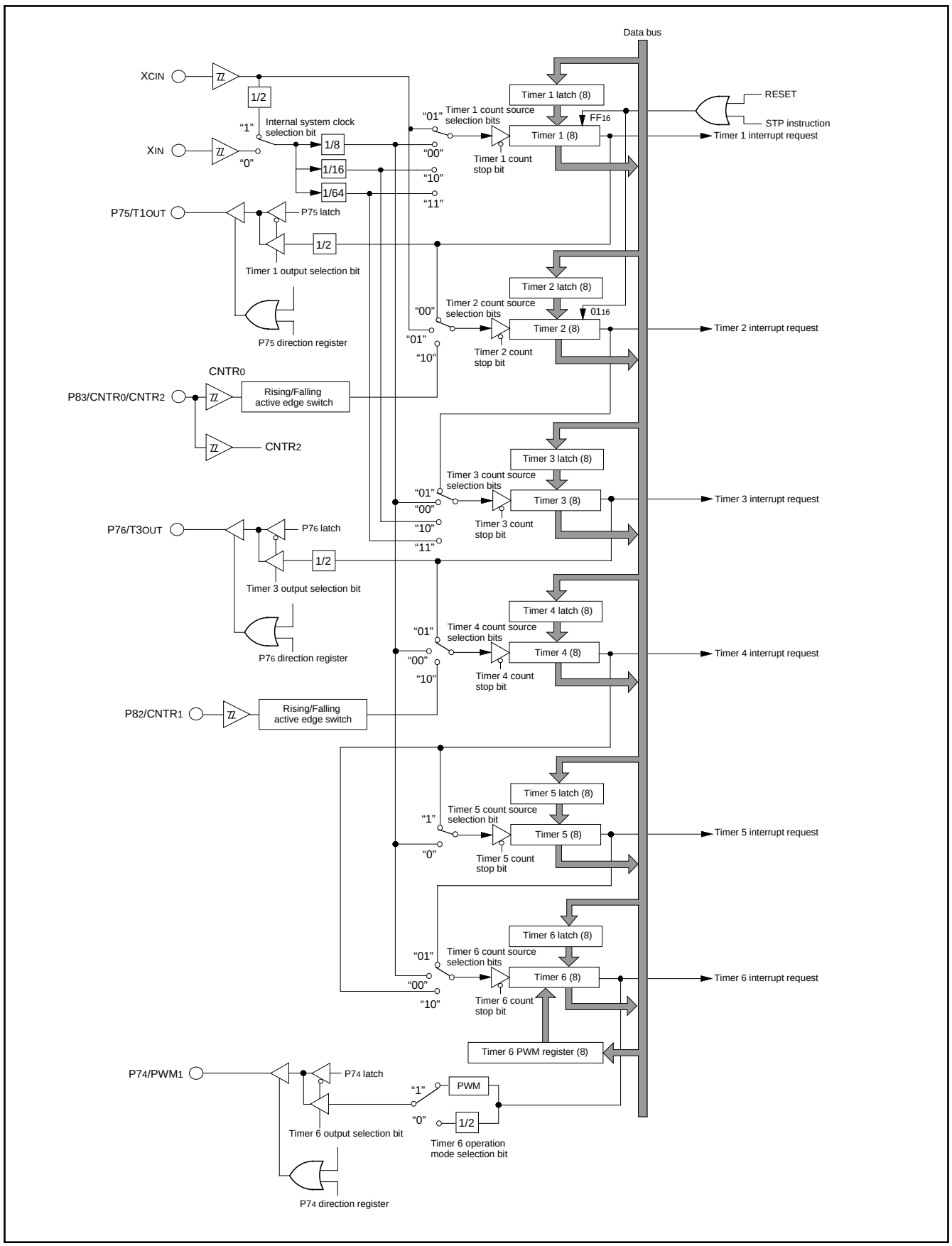
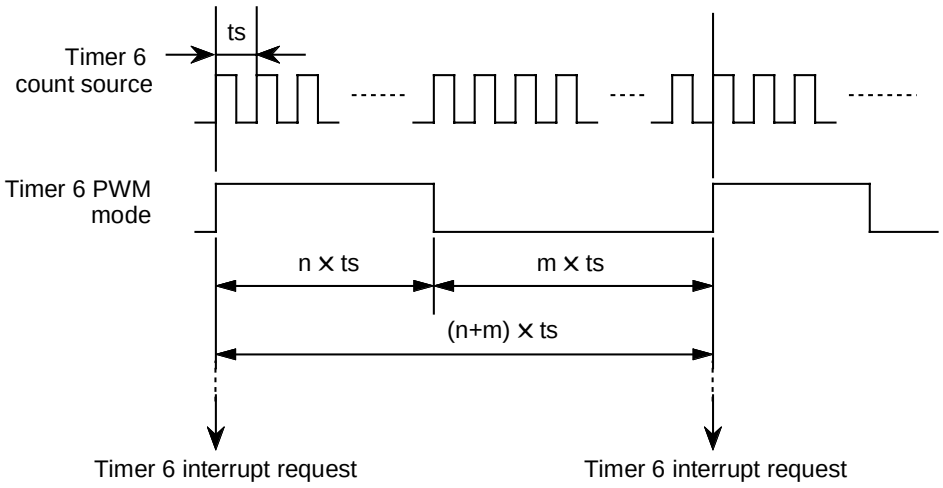


Fig. 17 Block diagram of timer



Note: PWM waveform (duty : n/(n + m) and period: (n + m) × ts) is output.
n : setting value of Timer 6
m: setting value of Timer 6 PWM register
ts: period of Timer 6 count source

Fig. 18 Timing chart of timer 6 PWM1 mode

16-Bit Timer

Timer X is a 16-bit timer that can be selected in one of four modes by the Timer X mode registers 1, 2 and can be controlled for the timer X write and the real time port by setting the timer X mode registers.
Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read from the high-order byte first. When writing to 16-bit timer, write to the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during write operation, or when writing during read operation.

●Timer X

Timer X is a down-counter. When the timer reaches "0000_{16}", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

(1) Timer mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1.

(2) Pulse output mode

Each time the timer underflows, a signal output from the $CNTR_2$ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the port shared with the $CNTR_2$ pin to output.

(3) Event counter mode

The timer counts signals input through the $CNTR_2$ pin. Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the port shared with the $CNTR_2$ pin to input.

(4) Pulse width measurement mode

A count source can be selected by setting the Timer X count source selection bits (bits 1 and 2) of the Timer X mode register 1. When $CNTR_2$ active edge switch bit is "0", the timer counts while the input signal of the $CNTR_2$ pin is at "H". When it is "1", the timer counts while the input signal of the $CNTR_2$ pin is at "L". When using a timer in this mode, set the port shared with the $CNTR_2$ pin to input.

■ Note

•Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
When the value is written in latch only, unexpected value may be set in the high-order counter if the writing in high-order latch and the underflow of timer X are performed at the same timing.

•Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports $P9_4$ and $P9_5$ each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1", data are output independent of the timer X.) When the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

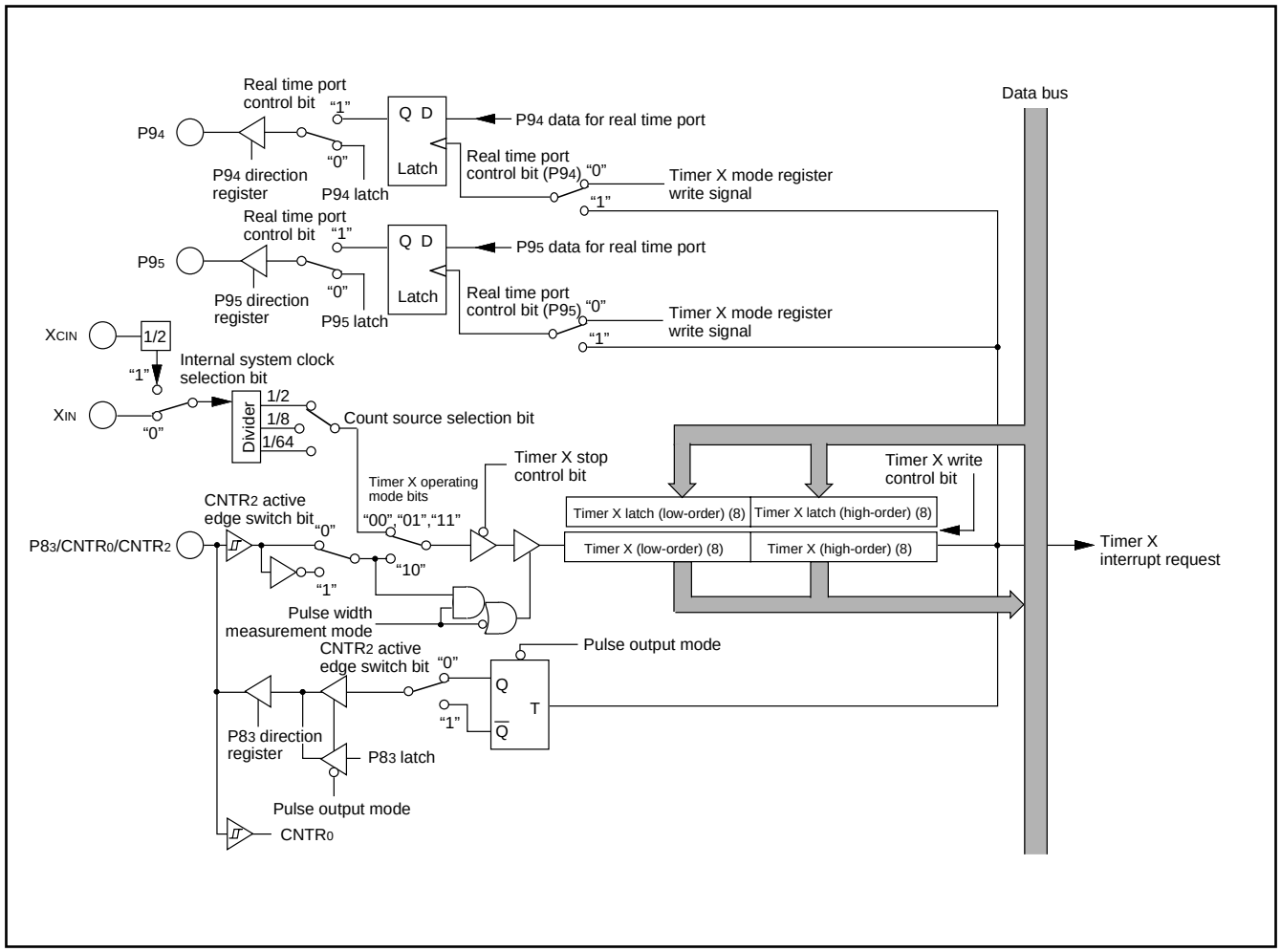


Fig. 19 Block diagram of timer X

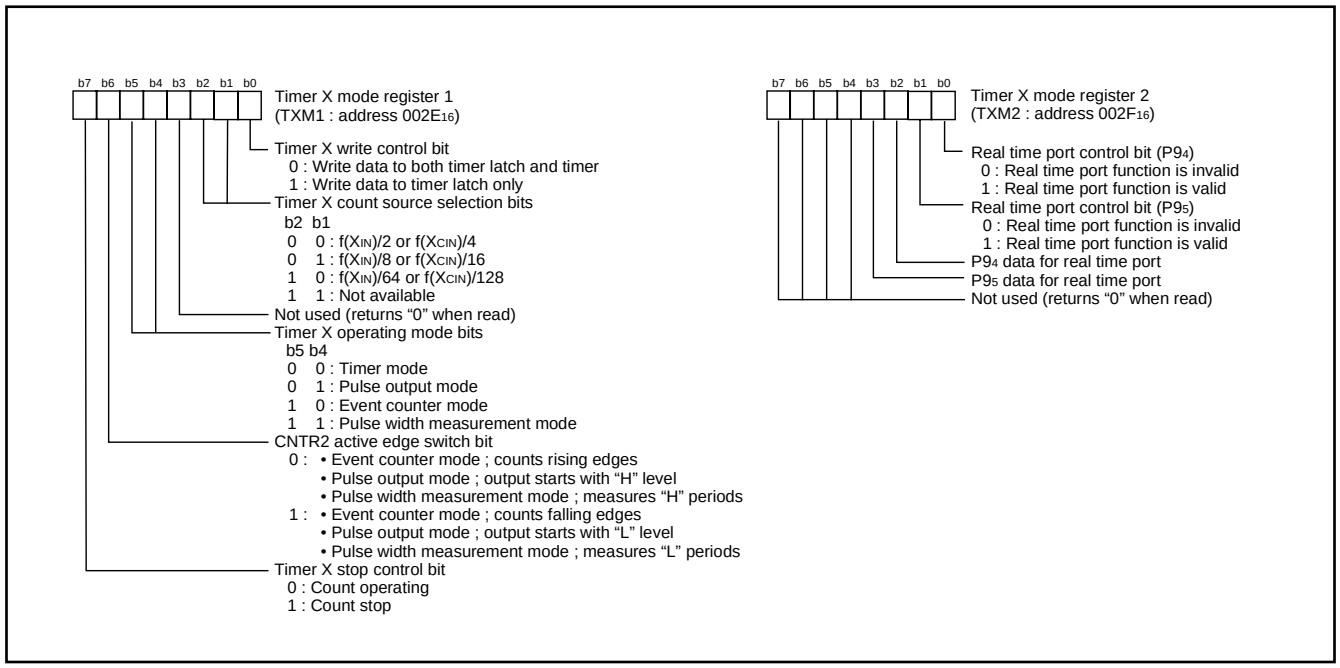


Fig. 20 Structure of timer X related registers

SERIAL I/O
Serial I/O1

Serial I/O1 is used as the clock synchronous serial I/O and has an ordinary mode and an automatic transfer mode. In the automatic transfer mode, serial transfer is performed through the serial I/O automatic transfer RAM which has up to 256 bytes (addresses 0F00$_{16}$ to 0FFF$_{16}$).

The PB1/SRDY1, PB2/SBUSY1, and PB3/SSTB1 pins each have a handshake I/O signal function and can select either “H” active or “L” active for active logic.

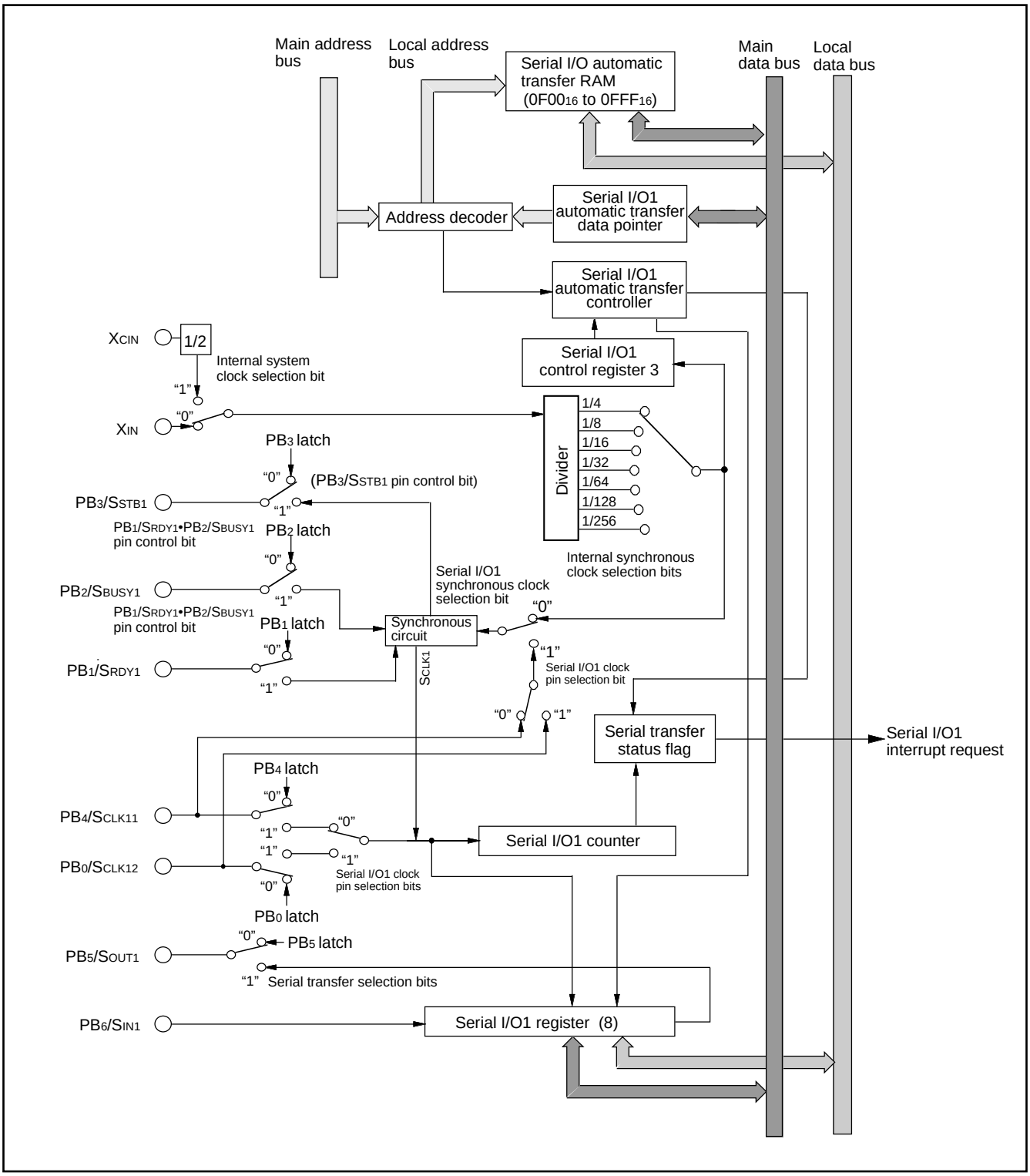
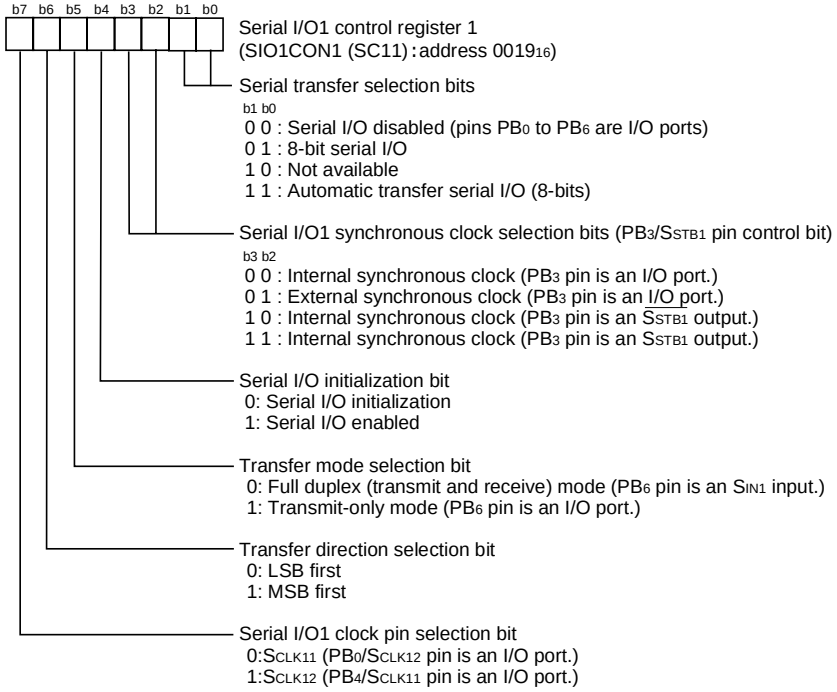


Fig. 21 Block diagram of serial I/O1



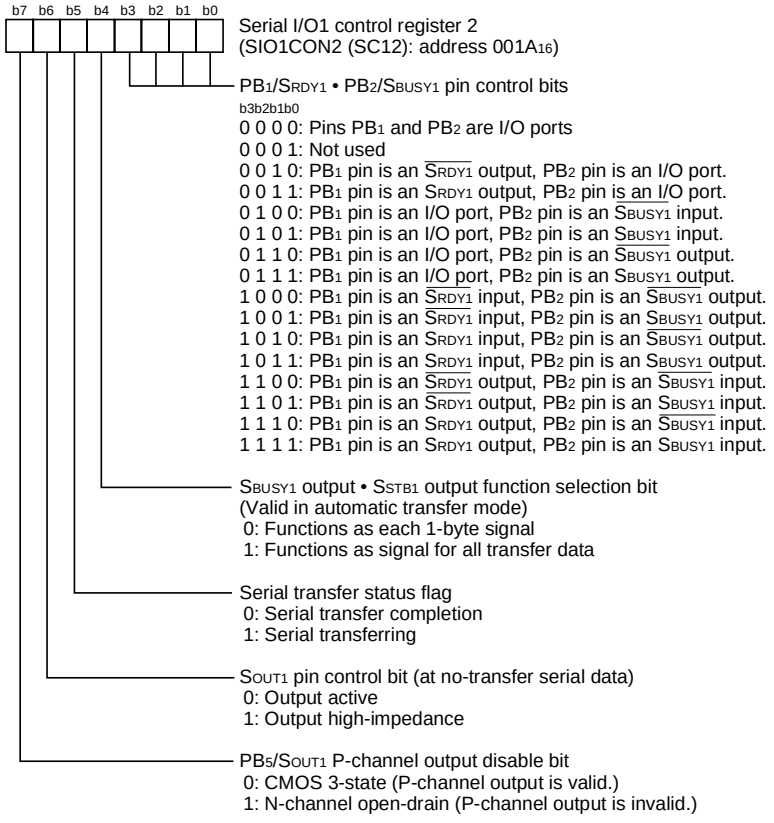


Fig. 22 Structure of serial I/O1 control registers 1, 2

(1) Serial I/O1 operation

Either the internal synchronous clock or external synchronous clock can be selected by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019_{16}) of serial I/O1 control register 1 as synchronous clock for serial transfer.

The internal synchronous clock has a built-in dedicated divider where 7 different clocks are selected by the internal synchronous clock selection bits (b5, b6 and b7 of address $001C_{16}$) of serial I/O1 control register 3.

The P_{B1}/S_{RDY1}, P_{B2}/S_{BUSY1}, and P_{B3}/S_{STB1} pins each select either I/O port or handshake I/O signal by the serial I/O1 synchronous clock selection bits (b2 and b3 of address 0019_{16}) of serial I/O1 control register 1 as well as the P_{B1}/S_{RDY1} • P_{B2}/S_{BUSY1} pin control bits (b0 to b3 of address $001A_{16}$) of serial I/O1 control register 2.

For the $SOUT_1$ being used as an output pin, either CMOS output or N-channel open-drain output is selected by the P_{B5}/S_{OUT1} P-channel output disable bit (b7 of address $001A_{16}$) of serial I/O1 control register 2.

Either output active or high-impedance can be selected as a S_{OUT1} pin state at serial non-transfer by the S_{OUT1} pin control bit (b6 of address $001A_{16}$) of serial I/O1 control register 2. However, when the external synchronous clock is selected, perform the following setup to put the S_{OUT1} pin into a high-impedance state:

When the S_{CLK1} input is "H" after completion of transfer, set the S_{OUT1} pin control bit to "1".

When the S_{CLK1} input goes to "L" after the start of the next serial transfer, the S_{OUT1} pin control bit is automatically reset to "0" and put into an output active state.

Regardless of whether the internal synchronous clock or external synchronous clock is selected, the full duplex mode and the transmit-only mode are available for serial transfer, one of which is selected by the transfer mode selection bit (b5 of address 0019_{16}) of serial I/O1 control register 1.

Either LSB first or MSB first is selected for the I/O sequence of the serial transfer bit strings by the transfer direction selection bit (b6 of address 0019_{16}) of serial I/O1 control register 1.

When using serial I/O1, first select either 8-bit serial I/O or automatic transfer serial I/O by the serial transfer selection bits (b0 and b1 of address 0019_{16}) of serial I/O1 control register 1, after completion of the above bit setup. Next, set the serial I/O initialization bit (b4 of address 0019_{16}) of serial I/O1 control register 1 to "1" (Serial I/O enable) .

When stopping serial transfer while data is being transferred, regardless of whether the internal or external synchronous clock is selected, reset the serial I/O initialization bit (b4) to "0".

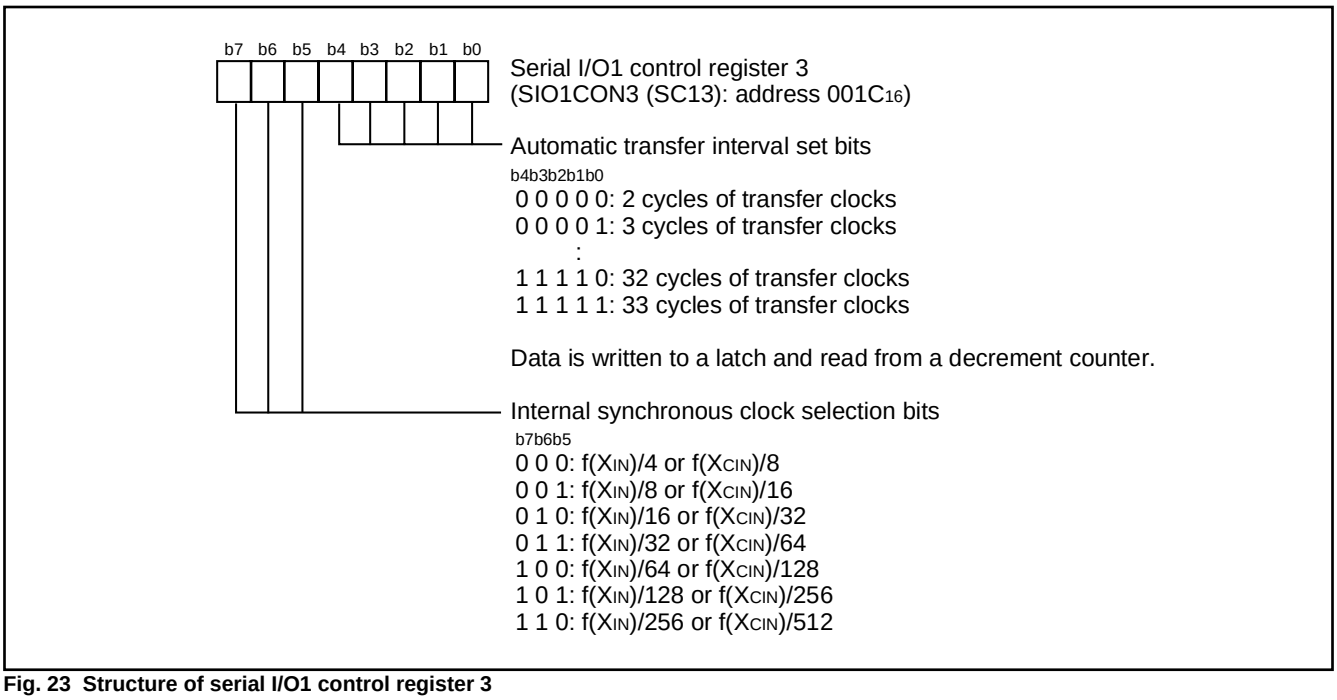


Fig. 23 Structure of serial I/O1 control register 3

(2) 8-bit serial I/O mode

Address 001B16 is assigned to the serial I/O1 register.

When the internal synchronous clock is selected, a serial transfer of the 8-bit serial I/O is started by a write signal to the serial I/O1 register (address 001B16).

The serial transfer status flag (b5 of address 001A16) of serial I/O1 control register 2 indicates the shift register status of serial I/O1, and is set to "1" by writing into the serial I/O1 register, which becomes a transfer start trigger and reset to "0" after completion of 8-bit transfer. At the same time, a serial I/O1 interrupt request occurs.

When the external synchronous clock is selected, the contents of the serial I/O1 register are continuously shifted while transfer clocks are input to SCLK1. Therefore, the clock needs to be controlled externally.

(3) Automatic transfer serial I/O mode

The serial I/O1 automatic transfer controller controls the write and read operations of the serial I/O1 register, so that the function of address 001B16 is used as a transfer counter (1-byte unit).

When performing serial transfer through the serial I/O automatic transfer RAM (addresses 0F0016 to 0FFF16), it is necessary to set the serial I/O1 automatic transfer data pointer (address 001816) beforehand.

Input the low-order 8 bits of the first data store address to be serially transferred to the automatic transfer data pointer set bits.

When the internal synchronous clock is selected, the transfer interval for each 1-byte data can be set by the automatic transfer interval set bits (b0 to b4 of address 001C16) of serial I/O1 control register 3 in the following cases:

1. When using no handshake signal
2. When using the SRDY1 output, SBUSY1 output, and SSTB1 output of the handshake signal independently
3. When using a combination of SRDY1 output and SSTB1 output or a combination of SBUSY1 output and SSTB1 output of the handshake signal.

It is possible to select one of 32 different values, namely 2 to 33 cycles of the transfer clock, as a setting value.

When using the SBUSY1 output and selecting the SBUSY1 output • SSTB1 output function selection bit (b4 of address 001A16) of serial I/O1 control register 2 as the signal for all transfer data, provided that the automatic transfer interval setting is valid, a transfer interval is placed before the start of transmission/reception of the first data and after the end of transmission/reception of the last data.

For SSTB1 output, regardless of the contents of the SBUSY1 output • SSTB1 output function selection bit (b4), the transfer interval for each 1-byte data is longer than the set value by 2 cycles.

Furthermore, when using a combination of SBUSY1 output and SSTB1 output as a signal for all transfer data, the transfer interval after the end of transmission/reception of the last data is longer than the set value by 2 cycles.

When the external synchronous clock is selected, automatic transfer interval setting is disabled.

After completion of the above bit setup, if the internal synchronous clock is selected, automatic serial transfer is started by writing the value of "number of transfer bytes – 1" into the transfer counter (address 001B16).

When the external synchronous clock is selected, write the value of "number of transfer bytes – 1" into the transfer counter and keep an internal system clock interval of 5 cycles or more. After that, input transfer clock to SCLK1.

As a transfer interval for each 1-byte data transfer, keep an internal system clock interval of 5 cycles or more from the clock rise time of the last bit.

Regardless of whether the internal or external synchronous clock is selected, the automatic transfer data pointer and the transfer counter are decremented after each 1-byte data is received and then written into the automatic transfer RAM. The serial transfer status flag (b5 of address 001A16) is set to "1" by writing data into the transfer counter. Writing data becomes a transfer start trigger, and the serial transfer status flag is reset to "0" after the last data is written into the automatic transfer RAM. At the same time, a serial I/O1 interrupt request occurs.

The values written in the automatic transfer data pointer set bits (b0 to b7 of address 001816) and the automatic transfer interval set bits (b0 to b4 of address 001C16) are held in the latch.

When data is written into the transfer counter, the values latched in the automatic transfer data pointer set bits (b0 to b7) and the automatic transfer interval set bits (b0 to b4) are transferred to the decrement counter.

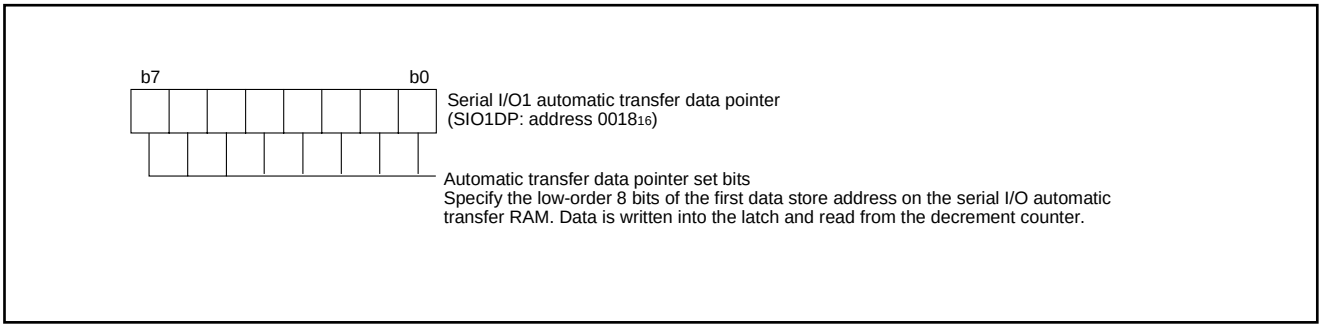


Fig. 24 Structure of serial I/O1 automatic transfer data pointer

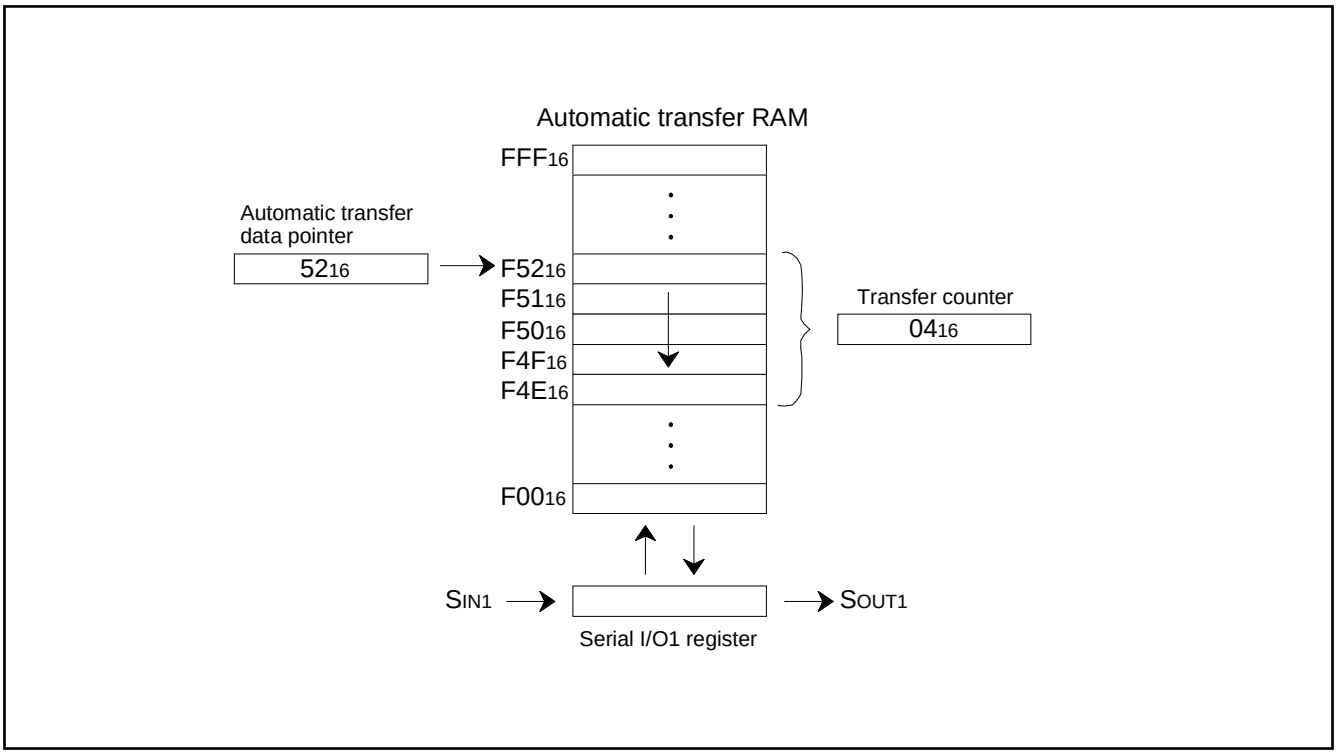


Fig. 25 Automatic transfer serial I/O operation

(4) Handshake signal

1. SSTB1 output signal

The SSTB1 output is a signal to inform an end of transmission/reception to the serial transfer destination . The SSTB1 output signal can be used only when the internal synchronous clock is selected.
In the initial status, namely, in the status in which the serial I/O initialization bit (b4) is reset to "0", the SSTB1 output goes to "L", or the $\overline{\text{SSTB1}}$ output goes to "H".
At the end of transmit/receive operation, when the data of the serial I/O1 register is all output from SOUT1, pulses are output in the period of 1 cycle of the transfer clock so as to cause the SSTB1 output to go "H" or the $\overline{\text{SSTB1}}$ output to go "L". After that, each pulse is returned to the initial status in which SSTB1 output goes to "L" or the $\overline{\text{SSTB1}}$ output goes to "H".
Furthermore, after 1 cycle, the serial transfer status flag (b5) is reset to "0".
In the automatic transfer serial I/O mode, whether the SSTB1 output is to be active at an end of each 1-byte data or after completion of transfer of all data can be selected by the SBUSY1 output • SSTB1 output function selection bit (b4 of address $001A_{16}$) of serial I/O1 control register 2.

2. SBUSY1 input signal

The SBUSY1 input is a signal which receives a request for a stop of transmission/reception from the serial transfer destination.
When the internal synchronous clock is selected, input an "H" level signal into the SBUSY1 input and an "L" level signal into the $\overline{\text{SBUSY1}}$ input in the initial status in which transfer is stopped.
When starting a transmit/receive operation, input an "L" level signal into the SBUSY1 input and an "H" level signal into the $\overline{\text{SBUSY1}}$ input in the period of 1.5 cycles or more of the transfer clock. Then, transfer clocks are output from the SCLK1 output.
When an "H" level signal is input into the SBUSY1 input and an "L" level signal into the $\overline{\text{SBUSY1}}$ input after a transmit/receive operation is started, this transmit/receive operation are not stopped immediately and the transfer clocks from the SCLK1 output is not stopped until the specified number of bits are transmitted and received.
The handshake unit of the 8-bit serial I/O is 8 bits and that of the automatic transfer serial I/O is 8 bits.
When the external synchronous clock is selected, input an "H" level signal into the SBUSY1 input and an "L" level signal into the $\overline{\text{SBUSY1}}$ input in the initial status in which transfer is stopped. At this time, the transfer clocks to be input in SCLK1 become invalid.
During serial transfer, the transfer clocks to be input in SCLK1 become valid, enabling a transmit/receive operation, while an "L" level signal is input into the SBUSY1 input and an "H" level signal is input into the $\overline{\text{SBUSY1}}$ input.
When changing the input values in the SBUSY1 input and the $\overline{\text{SBUSY1}}$ input at these operations, change them when the SCLK1 input is in a high state.
When the high impedance of the SOUT1 output is selected by the SOUT1 pin control bit (b6), the SOUT1 output becomes active, enabling serial transfer by inputting a transfer clock to SCLK1, while an "L" level signal is input into the SBUSY1 input and an "H" level signal is input into the $\overline{\text{SBUSY1}}$ input.

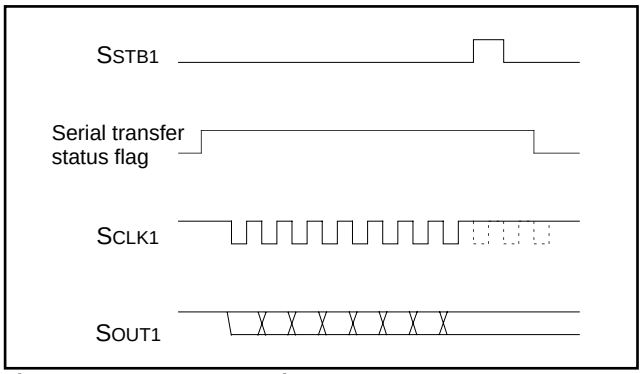


Fig. 26 SSTB1 output operation

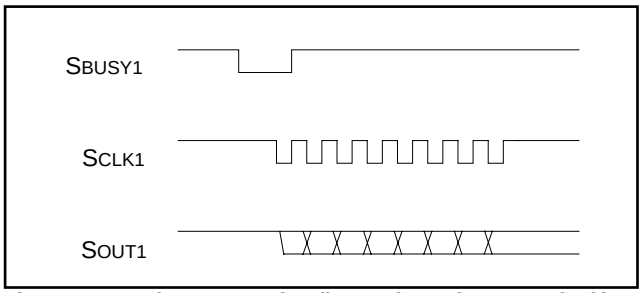


Fig. 27 SBUSY1 input operation (internal synchronous clock)

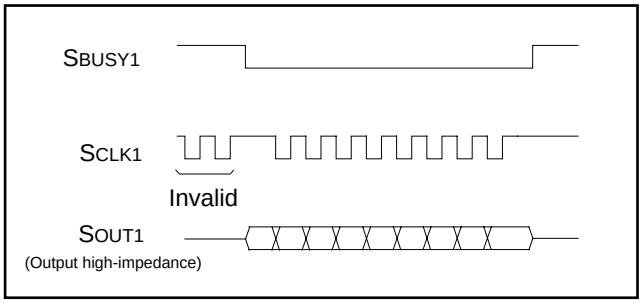


Fig. 28 SBUSY1 input operation (external synchronous clock)

3. SBUSY1 output signal

The SBUSY1 output is a signal which requests a stop of transmission/reception to the serial transfer destination. In the automatic transfer serial I/O mode, regardless of the internal or external synchronous clock, whether the SBUSY1 output is to be active at transfer of each 1-byte data or during transfer of all data can be selected by the SBUSY1 output • SSTB1 output function selection bit (b4).
In the initial status, the status in which the serial I/O initialization bit (b4) is reset to "0", the SBUSY1 output goes to "H" and the $\overline{\text{SBUSY1}}$ output goes to "L".

When the internal synchronous clock is selected, in the 8-bit serial I/O mode and the automatic transfer serial I/O mode (SBUSY1 output function outputs in 1-byte units), the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" before 0.5 cycle (transfer clock) of the timing at which the transfer clock from the SCLK1 output goes to "L" at a start of transmit/receive operation.

In the automatic transfer serial I/O mode (the SBUSY1 output function outputs all transfer data), the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" when the first transmit data is written into the serial I/O1 register (address $001B_{16}$).

When the external synchronous clock is selected, the SBUSY1 output goes to "L" and the $\overline{\text{SBUSY1}}$ output goes to "H" when transmit data is written into the serial I/O1 register to start a transmit operation, regardless of the serial I/O transfer mode.

At termination of transmit/receive operation, the SBUSY1 output returns to "H" and the $\overline{\text{SBUSY1}}$ output returns to "L", the initial status, when the serial transfer status flag is set to "0", regardless of whether the internal or external synchronous clock is selected.

Furthermore, in the automatic transfer serial I/O mode (SBUSY1 output function outputs in 1-byte units), the SBUSY1 output goes to "H" and the $\overline{\text{SBUSY1}}$ output goes to "L" each time 1-byte of receive data is written into the automatic transfer RAM.

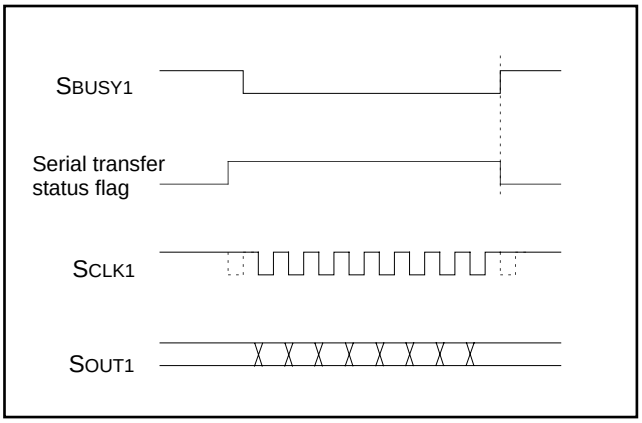


Fig. 29 SBUSY1 output operation (internal synchronous clock, 8-bit serial I/O)

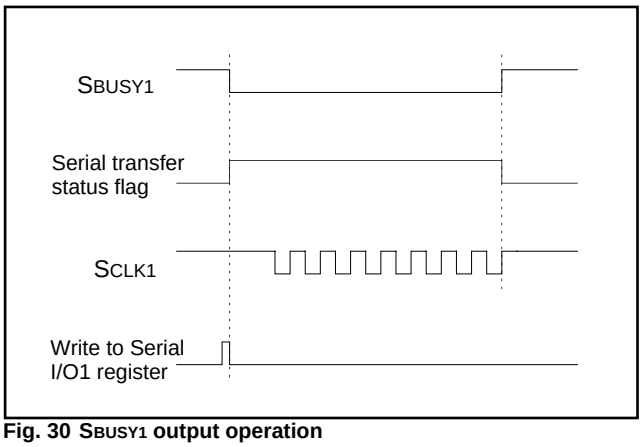


Fig. 30 SBUSY1 output operation (external synchronous clock, 8-bit serial I/O)

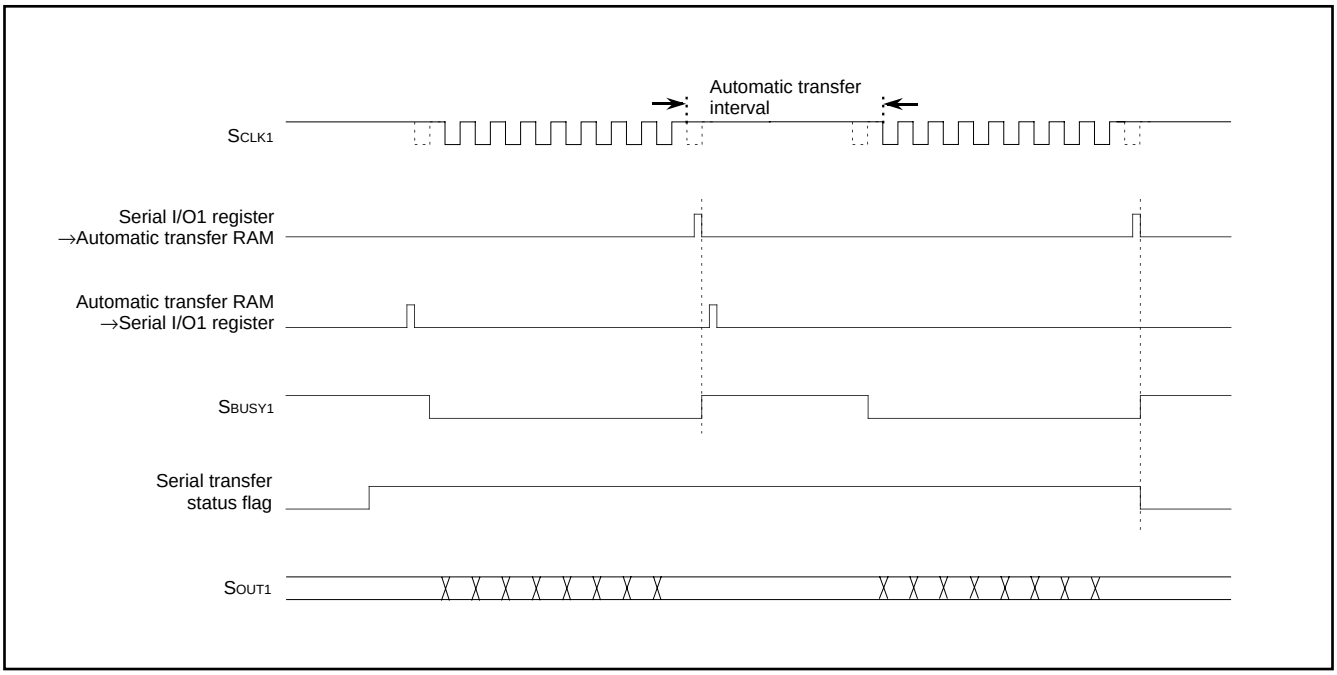


Fig. 31 SBUSY1 output operation in automatic transfer serial I/O mode (internal synchronous clock, SBUSY1 output function outputs each 1-byte)

4. SRDY1 output signal

The SRDY1 output is a transmit/receive enable signal which informs the serial transfer destination that transmit/receive is ready. In the initial status, when the serial I/O initialization bit (b4) is reset to "0", the SRDY1 output goes to "L" and the $\overline{\text{SRDY1}}$ output goes to "H". After transmitted data is stored in the serial I/O1 register (address 001B16) and a transmit/receive operation becomes ready, the SRDY1 output goes to "H" and the $\overline{\text{SRDY1}}$ output goes to "L". When a transmit/receive operation is started and the transfer clock goes to "L", the SRDY1 output goes to "L" and the $\overline{\text{SRDY1}}$ output goes to "H".

5. SRDY1 input signal

The SRDY1 input signal becomes valid only when the SRDY1 input and the SBUSY1 output are used. The SRDY1 input is a signal for receiving a transmit/receive ready completion signal from the serial transfer destination.

When the internal synchronous clock is selected, input a low level signal into the SRDY1 input and a high level signal into the $\overline{\text{SRDY1}}$ input in the initial status in which the transfer is stopped.

When an "H" level signal is input into the SRDY1 input and an "L" level signal is input into the $\overline{\text{SRDY1}}$ input for a period of 1.5 cycles or more of transfer clock, transfer clocks are output from the SCLK1 output and a transmit/receive operation is started.

After the transmit/receive operation is started and an "L" level signal is input into the SRDY1 input and an "H" level signal into the $\overline{\text{SRDY1}}$ input, this operation cannot be immediately stopped.

After the specified number of bits are transmitted and received, the transfer clocks from the SCLK1 output is stopped. The handshake unit of the 8-bit serial I/O and that of the automatic transfer serial I/O are of 8 bits.

When the external synchronous clock is selected, the SRDY1 input becomes one of the triggers to output the SBUSY1 signal.

To start a transmit/receive operation (SBUSY1 output: "L", $\overline{\text{SBUSY1}}$ output: "H"), input an "H" level signal into the SRDY1 input and an "L" level signal into the $\overline{\text{SRDY1}}$ input, and also write transmit data into the serial I/O1 register.

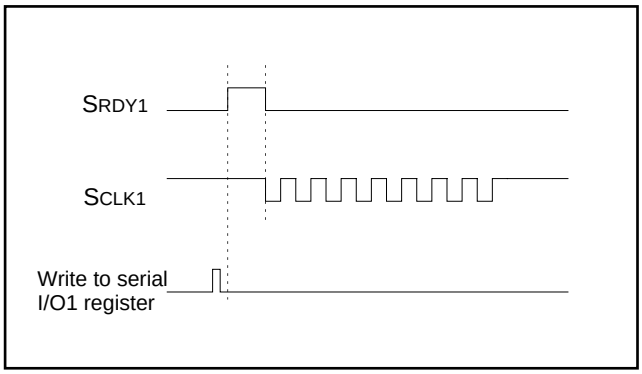


Fig. 32 SRDY1 output operation

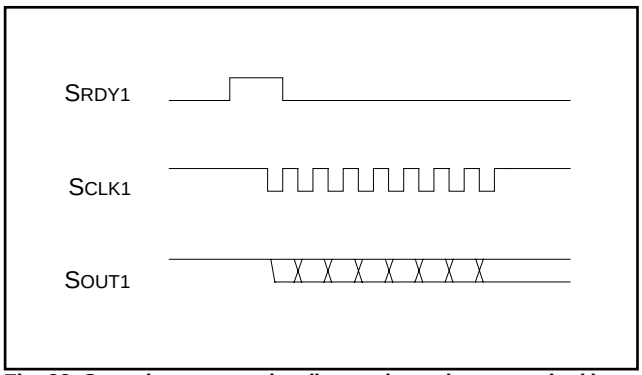


Fig. 33 SRDY1 input operation (internal synchronous clock)

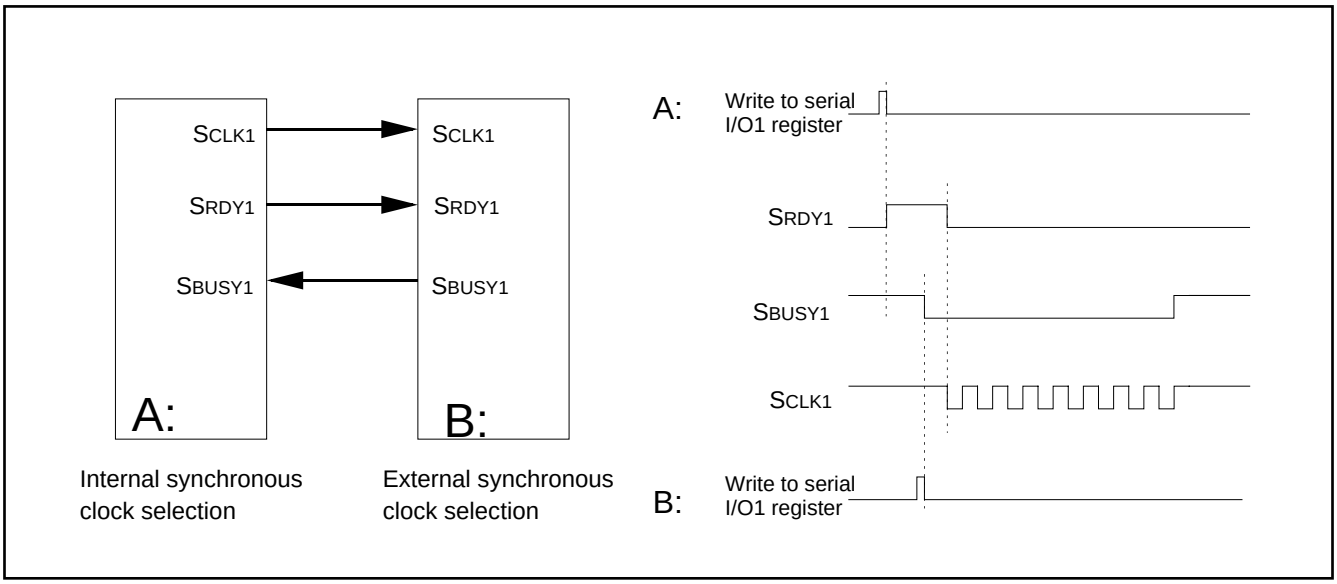


Fig. 34 Handshake operation at serial I/O1 mutual connecting (1)

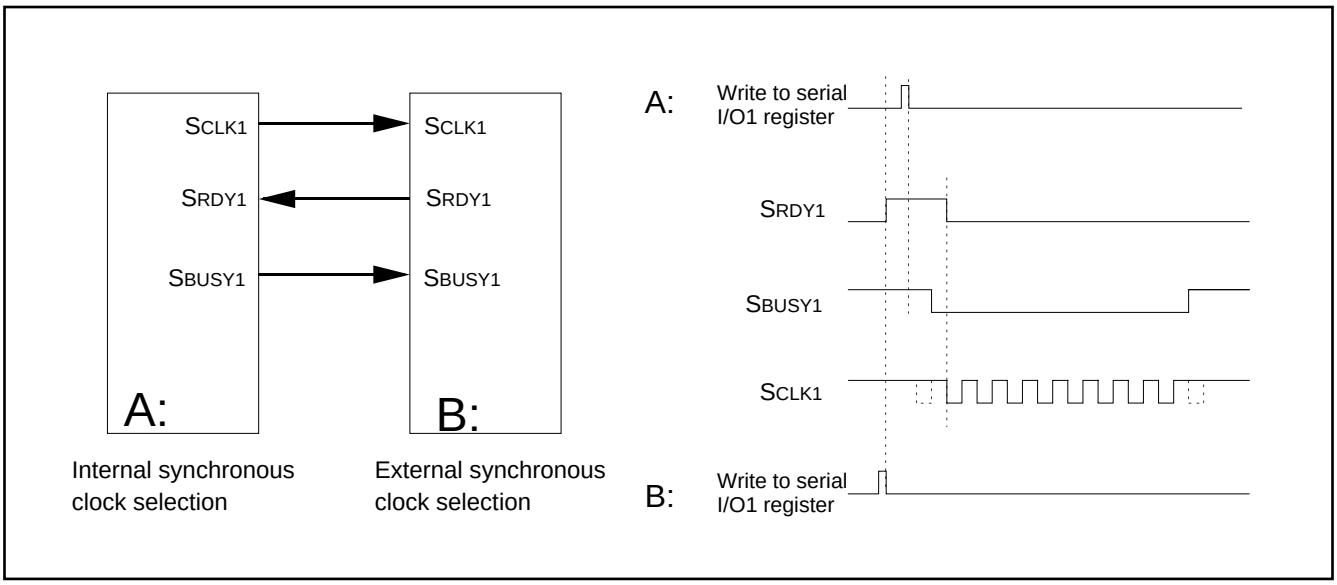


Fig. 35 Handshake operation at serial I/O1 mutual connecting (2)

Serial I/O2

Serial I/O2 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation during serial I/O2 operation.

(1) Clock synchronous serial I/O mode

The clock synchronous serial I/O mode can be selected by setting the serial I/O2 mode selection bit (b6) of the serial I/O2 control register (address 001D16) to "1". For clock synchronous serial I/O, the transmitter and the receiver must use the same clock for serial I/O2 operation. If an internal clock is used, transmit/receive is started by a write signal to the serial I/O2 transmit/receive buffer register (TB/RB) (address 001F16).

When P67 (SCLK22) is selected as a clock I/O pin, $\overline{\text{SRDY2}}$ output function is invalid, and P66 (SCLK21) is used as an I/O port.

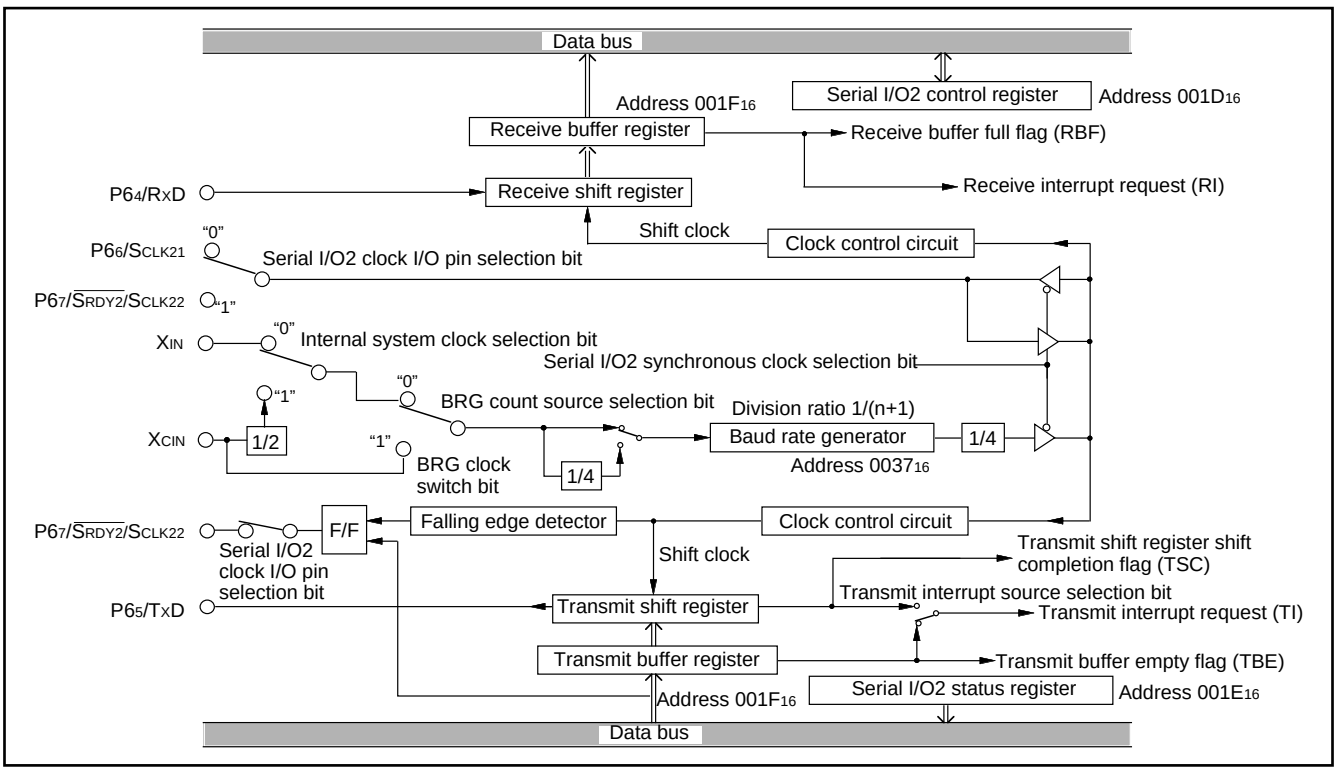
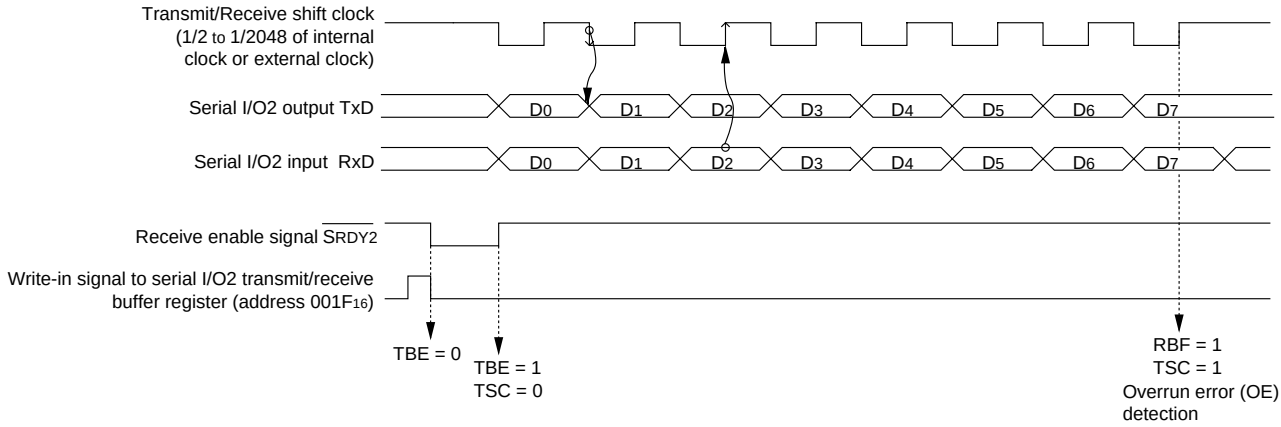


Fig. 36 Block diagram of clock synchronous serial I/O2



Notes 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting transmit interrupt source selection bit (TIC) of the serial I/O2 control register.

2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes "1".

Fig. 37 Operation of clock synchronous serial I/O2 function

(2) Asynchronous serial I/O (UART) mode

The asynchronous serial I/O (UART) mode can be selected by clearing the serial I/O2 mode selection bit (b6) of the serial I/O2 control register (address 001D16) to "0". Eight serial data transfer formats can be selected and the transfer formats used by the transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer (the two buffers have the same address in memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can receive 2-byte data continuously.

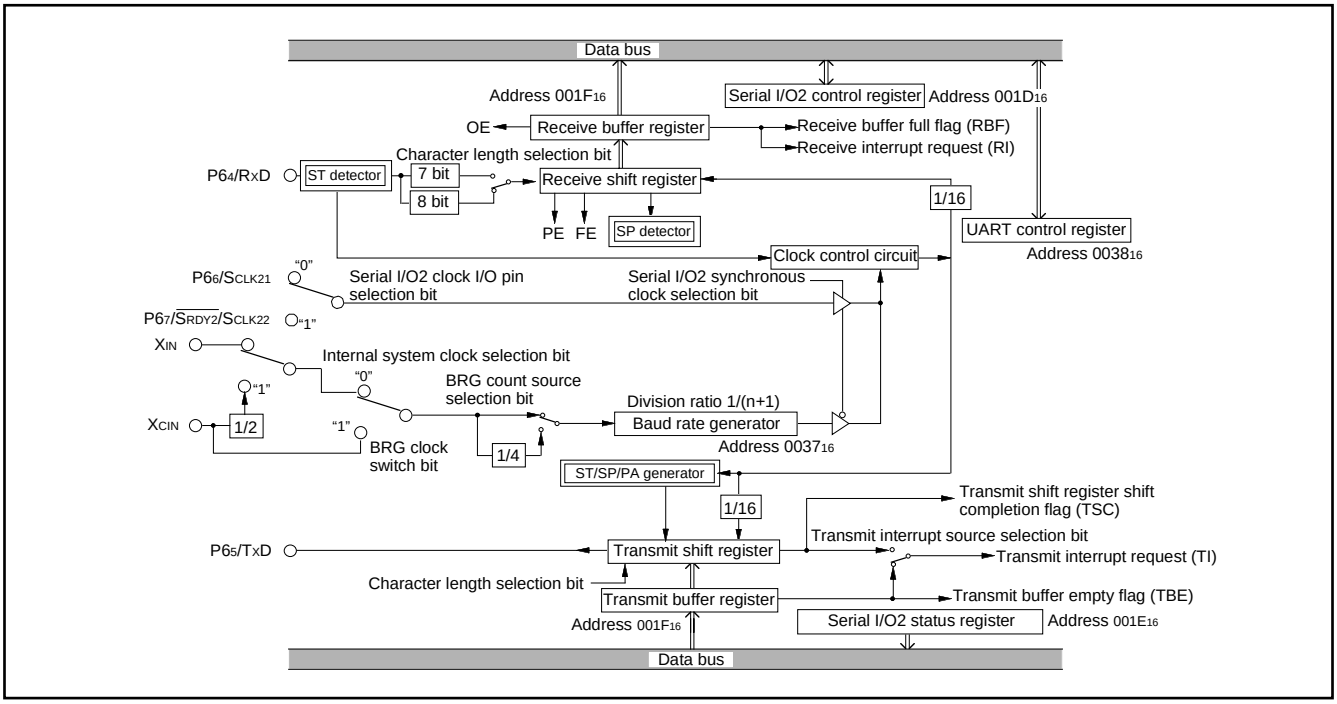


Fig. 38 Block diagram of UART serial I/O2

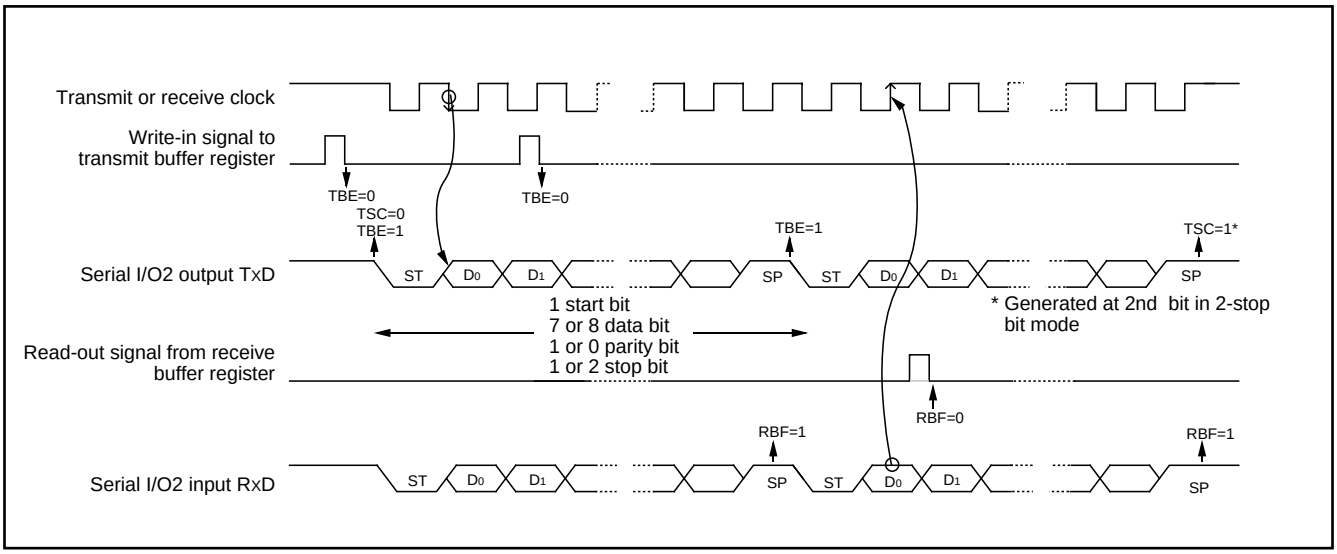


Fig. 39 Operation of UART serial I/O2 function

[Serial I/O2 Control Register] SIO2CON (001D16)

The serial I/O2 control register contains eight control bits for serial I/O2 functions.

[UART Control Register] UARTCON (003816)

This is a 7 bit register containing four control bits, of which four bits are valid when UART is selected, and of which three bits are always valid.

Data format of serial data receive/transfer and the output structure of the P65/TxD pin and others are set by this register.

[Serial I/O2 Status Register] SIO2STS (001E16)

The read-only serial I/O2 status register consists of seven flags (b0 to b6) which indicate the operating status of the serial I/O2 function and various errors. Three of the flags (b4 to b6) are only valid in the UART mode. The receive buffer full flag (b1) is cleared to "0" when the receive buffer is read.

The error detection is performed at the same time data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A writing to the serial I/O2 status register clears error flags OE, PE, FE, and SE (b3 to b6, respectively). Writing "0" to the serial I/O2 enable bit (SIOE : b7 of the serial I/O2 control register) also clears all the status flags, including the error flags.

All bits of the serial I/O2 status register are initialized to "0" at reset, but if the transmit enable bit (b4) of the serial I/O2 control register has been set to "1", the transmit shift register shift completion flag (b2) and the transmit buffer empty flag (b0) become "1".

[Serial I/O2 Transmit Buffer Register/Receive Buffer Register] TB/RB (001F16)

The transmit buffer and the receive buffer are located in the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator] BRG (003716)

The baud rate generator determines the baud rate for serial transfer. With the 8-bit counter having a reload register, the baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.

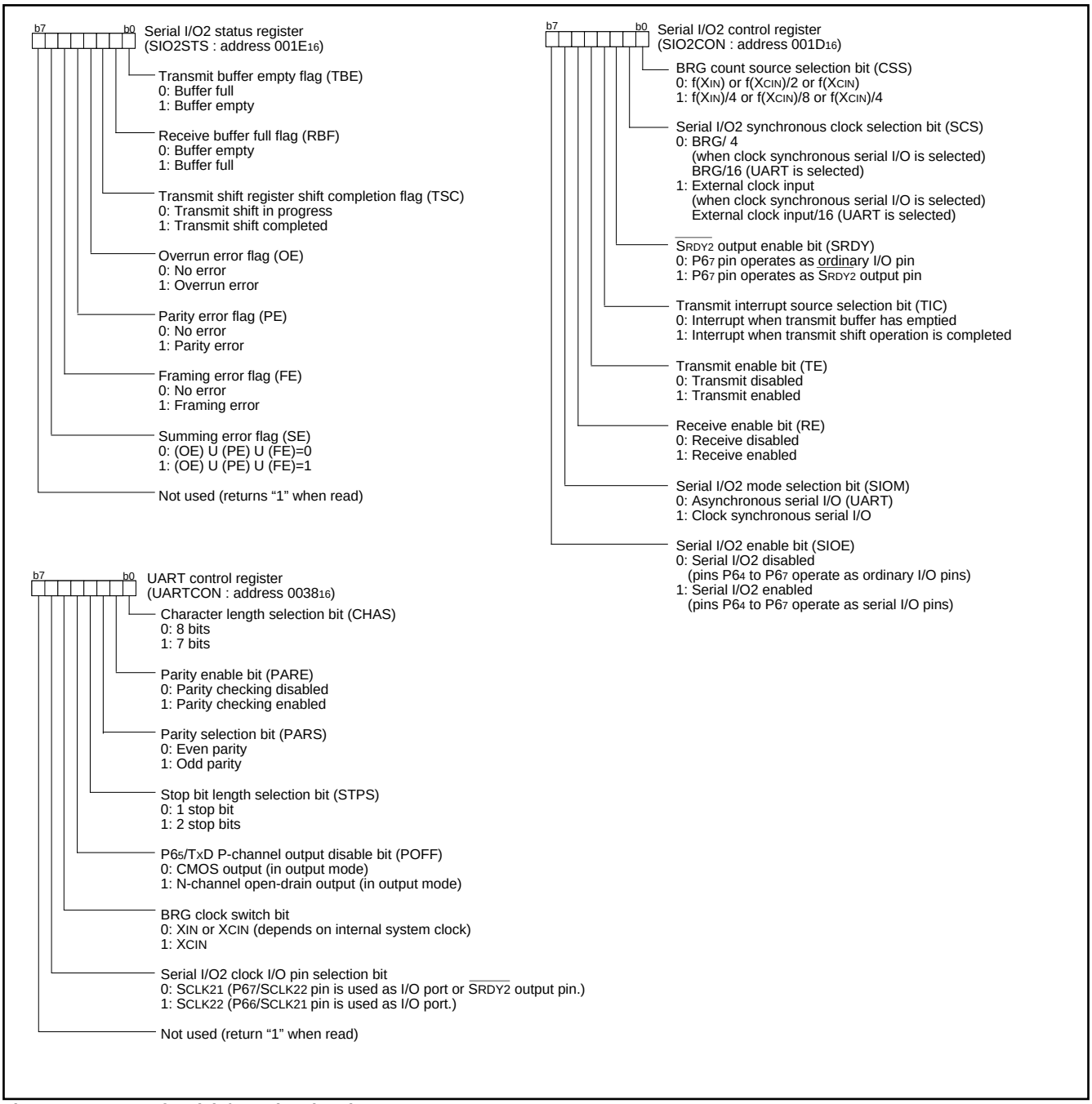


Fig. 40 Structure of serial I/O2 related register

Serial I/O3

The serial I/O3 function can be used only for 8-bit clock synchronous serial I/O.

All serial I/O pins are shared with port P9, which can be set with the serial I/O3 control register (address 0EEC16).

[Serial I/O3 Control Register (SIO3CON)] 0EEC16

The serial I/O3 control register contains eight bits which control various serial I/O functions.

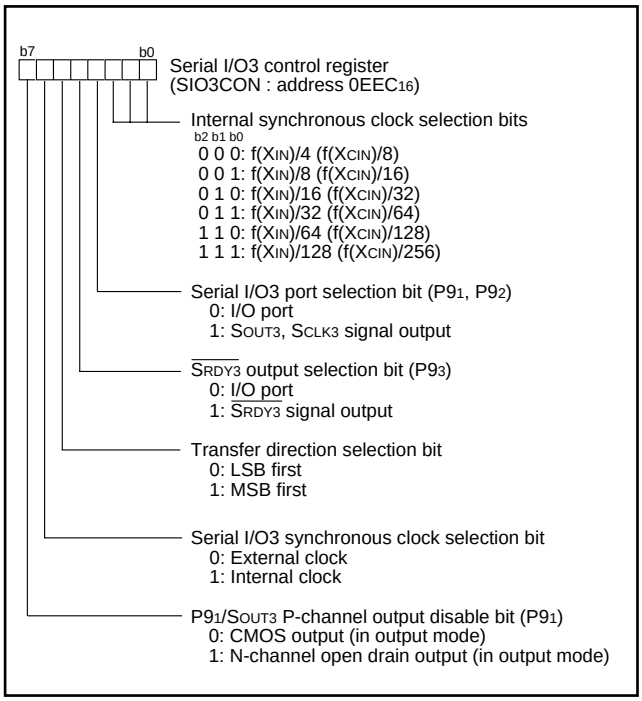


Fig. 42 Structure of serial I/O3 control register

● Serial I/O3 Operation

Either the internal clock or external clock can be selected as synchronous clock for serial I/O3 transfer.

The internal clock can use a built-in dedicated divider where 6 different clocks are selected. In the case of the internal clock used, transfer is started by a write signal to the serial I/O3 register (address 0EED16). When 8-bit data has been transferred, the SOUT3 pin goes to high impedance state.

In the case of the external clock used, the clock must be externally controlled. It is because the contents of serial I/O3 register is kept shifted while the clock is being input. Additionally, the function to put the SOUT3 pin high impedance state at completion of data transfer is not available.

The serial I/O3 interrupt request bit is set at completion of 8-bit data transfer, regardless of use of the internal clock or external clock.

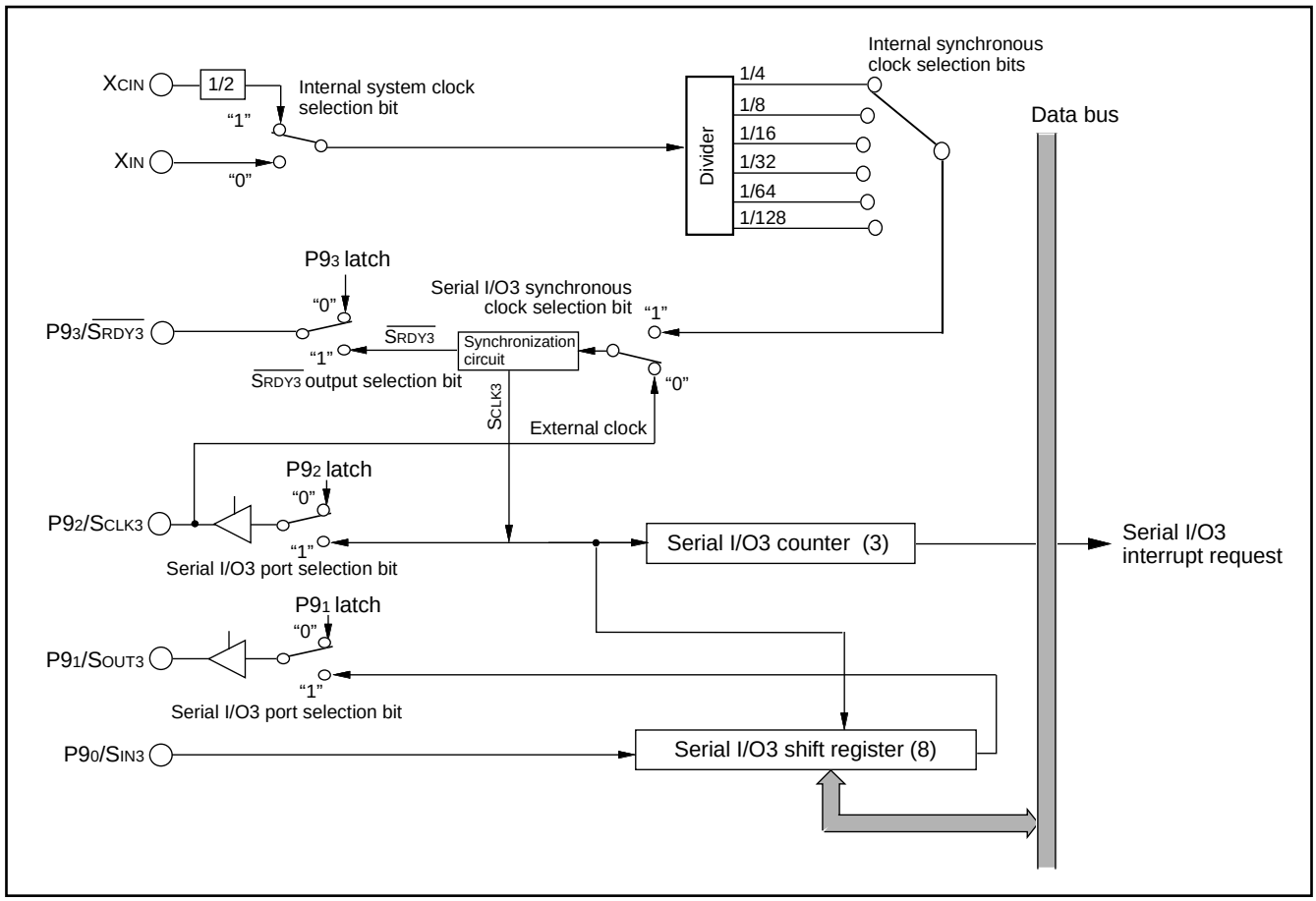
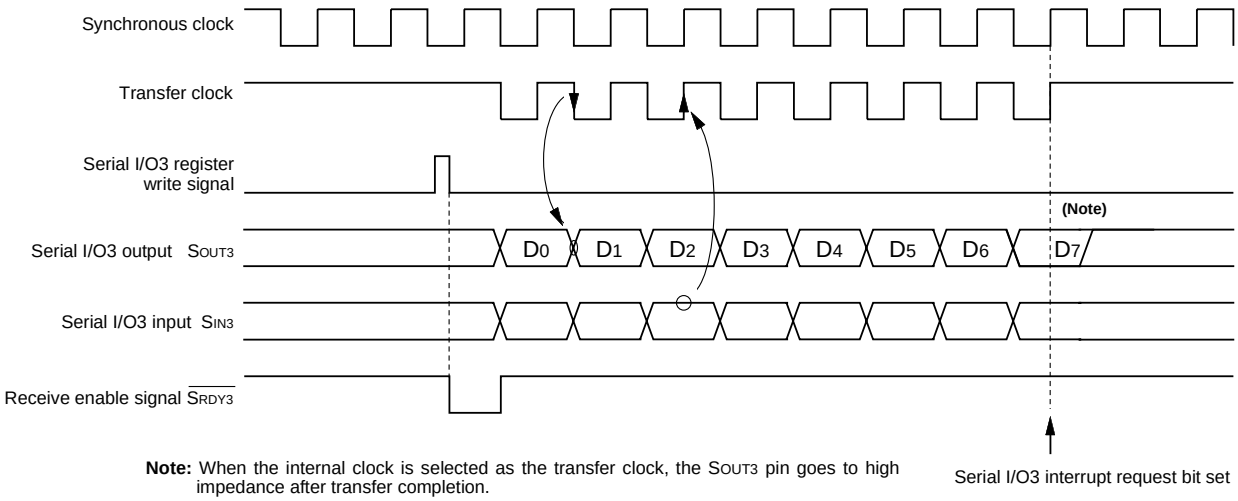


Fig. 41 Block diagram of serial I/O3



Note: When the internal clock is selected as the transfer clock, the SOUT3 pin goes to high impedance after transfer completion.

Fig. 43 Timing of serial I/O3 (LSB first)

FLD CONTROLLER

The M38B7 group has fluorescent display (FLD) drive and control circuits.
Table 9 shows the FLD controller specifications.

Table 9 FLD controller specifications

Item		Specifications
FLD controller port	High-breakdown-voltage output port	• 52 pins (20 pins can be switched to general-purpose ports)
	CMOS port	• 4 pins (all 4 pins can be switched to general-purpose ports) (A driver IC must be installed externally)
Display pixel number		• Used FLD output 28 segment × 28 digit (segment number + digit number ≤ 56) • Used digit output 40 segment × 16 digit (segment number ≤ 40, digit number ≤ 16) • Connected to M35501 56 segment × (connected number of M35501) digit (segment number ≤ 56, digit number ≤ number of M35501 × 16) • Used $P6_4$ to $P6_7$ expansion 52 segment × 16 digit (segment number ≤ 52, digit number ≤ 16)
Period		• 4.0 µs to 1024 µs (count source X_{IN}/16, 4 MHz) • 16.0 µs to 4096 µs (count source X_{IN}/64, 4 MHz)
Dimmer time		• 4.0 µs to 1024 µs (count source X_{IN}/16, 4 MHz) • 16.0 µs to 4096 µs (count source X_{IN}/64, 4 MHz)
Interrupt		• Digit interrupt • FLD blanking interrupt
Key-scan		• Key-scan using digit • Key-scan using segment
Expanded function		• Digit pulse output function This function automatically outputs digit pulses. • M35501 connection function The number of digits can be increased easily by using the output of DIM_{OUT}($P7_3$) as CLK for the M35501. • Toff section generating/nothing function This function does not generate Toff1 section when the connected outputs are the same. • Gradation display function This function allows each segment to be set for dark or bright display. • $P6_4$ to $P6_7$ expansion function This function provides 16 lines of digit outputs from four ports by attaching the decoder converting 4-bit data to 16-bit data.

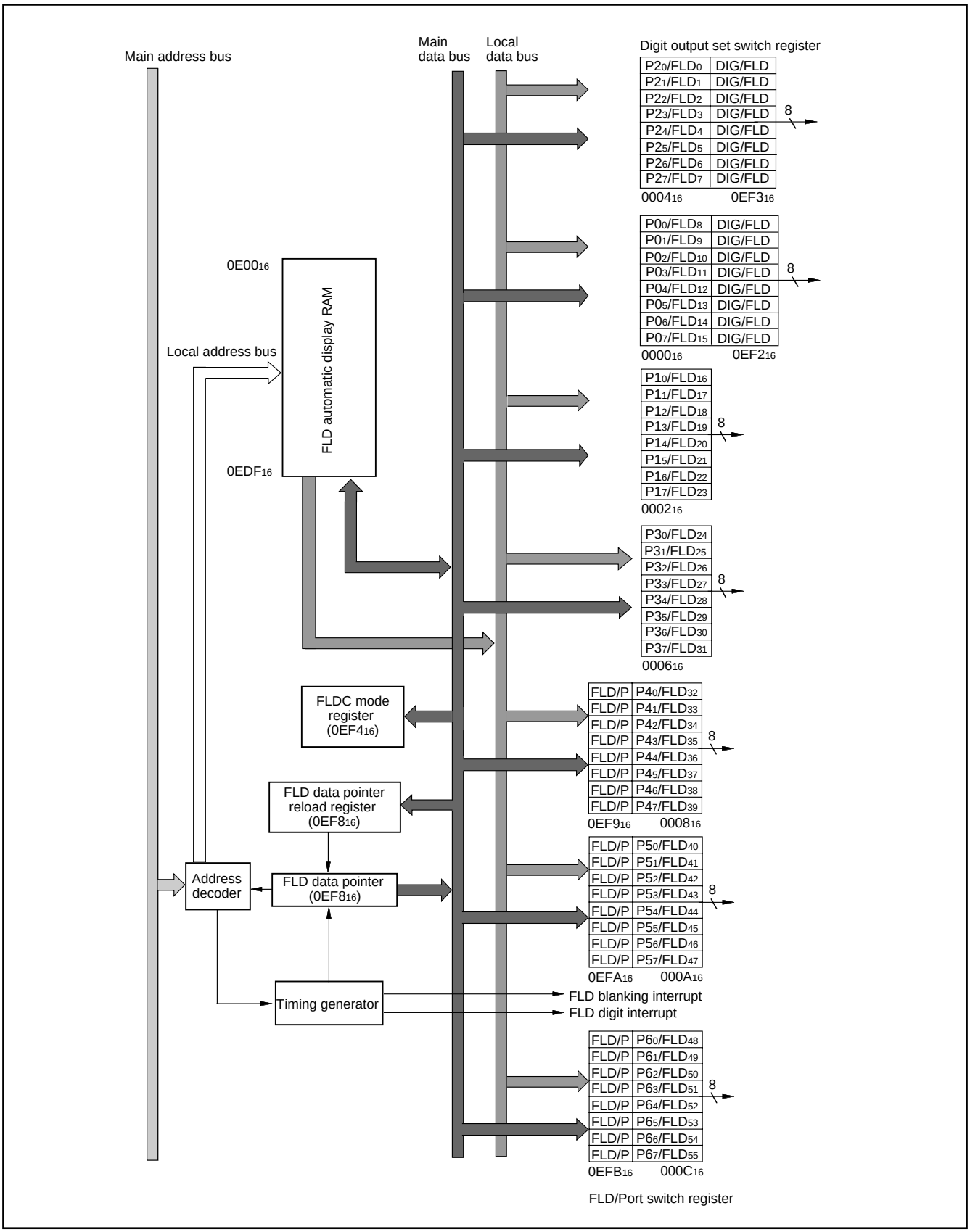
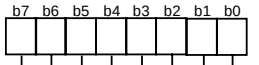


Fig. 44 Block diagram of FLD control circuit



FLDC mode register
(FLDM: address $0EF4_{16}$)

Automatic display control bit
0 : General-purpose mode
1 : Automatic display mode

Display start bit
0 : Stop display
1 : Display (start to display by switching "0" to "1")

Tscan control bits
b3b2
0 0 : FLD digit interrupt (at rising edge of each digit)
0 1 : 1 × Tdisp
1 0 : 2 × Tdisp } FLD blanking interrupt
1 1 : 3 × Tdisp } (at falling edge of the last digit)

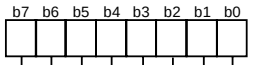
Timing number control bit
0 : 16 timing mode
1 : 32 timing mode

Gradation display mode selection control bit
0 : Not selecting
1 : Selecting (**Note**)

Tdisp counter count source selection bit
0 : $f(X_{IN})/16$
1 : $f(X_{IN})/64$

High-breakdown voltage port drivability selection bit
0 : Drivability strong
1 : Drivability weak

Note: When the gradation display mode is selected, the max. number of timing is 16 timing. (Be sure to set the timing number control bit to "0".)



FLD output control register
(FLDCON: address $0EFC_{16}$)

$P6_4$ to $P6_7$ output reverse bit
0 : Output normally
1 : Reverse output

Not used (return "0" when read); (Do not write "1".)

$P6_4$ to $P6_7$ Toff invalid bit
0 : Operation normally
1 : Toff invalid

Not used (return "0" when read); (Do not write "1".)

$P7_3$ dimmer output control bit
0 : Normal port
1 : Dimmer output

Generating/Not of CMOS port Toff section selection bit
0 : Toff section not generated
1 : Toff section generated

Generating/Not of high-breakdown voltage port Toff section selection bit
0 : Toff section not generated
1 : Toff section generated

Toff2 SET/RESET switch bit
0 : Toff2 RESET; Toff1 SET
1 : Toff2 SET; Tdisp RESET

Fig. 45 Structure of FLDC related registers (1)

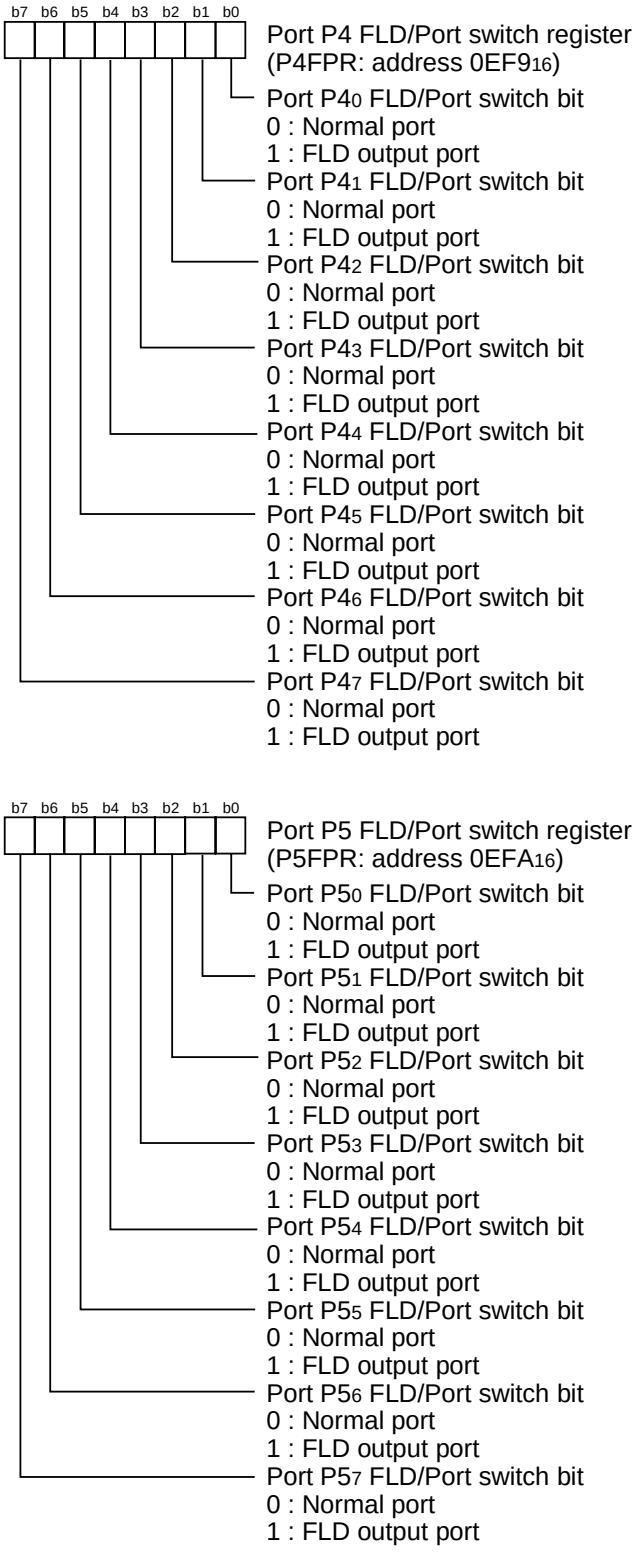


Fig. 46 Structure of FLDC related registers (2)

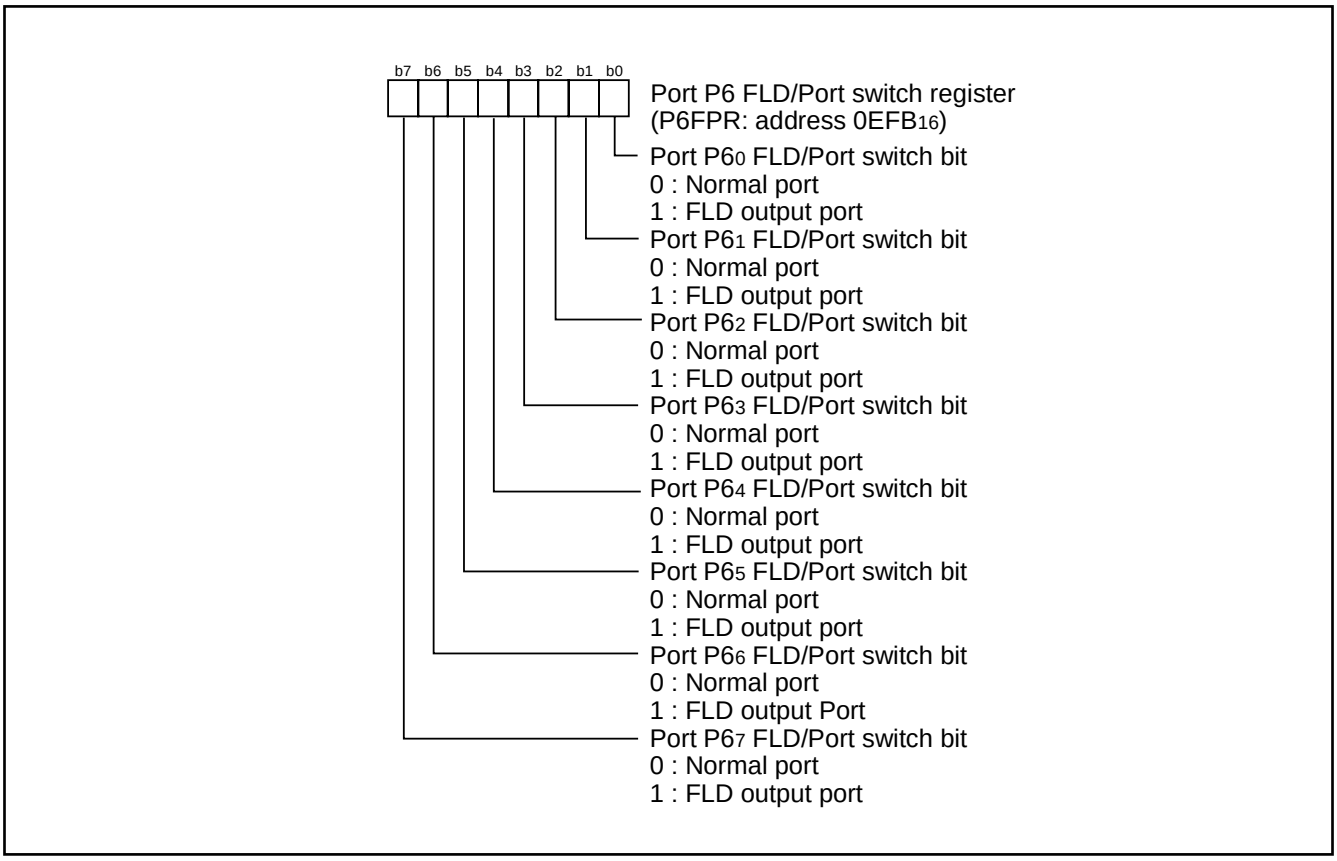


Fig. 47 Structure of FLDC related registers (3)

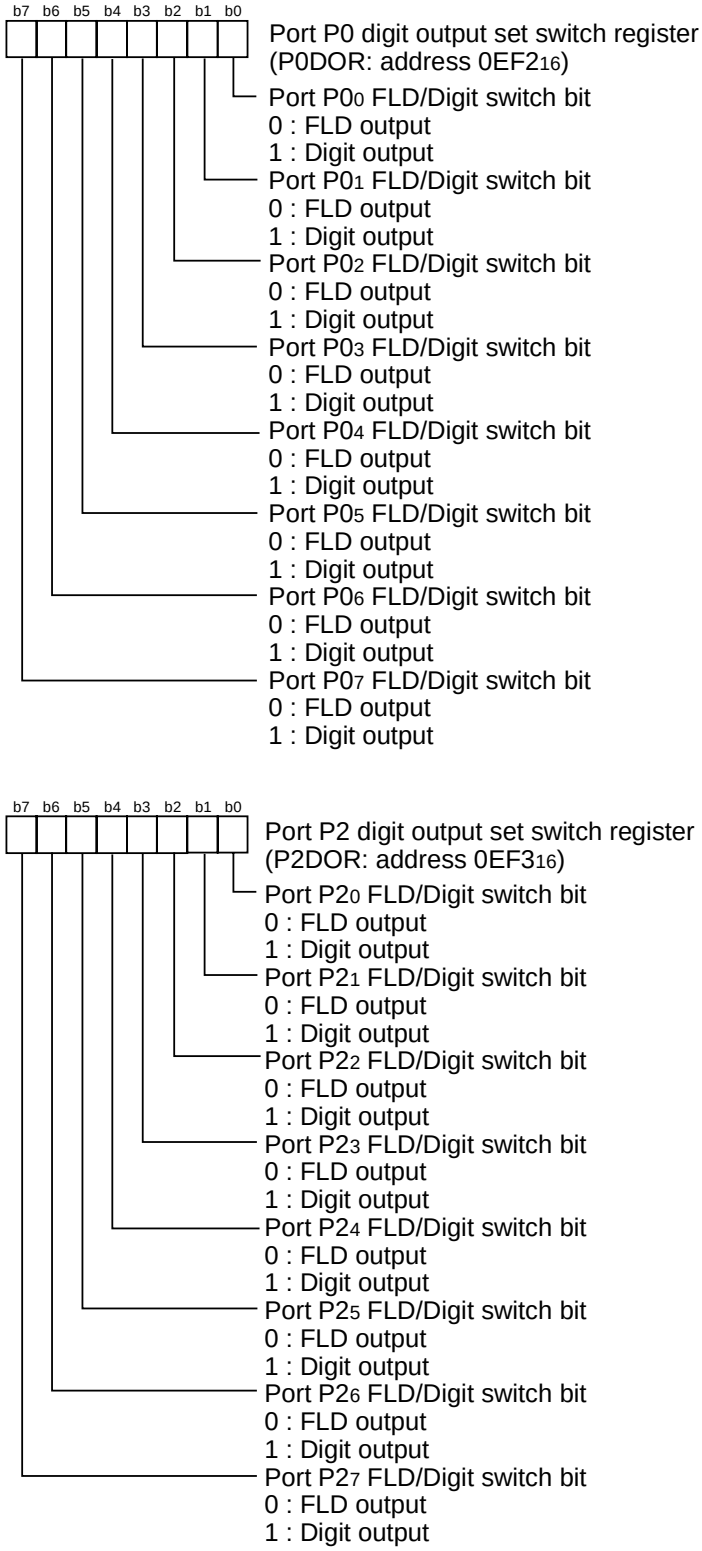


Fig. 48 Structure of FLDC related registers (4)

FLD Automatic Display Pins

P0 to P6 are the pins capable of automatic display output for the FLD. The FLD starts operating by setting the automatic display control bit (bit 0 at address 0EF4$_{16}$) to "1". There is the FLD output function that outputs the RAM contents from the port every timing or the digit output function that drives the port high with a digit timing. The FLD can be displayed using the FLD output for the segments and the digit or FLD output for the digits. When using the FLD output for the digits, be sure to write digit display patterns to the RAM in advance. The remaining segment and digit lines can be used as general-purpose ports. Settings of each port are shown below.

Table 10 Pins in FLD automatic display mode

Port	Automatic display pin	Setting method
P0, P2	FLD$_0$ to FLD$_{15}$	The individual bits of the digit output set switch registers (addresses 0EF2$_{16}$, 0EF3$_{16}$) can set each pin to either an FLD port ("0") or a digit port ("1"). When the pins are set for the digit port, the digit pulse output function is enabled, so that the digit pulses can always be output regardless the value of FLD automatic display RAM.
P1, P3	FLD$_{16}$ to FLD$_{31}$	Setting the automatic display control bit (bit 0 of address 0EF4$_{16}$) to "1" can set these ports to the FLD exclusive use port.
P4, P5, P6$_0$ to P6$_3$	FLD$_{32}$ to FLD$_{51}$	The individual bits of the FLD/Port switch register (addresses 0EF9$_{16}$ to 0EFB$_{16}$) can set each pin to either an FLD port ("1") or a general-purpose port ("0").
P6$_4$ to P6$_7$	FLD$_{52}$ to FLD$_{55}$	The individual bits of the port P6 FLD/Port switch register (address 0EFB$_{16}$) can set each pin to either FLD port ("1") or general-purpose port ("0"). A variety of output pulses can be available by setting of the FLD output control register (address 0EFC$_{16}$). The port output structure is the CMOS output. When using the port as a display pin, a driver IC must be installed externally.

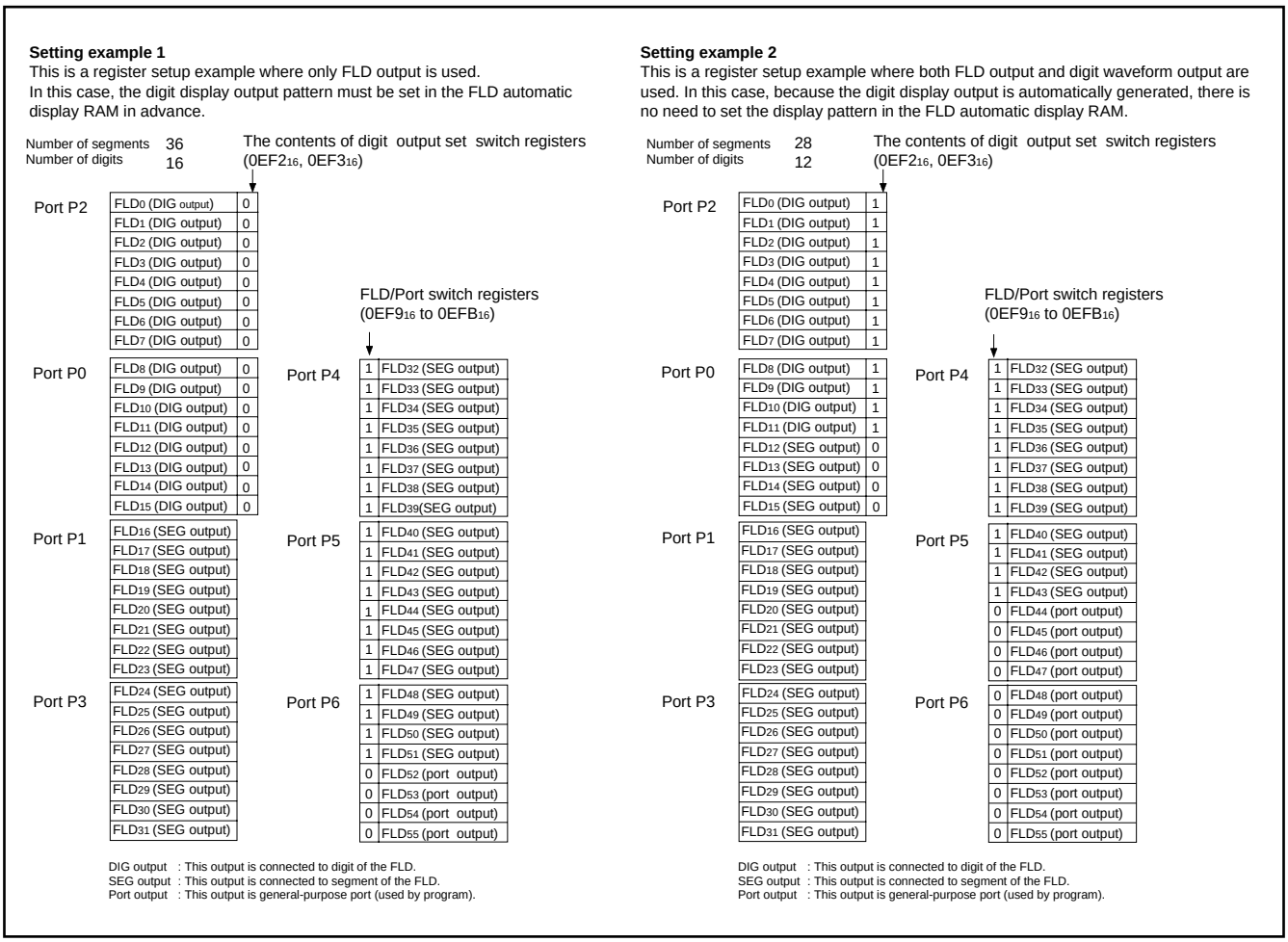


Fig. 49 Segment/Digit setting example

FLD Automatic Display RAM

The FLD automatic display RAM uses the 224 bytes of addresses $0E00_{16}$ to $0EDF_{16}$. For FLD, the 3 modes of 16-timing•ordinary mode, 16-timing•gradation display mode and 32-timing mode are available depending on the number of timings and the use/not use of gradation display.
The automatic display RAM in each mode is as follows:

(1) 16-timing•ordinary mode

This mode is used when the display timing is 16 or less. The 112 bytes of addresses $0E70_{16}$ to $0EDF_{16}$ are used as a FLD display data store area. Because addresses $0E00_{16}$ to $0E6F_{16}$ are not used as the automatic display RAM, they can be the ordinary RAM.

(2) 16-timing•gradation display mode

This mode is used when the display timing is 16 or less, in which mode each segment can be set for dark or bright display. The 224 bytes of addresses $0E00_{16}$ to $0EDF_{16}$ are used. The 112 bytes of addresses $0E70_{16}$ to $0EDF_{16}$ are used as an FLD display data store area, while the 112 bytes of addresses $0E00_{16}$ to $0E6F_{16}$ are used as a gradation display control data store area.

(3) 32-timing mode

This mode is used when the display timing is 16 or greater. This mode can be used for up to 32-timing.
The 224 bytes of addresses $0E00_{16}$ to $0EDF_{16}$ are used as an FLD display data store area.

The FLD data pointer (address $0EF8_{16}$) is a register to count display timings. This pointer has a reload register. When the pointer underflow occurs, it starts counting over again after being reloaded with the initial value in the reload register. Make sure that (the timing counts – 1) is set to the FLD data pointer. When writing data to this address, the data is written to the FLD data pointer reload register; when reading data from this address, the value in the FLD data pointer is read.

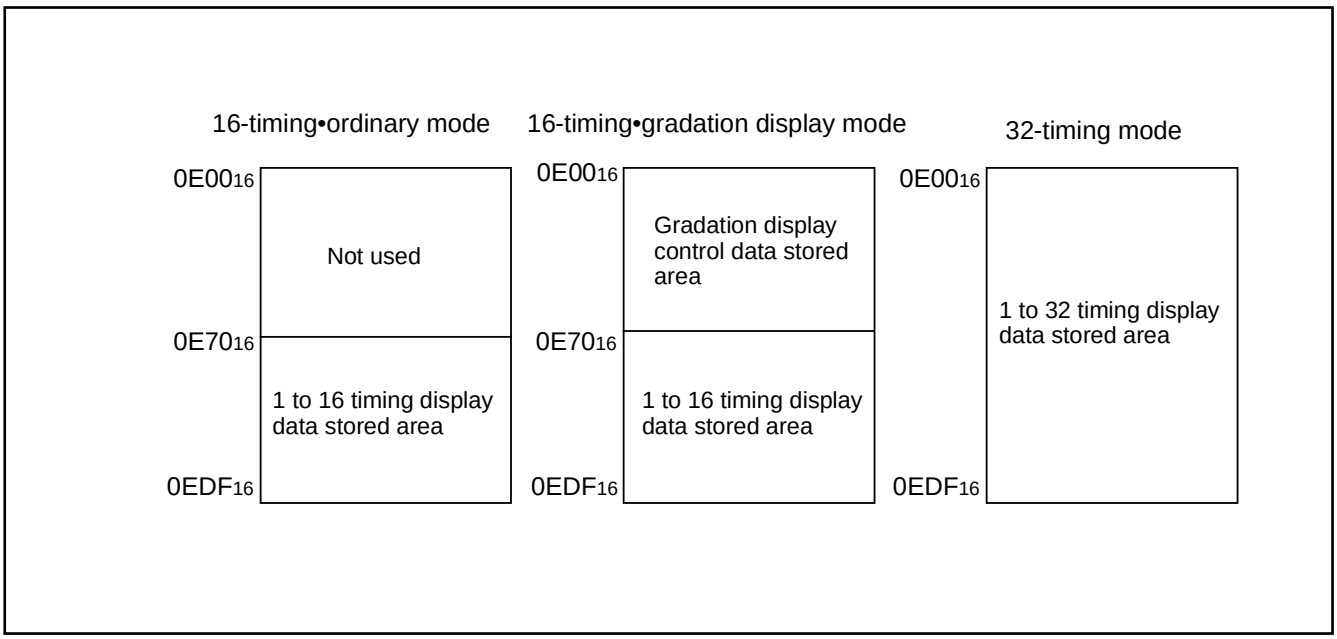


Fig. 50 FLD automatic display RAM assignment

Data Setup

(1) 16-timing•ordinary mode

The area of addresses $0E70_{16}$ to $0EDF_{16}$ are used as a FLD automatic display RAM.

When data is stored in the FLD automatic display RAM, the last data of FLD port P6 is stored at address $0E70_{16}$, the last data of FLD port P5 is stored at address $0E80_{16}$, the last data of FLD port P4 is stored at address $0E90_{16}$, the last data of FLD port P3 is stored at address $0EA0_{16}$, the last data of FLD port P1 is stored at address $0EB0_{16}$, the last data of FLD port P0 is stored at address $0EC0_{16}$, and the last data of FLD port P2 is stored at address $0ED0_{16}$, to assign in sequence from the last data respectively.

The first data of the FLD port P6, P5, P4, P3, P1, P0, and P2 is stored at an address which adds the value of (the timing number – 1) to the corresponding addresses $0E70_{16}$, $0E80_{16}$, $0E90_{16}$, $0EA0_{16}$, $0EB0_{16}$, $0EC0_{16}$ and $0ED0_{16}$.

Set the FLD data pointer reload register to the value given by (the timing number – 1).

(2) 16-timing•gradation display mode

Display data setting is performed in the same way as that of the 16-timing•ordinary mode. Gradation display control data is arranged at an address resulting from subtracting 0070_{16} from the display data store address of each timing and pin. Bright display is performed by setting “0”, and dark display is performed by setting “1” .

(3) 32-timing Mode

The area of addresses $0E00_{16}$ to $0EDF_{16}$ is used as a FLD automatic display RAM.

When data is stored in the FLD automatic display RAM, the last data of FLD port P6 is stored at address $0E00_{16}$, the last data of FLD port P5 is stored at address $0E20_{16}$, the last data of FLD port P4 is stored at address $0E40_{16}$, the last data of FLD port P3 is stored at address $0E60_{16}$, the last data of FLD port P1 is stored at address $0E80_{16}$, the last data of FLD port P0 is stored at address $0EA0_{16}$, and the last data of FLD port P2 is stored at address $0EC0_{16}$, to assign in sequence from the last data respectively.

The first data of the FLD port P6, P5, P4, P3, P1, P0, and P2 is stored at an address which adds the value of (the timing number – 1) to the corresponding addresses $0E00_{16}$, $0E20_{16}$, $0E40_{16}$, $0E60_{16}$, $0E80_{16}$, $0EA0_{16}$ and $0EC0_{16}$.

Set the FLD data pointer reload register to the value given by (the timing number – 1).

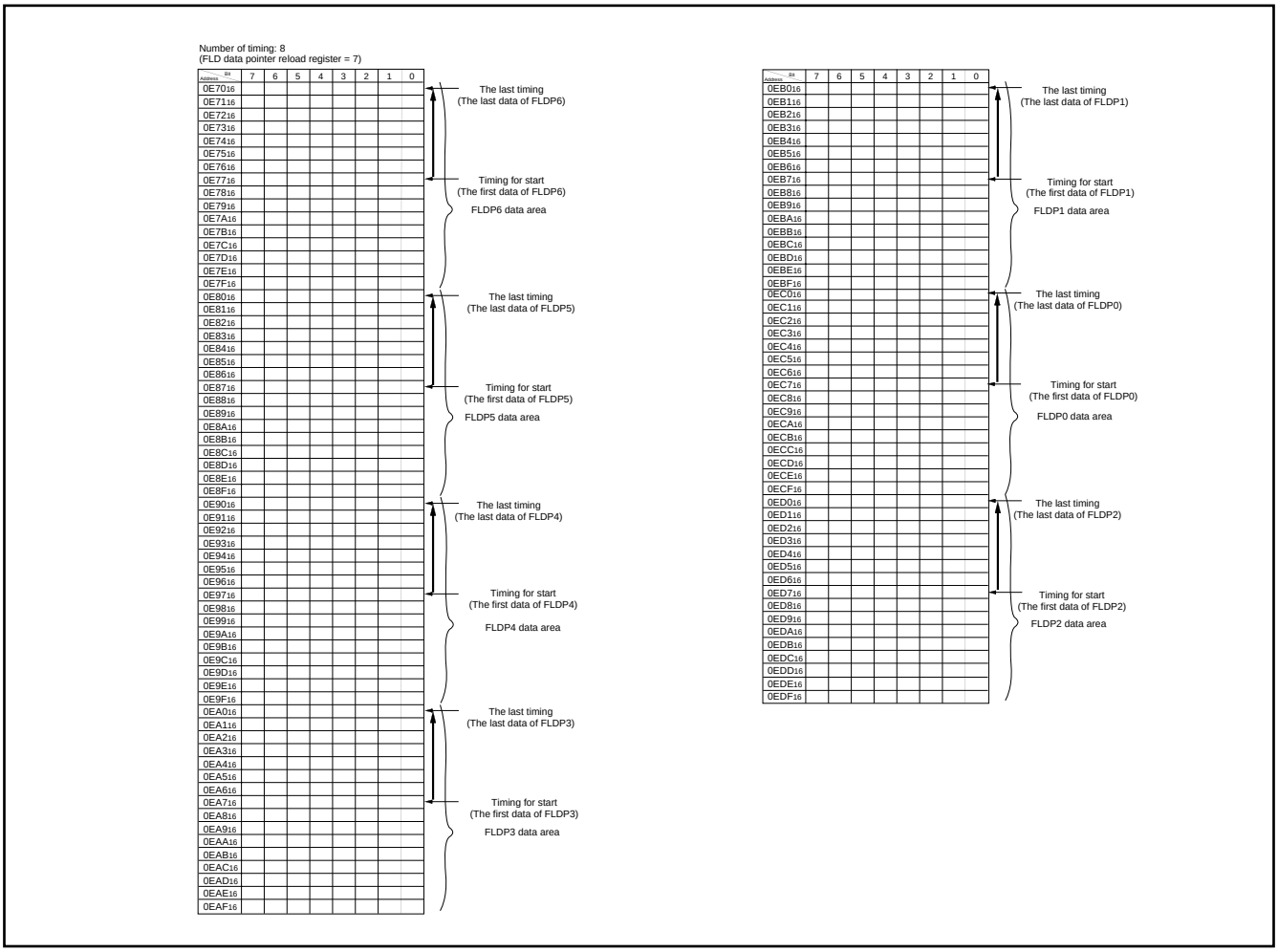


Fig. 51 Example of using FLD automatic display RAM in 16-timing•ordinary mode

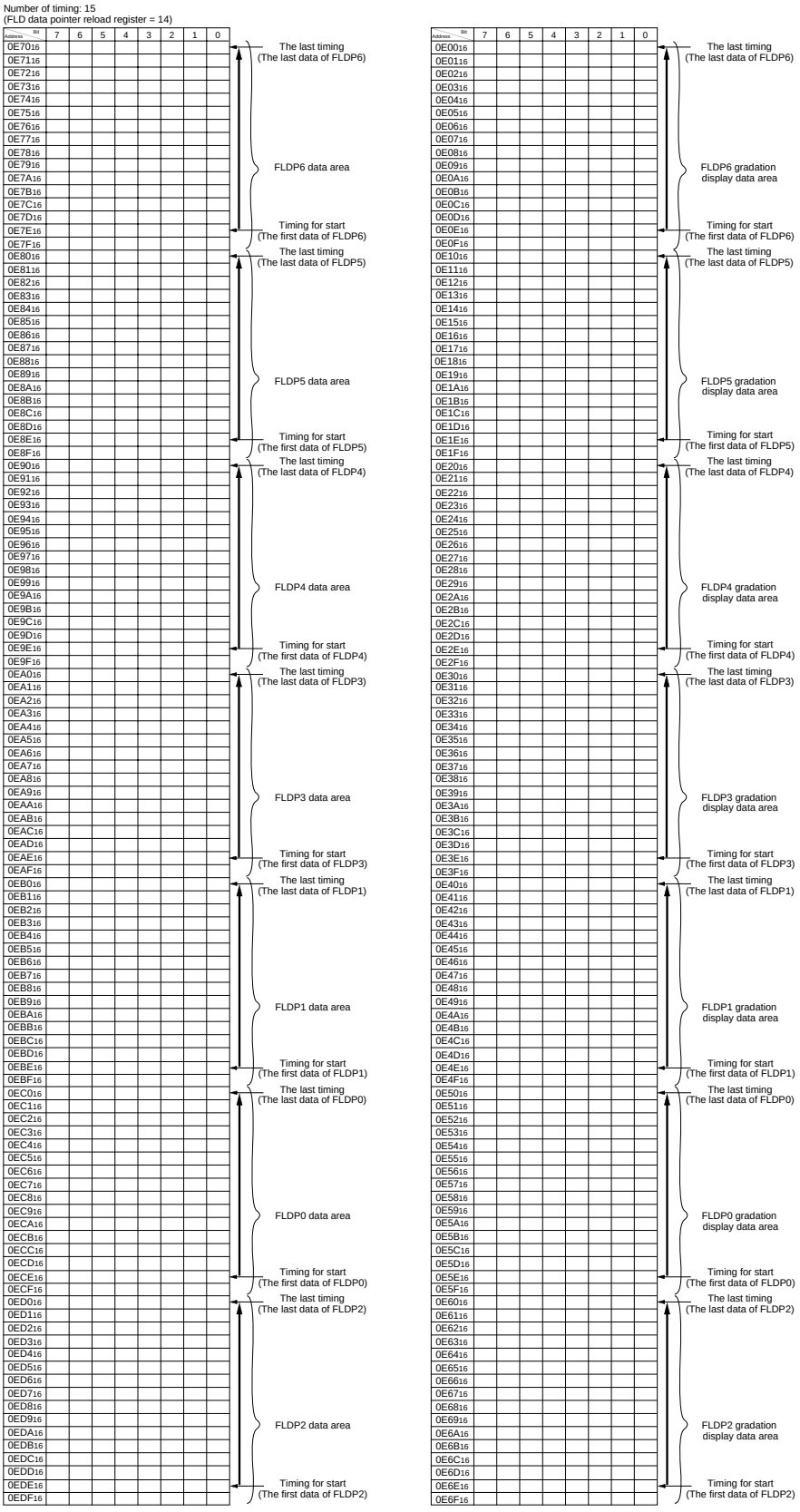


Fig. 52 Example of using FLD automatic display RAM in 16-timing•gradation display mode

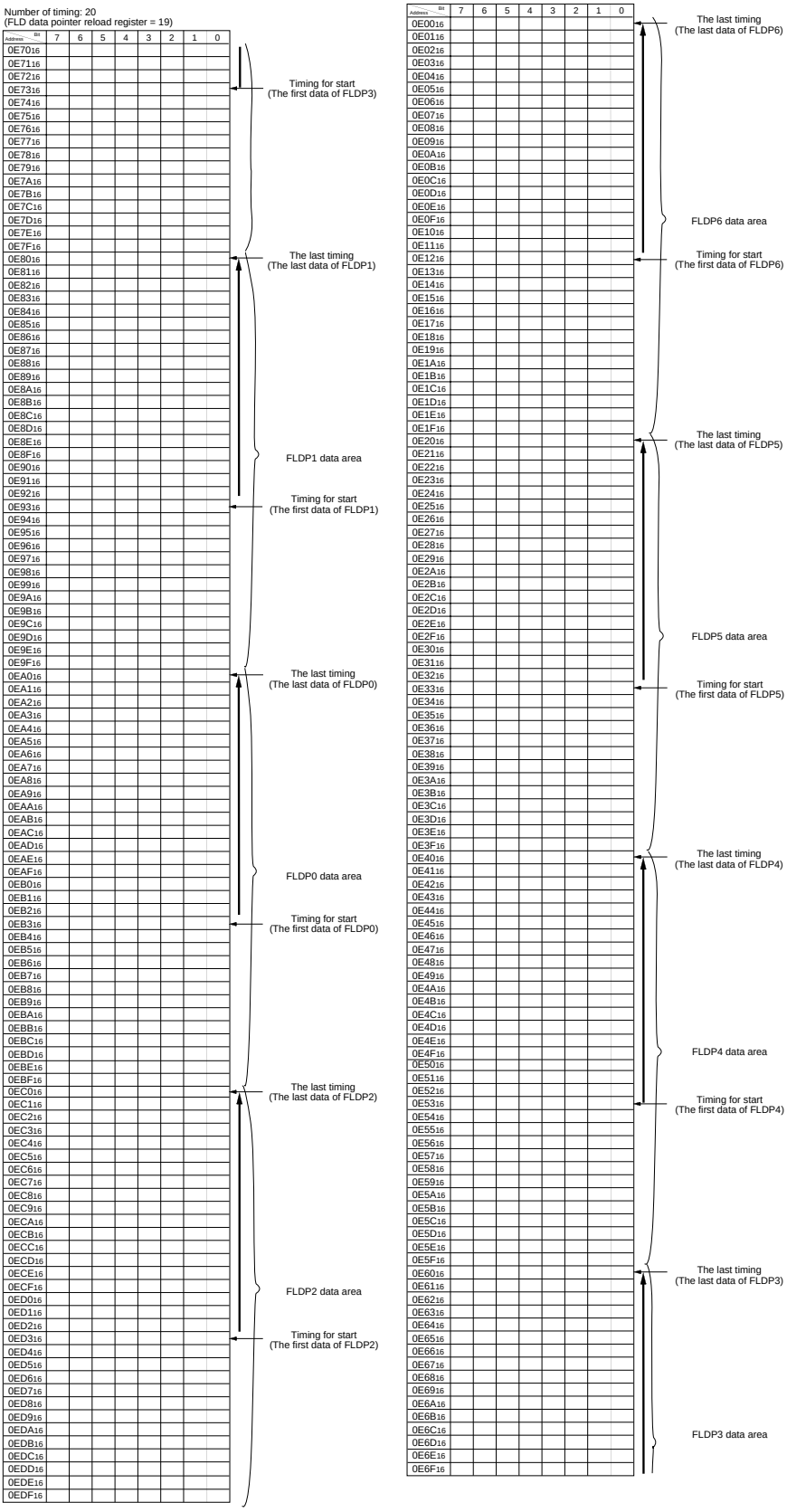


Fig. 53 Example of using FLD automatic display RAM in 32-timing mode

Timing Setting

Each timing is set by the FLDC mode register, Tdisp time set register, Toff1 time set register, and Toff2 time set register.

(1) Tdisp time setting

The Tdisp time means the length of display timing. In non-gradation display mode, it consists of the FLD display output term and the Toff1 time. In gradation display mode, it consists of the display output term and the Toff1 time plus a low signal output term for dark display. Set the Tdisp time by the Tdisp counter count source selection bit of the FLDC mode register and the Tdisp time set register. Supposing that the value of the Tdisp time set register is n, the Tdisp time is represented as Tdisp = (n+1) × t (t: count source). When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Tdisp time set register is 200 ($C8_{16}$), the Tdisp time is: Tdisp = (200 + 1) × 4.0 µs (at X_{IN} = 4 MHz) = 804 µs. When reading the Tdisp time set register, the counting value is read out.

(2) Toff1 time setting

The Toff1 time means a non-output (low signal output) time to prevent blurring of FLD and for dimmer display. Use the Toff1 time set register to set this Toff1 time. Make sure the value set to Toff1 is smaller than Tdisp and Toff2. Supposing that the value of the Toff1 time set register is n1, the Toff1 time is represented as Toff1 = n1 × t. When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff1 time set register is 30 ($1E_{16}$), Toff1 = 30 × 4.0 µs (at X_{IN} = 4 MHz) = 120 µs.
Be sure to set the value of 03_{16} or more to the Toff1 time set register (address $0EF6_{16}$).

(3) Toff2 time setting

The Toff2 time is time for dark display. For bright display, the FLD display output remains effective until the counter that is counting Tdisp underflows. For dark display, however, "L" (or "off") signal is output when the counter that is counting Toff2 underflows. This Toff2 time setting is valid only for FLD ports which are in the gradation display mode and whose gradation display control RAM value is "1" .
Set the Toff2 time by the Toff2 time set register. Make sure the value set to Toff2 is smaller than Tdisp but larger than Toff1. Supposing that the value of the Toff2 time set register is n2, the Toff2 time is represented as Toff2 = n2 × t. When the Tdisp counter count source selection bit of the FLDC mode register is "0" and the value of the Toff2 time set register is 180 ($B4_{16}$), Toff2 = 180 × 4.0 µs (at X_{IN} = 4 MHz) = 720 µs.
When bit 7 of the FLD output control register (address $0EFC_{16}$) is set to "1", be sure to set the value of 03_{16} or more to the Toff2 time set register (address $0EF7_{16}$).

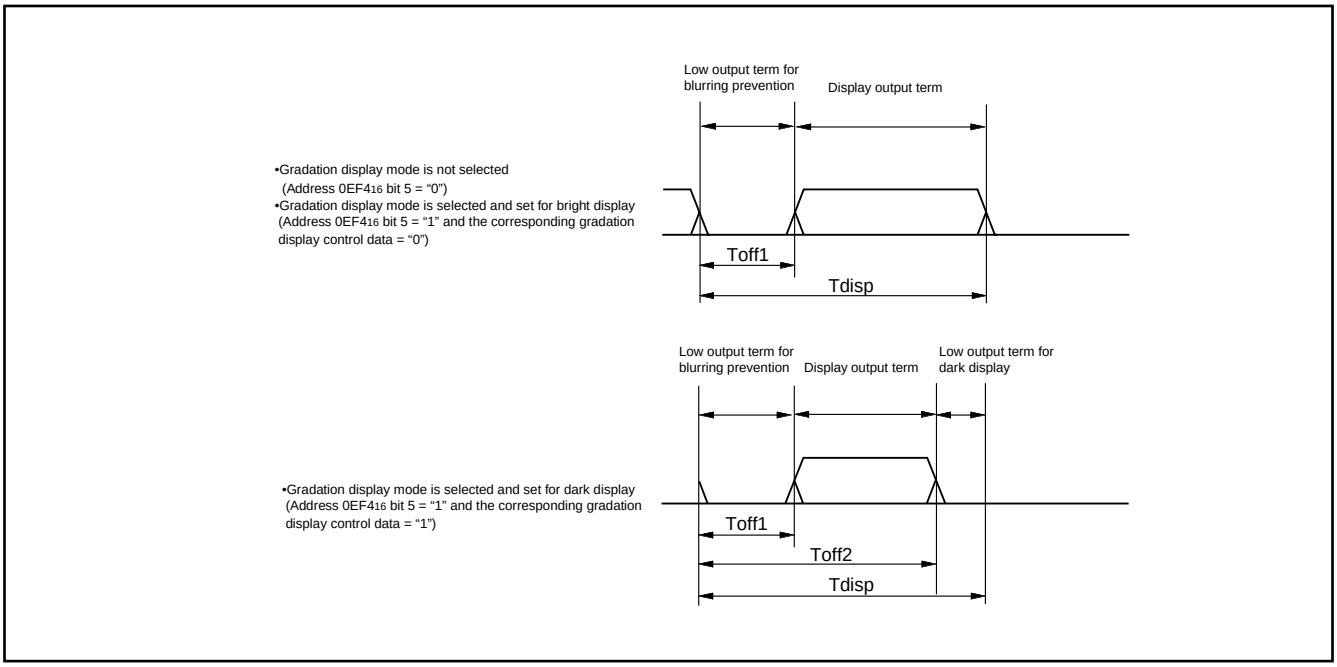


Fig. 54 FLD and digit output timing

FLD Automatic Display Start

Automatic display starts by setting both the automatic display control bit (bit 0 of address 0EF4$_{16}$) and the display start bit (bit 1 of address 0EF4$_{16}$) to "1". The RAM contents at a location apart from the start address of the automatic display RAM for each port by (FLD data pointer (address 0EF8$_{16}$) – 1) are output to each port. The FLD data pointer (address 0EF8$_{16}$) counts down in the Tdisp interval. When the count results in "FF$_{16}$", the pointer is reloaded and starts counting over again. Before setting the display start bit (bit 1 of address 0EF4$_{16}$) to "1", be sure to set the FLD/port switch registers, digit output set switch registers, FLDC mode register, Tdisp time set register, Toff1 time set register, Toff2 time set register, and FLD data pointer.

During FLD automatic display, the display start bit always keeps "1", and FLD automatic display can be interrupted by writing "0" to this bit.

Key-scan and Interrupt

Either the FLD digit interrupt or FLD blanking interrupt can be selected using the Tscan control bits (bits 2, 3 of address 0EF4$_{16}$).

The FLD digit interrupt is generated when the Toff1 time in each timing expires (at rising edge of digit output). Key scanning that makes use of FLD digits can be achieved using each FLD digit interrupt. To use FLD digit interrupts for key scanning, follow the procedure described below:

(1) Read the port value each time the interrupt occurs.

(2) The key is fixed on the last digit interrupt.

The output digit positions can be determined by reading the FLD data pointer (address 0EF8$_{16}$).

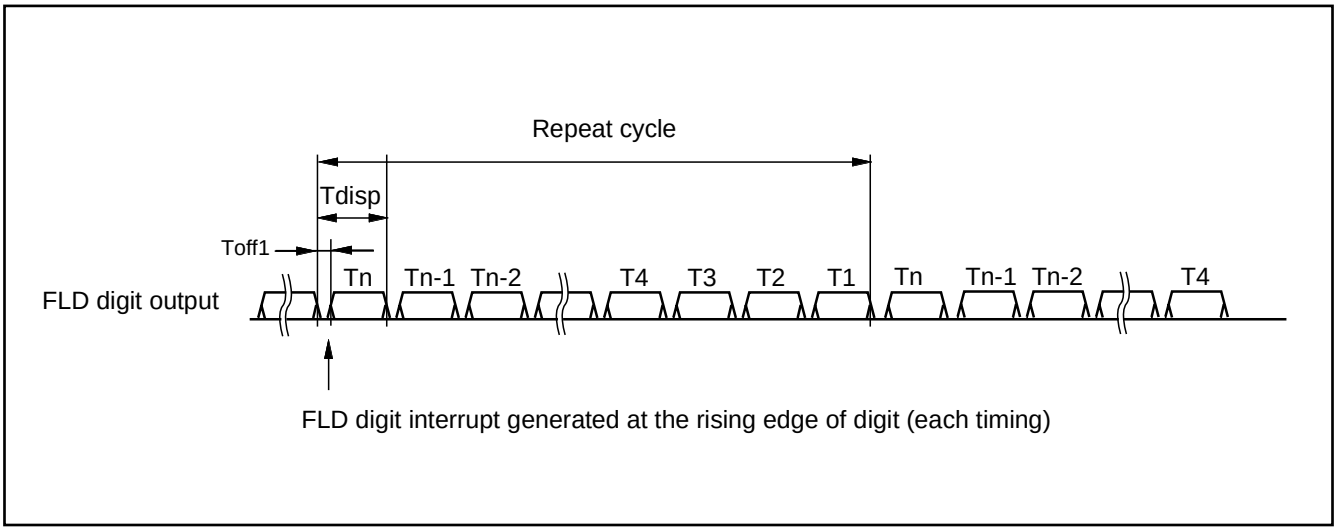


Fig. 55 Timing using digit interrupt

The FLD blanking interrupt is generated when the FLD data pointer (address 0EF8$_{16}$) reaches "FF$_{16}$". The FLD automatic display output is turned off for a duration of 1 × Tdisp, 2 × Tdisp, or 3 × Tdisp depending on post-interrupt settings. During this time, key scanning that makes use of FLD segments can be achieved. When the key scanning is performed with the segment during key-scan blanking time Tscan, follow the procedure described below:

(1) Write "0" to the automatic display control bit (bit 0 of address 0EF4$_{16}$).
(2) Set the port corresponding to the segment for key scanning to the output port.
(3) Perform key scanning.
(4) Write "1" to the automatic display control bit.

■ Note

When performing a key-scan according to the above steps 1 to 4, take the following points into consideration.

1. Do not set the display start bit (bit 1 of address 0EF4$_{16}$) to "0".
2. Do not set "1" in the ports corresponding to digits.

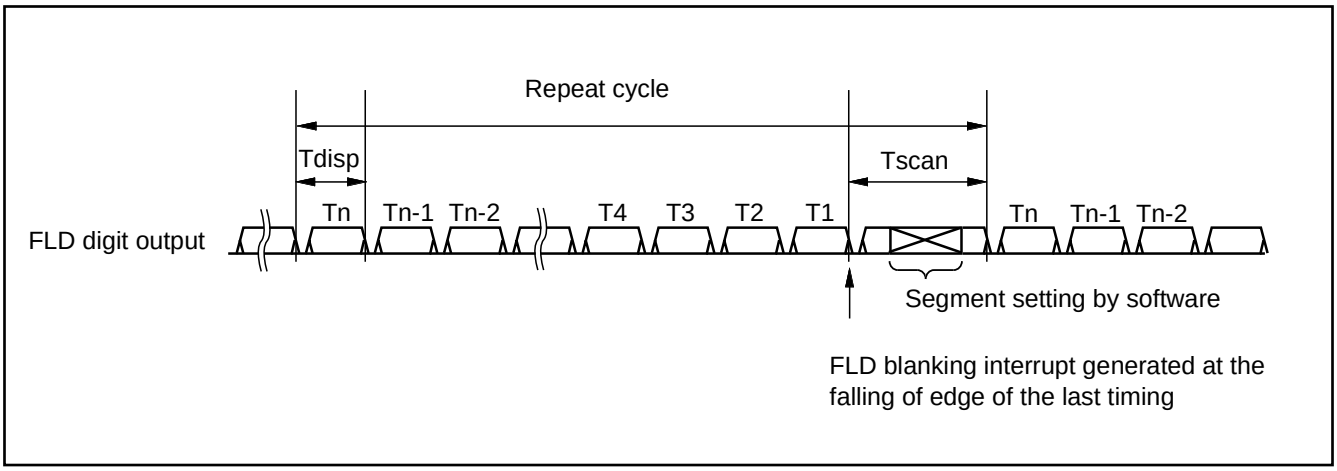


Fig. 56 Timing using FLD blanking interrupt

P64 to P67 Expansion Function

Ports P64 to P67 are CMOS output structure. FLD digit outputs can be increased as many as 16 lines by connecting a decoder converting 4-bit to 16-bit data to these ports. P64 to P67 have the function to allow for connection to a decoder converting 4-bit to 16-bit data.

(1) P64 to P67 Toff invalid function

This function disables the Toff1 time and Toff2 time and outputs display data for the duration of Tdisp. (See Figure 57.) This can be achieved by setting the P64 to P67 Toff invalid bit (bit 2 of address $0EFC_{16}$) to "1".

(2) Dimmer signal output function

This function allows a dimmer signal creation signal to be output from DIMOUT (P73). The dimmer function can be achieved by controlling the decoder with this signal. (See Figure 57.) This function can be set by setting P73 dimmer output control bit (bit 4 of address $0EFC_{16}$) to "1".

Unlike the Toff section generating/nothing function, this function disables all display data.

(3) P64 to P67 FLD output reverse function

P64 to P67 have the function to reverse the polarity of the FLD output. This function is useful in adjusting the polarity when using an externally installed driver.

The output polarity can be reversed by setting the P64 to P67 output reverse bit of the FLD output control register (bit 0 of address $0EFC_{16}$) to "1".

■ Note

In the case of gradation display mode and dark display, P64 to P67 Toff invalid function is disabled.

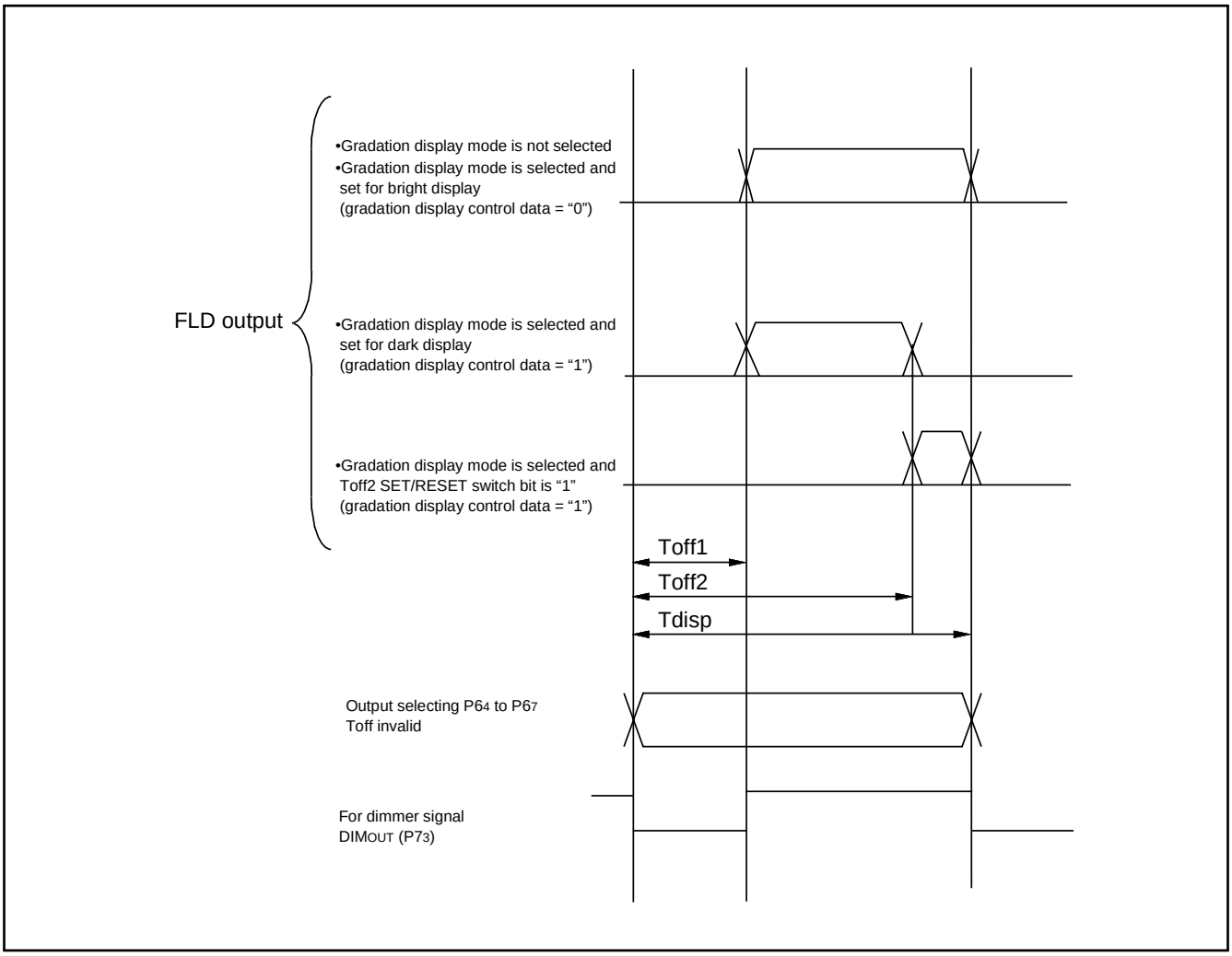


Fig. 57 P64 to P67 FLD output pulses

Toff Section Generate/Nothing Function

The function is for reduction of useless noises which generated as every switching of ports, because of the combined capacity of among FLD ports. When the continuous data is output to each FLD port, the Toff1 section of the continuous parts is not generated. (See Figure 58)

If it needs Toff1 section on FLD pulses, set the generating /not of CMOS port Toff section selection bit (bit 5 of address 0EFC16) to "1" and set the generating /not of high-breakdown-voltage port Toff section selection bit to "1".

High-breakdown-voltage ports (P2, P0, P1, P3, P4, P5, P63 to P60, total 52 pins) generate Toff1 section by setting the generating /not of high-breakdown-voltage port Toff section selection bit to "1".

The CMOS ports (P64 to P67, total 4 pins) generate Toff1 section by setting the generating /not of CMOS port Toff section selection bit to "1".

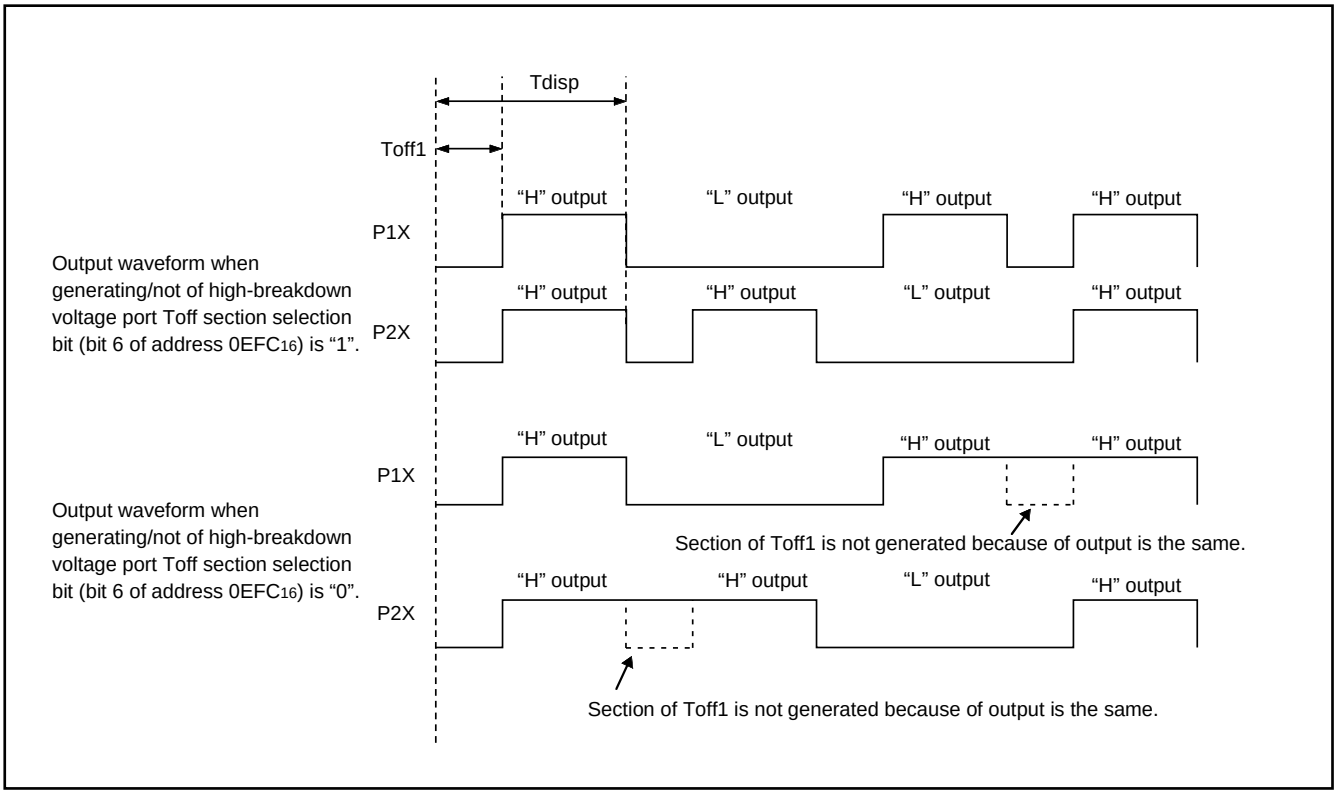


Fig. 58 Toff section generating/nothing function

Toff2 SET/RESET Switch Function

In gradation display mode, the values set by the Toff2 time set register (TOFF2) are effective. When the Toff2 SET/RESET switch bit of FLD output control register (bit 7 of address 0EFC16) is "0", RAM data is output to the FLD output ports (SET) at the time that is set by TOFF1 and it is turned to "0" (RESET) at the time that is set by TOFF2.

When Toff2 SET/RESET switch bit is "1", RAM data is output (SET) at the time that is set by TOFF2 and it is turned to "0" (RESET) when the Tdisp time expires.

■ Note

In the case of gradation display mode and dark display, the Toff section generate/nothing function is disabled.

Digit Pulses Output Function

$P0_0$ to $P0_7$ and $P2_0$ to $P2_7$ can output digit pulses by using the digit output set switch registers. Set the digit output set switch registers by setting as many consecutive 1s as the timing count from $P2_0$. The contents of FLD automatic display RAM for the ports that have been selected for digit output are disabled, and the pulse shown in Figure 59 is output automatically.

The output timing consists of Tdisp time and Toff1 time, and Toff2 time does not exist.

Because the contents of FLD automatic display RAM are disabled, the segment data can be changed easily even when segment data and digit data coexist at the same address in the FLD automatic display RAM.

This function is effective in 16-timing•ordinary mode and 16-timing gradation display mode. If a value is set exceeding the timing count (FLD data pointer reload register's set value + 1) for any port, the output of such port is "L".

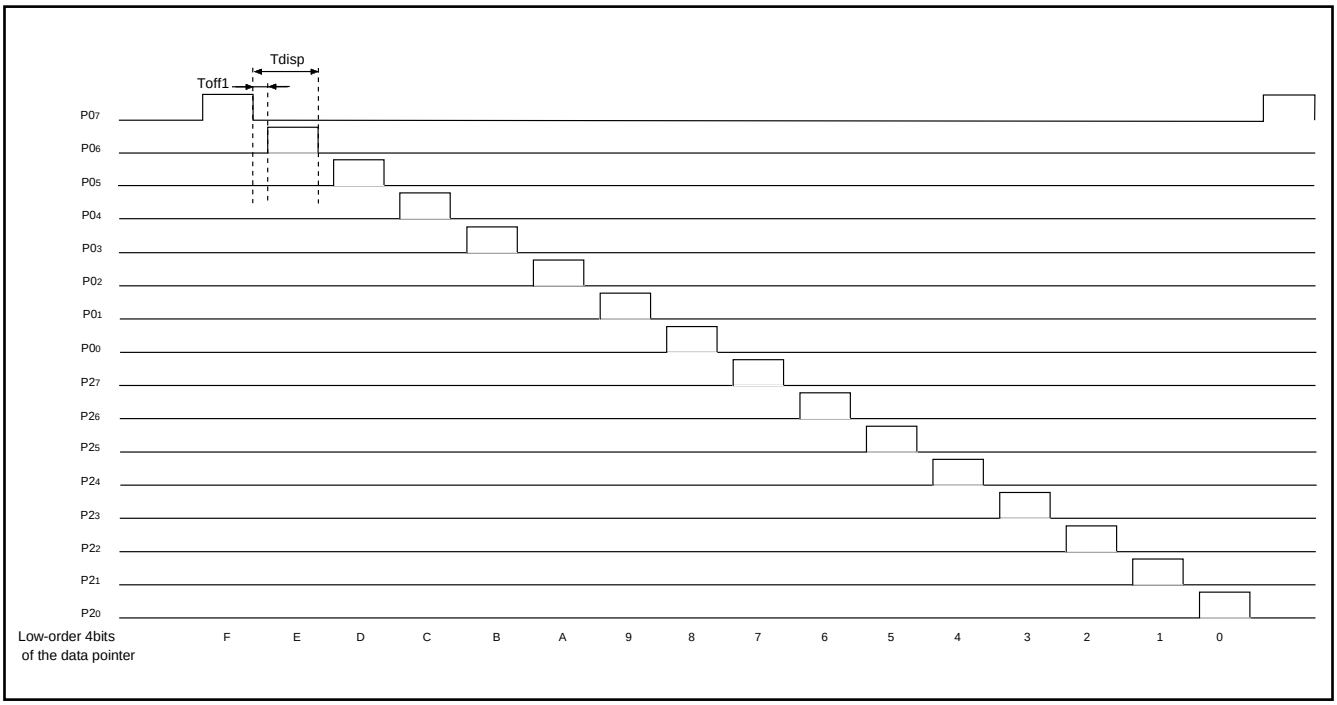


Fig. 59 Digit pulses output function

A-D CONVERTER

The 38B7 group has a 10-bit A-D converter. The A-D converter performs successive approximation conversion.

[A-D Conversion Register] ADH, ADL

One of these registers is a high-order register, and the other is a low-order register. The high-order 8 bits of a conversion result is stored in the A-D conversion register (high-order) (address 0034_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the A-D conversion register (low-order) (address 0033_{16}).

During A-D conversion, do not read these registers.

[AD/DA Control Register] ADCON

This register controls A-D converter. Bits 3 to 0 are analog input pin selection bits. Bit 4 is an AD conversion completion bit and "0" during A-D conversion. This bit is set to "1" upon completion of A-D conversion.

A-D conversion is started by writing "0" in this bit.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVss and V_{REF} by 1024, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports PA_7/AN_7–PA_0/AN_0, and $P9_7/BUZ0_2/AN_{15}$ to $P9_0/SIN_3/AN_8$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog inputvoltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so that set f(X_{IN}) to at least 250 kHz during A-D conversion. Additionally, bit 7 of the CPU mode register (address $003B_{16}$) must be set to "0".

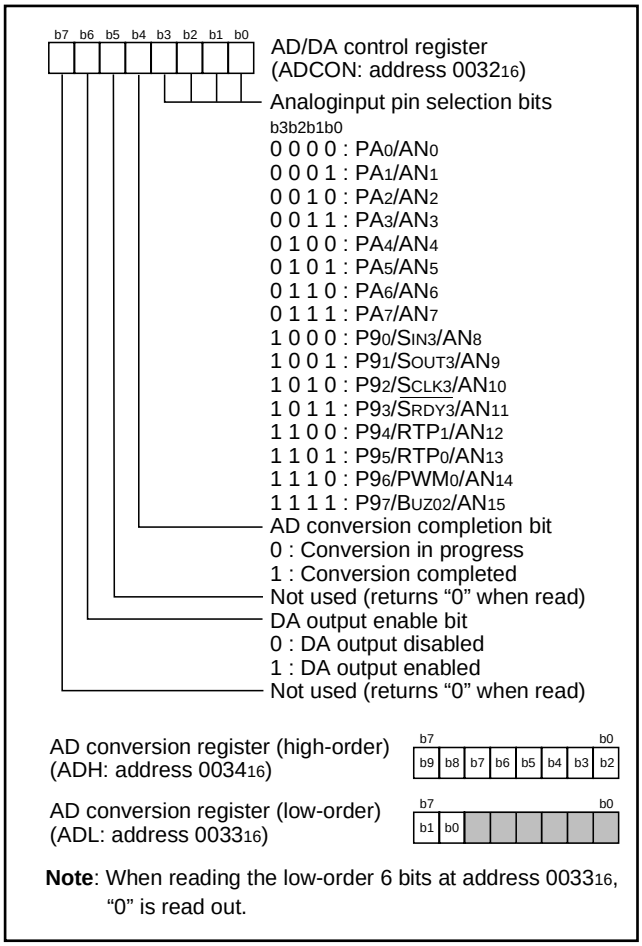


Fig. 60 Structure of AD/DA control register

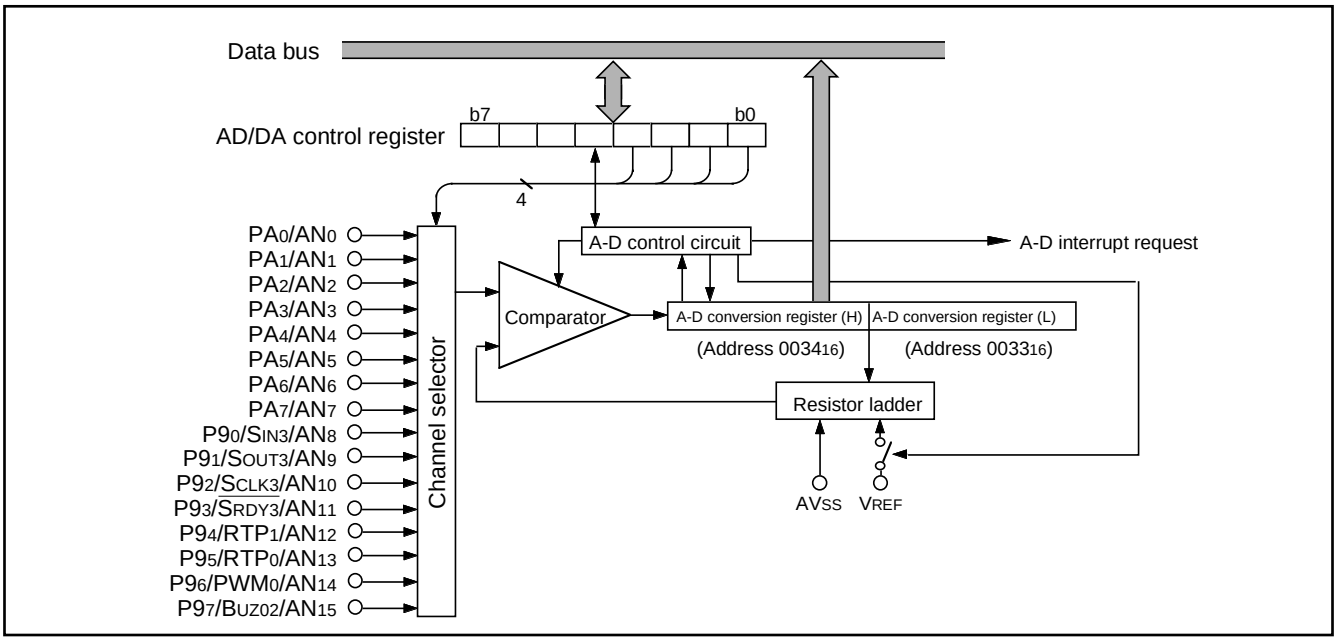


Fig. 61 Block diagram of A-D converter

D-A CONVERTER

The 38B7 group has one internal D-A converter with 8-bit resolution.

The D-A conversion is performed by setting the value in the D-A conversion register. The result of D-A conversion is output from the DA pin by setting the DA output enable bit to "1".

When using the D-A converter, the PB_0/DA port direction register bit must be set to "0" (input status).

The output analog voltage V is determined by the value n (decimal notation) in the D-A conversion register as follows:

$V = V_{REF} \times n/256$ (n = 0 to 255)

Where V_{REF} is the reference voltage.

At reset, the D-A conversion register is cleared to "00_{16}", and the DA output enable bit is cleared to "0", and PB_0/DA pin becomes high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

Set V_{CC} to 3.0 V or more when using the D-A converter.

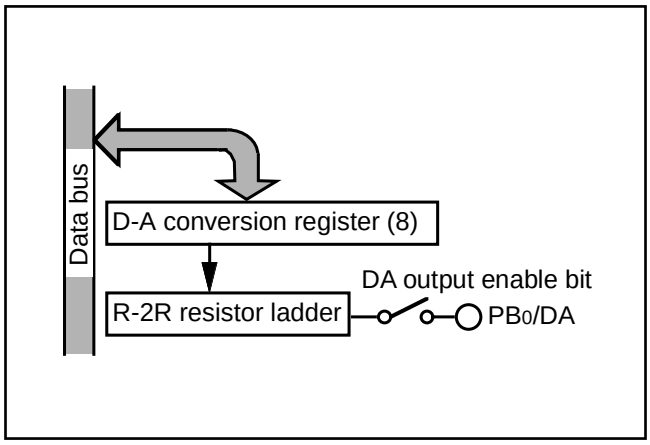


Fig. 62 Block diagram of D-A converter

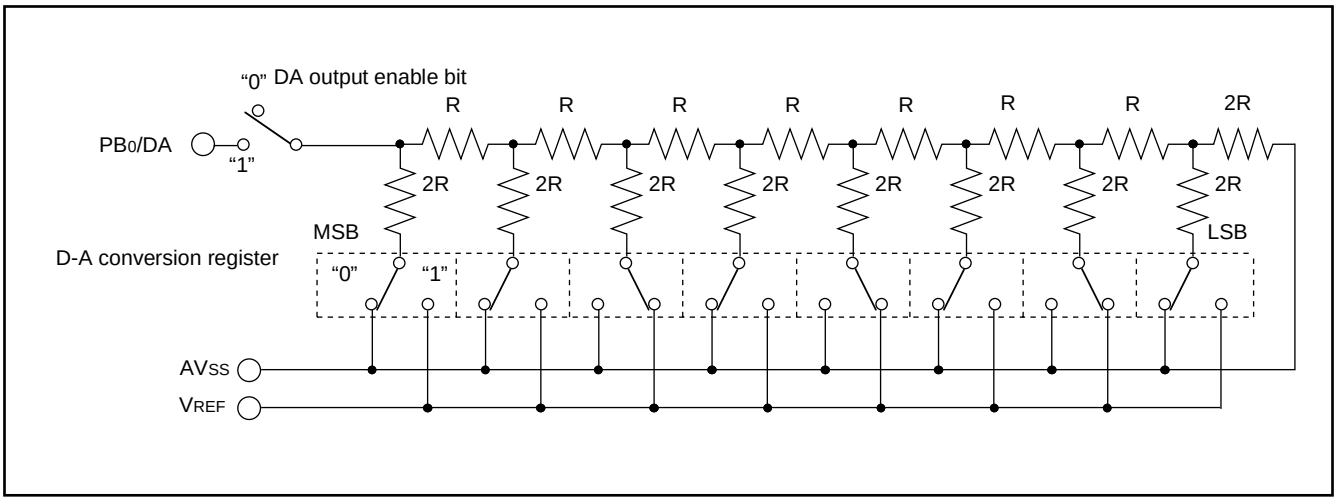


Fig. 63 Equivalent connection circuit of D-A converter

PWM (Pulse Width Modulation)

The 38B7 group has a PWM function with a 14-bit resolution. When the oscillation frequency X_{IN} is 4 MHz, the minimum resolution bit width is 250 ns and the cycle period is 4096 µs. The PWM timing generator supplies a PWM control signal based on a signal that is the frequency of the X_{IN} clock.

The explanation in the rest assumes X_{IN} = 4 MHz.

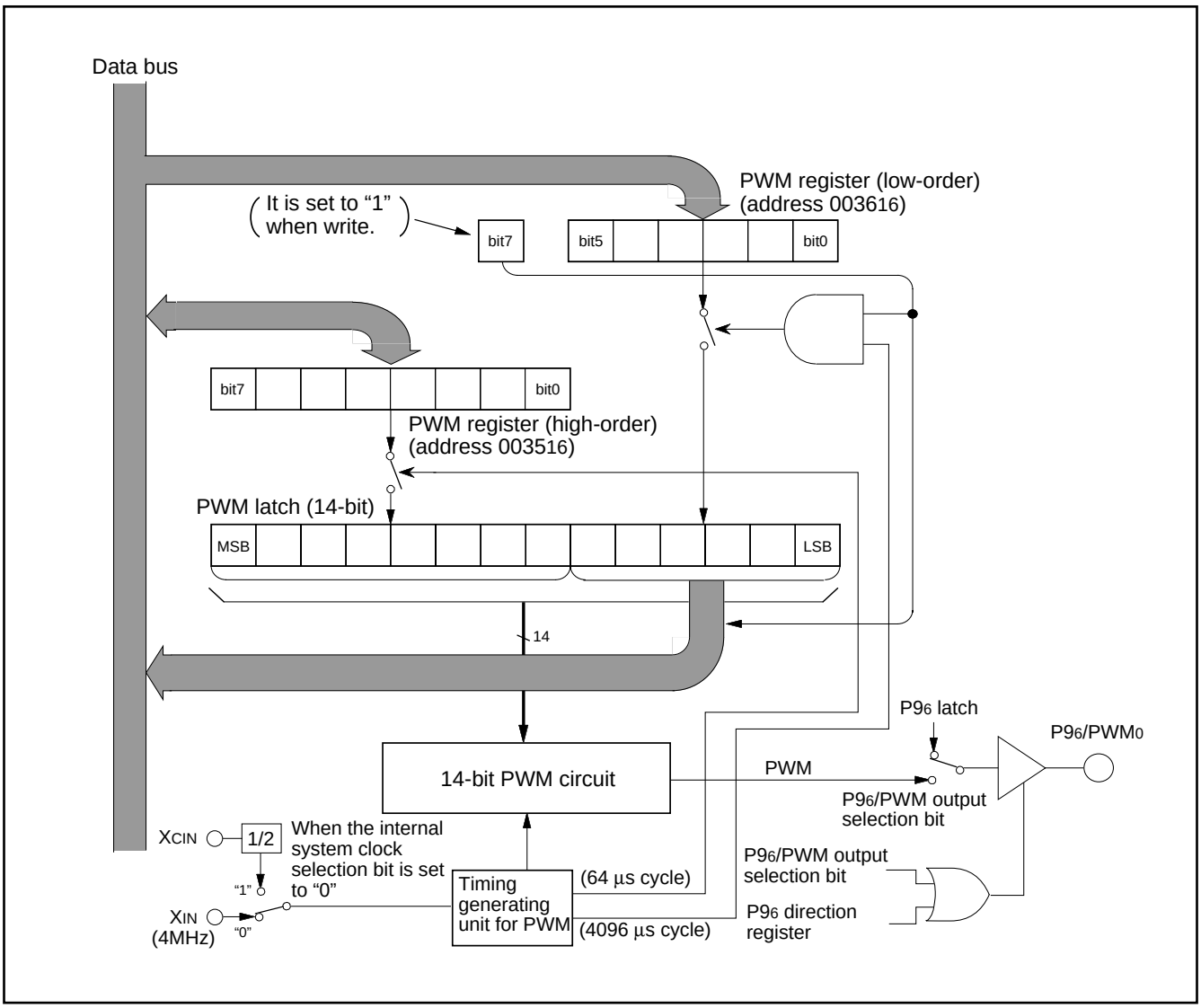


Fig. 64 PWM block diagram

Data Setup

The PWM output pin also function as port $P9_6$. Set port $P9_6$ to be the PWM output pin by setting bit 0 of the PWM control register (address 0026_{16}) to "1". The high-order 8 bits of output data are set in the high-order PWM register PWMH (address 0035_{16}) and the low-order 6 bits are set in the low-order PWM register PWML (address 0036_{16}).

PWM Operation

The timing of the 14-bit PWM function is shown in Figure 65.

The 14-bit PWM data is divided into the low-order 6 bits and the high-order 8 bits in the PWM latch.

The high-order 8 bits of data determine how long an "H" level signal is output during each sub-period. There are 64 sub-periods in each period, and each sub-period t is 256 × τ (= 64 µs) long. The signal's "H" has a length equal to N times τ, and its minimum resolution = 250 ns.

The last bit of the sub-period becomes the ADD bit which is specified either "H" or "L," by the contents of PWML. As shown in Table 11, the ADD bit is decided either "H" or "L."

That is, only in the sub-period tm shown in Table 11 in the PWM cycle period T = 64 t, the "H" duration is lengthened during the minimum resolution width τ period in comparison with the other period.

For example, if the high-order eight bits of the 14-bit data are "03_{16}" and the low-order six bits are "05_{16}," the length of the "H" level output in sub-periods t8, t24, t32, t40 and t56 is 4 τ, and its length 3 τ in all other sub-periods.

Time at the "H" level of each sub-period almost becomes equal because the time becomes length set in the high-order 8 bits or becomes the value plus t, and this sub-period t (= 64 µs, approximate 15.6 kHz) becomes cycle period approximately.

Transfer From Register to Latch

Data written to the PWML register is transferred to the PWM latch once in each PWM period (every 4096 µs), and data written to the PWMH register is transferred to the PWM latch once in each sub-period (every 64 µs). Pulses output from the PWM output pin correspond to this latch contents.

When the PWML register is read, the contents of the latch are read. However, bit 7 of the PWML register indicates whether the transfer to the PWM latch is completed: the transfer is completed when bit 7 is "0", it is not done when bit 7 is "1".

Table 11 Relationship between low-order 6-bit data and setting period of ADD bit

Low-order 6-bit data (LSB)	Sub-periods tm lengthened (m = 0 to 63)
0 0 0 0 0 0	None
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ..., 57, 59, 61, 63

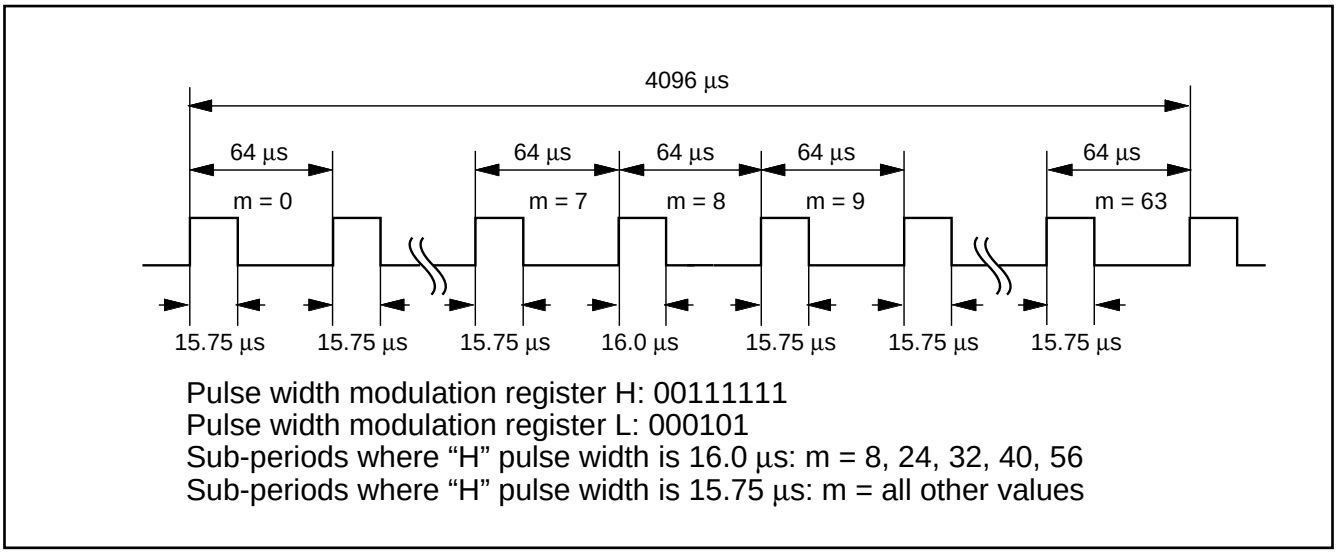


Fig. 65 PWM timing

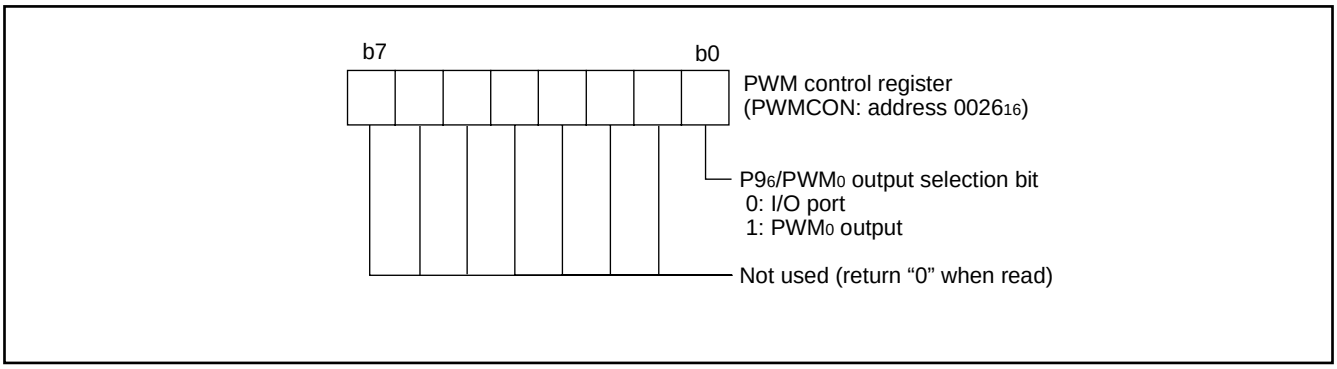


Fig. 66 Structure of PWM control register

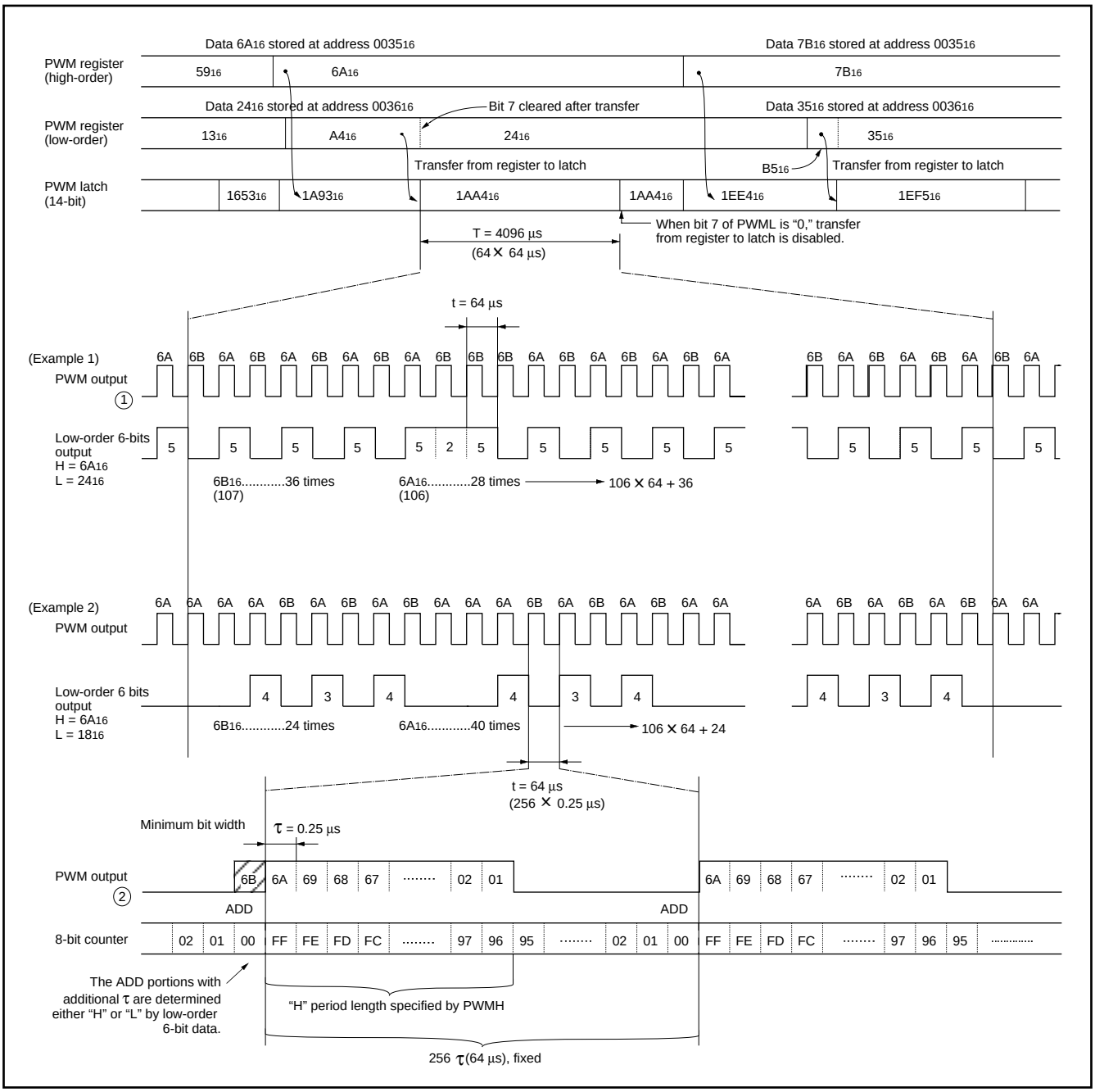


Fig. 67 14-bit PWM timing

INTERRUPT INTERVAL DETERMINATION FUNCTION

The 38B7 group has an interrupt interval determination circuit.

This interrupt interval determination circuit has an 8-bit binary up counter. Using this counter, it determines a duration of time from the rising edge (falling edge) of an input signal pulse on the P72/INT2 pin to the rising edge (falling edge) of the signal pulse that is input next.

How to determine the interrupt interval is described below.

1. Enable the INT2 interrupt by setting bit 2 of the interrupt control register 1 (address 003E16). Select the rising interval or falling interval by setting bit 2 of the interrupt edge selection register (address 003A16).
2. Set bit 0 of the interrupt interval determination control register (address 003116) to "1" (interrupt interval determination operating).
3. Select the sampling clock of 8-bit binary up counter by setting bit 1 of the interrupt interval determination control register.
4. When the signal of polarity which is set on the INT2 pin (rising or falling edge) is input, the 8-bit binary up counter starts counting up of the selected counter sampling clock.
5. When the signal of polarity selected above is input again, the value of the 8-bit binary up counter is transferred to the interrupt interval determination register (address 003016), and the remote control interrupt request occurs. Immediately after that, the 8-bit binary up counter continues to count up again from "0016".
6. When count value reaches "FF16", the 8-bit binary up counter stops counting up. Then, simultaneously when the next counter sampling clock is input, the counter sets value "FF16" to the interrupt interval determination register to generate the counter overflow interrupt request.

Noise Filter

The P72/INT2 pin builds in the noise filter.

The noise filter operation is described below.

1. Select the sampling clock of the input signal with bits 2 and 3 of the interrupt interval determination control register. When not using the noise filter, set "0016".
2. The P72/INT2 input signal is sampled in synchronization with the selected clock. When sampling the same level signal in a series of three sampling, the signal is recognized as the interrupt signal, and the interrupt request occurs.

When setting bit 4 of interrupt interval determination control register to "1", the interrupt request can occur at both rising and falling edges.

When using the noise filter, set the minimum pulse width of the INT2 input signal to 3 cycles or more of the sample clock.

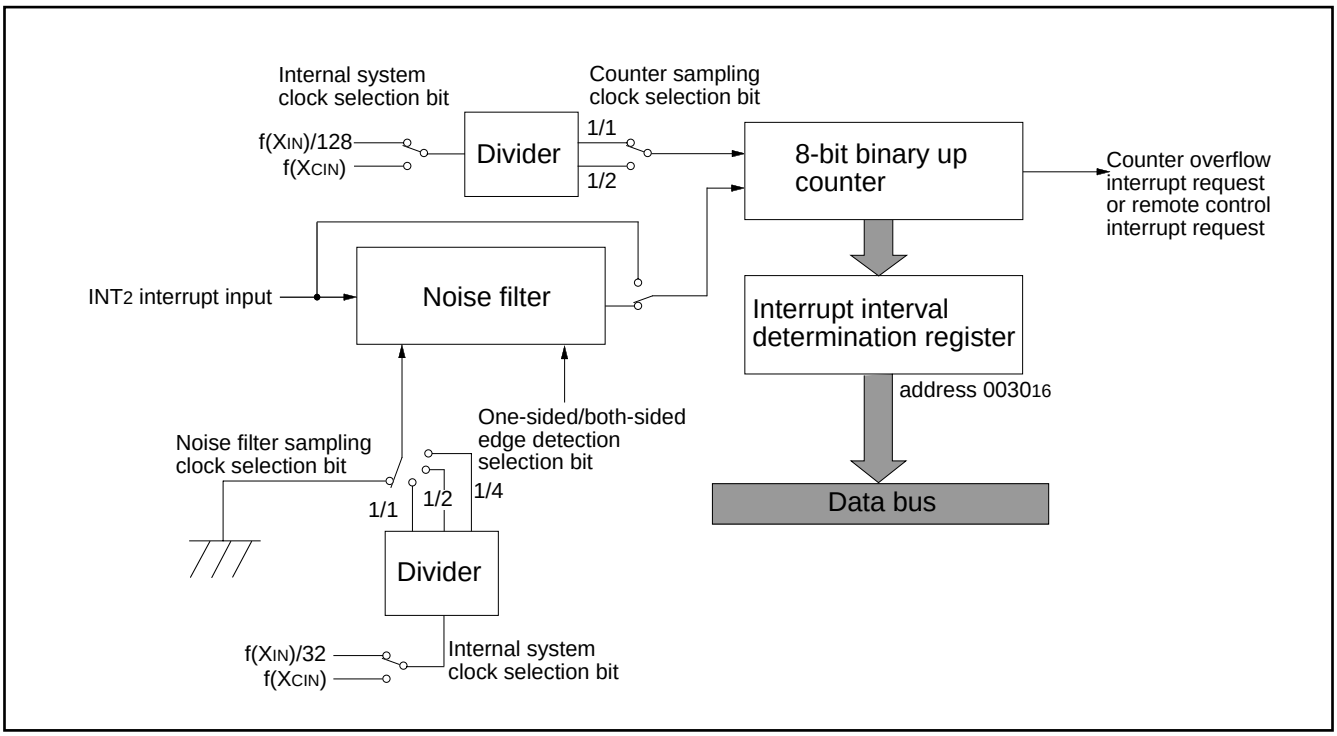


Fig. 68 Interrupt interval determination circuit block diagram

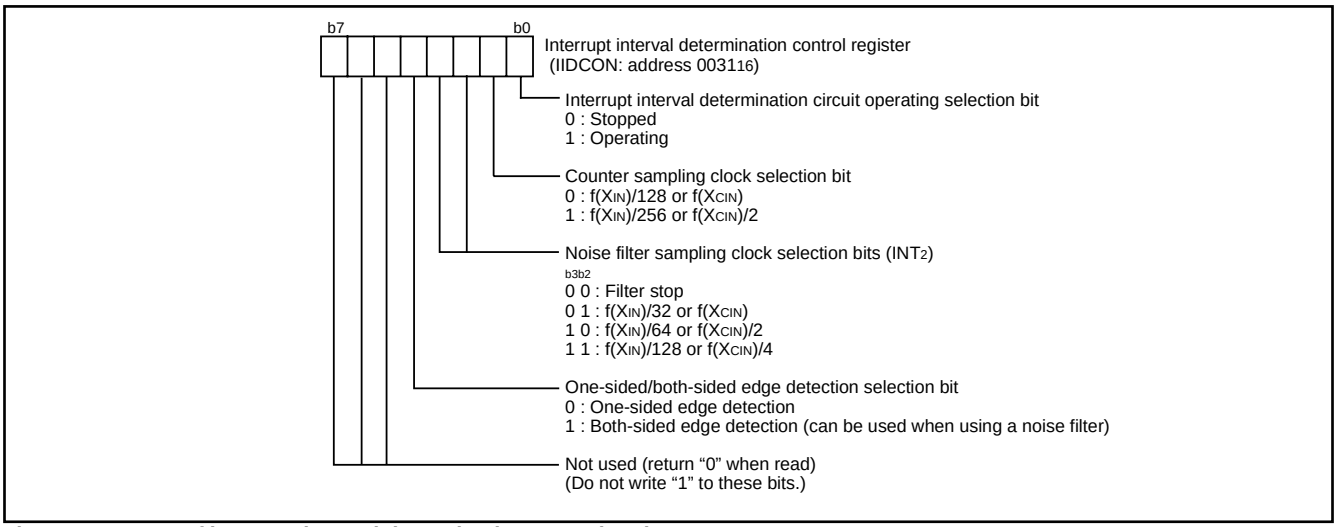


Fig. 69 Structure of interrupt interval determination control register

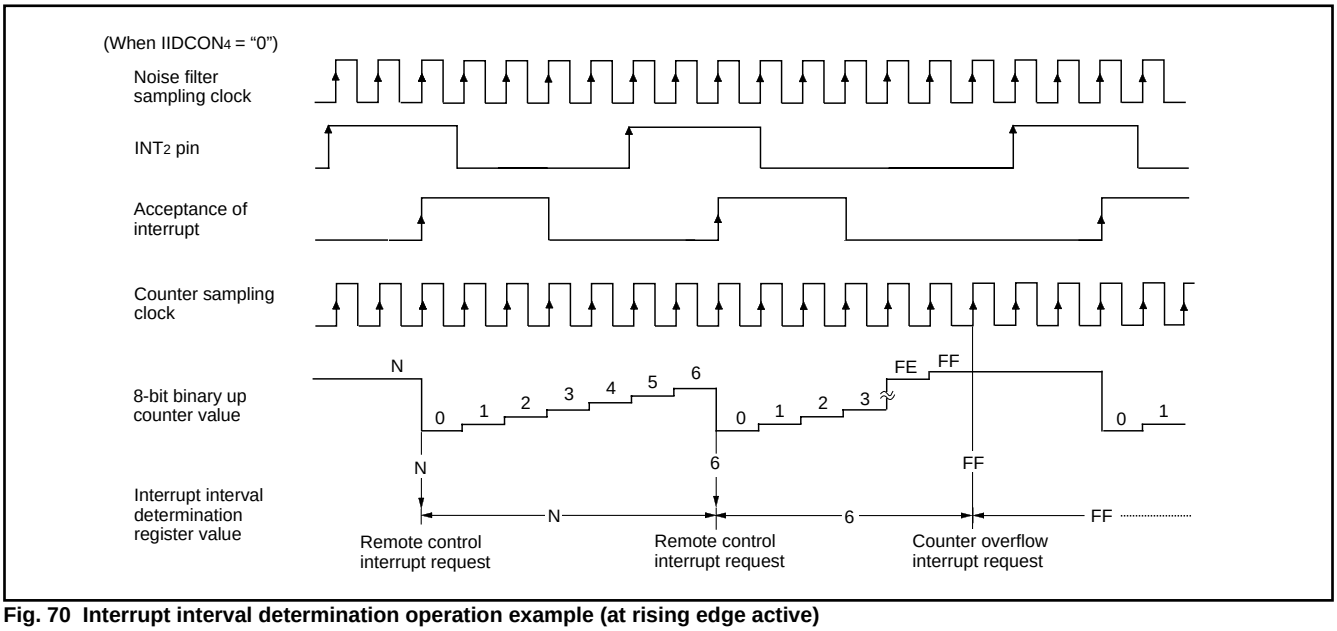


Fig. 70 Interrupt interval determination operation example (at rising edge active)

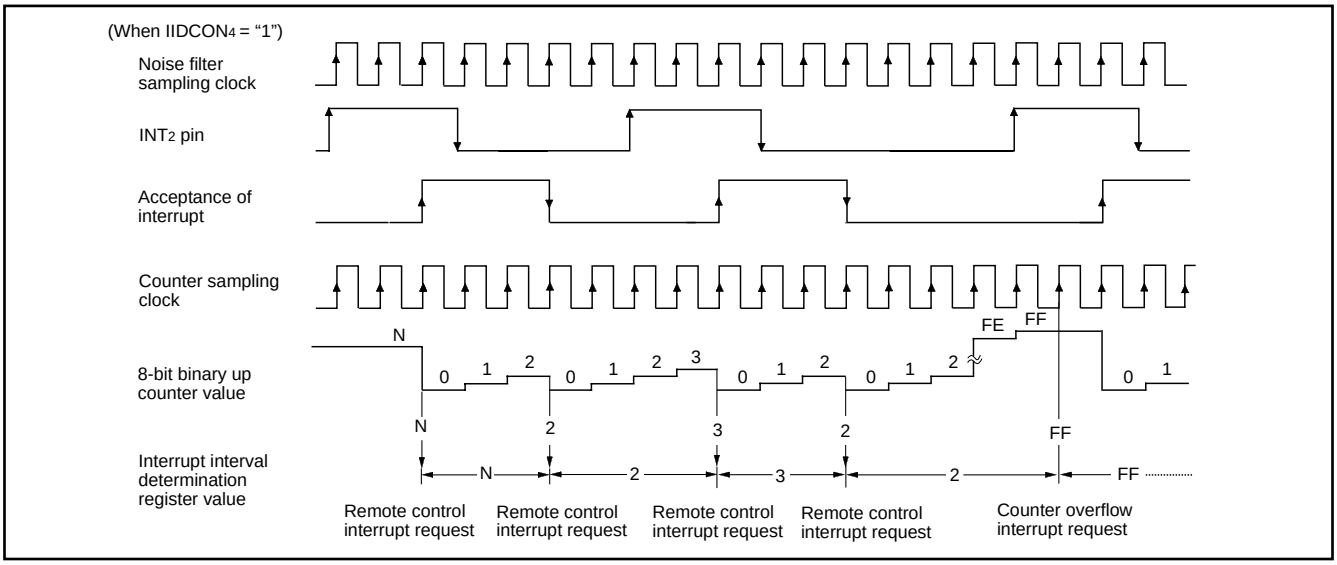


Fig. 71 Interrupt interval determination operation example (at both-sided edge active)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway). The watchdog timer consists of an 8-bit watchdog timer L and a 8-bit watchdog timer H.

Standard Operation Of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0EEE16) after reset, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register and an internal reset occurs at an underflow of the watchdog timer H.
Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow. When the watchdog timer control register is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

(1) Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0EEE16), a watchdog timer H is set to "FF16" and a watchdog timer L to "FF16".

(2) Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0EEE16) permits selecting a watchdog timer H count source. When this bit is set to "0", the underflow signal of watchdog timer L becomes the count source. The detection time is set to 131.072 ms at f(XIN) = 4 MHz frequency, and 32.768 s at f(XCIN) = 32 kHz frequency.
When this bit is set to "1", the count source becomes the signal divided by 8 for f(XIN) or divided by 16 for f(XCIN). The detection time in this case is set to 512 µs at f(XIN) = 4 MHz frequency, and 128 ms at f(XCIN) = 32 kHz frequency.
This bit is cleared to "0" after reset.

(3) Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0EEE16) permits disabling the STP instruction when the watchdog timer is in operation.
When this bit is "0", the STP instruction is enabled.
When this bit is "1", the STP instruction is disabled.
If the STP instruction is executed, an internal resetting occurs. When this bit is set to "1", it cannot be rewritten to "0" by program. This bit is cleared to "0" after reset.

■ Note

When releasing the stop mode, the watchdog timer performs its count operation even in the stop release waiting time. Be careful not to cause the watchdog timer H to underflow in the stop release waiting time, for example, by writing any data in the watchdog timer control register (address 0EEE16) before executing the STP instruction.

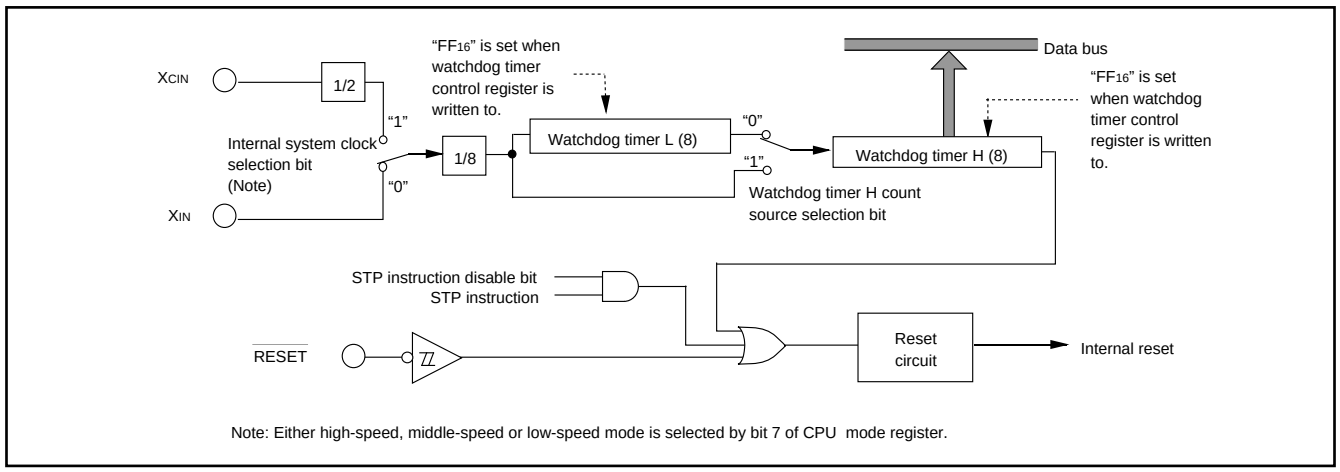


Fig. 72 Block diagram of watchdog timer

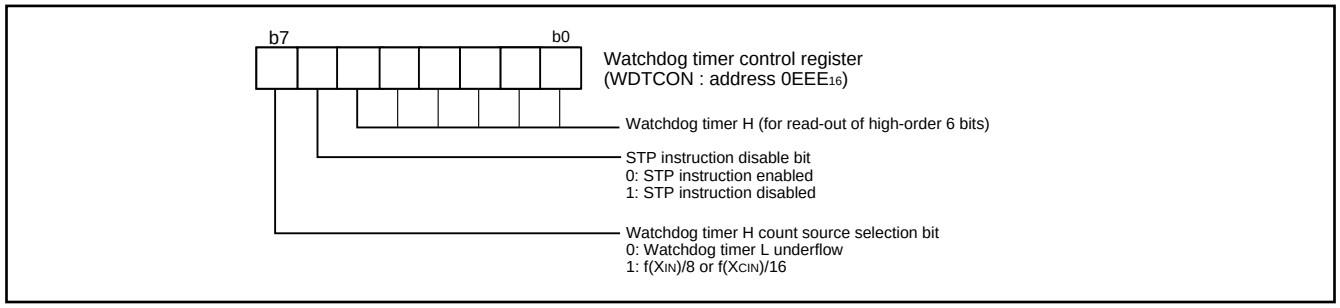


Fig. 73 Structure of watchdog timer control register

BUZZER OUTPUT CIRCUIT

The 38B7 group has a buzzer output circuit. One of 1 kHz, 2 kHz and 4 kHz (at X_{IN} = 4.19 MHz) frequencies can be selected by the buzzer output control register (address $0EFD_{16}$). Either $P7_7/BUZ01$ or $P9_7/BUZ02/AN_{15}$ can be selected as a buzzer output port by the output port selection bits (b2 and b3 of address $0EFD_{16}$).
The buzzer output is controlled by the buzzer output ON/OFF bit (b4).

Note: In the low-speed mode, a buzzer output is made OFF.

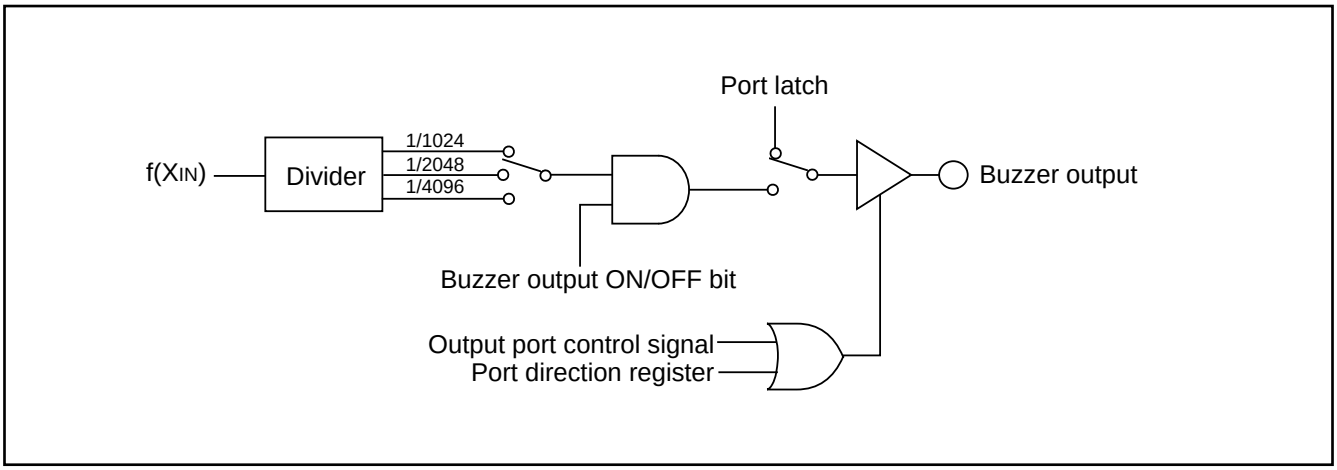


Fig. 74 Block diagram of buzzer output circuit

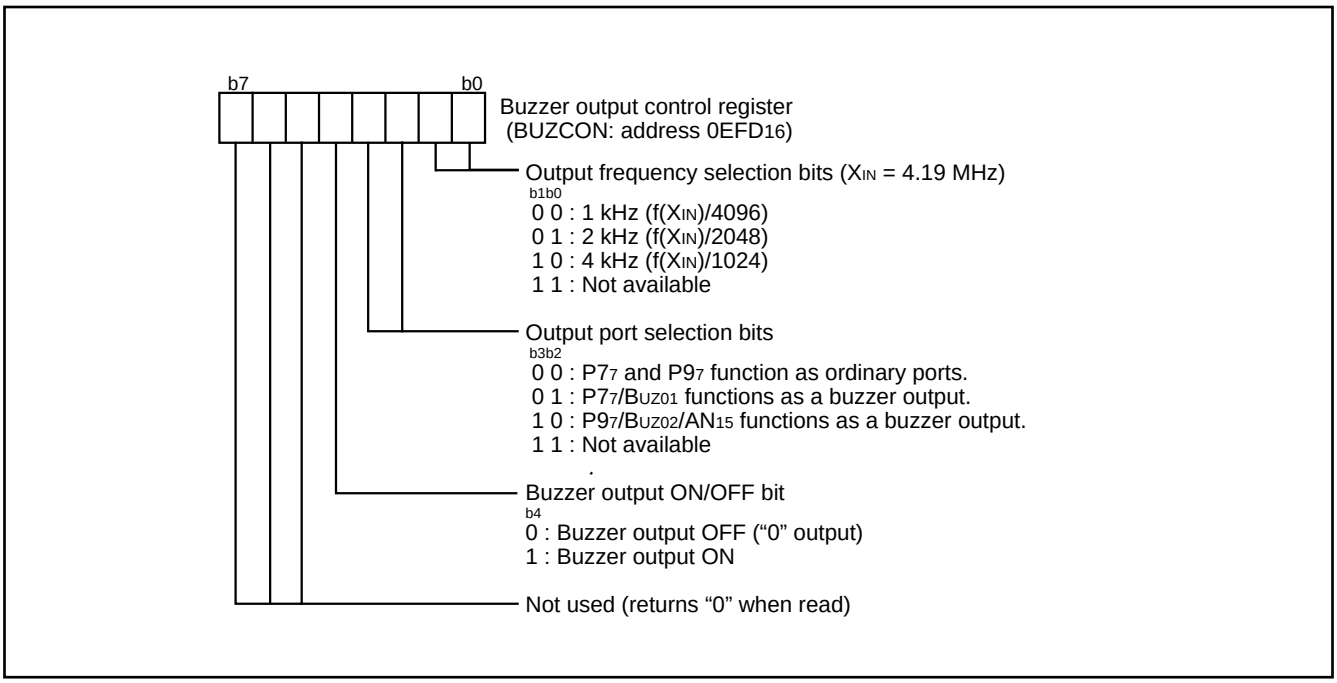


Fig. 75 Structure of buzzer output control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.7 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.54 V for Vcc of 2.7 V (switching to the high-speed mode, a power source voltage must be between 4.0 V and 5.5 V).

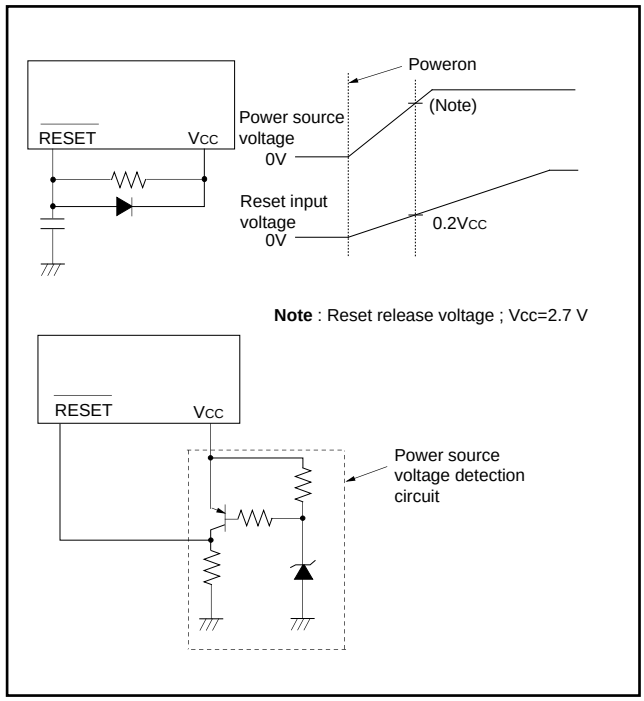


Fig. 76 Reset circuit example

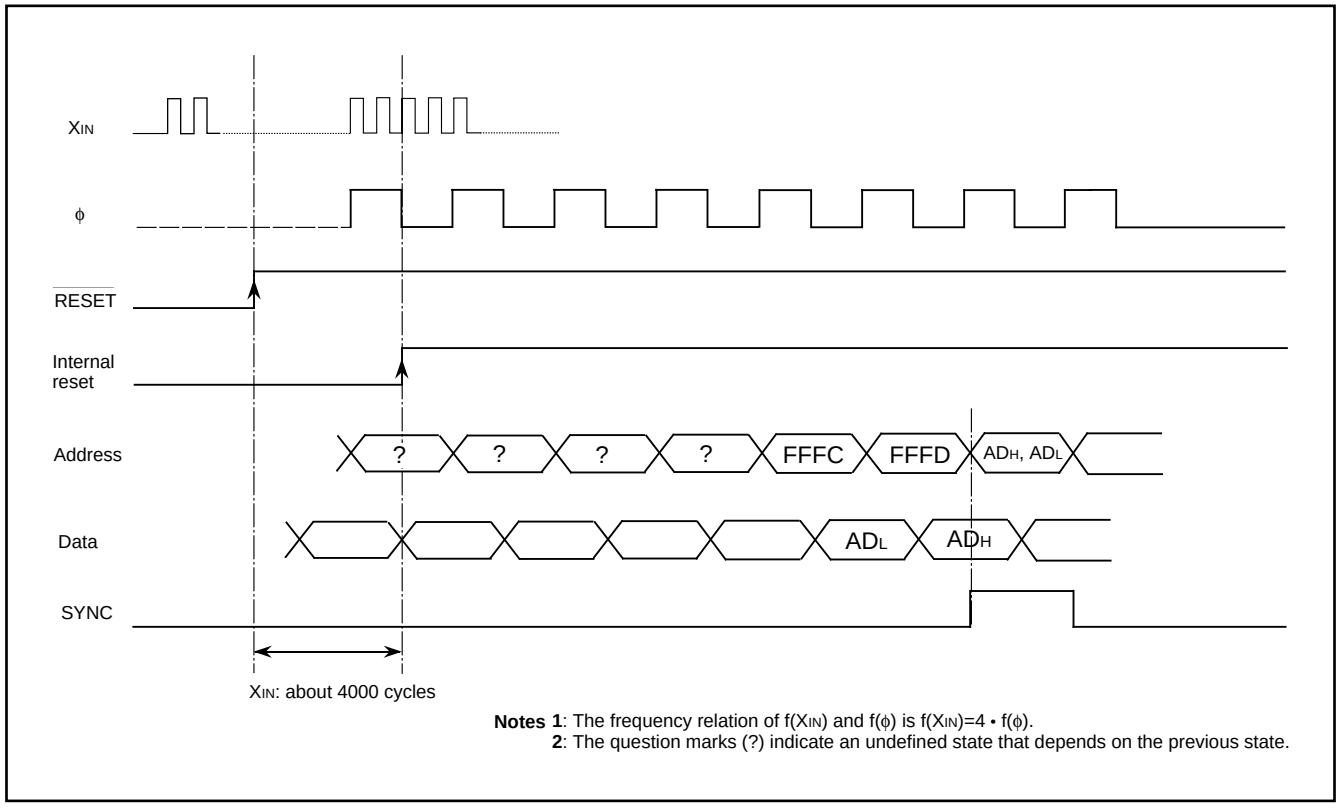


Fig. 77 Reset sequence

	Address	Register contents
(1) Port P0	0000_{16}	00_{16}
(2) Port P1	0002_{16}	00_{16}
(3) Port P1 direction register	0003_{16}	00_{16}
(4) Port P2	0004_{16}	00_{16}
(5) Port P3	0006_{16}	00_{16}
(6) Port P3 direction register	0007_{16}	00_{16}
(7) Port P4	0008_{16}	00_{16}
(8) Port P4 direction register	0009_{16}	00_{16}
(9) Port P5	$000A_{16}$	00_{16}
(10) Port P5 direction register	$000B_{16}$	00_{16}
(11) Port P6	$000C_{16}$	00_{16}
(12) Port P6 direction register	$000D_{16}$	00_{16}
(13) Port P7	$000E_{16}$	00_{16}
(14) Port P7 direction register	$000F_{16}$	00_{16}
(15) Port P8	0010_{16}	00_{16}
(16) Port P8 direction register	0011_{16}	00_{16}
(17) Port P9	0012_{16}	00_{16}
(18) Port P9 direction register	0013_{16}	00_{16}
(19) Port PA	0014_{16}	00_{16}
(20) Port PA direction register	0015_{16}	00_{16}
(21) Port PB	0016_{16}	00_{16}
(22) Port PB direction register	0017_{16}	00_{16}
(23) Serial I/O1 control register 1	0019_{16}	00_{16}
(24) Serial I/O1 control register 2	$001A_{16}$	00_{16}
(25) Serial I/O1 control register 3	$001C_{16}$	00_{16}
(26) Serial I/O2 control register	$001D_{16}$	00_{16}
(27) Serial I/O2 status register	$001E_{16}$	80_{16}
(28) Timer 1	0020_{16}	FF_{16}
(29) Timer 2	0021_{16}	01_{16}
(30) Timer 3	0022_{16}	FF_{16}
(31) Timer 4	0023_{16}	FF_{16}
(32) Timer 5	0024_{16}	FF_{16}
(33) Timer 6	0025_{16}	FF_{16}
(34) PWM control register	0026_{16}	00_{16}
(35) Timer 12 mode register	0028_{16}	00_{16}
(36) Timer 34 mode register	0029_{16}	00_{16}
(37) Timer 56 mode register	$002A_{16}$	00_{16}

	Address	Register contents
(38) D-A conversion register	$002B_{16}$	00_{16}
(39) Timer X (low-order)	$002C_{16}$	FF_{16}
(40) Timer X (high-order)	$002D_{16}$	FF_{16}
(41) Timer X mode register 1	$002E_{16}$	00_{16}
(42) Timer X mode register 2	$002F_{16}$	00_{16}
(43) Interrupt interval determination register	0030_{16}	00_{16}
(44) Interrupt interval determination control register	0031_{16}	00_{16}
(45) AD/DA control register	0032_{16}	10_{16}
(46) UART control register	0038_{16}	80_{16}
(47) Interrupt source switch register	0039_{16}	00_{16}
(48) Interrupt edge selection register	$003A_{16}$	00_{16}
(49) CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(50) Interrupt request register 1	$003C_{16}$	00_{16}
(51) Interrupt request register 2	$003D_{16}$	00_{16}
(52) Interrupt control register 1	$003E_{16}$	00_{16}
(53) Interrupt control register 2	$003F_{16}$	00_{16}
(54) Serial I/O3 control register	$0EEC_{16}$	00_{16}
(55) Watchdog timer control register	$0EEE_{16}$	$3F_{16}$
(56) Pull-up control register 3	$0EEF_{16}$	00_{16}
(57) Pull-up control register 1	$0EF0_{16}$	00_{16}
(58) Pull-up control register 2	$0EF1_{16}$	00_{16}
(59) Port P0 digit output set switch register	$0EF2_{16}$	00_{16}
(60) Port P2 digit output set switch register	$0EF3_{16}$	00_{16}
(61) FLDC mode register	$0EF4_{16}$	00_{16}
(62) Tdisp time set register	$0EF5_{16}$	00_{16}
(63) Toff1 time set register	$0EF6_{16}$	FF_{16}
(64) Toff2 time set register	$0EF7_{16}$	FF_{16}
(65) Port P4 FLD/Port switch register	$0EF9_{16}$	00_{16}
(66) Port P5 FLD/Port switch register	$0EFA_{16}$	00_{16}
(67) Port P6 FLD/Port switch register	$0EFB_{16}$	00_{16}
(68) FLD output control register	$0EFC_{16}$	00_{16}
(69) Buzzer output control register	$0EFD_{16}$	00_{16}
(70) Flash memory control register	$0EFE_{16}$	00_{16}
(71) Flash command register	$0EFF_{16}$	00_{16}
(72) Processor status register	(PS)	X X X X X 1 X X
(73) Program counter	(PC_H)	$FFFD_{16}$ contents
	(PC_L)	$FFFC_{16}$ contents

X: Not fixed

Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 78 Internal status at reset

CLOCK GENERATING CIRCUIT

The 38B7 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT or XCIN and XCOUT. Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feedback resistor exists on-chip. However, an external feedback resistor is needed between XCIN and XCOUT.

Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control

(1) Middle-speed mode

The internal system clock is the frequency of XIN divided by 4. After reset, this mode is selected.

(2) High-speed mode

The internal system clock is the frequency of XIN.

(3) Low-speed mode

The internal system clock is the frequency of XCIN divided by 2.

■ Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3 • f(XCIN).

(4) Low power consumption mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set the main clock stop bit (bit 5) of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set enough time for oscillation to stabilize.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal system clock stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN divided by 8 or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 12 mode register are cleared to "0". Set the interrupt enable bits of the timer 1 and timer 2 to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal system clock is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal system clock stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal system clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

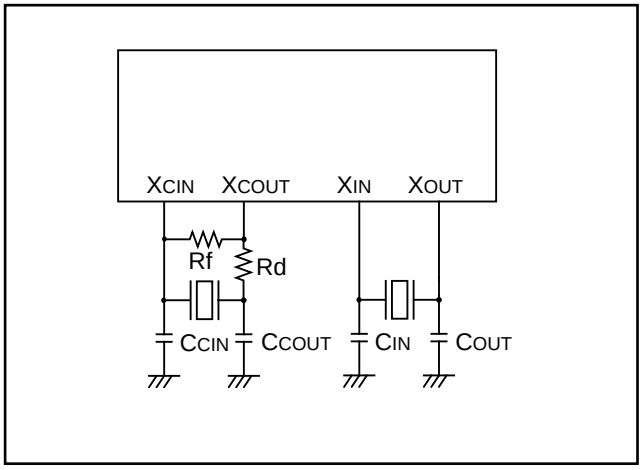


Fig. 79 Ceramic resonator circuit

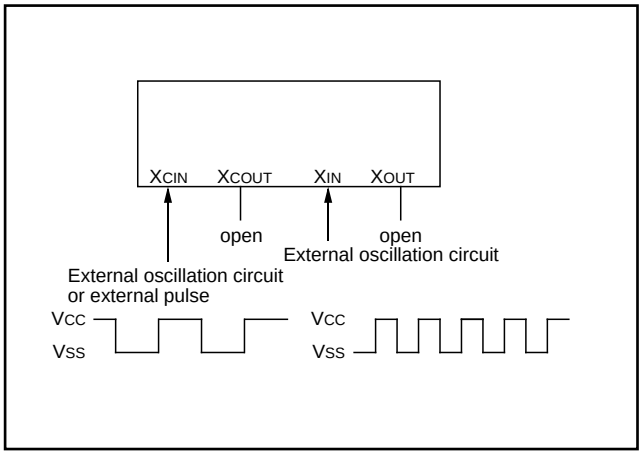
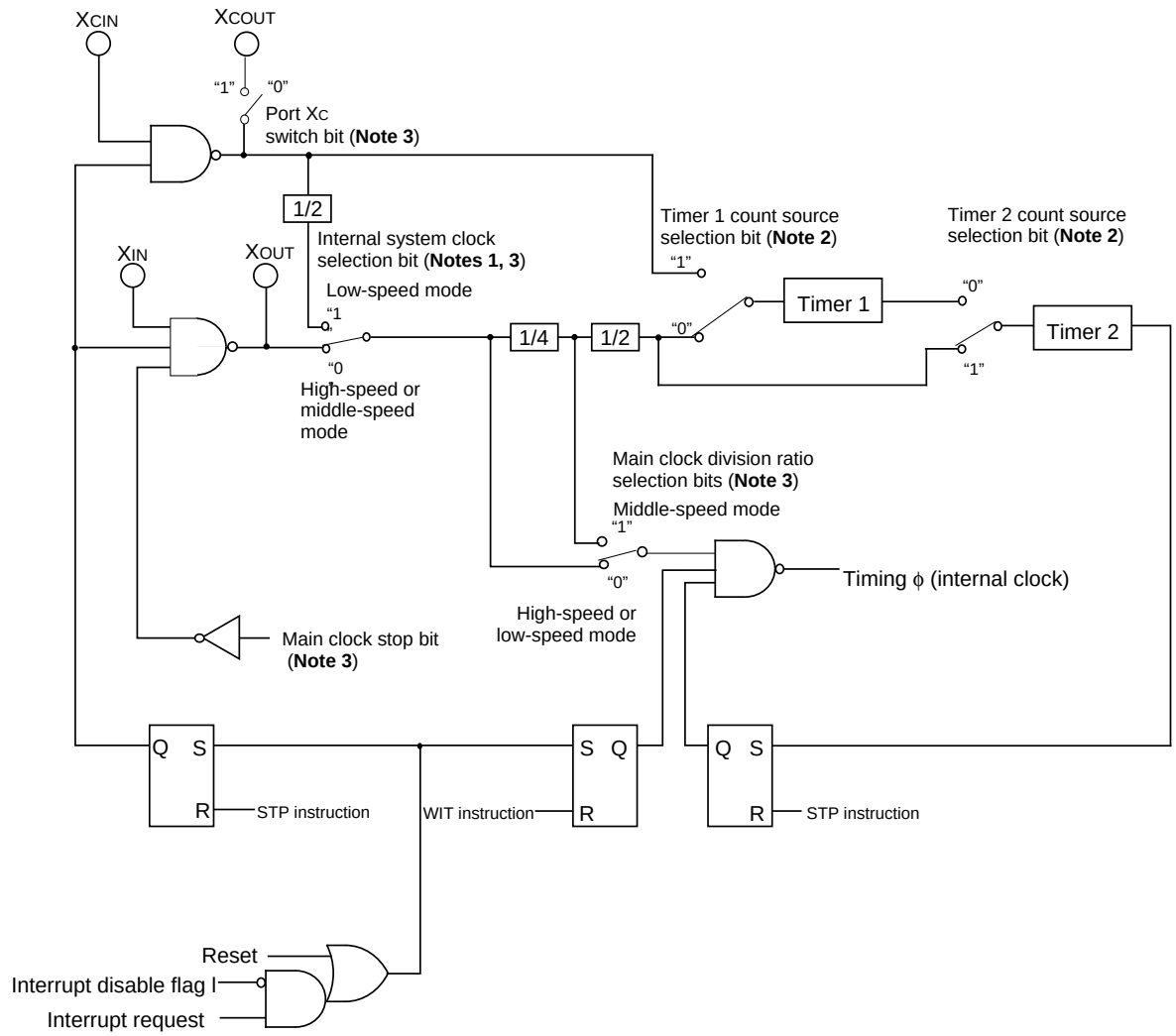
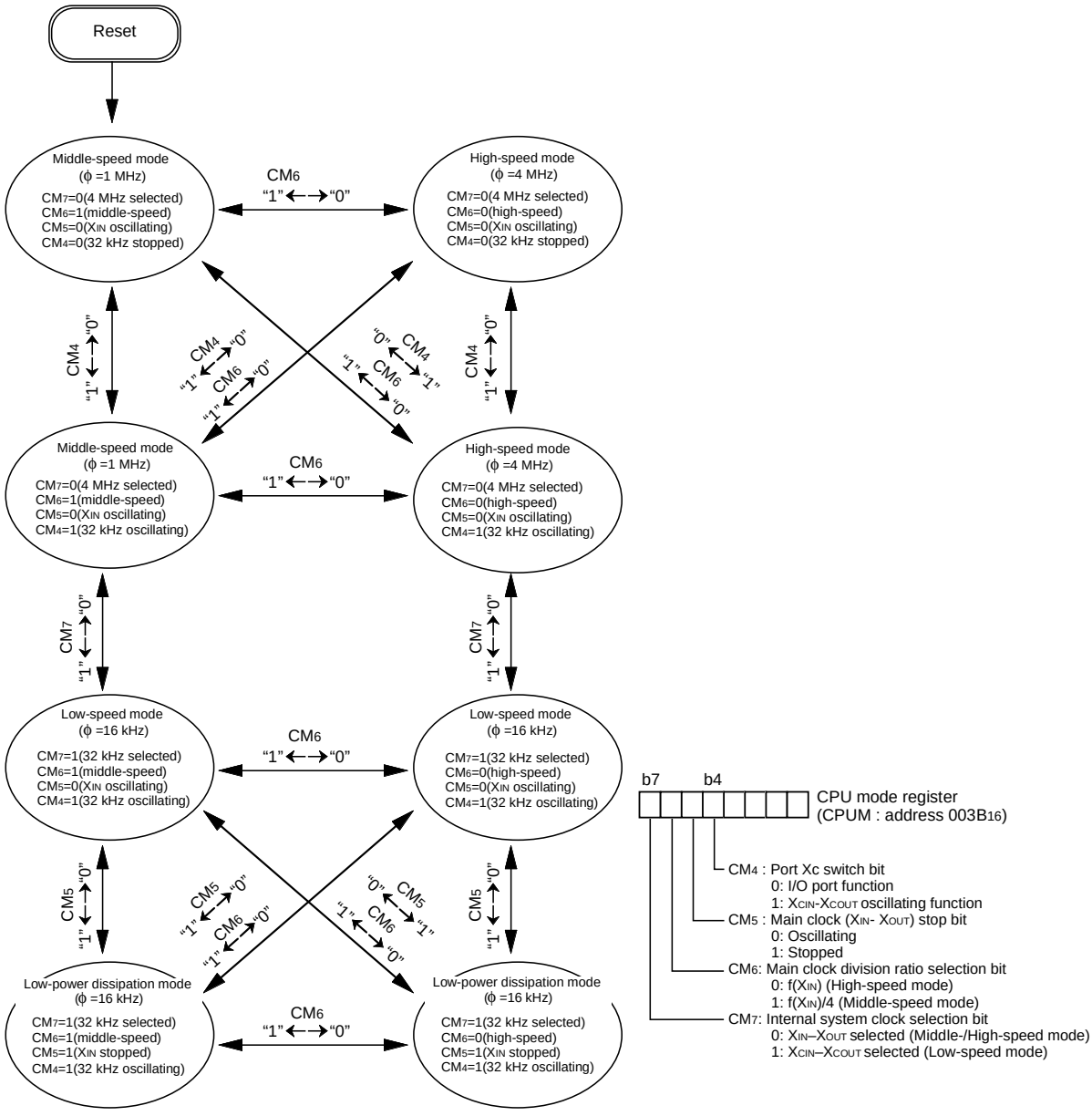


Fig. 80 External clock input circuit



Notes 1: When low-speed mode is selected, set the port Xc switch bit (b4) to "1".
2: Refer to the structure of the timer 12 mode register.
3: Refer to the structure of the CPU mode register.

Fig. 81 Clock generating circuit block diagram



Notes 1: Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2: The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3: Timer operates in the wait mode.
4: When the stop mode is ended, a delay of approximately 1 ms occurs by Timer 1 in middle-/high-speed mode.
5: When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 in low-speed mode.
6: The example assumes that 4 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal system clock.

Fig. 82 State transitions of system clock

MASK OPTION OF PULL-DOWN RESISTOR (object product: mask ROM version)

Whether built-in pull-down resistors are connected or not to high-breakdown voltage ports $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, and $P6_0$ to $P6_3$ can be specified in ordering mask ROM. The option type can be specified from among 7 types; A to G.

	$P4_0$	$P4_1$	$P4_2$	$P4_3$	$P4_4$	$P4_5$	$P4_6$	$P4_7$	$P5_0$	$P5_1$	$P5_2$	$P5_3$	$P5_4$	$P5_5$	$P5_6$	$P5_7$	$P6_0$	$P6_1$	$P6_2$	$P6_3$
A	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
D	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
E	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
F	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
G	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes 1: The electrical characteristics of high-breakdown voltage ports $P4_0$ to $P4_7$, $P5_0$ to $P5_7$, and $P6_0$ to $P6_3$'s built-in pull-down resistors are the same as that of high-breakdown voltage ports $P0_0$ to $P0_7$.

2: The absolute maximum ratings of power dissipation may be exceed owing to the number of built-in pull-down resistor. After calculating the power dissipation, specify the option type.

3: The flash memory version cannot select whether built-in pull-down resistors are connected or not. This is the same as option type A.

Power Dissipation Calculating Method

(Fixed number depending on microcomputer's standard)

- V_{OH} output fall voltage of high-breakdown port
  2 V (max.); | Current value | = at 18 mA
- Resistor value = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.)
  = 5 V × 15 mA = 75 mW

(**Fixed number depending on use condition)**

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number a; digit number b; segment number c
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: d
- All segment number during repeat cycle: e (= a × c)
- Total number of built-in resistor: for digit, f; for segment, g
- Digit pin current value h (mA)
- Segment pin current value i (mA)

(1) Digit pin power dissipation
{h × b × (1 – Toff / Tdisp) × voltage} / a

(2) Segment pin power dissipation
{i × d × (1–Toff / Tdisp) × voltage} / a

(3) Pull-down resistor power dissipation (digit)
{power dissipation per 1 digit × (b × f / b) × (1–Toff / Tdisp) } / a

(4) Pull-down resistor power dissipation (segment)
{power dissipation per 1 segment × (d × g / c) × (1–Toff / Tdisp) } / a

(5) Internal circuit power dissipation (CPU, ROM, RAM etc.)
= 190 mW

(1) + (2)+ (3) + (4) + (5) = X mW

Power Dissipation Calculating Example 1

(Fixed number depending on microcomputer's standard)

- V_{OH} output fall voltage of high-breakdown port 2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 μs = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V × 15 mA = 75 mW

(**Fixed number depending on use condition)**

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number 17; digit number 16; segment number 20
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: 31
- All segment number during repeat cycle: 340 (= 17 × 20)
- Total number of built-in resistor: for digit, 16; for segment, 20
- Digit pin current value 18 (mA)
- Segment pin current value 3 (mA)

(1) Digit pin power dissipation
{18 × 16 × (1 – 1 / 16) × 2} / 17 = 31.77 mW
(2) Segment pin power dissipation
{3 × 31 × (1– 1 / 16) × 2} / 17 = 10.26 mW
(3) Pull-down resistor power dissipation (digit)
$[\{45 - 2\}^2 / 48 \times (16 \times 16 / 16) \times (1 - 1 / 16)] / 17 = 33.94$ mW
(4) Pull-down resistor power dissipation (segment)
$[\{45 - 2\}^2 / 48 \times (31 \times 20 / 20) \times (1 - 1 / 16)] / 17 = 65.86$ mW
(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

(1) + (2)+ (3) + (4) + (5) = 217 mW

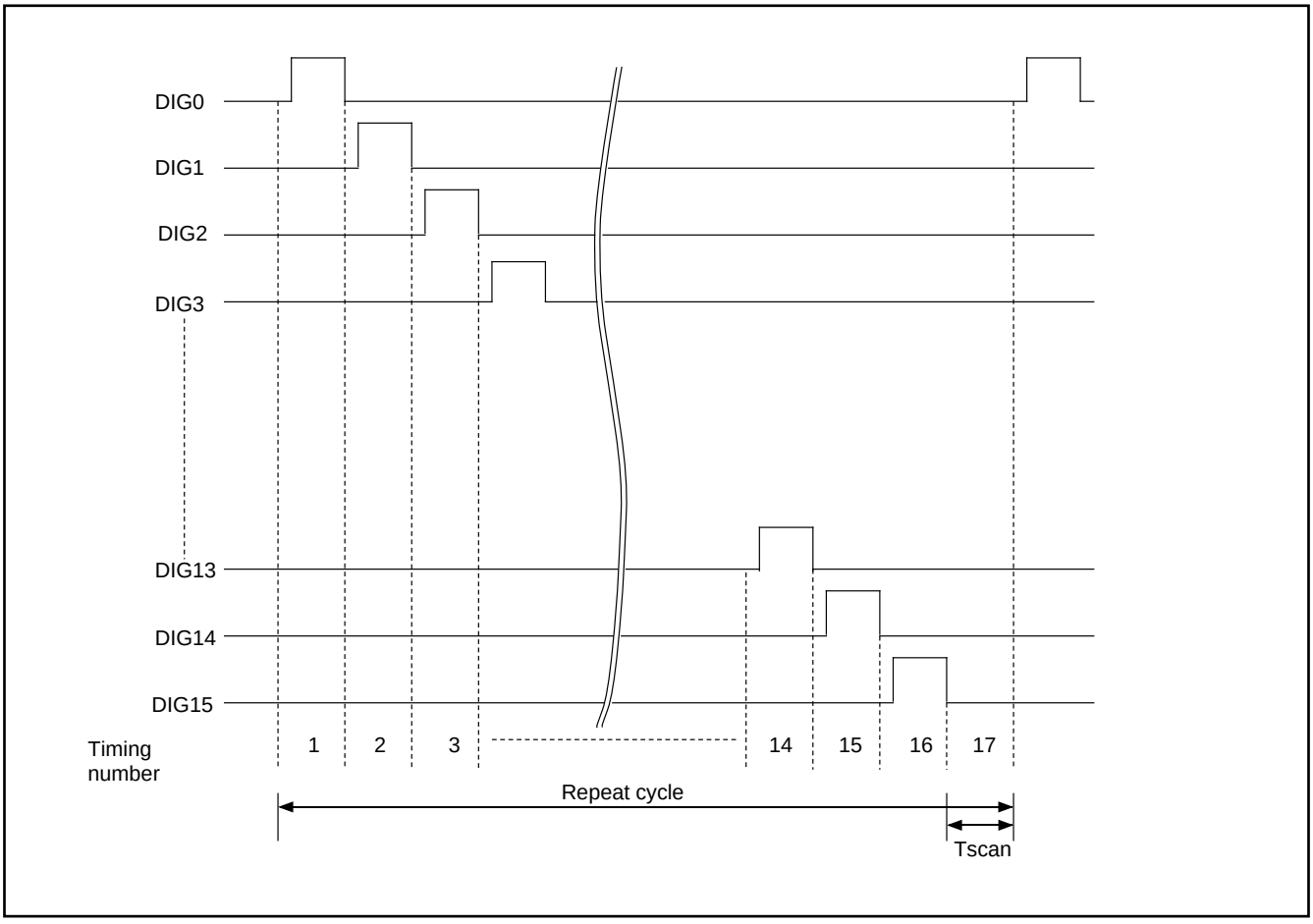


Fig. 83 Digit timing waveform (1)

Power Dissipation Calculating Example 2 (2 or more digits turned ON at the same time)

(Fixed number depending on microcomputer's standard)

- V_{OH} output fall voltage of high-breakdown port 2 V (max.); | Current value | = at 18 mA
- Resistor value 43 V / 900 μs = 48 kΩ (min.)
- Power dissipation of internal circuit (CPU, ROM, RAM etc.) = 5 V × 15 mA = 75 mW

(**Fixed number depending on use condition)**

- Apply voltage to V_{EE} pin: Vcc – 45 V
- Timing number 11; digit number 12; segment number 24
- Ratio of Toff time corresponding Tdisp time: 1/16
- Turn ON segment number during repeat cycle: 114
- All segment number during repeat cycle: 264 (= 11 × 24)
- Total number of built-in resistor: for digit, 10; for segment, 22
- Digit pin current value 18 (mA)
- Segment pin current value 3 (mA)

(1) Digit pin power dissipation
{18 × 12 × (1 – 1 / 16) × 2} / 11 = 36.82 mW
(2) Segment pin power dissipation
{3 × 114 × (1– 1 / 16) × 2} / 11 = 58.30 mW
(3) Pull-down resistor power dissipation (digit)
$[\{45 - 2\}^2 / 48 \times (12 \times 10 / 12) \times (1 - 1 / 16)] / 11 = 32.84$ mW
(4) Pull-down resistor power dissipation (segment)
$[\{45 - 2\}^2 / 48 \times (114 \times 22 / 24) \times (1 - 1 / 16)] / 11 = 343.08$ mW
(5) Internal circuit power dissipation (CPU, ROM, RAM etc.) = 75 mW

(1) + (2)+ (3) + (4) + (5) = 547 mW

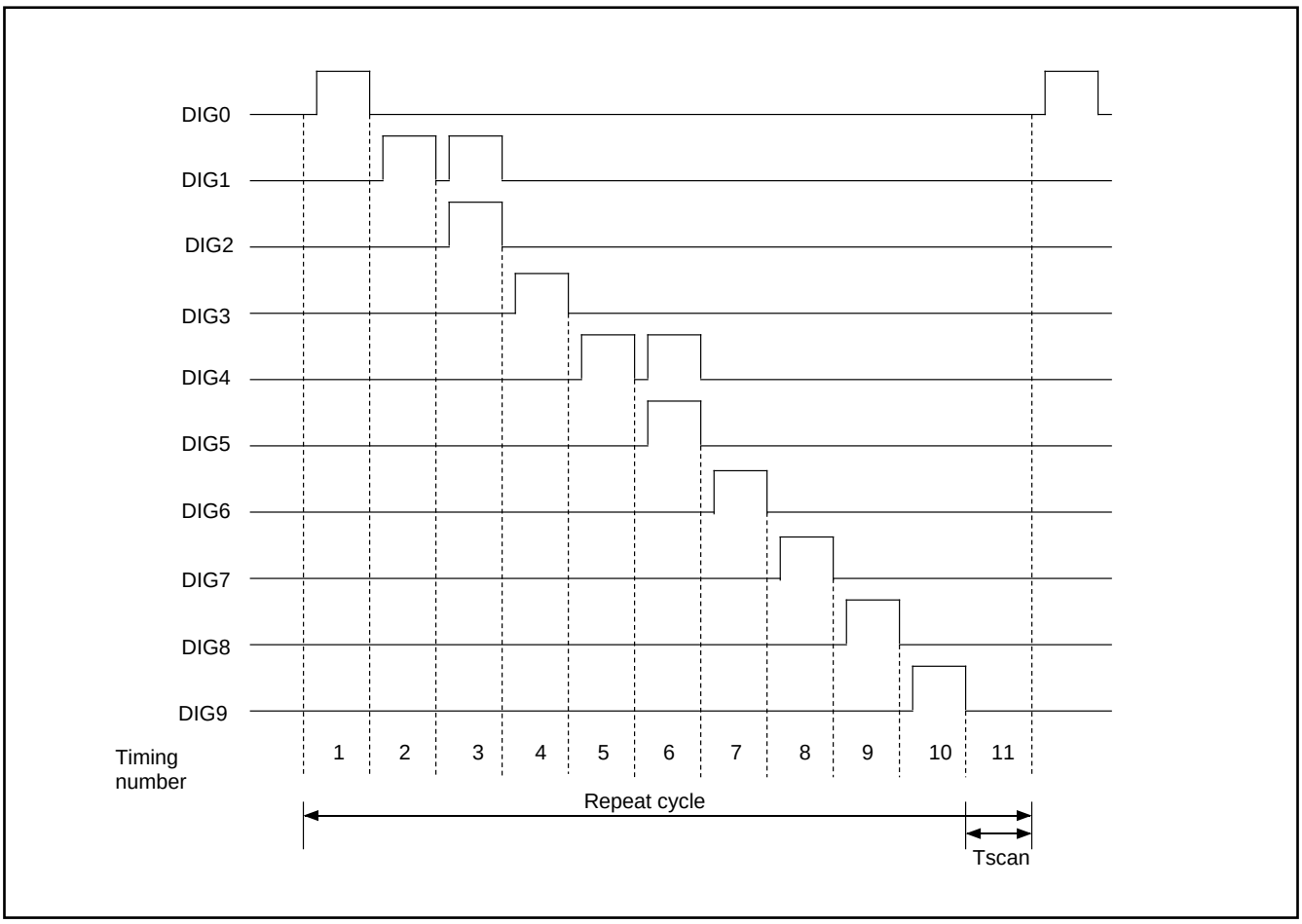


Fig. 84 Digit timing waveform (2)

FLASH MEMORY MODE

The M38B79FF has the flash memory mode in addition to the normal operation mode (microcomputer mode). The user can use this mode to perform read, program, and erase operations for the internal flash memory.

The M38B79FF has three modes the user can choose: the parallel input/output and serial input/output mode, where the flash memory is handled by using the external programmer, and the CPU reprogramming mode, where the flash memory is handled by the central processing unit (CPU). The following explains these modes.

(1) Flash memory mode 1 (parallel I/O mode)

The parallel I/O mode can be selected by connecting wires as shown in Figures 85 and supplying power to the V_{CC} and V_{PP} pins. In this mode, the M38B79FF operates as an equivalent of MITSUBISHI's CMOS flash memory M5M28F101. However, because the M38B79FF's internal memory has a capacity of 60 Kbytes, programming is available for addresses 01000_{16} to $0FFFF_{16}$, and make sure that the data in addresses 00000_{16} to $00FFF_{16}$ and addresses 10000_{16} to $1FFFF_{16}$ are FF_{16}. Note also that the M38B79FF does not contain a facility to read out a device identification code by applying a high voltage to address input (A_9). Be careful not to erratically set program conditions when using a general-purpose PROM programmer.

Table 12 shows the pin assignments when operating in the parallel input/output mode.

Table 12 Pin assignments of M38B79FF when operating in the parallel input/output mode

	M38B79FF	M5M28F101
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV$_{SS}$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, P3$_1$	A_0–A_{16}
Data I/O	Port P2	D_0–D_7
$\overline{CE}$	P3$_6$	$\overline{CE}$
$\overline{OE}$	P3$_7$	$\overline{OE}$
$\overline{WE}$	P3$_3$	$\overline{WE}$

Functional Outline (parallel input/output mode)

In the parallel input/output mode, the M38B79FF allow the user to choose an operation mode between the read-only mode and the read/write mode (software command control mode) depending on the voltage applied to the V_{PP} pin. When $V_{PP} = V_{PP}L$, the read-only mode is selected, and the user can choose one of three states (e.g., read, output disable, or standby) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. When $V_{PP} = V_{PP}H$, the read/write mode is selected, and the user can choose one of four states (e.g., read, output disable, standby, or write) depending on inputs to the $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ pins. Table 13 shows assignment states of control input and each state.

● Read

The microcomputer enters the read state by driving the $\overline{CE}$, and $\overline{OE}$ pins low and the $\overline{WE}$ pin high; and the contents of memory corresponding to the address to be input to address input pins (A_0–A_{16}) are output to the data input/output pins (D_0–D_7).

● Output disable

The microcomputer enters the output disable state by driving the $\overline{CE}$ pin low and the $\overline{WE}$ and $\overline{OE}$ pins high; and the data input/output pins enter the floating state.

● Standby

The microcomputer enters the standby state by driving the $\overline{CE}$ pin high. The M38B79FF is placed in a power-down state consuming only a minimal supply current. At this time, the data input/output pins enter the floating state.

● Write

The microcomputer enters the write state by driving the V_{PP} pin high ($V_{PP} = V_{PP}H$) and then the $\overline{WE}$ pin low when the $\overline{CE}$ pin is low and the $\overline{OE}$ pin is high. In this state, software commands can be input from the data input/output pins, and the user can choose program or erase operation depending on the contents of this software command.

Table 13 Assignment states of control input and each state

Mode \ Pin / State		$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	Data I/O
Read-only	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}L$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}L$	Floating
	Standby	V_{IH}	×	×	$V_{PP}L$	Floating
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	$V_{PP}H$	Output
	Output disable	V_{IL}	V_{IH}	V_{IH}	$V_{PP}H$	Floating
	Standby	V_{IH}	×	×	$V_{PP}H$	Floating
	Write	V_{IL}	V_{IH}	V_{IL}	$V_{PP}H$	Input

Note: × can be V_{IL} or V_{IH}.

Table 14 Pin description (flash memory parallel I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV$_{SS}$	V_{PP} input	Input	Connect to 5 V ± 10 % in read-only mode, connect to 11.7 V to 12.6 V in read/write mode.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV$_{SS}$	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
P0$_0$–P0$_7$	Address input (A$_0$–A$_7$)	Input	Port P0 functions as 8-bit address input (A$_0$–A$_7$).
P1$_0$–P1$_7$	Address input (A$_8$–A$_{15}$)	Input	Port P1 functions as 8-bit address input (A$_8$–A$_{15}$).
P2$_0$–P2$_7$	Data I/O (D$_0$–D$_7$)	I/O	Function as 8-bit data's I/O pins (D$_0$–D$_7$). Connect them to Vss through each resistor of 6.8 kΩ.
P3$_0$–P3$_7$	Control signal input	Input	P3$_7$, P3$_6$ and P3$_3$ function as the $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ input pins respectively. P3$_1$ functions as the A$_{16}$ input pin. Connect P3$_0$ and P3$_2$ to V_{SS}. Input "H" or "L" to P3$_4$, P3$_5$, or keep them open.
P4$_0$–P4$_7$	Input port P4	Input	Input "H" or "L", or keep them open.
P5$_0$–P5$_7$	Input port P5	Input	Input "H" or "L", or keep them open.
P6$_0$–P6$_7$	Input port P6	Input	Connect P6$_4$ and P6$_6$ to V_{SS}. Input "H" or "L" to P6$_0$–P6$_3$, P6$_5$, P6$_7$, or keep them open.
P7$_0$–P7$_7$	Input port P7	Input	Input "H" or "L", or keep them open.
P8$_0$–P8$_3$	Input port P8	Input	Input "H" or "L", or keep them open.
P9$_0$–P9$_7$	Input port P9	Input	Input "H" or "L", or keep them open.
PA$_0$–PA$_7$	Input port PA	Input	Input "H" or "L", or keep them open.
PB$_0$–PB$_6$	Input port PB	Input	Input "H" or "L", or keep them open.
V_{EE}	Pull-down power supply		Keep this open.

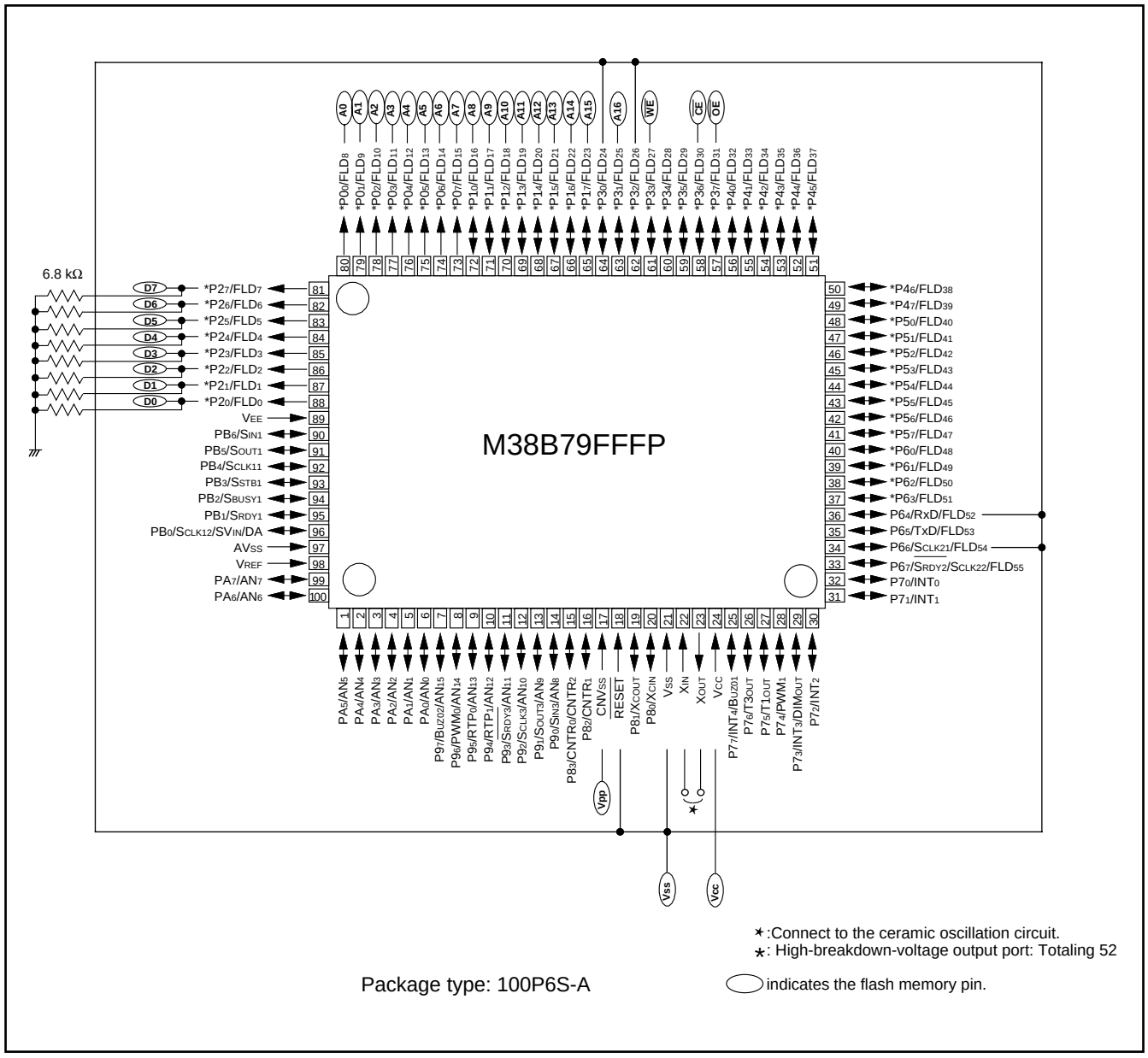


Fig. 85 Pin connection of M38B79FF when operating in parallel input/output mode

Read-only Mode

The microcomputer enters the read-only mode by applying $V_{PP}L$ to the V_{PP} pin. In this mode, the user can input the address of a memory location to be read and the control signals at the timing shown in Figure 86, and the M38B79FF will output the contents of the user's specified address from data I/O pin to the external. In this mode, the user cannot perform any operation other than read.

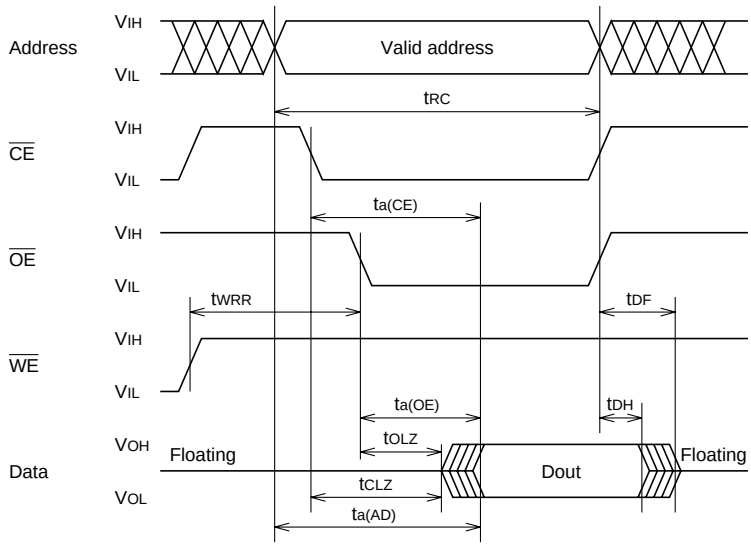


Fig. 86 Read timing

Read/Write Mode

The microcomputer enters the read/write mode by applying $V_{PP}H$ to the V_{PP} pin. In this mode, the user must first input a software command to choose the operation (e. g., read, program, or erase) to be performed on the flash memory (this is called the first cycle), and then input the information necessary for execution of the command (e.g, address and data) and control signals (this is called the second cycle). When this is done, the M38B79FF executes the specified operation.

Table 15 shows the software commands and the input/output information in the first and the second cycles. The input address is latched internally at the falling edge of the $\overline{WE}$ input; software commands and other input data are latched internally at the rising edge of the $\overline{WE}$ input.

The following explains each software command. Refer to Figures 87 to 89 for details about the signal input/output timings.

Table 15 Software command (parallel input/output mode)

Symbol	First cycle		Second cycle	
	Address input	Data input	Address input	Data I/O
Read	×	00_{16}	Read address	Read data (Output)
Program	×	40_{16}	Program address	Program data (Input)
Program verify	×	$C0_{16}$	×	Verify data (Output)
Erase	×	20_{16}	×	20_{16} (Input)
Erase verify	Verify address	$A0_{16}$	×	Verify data (Output)
Reset	×	FF_{16}	×	FF_{16} (Input)
Device identification	×	90_{16}	ADI	DDI (Output)

Note: ADI = Device identification address : manufacturer's code 00000_{16}, device code 0000_{16}
DDI = Device identification data : manufacturer's code $1C_{16}$, device code $D0_{16}$
× can be V_{IL} or V_{IH}.

● **Read command**

The microcomputer enters the read mode by inputting command code "00_{16}" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address of a memory location to be read is input in the second cycle, with control signals input at the timing shown in Figure 87, the M38B79FF outputs the contents of the specified address from the data I/O pins to the external.

The read mode is retained until any other command is latched into the command latch. Consequently, once the M38B79FF enters the read mode, the user can read out the successive memory contents simply by changing the input address and executing the second cycle only. Any command other than the read command must be input beginning from its command code over again each time the user execute it. The contents of the command latch immediately after power-on is 00_{16}.

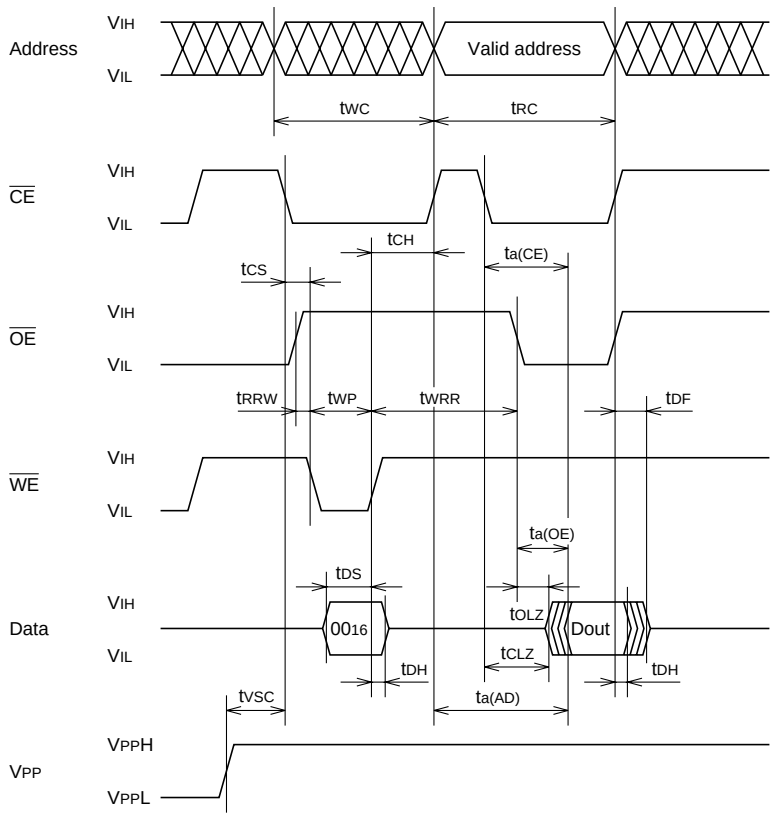


Fig. 87 Timings during reading

● **Program command**

The microcomputer enters the program mode by inputting command code "40$_{16}$" in the first cycle. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When the address which indicates a program location and data is input in the second cycle, the M38B79FF internally latches the address at the falling edge of the $\overline{WE}$ input and the data at the rising edge of the $\overline{WE}$ input. The M38B79FF starts programming at the rising edge of the $\overline{WE}$ input in the second cycle and finishes programming within 10 µs as measured by its internal timer. Programming is performed in units of bytes.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 90 for the programming flowchart.

● **Program verify command**

The microcomputer enters the program verify mode by inputting command code "C0$_{16}$" in the first cycle. This command is used to verify the programmed data after executing the program command. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 88, the M38B79FF outputs the programmed address's contents to the external. Since the address is internally latched when the program command is executed, there is no need to input it in the second cycle.

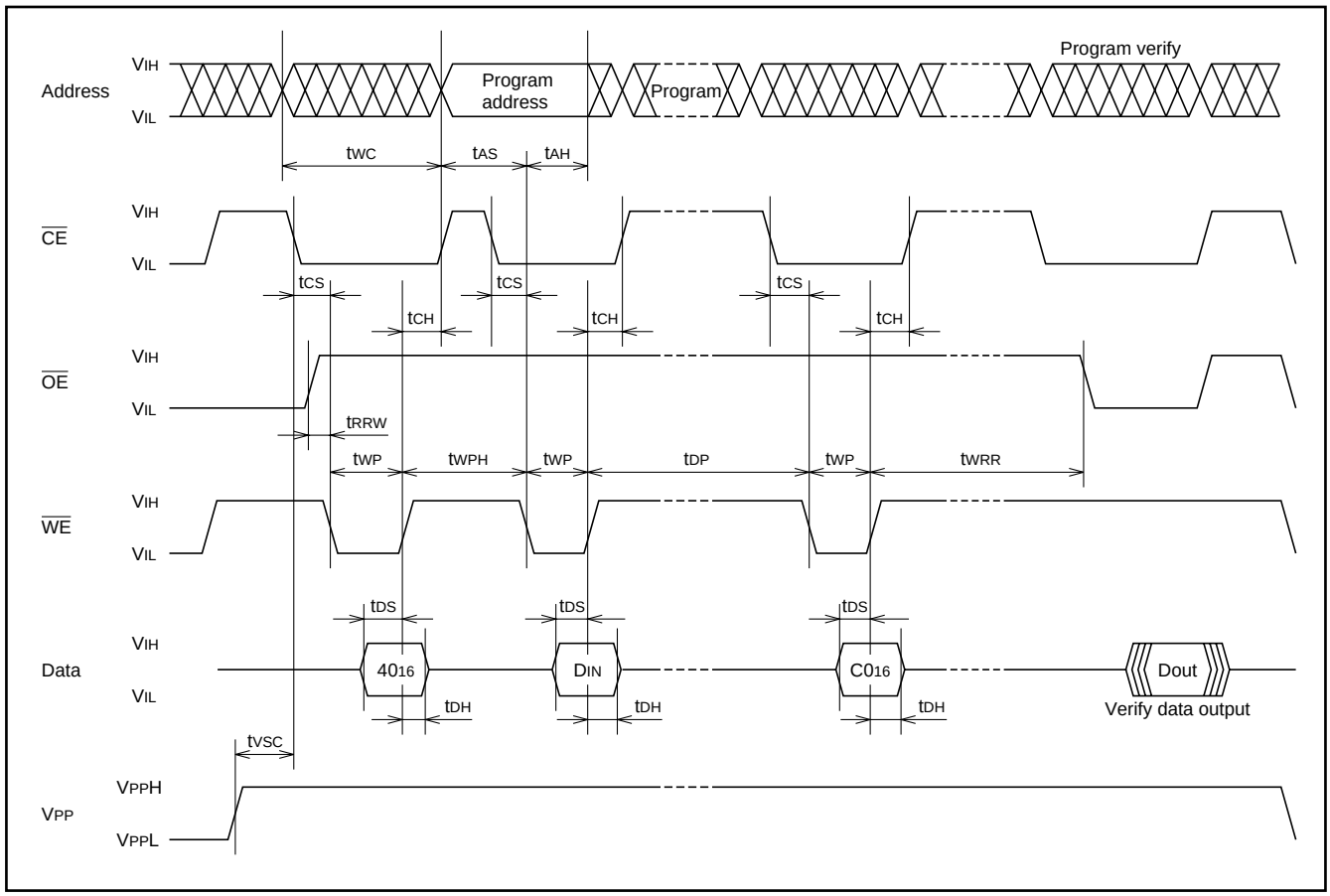


Fig. 88 Input/output timings during programming (Verify data is output at the same timing as for read.)

● **Erase command**

The erase command is executed by inputting command code 20_{16} in the first cycle and command code 20_{16} again in the second cycle. The command code is latched into the internal command latch at the rising edges of the $\overline{WE}$ input in the first cycle and in the second cycle, respectively. The erase operation is initiated at the rising edge of the $\overline{WE}$ input in the second cycle, and the memory contents are collectively erased within 9.5 ms as measured by the internal timer. Note that data 00_{16} must be written to all memory locations before executing the erase command.

Note: An erase operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 90 for the erase flowchart.

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. The microcomputer enters the erase verify mode by inputting the verify address and command code $A0_{16}$ in the first cycle. The address is internally latched at the falling edge of the $\overline{WE}$ input, and the command code is internally latched at the rising edge of the $\overline{WE}$ input. When control signals are input in the second cycle at the timing shown in Figure 89, the M38B79FF outputs the contents of the specified address to the external.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00_{16} to memory locations before erasing.

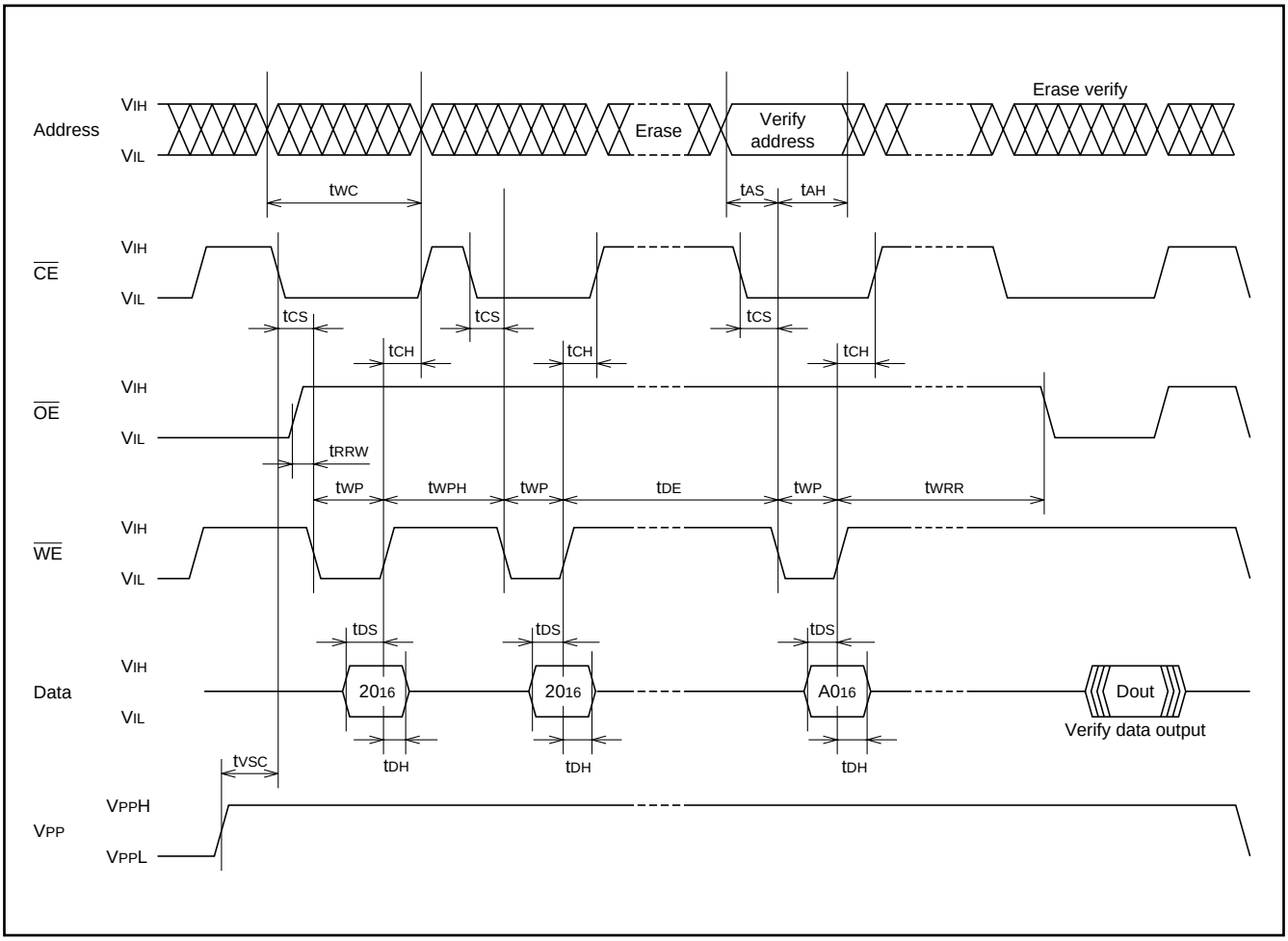


Fig. 89 Input/output timings during erasing (verify data is output at the same timing as for read.)

● **Reset command**

The reset command provides a means of stopping execution of the erase or program command safely. If the user inputs command code FF_{16} in the second cycle after inputting the erase or program command in the first cycle and again input command code FF_{16} in the third cycle, the erase or program command is disabled (i.e., reset), and the M38B79FF is placed in the read mode. If the reset command is executed, the contents of the memory does not change.

● **Device identification code command**

By inputting command code 90_{16} in the first cycle, the user can read out the device identification code. The command code is latched into the internal command latch at the rising edge of the $\overline{WE}$ input. At this time, the user can read out manufacture's code $1C_{16}$ (i.e., MITSUBISHI) by inputting 0000_{16} to the address input pins in the second cycle; the user can read out device code $D0_{16}$ (i. e., 1M-bit flash memory) by inputting 0001_{16}.

These command and data codes are input/output at the same timing as for read.

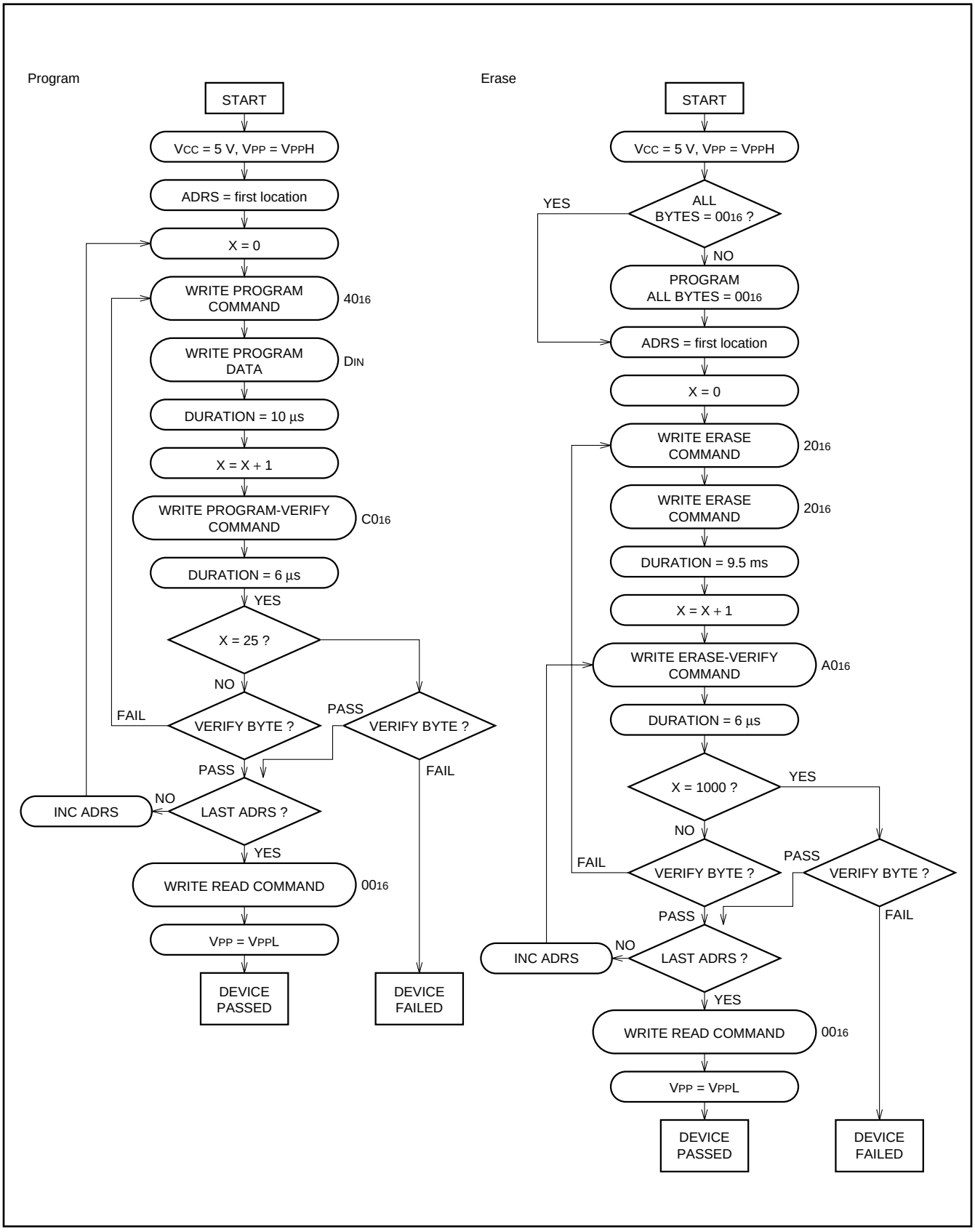


Fig. 90 Programming/Erasing algorithm flow chart

Table 16 DC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{SB1}	V_{CC} supply current (at standby)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IH}			1	mA
I_{SB2}		V_{CC} = 5.5 V, $\overline{CE}$ = V_{CC} ± 0.2 V			100	µA
I_{CC1}	V_{CC} supply current (at read)	V_{CC} = 5.5 V, $\overline{CE}$ = V_{IL}, t_{RC} = 150 ns, I_{OUT} = 0 mA			15	mA
I_{CC2}	V_{CC} supply current (at program)	V_{PP} = V_{PPH}			15	mA
I_{CC3}	V_{CC} supply current (at erase)	V_{PP} = V_{PPH}			15	mA
I_{PP1}	V_{PP} supply current (at read)	0≤V_{PP}≤V_{CC}			10	µA
		V_{CC}<V_{PP}≤V_{CC} + 1.0 V			100	µA
		V_{PP} = V_{PPH}			100	µA
I_{PP2}	V_{PP} supply current (at program)	V_{PP} = V_{PPH}			30	mA
I_{PP3}	V_{PP} supply current (at erase)	V_{PP} = V_{PPH}			30	mA
V_{IL}	"L" input voltage		0		0.2Vcc	V
V_{IH}	"H" input voltage		0.52Vcc		V_{CC}	V
V_{OH1}	"H" output voltage	I_{OH} = –400 µA	2.4			V
V_{OH2}		I_{OH} = –100 µA	V_{CC} –0.4			V
V_{PPL}	V_{PP} supply voltage (read only)		V_{CC}		V_{CC} + 1.0	V
V_{PPH}	V_{PP} supply voltage (read/write)		11.7	12.0	12.6	V

AC ELECTRICAL CHARACTERISTICS (T_a = 25 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Table 17 Read-only mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{RC}	Read cycle time	500		ns
$t_{a(AD)}$	Address access time		500	ns
$t_{a(CE)}$	$\overline{CE}$ access time		500	ns
$t_{a(OE)}$	$\overline{OE}$ access time		200	ns
t_{CLZ}	Output enable time (after $\overline{CE}$)	0		ns
t_{OLZ}	Output enable time (after $\overline{OE}$)	0		ns
t_{DF}	Output floating time (after $\overline{OE}$)		70	ns
t_{DH}	Output valid time (after $\overline{CE}$, $\overline{OE}$, address)	0		ns
t_{WRR}	Write recovery time (before read)	6		µs

Table 18 Read/Write mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{WC}	Write cycle time	300		ns
t_{AS}	Address set up time	0		ns
t_{AH}	Address hold time	120		ns
t_{DS}	Data setup time	100		ns
t_{DH}	Data hold time	20		ns
t_{WRR}	Write recovery time (before read)	6		µs
t_{RRW}	Read recovery time (before write)	0		µs
t_{CS}	$\overline{CE}$ setup time	40		ns
t_{CH}	$\overline{CE}$ hold time	0		ns
t_{WP}	Write pulse width	120		ns
t_{WPH}	Write pulse waiting time	40		ns
t_{DP}	Program time	10		µs
t_{DE}	Erase time	9.5		ms
t_{VSC}	V_{PP} setup time	1		µs

Note: Read timing of Read/Write mode is same as Read-only mode.

(2) Flash memory mode 2 (serial I/O mode)

The M38B79FF has a function to serially input/output the software commands, addresses, and data required for operation on the internal flash memory (e. g., read, program, and erase) using only a few pins. This is called the serial I/O (input/output) mode. This mode can be selected by driving the SDA (serial data input/output), SCLK (serial clock input), and $\overline{OE}$ pins high after connecting wires as shown in Figures 91 and powering on the V_{CC} pin and then applying $V_{PP}H$ to the V_{PP} pin.

In the serial I/O mode, the user can use six types of software commands: read, program, program verify, erase, erase verify and error check.

Serial input/output is accomplished synchronously with the clock, beginning from the LSB (LSB first).

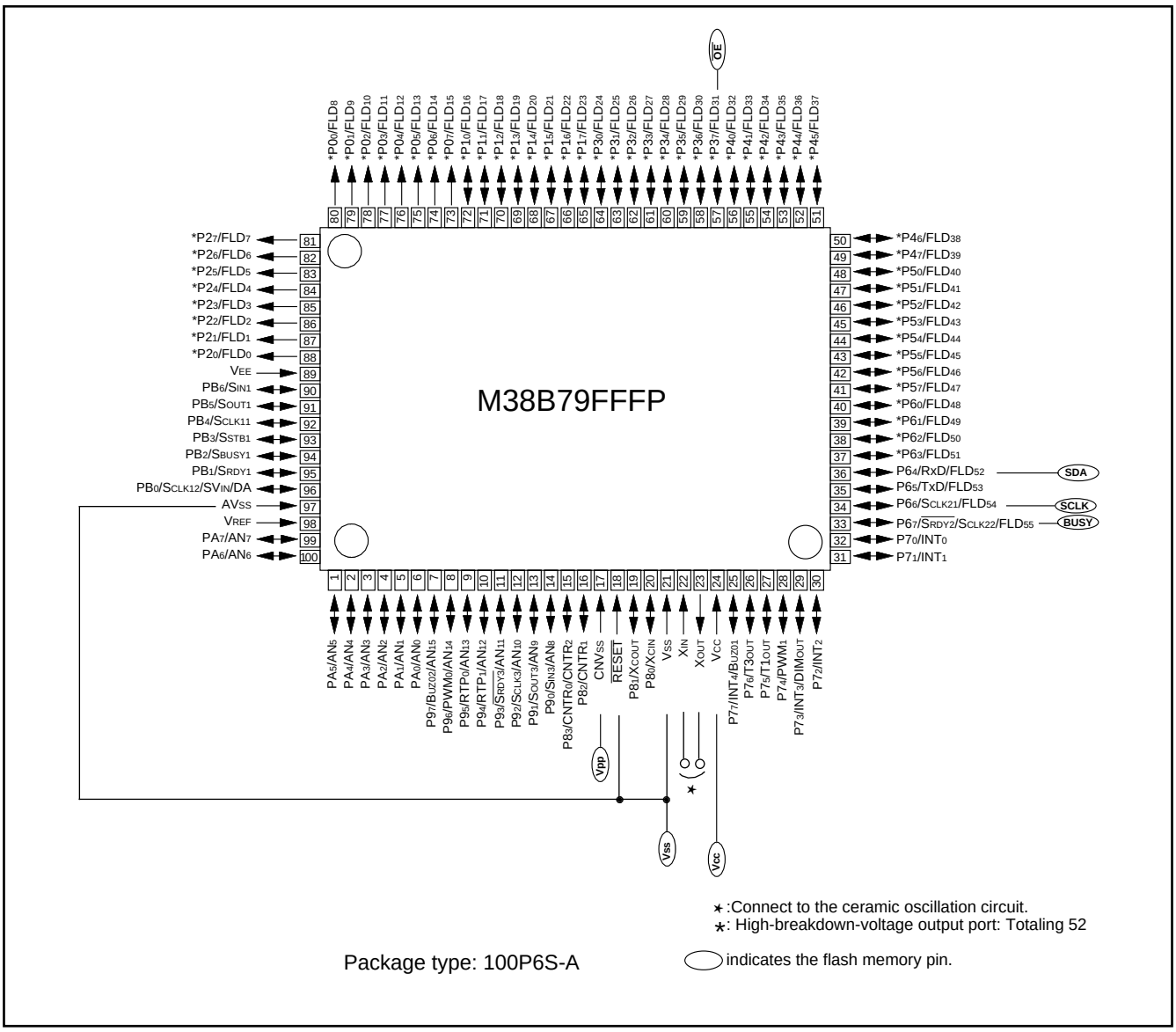


Fig. 91 Pin connection of M38B79FF when operating in serial I/O mode

Table 19 Pin description (flash memory serial I/O mode)

Pin	Name	Input /Output	Functions
V_{CC}, V_{SS}	Power supply	—	Supply 5 V ± 10 % to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to 11.7 V to 12.6 V.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
AV_{SS}	Analog supply input	—	Connect to V_{SS}.
V_{REF}	Reference voltage input	Input	Input an arbitrary level between the range of V_{SS} and V_{CC}.
$P0_0$–$P0_7$	Input port P0	Input	Input “H” or “L”, or keep them open.
$P1_0$–$P1_7$	Input port P1	Input	Input “H” or “L”, or keep them open.
$P2_0$–$P2_7$	Input port P2	Input	Input “H” or “L”, or keep them open.
$P3_0$–$P3_6$	Input port P3	Input	Input “H” or “L”, or keep them open.
$P3_7$	Control signal input	Input	$\overline{OE}$ input pin
$P4_0$–$P4_7$	Input port P4	Input	Input “H” or “L” , or keep them open.
$P5_0$–$P5_7$	Input port P5	Input	Input “H” or “L”, or keep them open.
$P6_0$–$P6_3$, $P6_5$	Input port P6	Input	Input “H” or “L” to $P6_0$–$P6_3$, $P6_5$, or keep them open.
$P6_4$	SDA I/O	I/O	This pin is for serial data I/O.
$P6_6$	SCLK input	Input	This pin is for serial clock input.
$P6_7$	BUSY output	Output	This pin is for BUSY signal output.
$P7_0$–$P7_7$	Input port P7	Input	Input “H” or “L”, or keep them open.
$P8_0$–$P8_3$	Input port P8	Input	Input “H” or “L”, or keep them open.
$P9_0$–$P9_7$	Input port P9	Input	Input “H” or “L”, or keep them open.
PA_0–PA_7	Input port PA	Input	Input “H” or “L”, or keep them open.
PB_0–PB_6	Input port PB	Input	Input “H” or “L”, or keep them open.
V_{EE}	Pull-down power supply		Keep this open.

Functional Outline (serial I/O mode)

In the serial I/O mode, data is transferred synchronously with the clock using serial input/output. The input data is read from the SDA pin into the internal circuit synchronously with the rising edge of the serial clock pulse; the output data is output from the SDA pin synchronously with the falling edge of the serial clock pulse.

Data is transferred in units of eight bits.

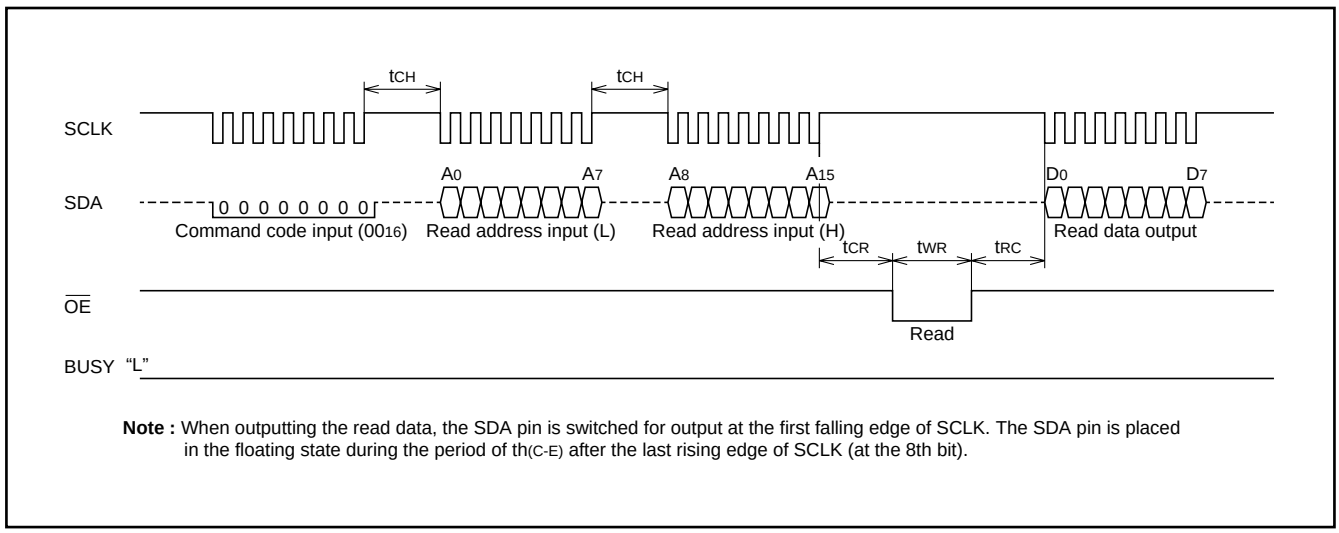
In the first transfer, the user inputs the command code. This is followed by address input and data input/output according to the contents of the command. Table 20 shows the software commands used in the serial I/O mode. The following explains each software command.

Table 20 Software command (serial I/O mode)

Number of transfers / Command	First command code input	Second	Third	Fourth
Read	00_{16}	Read address L (Input)	Read address H (Input)	Read data (Output)
Program	40_{16}	Program address L (Input)	Program address H (Input)	Program data (Input)
Program verify	$C0_{16}$	Verify data (Output)	————	————
Erase	20_{16}	20_{16} (Input)	————	————
Erase verify	$A0_{16}$	Verify address L (Input)	Verify address H (Input)	Verify data (Output)
Error check	80_{16}	Error code (Output)	————	————

● Read command

Input command code 00_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the M38B79FF reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the read data that has been latched into the data latch is serially output from the SDA pin.



Note : When outputting the read data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $th_{(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 92 Timings during reading

● **Program command**

Input command code 40_{16} in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and then program data. Programming is initiated at the last rising edge of the serial clock during program data transfer. The BUSY pin is driven high during program operation. Programming is completed within 10 μs as measured by the internal timer, and the BUSY pin is pulled low.

Note : A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in the verification, the user must repeatedly execute the program command until the pass in the verification. Refer to Figure 90 for the programming flowchart.

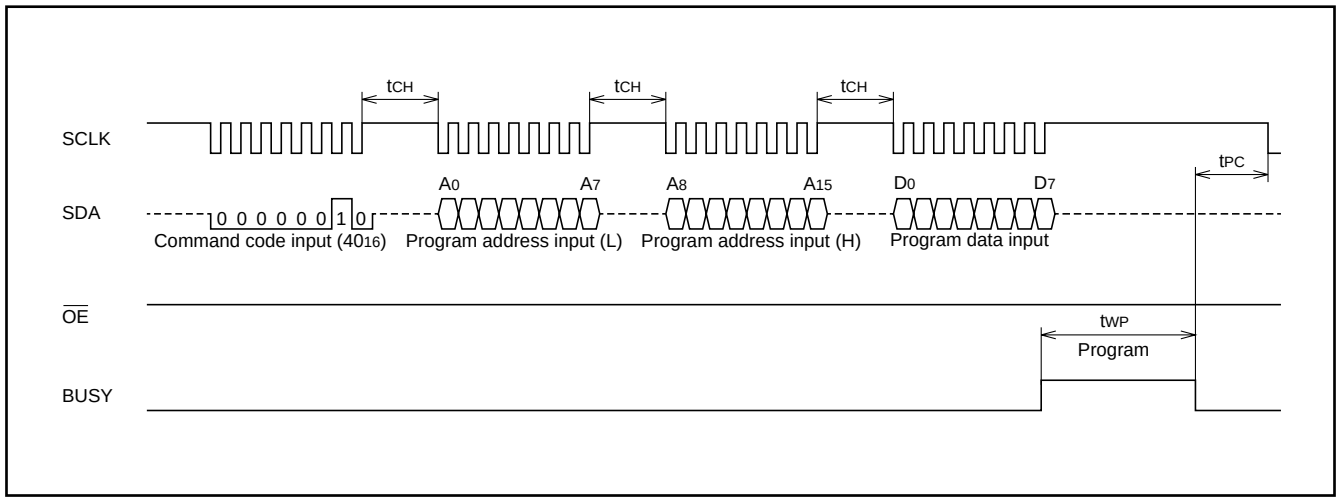
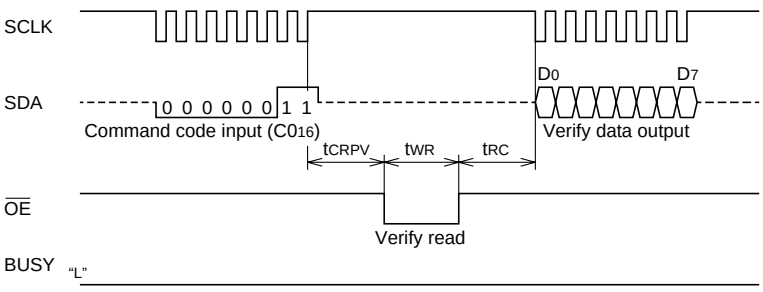


Fig. 93 Timings during programming

● **Program verify command**

Input command code $C0_{16}$ in the first transfer. Proceed and drive the $\overline{OE}$ pin low. When this is done, The M38B79FF verify-reads the programmed address's contents, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.



Note: When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $th_{(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 94 Timings during program verify

● **Erase command**

Input command code 20_{16} in the first transfer and command code 20_{16} again in the second transfer. When this is done, the M38B79FF executes an erase command. Erase is initiated at the last rising edge of the serial clock. The BUSY pin is driven high during the erase operation. Erase is completed within 9.5 ms as measured by the internal timer, and the BUSY pin is pulled low. Note that data 00_{16} must be written to all memory locations before executing the erase command.

Note: A erase operation is not completed by executing the erase command once. Always be sure to execute a erase verify command after executing the erase command. When the failure is found in the verification, the user must repeatedly execute the erase command until the pass in the verification. Refer to Figure 90 for the erase flowchart.

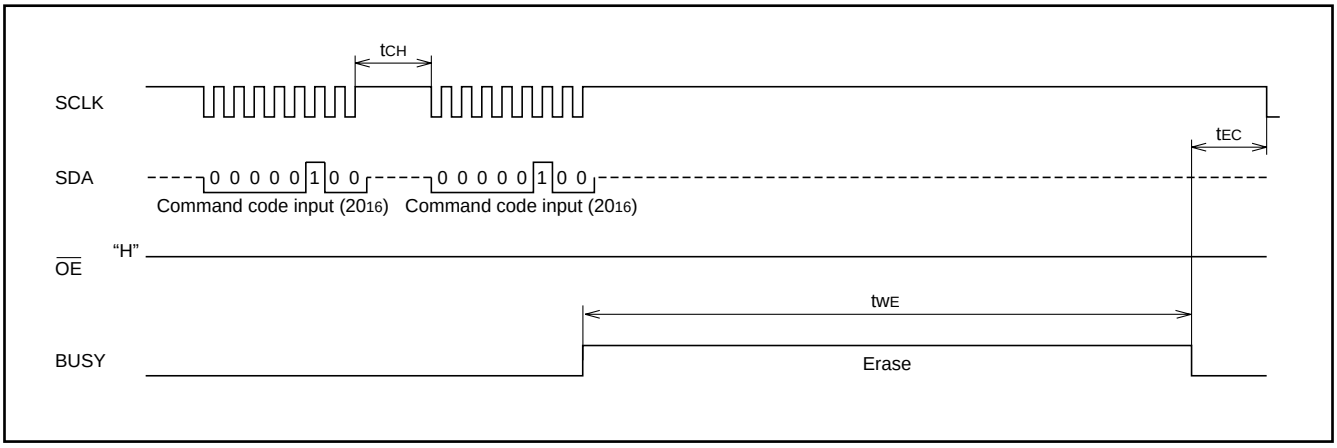
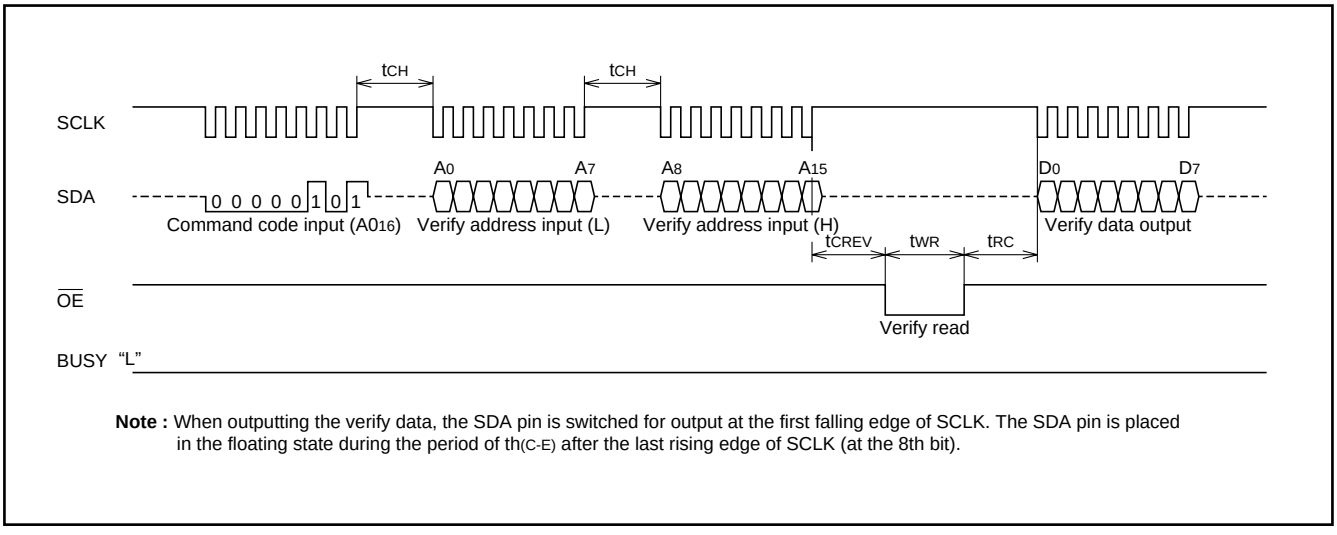


Fig. 95 Timings at erasing

● **Erase verify command**

The user must verify the contents of all addresses after completing the erase command. Input command code $A0_{16}$ in the first transfer. Proceed and input the low-order 8 bits and the high-order 8 bits of the address and pull the $\overline{OE}$ pin low. When this is done, the M38B79FF reads out the contents of the specified address, and then latchs it into the internal data latch. When the $\overline{OE}$ pin is released back high and serial clock is input to the SCLK pin, the verify data that has been latched into the data latch is serially output from the SDA pin.

Note: If any memory location where the contents have not been erased is found in the erase verify operation, execute the operation of "erase → erase verify" over again. In this case, however, the user does not need to write data 00_{16} to memory locations before erasing.



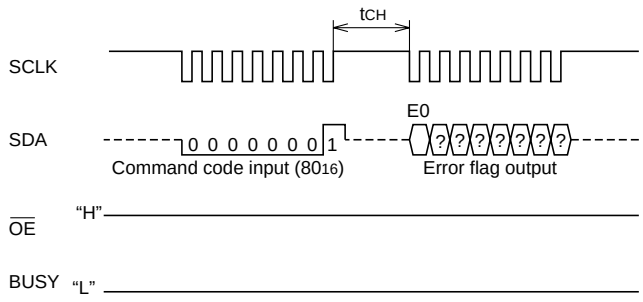
Note : When outputting the verify data, the SDA pin is switched for output at the first falling edge of SCLK. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of SCLK (at the 8th bit).

Fig. 96 Timings during erase verify

● **Error check command**

Input command code 80_{16} in the first transfer, and the M38B79FF outputs error information from the SDA pin, beginning at the next falling edge of the serial clock. If the LSB bit of the 8-bit error information is 1, it indicates that a command error has occurred. A command error means that some invalid commands other than commands shown in Table 20 has been input.

When a command error occurs, the serial communication circuit sets the corresponding flag and stops functioning to avoid an erroneous programming or erase. When being placed in this state, the serial communication circuit does not accept the subsequent serial clock and data (even including an error check command). Therefore, if the user wants to execute an error check command, temporarily drop the V_{PP} pin input to the $V_{PP}L$ level to terminate the serial input/output mode. Then, place the M38B79FF into the serial I/O mode back again. The serial communication circuit is reset by this operation and is ready to accept commands. The error flag alone is not cleared by this operation, so the user can examine the serial communication circuit's error conditions before reset. This examination is done by the first execution of an error check command after the reset. The error flag is cleared when the user has executed the error check command. Because the error flag is undefined immediately after power-on, always be sure to execute the error check command.



Note: When outputting the error flag, the SDA pin is switched for output at the first falling edge of the serial clock. The SDA pin is placed in the floating state during the period of $t_{h(C-E)}$ after the last rising edge of the serial clock (at the 8th bit).

Fig. 97 Timings at error checking

DC ELECTRICAL CHARACTERISTICS (Ta = 25 °C, Vcc = 5 V ± 10 %, Vpp = 11.7 to 12.6 V, unless otherwise noted)

Icc, Ipp-relevant standards during read, program, and erase are the same as in the parallel input/output mode. VIH, VIL, VOH, VOL, IIH, and IIL for the SCLK, SDA, BUSY, $\overline{OE}$ pins conform to the microcomputer modes.

Table 21 AC Electrical characteristics
(Ta = 25 °C, Vcc = 5 V ± 10 %, Vpp = 11.7 to 12.6 V, f(XIN) = 4 MHz, unless otherwise noted)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCH	Serial transmission interval	625(Note 1)		ns
tCR	Read waiting time after transmission	625(Note 1)		ns
tWR	Read pulse width	500(Note 2)		ns
tRC	Transfer waiting time after read	625(Note 1)		ns
tCRPV	Waiting time before program verify	6		µs
tWP	Programming time		10	µs
tPC	Transfer waiting time after programming	625(Note 1)		ns
tCREV	Waiting time before erase verify	6		µs
tWE	Erase time		9.5	ms
tEC	Transfer waiting time after erase	625(Note 1)		ns
tc(CK)	SCLK input cycle time	250		ns
tw(CKH)	SCLK high-level pulse width	100		ns
tw(CKL)	SCLK low-level pulse width	100		ns
tr(CK)	SCLK rise time	20		ns
tf(CK)	SCLK fall time	20		ns
td(C-Q)	SDA output delay time	0	90	ns
th(C-Q)	SDA output hold time	0		ns
th(C-E)	SDA output hold time (only the 8th bit)	187.5(Note 3)	312.5(Note 4)	ns
tsu(D-C)	SDA input set up time	30		ns
th(C-D)	SDA input hold time	90		ns

Notes 1: When f(XIN) = 4 MHz or less, calculate the minimum value according to formula 1.

$$\text{Formula 1} : \frac{2500}{f(X_{IN})} \times 10^6$$

2: When f(XIN) = 4 MHz or less, calculate the minimum value according to formula 2.

$$\text{Formula 2} : \frac{2000}{f(X_{IN})} \times 10^6$$

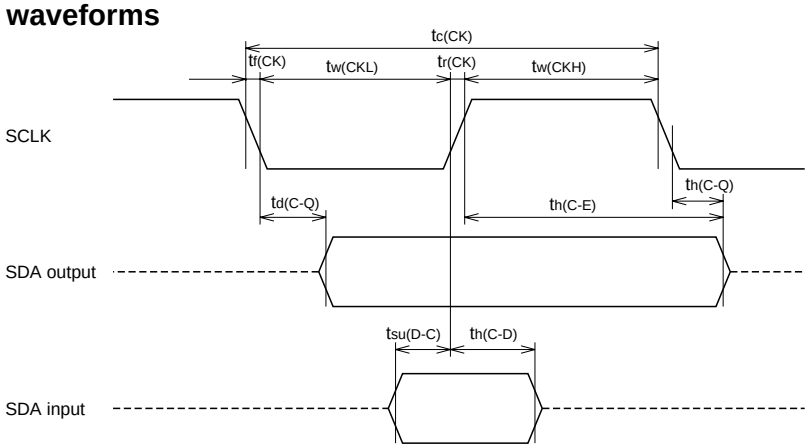
3: When f(XIN) = 4 MHz or less, calculate the minimum value according to formula 3.

$$\text{Formula 3} : \frac{750}{f(X_{IN})} \times 10^6$$

4: When f(XIN) = 4 MHz or less, calculate the minimum value according to formula 4

$$\text{Formula 4} : \frac{1250}{f(X_{IN})} \times 10^6$$

AC waveforms



Test conditions for AC characteristics

- Output timing voltage : VOL = 0.8 V, VOH = 2.0 V
- Input timing voltage : VIL = 0.2 Vcc, VIH = 0.8 Vcc

(3) Flash memory mode 3 (CPU reprogramming mode)

The M38B79FF has the CPU reprogramming mode where a built-in flash memory is handled by the central processing unit (CPU).
In CPU reprogramming mode, the flash memory is handled by writing and reading to/from the flash memory control register (see Figure 98) and the flash command register (see Figure 99).
The CNVSS pin is used as the VPP power supply pin in CPU reprogramming mode. It is necessary to apply the power-supply voltage of VPPH from the external to this pin.

Functional Outline (CPU reprogramming mode)

Figure 98 shows the flash memory control register bit configuration. Figure 99 shows the flash command register bit configuration.
Bit 0 of the flash memory control register is the CPU reprogramming mode select bit. When this bit is set to "1" and VPPH is applied to the CNVss/VPP pin, the CPU reprogramming mode is selected. Whether the CPU reprogramming mode is realized or not is judged by reading the CPU reprogramming mode monitor flag (bit 2 of the flash memory control register).
Bit 1 is a busy flag which becomes "1" during erase and program execution.
Whether these operations have been completed or not is judged by checking this flag after each command of erase and the program is executed.
Bits 4, 5 of the flash memory control register are the erase/program area select bits. These bits specify an area where erase and program is operated. When the erase command is executed after an area is specified by these bits, only the specified area is erased. Only for the specified area, programming is enabled; for the other areas, programming is disabled.
Figure 100 shows the CPU mode register bit configuration in the CPU reprogramming mode.

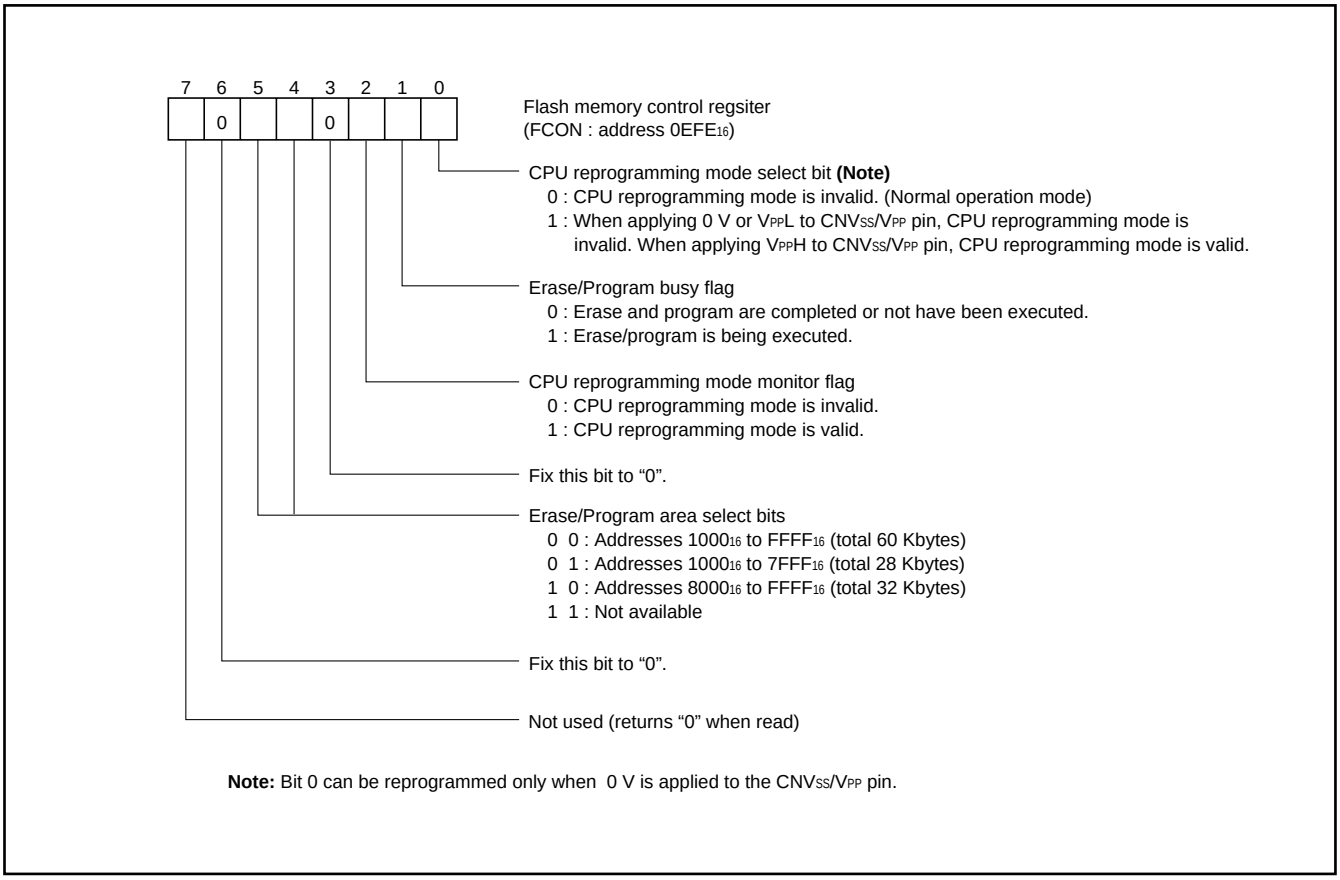


Fig. 98 Flash memory control register bit configuration

● **CPU reprogramming mode operation procedure**

The operation procedure in CPU reprogramming mode is described below.

< Beginning procedure >

① Apply 0 V to the CNVss/VPP pin for reset release.
② Set the CPU mode register. (see Figure 100)
③ After CPU reprogramming mode control program is transferred to internal RAM, jump to this control program on RAM. (The following operations are controlled by this control program).
④ Set "1" to the CPU reprogramming mode select bit.
⑤ Apply VPPH to the CNVSS/VPP pin.
⑥ Wait till CNVSS/VPP pin becomes 12 V.
⑦ Read the CPU reprogramming mode monitor flag to confirm whether the CPU reprogramming mode is valid.
⑧ The operation of the flash memory is executed by software-command-writing to the flash command register .

Note: The following are necessary other than this:
- •Control for data which is input from the external (serial I/O etc.) and to be programmed to the flash memory
- •Initial setting for ports etc.
- •Writing to the watchdog timer

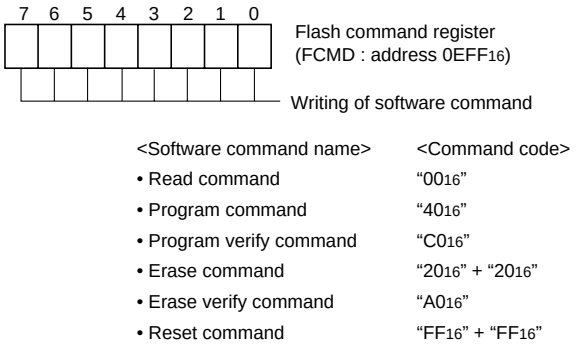
< Release procedure >

① Apply 0V to the CNVSS/VPP pin.
② Wait till CNVSS/VPP pin becomes 0V.
③ Set the CPU reprogramming mode select bit to "0".

Each software command is explained as follows.

● **Read command**

When "00$_{16}$" is written to the flash command register, the M38B79FF enters the read mode. The contents of the corresponding address can be read by reading the flash memory (For instance, with the LDA instruction etc.) under this condition.
The read mode is maintained until another command code is written to the flash command register. Accordingly, after setting the read mode once, the contents of the flash memory can continuously be read.
After reset and after the reset command is executed, the read mode is set.



<Software command name>	<Command code>
• Read command	"00$_{16}$"
• Program command	"40$_{16}$"
• Program verify command	"C0$_{16}$"
• Erase command	"20$_{16}$" + "20$_{16}$"
• Erase verify command	"A0$_{16}$"
• Reset command	"FF$_{16}$" + "FF$_{16}$"

Note: The flash command register is write-only register.

Fig. 99 Flash command register bit configuration

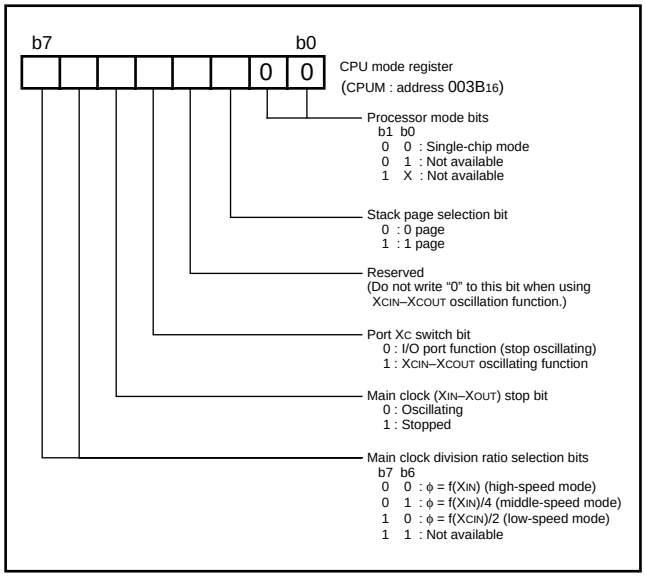


Fig. 100 CPU mode register bit configuration in CPU rewriting mode

● **Program command**

When "40$_{16}$" is written to the flash command register, the M38B79FF enters the program mode.

Subsequently to this, if the instruction (for instance, STA instruction) for writing byte data in the address to be programmed is executed, the control circuit of the flash memory executes the program. The erase/program busy flag of the flash memory control register is set to "1" when the program starts, and becomes "0" when the program is completed. Accordingly, after the write instruction is executed, CPU can recognize the completion of the program by polling this bit.

The programmed area must be specified beforehand by the erase/program area select bits.

During programming, watchdog timer stops with "FFFF$_{16}$" set.

Note: A programming operation is not completed by executing the program command once. Always be sure to execute a program verify command after executing the program command. When the failure is found in this verification, the user must repeatedly execute the program command until the pass. Refer to Figure 101 for the flow chart of the programming.

● **Program verify command**

When "C0$_{16}$" is written to the flash command register, the M38B79FF enters the program verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified (i.e., previously programmed address), the contents which has been written to the address actually is read.

CPU compares this read data with data which has been written by the previous program command. In consequence of the comparison, if not agreeing, the operation of "program → program verify" must be executed again.

● **Erase command**

When writing "20$_{16}$" twice continuously to the flash command register, the flash memory control circuit performs erase to the area specified beforehand by the erase/program area select bits.

Erase/program busy flag of the flash memory control register becomes "1" when erase begins, and it becomes "0" when erase completes. Accordingly, CPU can recognize the completion of erase by polling this bit.

Data "00$_{16}$" must be written to all areas to be erased by the program and the program verify commands before the erase command is executed.

During erasing, watchdog timer stops with "FFFF$_{16}$" set.

Note: The erasing operation is not completed by executing the erase command once. Always be sure to execute an erase verify command after executing the erase command. When the failure is found in this verification, the user must repeatedly execute the erase command until the pass. Refer to Figure 101 for the erasing flowchart.

● **Erase verify command**

When "A0$_{16}$" is written to the flash command register, the M38B79FF enters the erase verify mode. Subsequently to this, if the instruction (for instance, LDA instruction) for reading byte data from the address to be verified, the contents of the address is read.

CPU must erase and verify to all erased areas in a unit of address.

If the address of which data is not "FF$_{16}$" (i.e., data is not erased) is found, it is necessary to discontinue erasure verification there, and execute the operation of "erase → erase verify" again.

Note: By executing the operation of "erase → erase verify" again when the memory not erased is found. It is unnecessary to write data "00$_{16}$" before erasing in this case.

● **Reset command**

The reset command is a command to discontinue the program or erase command on the way. When "FF$_{16}$" is written to the command register two times continuously after "40$_{16}$" or "20$_{16}$" is written to the flash command register, the program, or erase command becomes invalid (reset), and the M38B79FF enters the reset mode.

The contents of the memory does not change even if the reset command is executed.

DC Electric Characteristics

Note: The characteristic concerning the flash memory part are the same as the characteristic of the parallel I/O mode.

AC Electric Characteristics

Note: The characteristics are the same as the characteristic of the microcomputer mode.

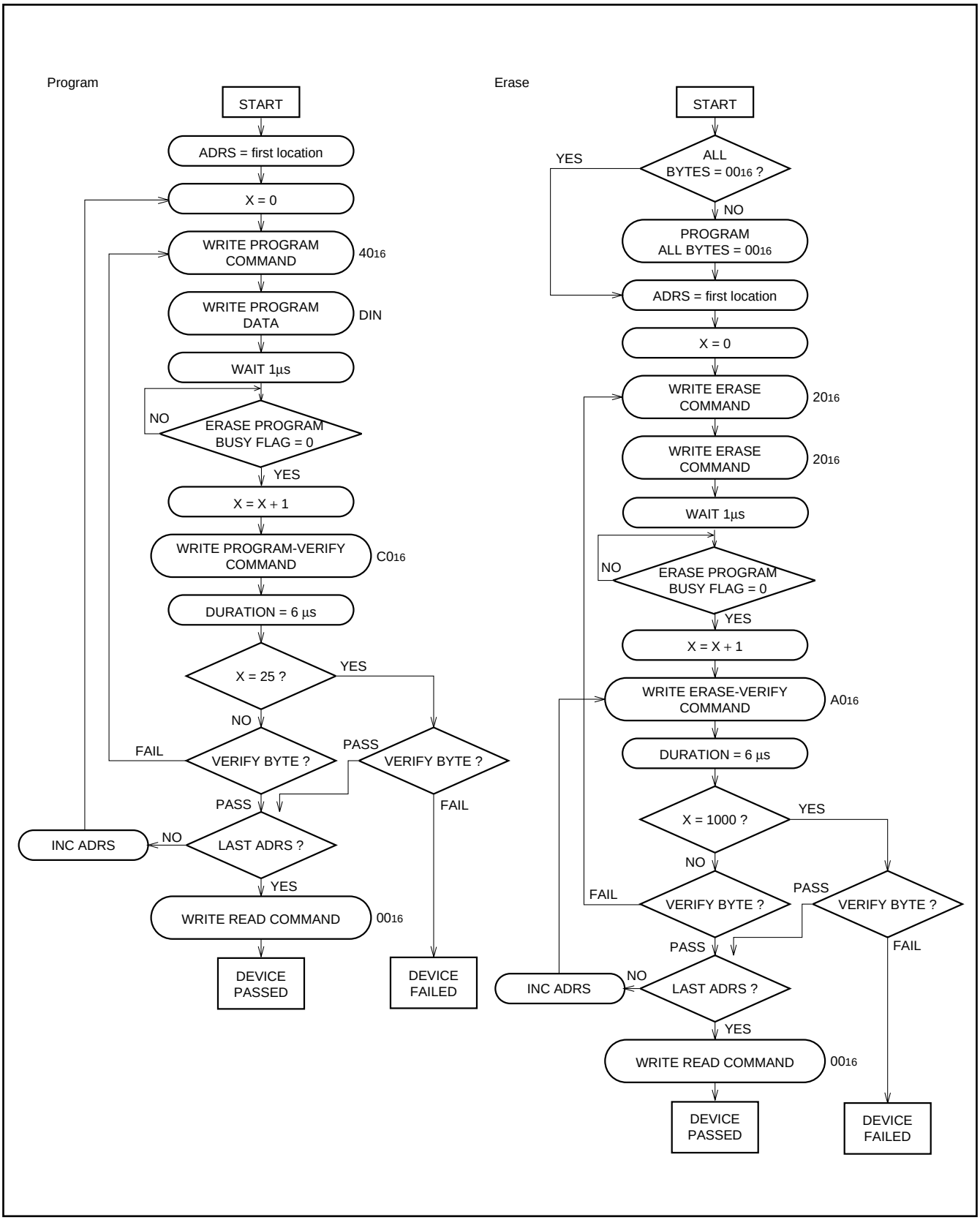


Fig. 101 Flowchart of program/erase operation at CPU reprogramming mode

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

•Using an external clock

When using an external clock, input "H" to the external clock input pin and clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

•Using an internal clock

When using an internal clock, set the synchronous clock to the internal clock, then clear the serial I/O interrupt request bit before executing serial I/O transfer and serial I/O automatic transfer.

Automatic Transfer Serial I/O

When using the automatic transfer serial I/O mode of the serial I/O1, set an automatic transfer interval as the following.

Otherwise the serial data might be incorrectly transmitted/received.

•Set an automatic transfer interval for each 1-byte data transfer as the following:

(1) Not using FLD controller

Keep the interval for **5 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.

(2) Using FLD controller

(a) Not using gradation display

Keep the interval for **17 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.

(b) Using gradation display

Keep the interval for **27 cycles or more of internal system clock** from clock rising of the last bit of 1-byte data.

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(X_{IN}) is at least on 250 kHz during an A-D conversion.

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes rapidly poor under the V_{CC} = 4.0 V or less condition; a supply voltage of $V_{CC} \geq 4.0$ V is recommended. When a D-A converter is not used, set the value of D-A conversion register to "00_{16}".

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is half of the X_{IN} period in high-speed mode.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin), between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin), and between program power source pin (CNV_{SS}/V_{PP}) and GND pin for flash memory version when on-board reprogramming is executed. Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF–0.1 μF is recommended.

Flash Memory Version

The CNV_{SS} pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNV_{SS} pin and V_{SS} pin or V_{CC} pin with 1 to 10 kΩ resistance.
The mask ROM version track of CNV_{SS} pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies) or in one floppy disk.

ELECTRICAL CHARACTERISTICS

Table 22 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltages	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_{EE}	Pull-down power source voltages		V_{CC} –48 to V_{CC} +0.3	V
V_I	Input voltage $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$		V_{CC} –48 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}, CNV_{SS}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage X_{CIN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$		V_{CC} –48 to V_{CC} +0.3	V
V_O	Output voltage $P6_4$–$P6_7$, $P8_0$–$P8_3$, $P7_0$–$P7_7$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6, X_{OUT}, X_{COUT}		–0.3 to V_{CC} +0.3	V
P_d	Power dissipation	T_a = –20 to 65 °C	800	mW
		T_a = 65 to 85 °C	800 –12.5 × (T_a –65)	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Table 23 Recommended operating conditions

(V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (mask ROM version)	High-speed mode	4.0	5.0	5.5	V
		Middle/Low-speed mode	2.7	5.0	5.5	V
V_{CC}	Power source voltage (flash memory version)		4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{EE}	Pull-down power source voltage		Vcc –43		V_{CC}	V
V_{REF}	Analog reference voltage	when A-D converter is used	2.0		V_{CC}	V
		when D-A converter is used	3.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_{15}		0		V_{CC}	V
V_{IH}	“H” input voltage $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6		0.75V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P6_4$–$P6_7$		0.4V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$		0.52V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage RxD, S_{CLK21}, S_{CLK22}		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage X_{IN}, X_{CIN}, $\overline{RESET}$, CNVss		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6		0		0.25V_{CC}	V
V_{IL}	“L” input voltage $P6_4$–$P6_7$		0		0.16V_{CC}	V
V_{IL}	“L” input voltage $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$		0		0.2V_{CC}	V
V_{IL}	“L” input voltage RxD, S_{CLK21}, S_{CLK22}		0		0.2V_{CC}	V
V_{IL}	“L” input voltage X_{IN}, X_{CIN}, $\overline{RESET}$, CNVss		0		0.2V_{CC}	V

Table 24 Recommended operating conditions
(V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$			–240	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current **(Note 1)** $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			–60	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P6_4$–$P6_7$, $P7_0$–$P7_7$			100	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current **(Note 1)** $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			60	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$			–120	mA
$\Sigma I_{OH(avg)}$	"H" total average output current **(Note 1)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			–30	mA
$\Sigma I_{OL(avg)}$	"L" total average output current **(Note 1)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			50	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$			–40	mA
$I_{OH(peak)}$	"H" peak output current **(Note 2)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			–10	mA
$I_{OL(peak)}$	"L" peak output current **(Note 2)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			10	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$			–18	mA
$I_{OH(avg)}$	"H" average output current **(Note 3)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			–5	mA
$I_{OL(avg)}$	"L" average output current **(Note 3)** $P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6			5	mA
f(CNTR)	Clock input frequency for timers 2, 4, and X (duty cycle 50 %)			250	kHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**			4.2	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**		32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50%.
5: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

Table 25 Electrical characteristics
(V_{CC} = 4.0 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$-$P5_7$, $P6_0$–$P6_3$	I_{OH} = –18 mA	V_{CC}–2.0			V
V_{OH}	"H" output voltage	$P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6	I_{OH} = –10 mA	V_{CC}–2.0			V
V_{OL}	"L" output voltage	$P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6	I_{OL} = 10 mA			2.0	V
V_{T+}–V_{T-}	Hysteresis	RxD, S_{CLK21}, S_{CLK22}, S_{RDY1}, $P7_0$–$P7_3$, $P7_7$, $P8_2$–$P8_3$, $P9_0$–$P9_2$, PB_0, PB_2, PB_4–PB_6			0.4		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$, X_{IN}			0.5		V
V_{T+}–V_{T-}	Hysteresis	X_{CIN}			0.5		V
I_{IH}	"H" input current	$P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$-$P5_7$, $P6_0$–$P6_3$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$, CNVss, X_{CIN}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current	$P6_4$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_3$, $P9_0$–$P9_7$, PA_0–PA_7, PB_0–PB_6	V_I = V_{SS} Pull-up "off"			–5.0	µA
			V_{CC} = 5 V, V_I = V_{SS} Pull-up "on"	–30	–70	–140	µA
			V_{CC} = 3 V, V_I = V_{SS} Pull-up "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current	$P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$ **(Note)**	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNVss, X_{CIN}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4.0		µA

Note: Except when reading ports P1, P3, P4, P5 or P6.

Table 26 Electrical characteristics
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{LOAD}	Output load current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, ($P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$ at option)	V_{EE} = V_{CC}–43 V, V_{OL} = V_{CC} Output transistors "off"	400	600	900	µA
I_{LEAK}	Output leak current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$	V_{EE} = V_{CC}–43 V, V_{OL} = V_{CC}–43 V Output transistors "off"			–10	µA
I_{READH}	"H" read current $P1_0$–$P1_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_3$	V_I = 5 V		1		µA
V_{RAM}	RAM hold voltage	When clock is stopped	2		5.5	V
I_{CC}	Power source current	High-speed mode, Vcc = 5 V, f(X_{IN}) = 4.2 MHz f(X_{CIN}) = 32.768 kHz Output transistors "off"		7.0	15	mA
		High-speed mode, Vcc = 5 V, f(X_{IN}) = 4.2 MHz (in WIT state) f(X_{CIN}) = 32.768 kHz Output transistors "off"		1		mA
		Middle-speed mode, Vcc = 5 V, f(X_{IN}) = 4.2 MHz f(X_{CIN}) = stopped Output transistors "off"		3		mA
		Middle-speed mode, Vcc = 5 V, f(X_{IN}) = 4.2 MHz (in WIT state) f(X_{CIN}) = stopped Output transistors "off"		1		mA
		Low-speed mode, Vcc = 3 V, f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz Output transistors "off"		20	55	µA
		Low-speed mode, Vcc = 3 V, f(X_{IN}) = stopped f(X_{CIN}) = 32.768 kHz (in WIT state) Output transistors "off"		8	20	µA
		Increment when A-D conversion is executed		0.6		mA
		All oscillation stopped (in STP state) Output transistors "off" — Ta = 25 °C		0.1	1	µA
		All oscillation stopped (in STP state) Output transistors "off" — Ta = 85 °C			10	µA

Table 27 A-D converter characteristics

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 250 kHz to 4.2 MHz in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				10	Bits
—	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5.12 V		±1	±2.5	LSB
T_{CONV}	Conversion time		61		62	tc(ϕ)
IV_{REF}	Reference input current	V_{REF} = 5.0 V	50	150	200	µA
I_{IA}	Analog port input current			0.5	5.0	µA
R_{LADDER}	Ladder resistor			35		kΩ

Table 28 D-A converter characteristics

(V_{CC} = 4.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, V_{REF} = 3.0 to Vcc, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy	V_{CC} = 4.0–5.5 V			1.0	%
	(excluding quantization error)	V_{CC} = 3.0–5.5 V			2.5	%
tsu	Setting time				3	µs
RO	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power source input current **(Note)**				3.2	mA

Note: Except ladder resistor for A-D converter

TIMING REQUIREMENTS

Table 29 Timing requirements (1)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2.0			µs
$t_{C(XIN)}$	Main clock input cycle time (X_{IN} input)	238			ns
$t_{WH(XIN)}$	Main clock input “H” pulse width	60			ns
$t_{WL(XIN)}$	Main clock input “L” pulse width	60			ns
$t_{C(XCIN)}$	Sub-clock input cycle time (X_{CIN} input)	20			µs
$t_{WH(XCIN)}$	Sub-clock input “H” pulse width	5.0			µs
$t_{WL(XCIN)}$	Sub-clock input “L” pulse width	5.0			µs
$t_{C(CNTR)}$	$CNTR_0$–$CNTR_2$ input cycle time	4.0			µs
$t_{WH(CNTR)}$	$CNTR_0$–$CNTR_2$ input “H” pulse width	1.6			µs
$t_{WL(CNTR)}$	$CNTR_0$–$CNTR_2$ input “L” pulse width	1.6			µs
$t_{WH(INT)}$	INT_0–INT_4 input “H” pulse width (INT_2 when noise filter is not used) **(Note 1)**	80			ns
$t_{WL(INT)}$	INT_0–INT_4 input “L” pulse width (INT_2 when noise filter is not used) **(Note 1)**	80			ns
$t_{WH(INT2)}$	INT_2 input “H” pulse width (when noise filter is used) **(Notes 1, 2)**	3			CLKs
$t_{WL(INT2)}$	INT_2 input “L” pulse width (when noise filter is used) **(Notes 1, 2)**	3			CLKs
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time	950			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width	400			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width	400			ns
$t_{su(SIN1-SCLK1)}$	Serial I/O1 input setup time	200			ns
$t_{h(SCLK1-SIN1)}$	Serial I/O1 input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	800			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	370			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	370			ns
$t_{su(RxD-SCLK2)}$	Serial I/O2 input setup time	220			ns
$t_{h(SCLK2-RxD)}$	Serial I/O2 input hold time	100			ns
$t_{C(SCLK3)}$	Serial I/O3 clock input cycle time	1000			ns
$t_{WH(SCLK3)}$	Serial I/O3 clock input “H” pulse width	400			ns
$t_{WL(SCLK3)}$	Serial I/O3 clock input “L” pulse width	400			ns
$t_{su(SIN3-SCLK3)}$	Serial I/O3 input setup time	200			ns
$t_{h(SCLK3-SIN3)}$	Serial I/O3 input hold time	200			ns

Notes 1: IIDCON2, IIDCON3 = “00” when noise filter is not used
IIDCON2, IIDCON3 = “01” or “10” when noise filter is used
2: Unit indicates sample clock number of noise filter.

Table 30 Switching characteristics
(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tWH (SCLK)	Serial I/O clock output "H" pulse width	CL = 100 pF	tc(SCLK)/2–160			ns
tWL (SCLK)	Serial I/O clock output "L" pulse width	CL = 100 pF	tc(SCLK)/2–160			ns
td (SCLK1-SOUT1)	Serial I/O1 output delay time **(Note 1)**				200	ns
tv (SCLK1-SOUT1)	Serial I/O1 output valid time **(Note 1)**		0			ns
td (SCLK2-TxD)	Serial I/O2 output delay time **(Note 2)**				140	ns
tv (SCLK2-TxD)	Serial I/O2 output valid time **(Note 2)**		–30			ns
td (SCLK3-SOUT3)	Serial I/O3 output delay time **(Note 3)**				200	ns
tv (SCLK3-SOUT3)	Serial I/O3 output valid time **(Note 3)**		0			ns
tr (SCLK)	Serial I/O clock output rising time	CL = 100 pF			40	ns
tf (SCLK)	Serial I/O clock output falling time	CL = 100 pF			40	ns
tr (Pch–strg)	P-channel high-breakdodwn-voltage output rising time **(Note 4)**	CL = 100 pF VEE = Vcc –43 V		55		ns
tr (Pch–weak)	P-channel high-breakdodwn-voltage output rising time **(Note 5)**	CL = 100 pF VEE = Vcc –43 V		1.8		µs

Notes 1: When the PB5/SOUT1 P-channel output disable bit of the serial I/O1 control register (bit 7 of address 001A16) is "0".
2: When the P65/TxD P-channel output disable bit of the UART control register (bit 4 of address 003816) is "0".
3: When the P91/SOUT3 P-channel output disable bit of the serial I/O3 control register (bit 7 of address 0EEC16) is "0".
4: When the high-breakdown voltage port drivability selection bit of the FLDC mode register (bit 7 of address 0EF416) is "0".
5: When the high-breakdown voltage port drivability selection bit of the FLDC mode register (bit 7 of address 0EF416) is "1".

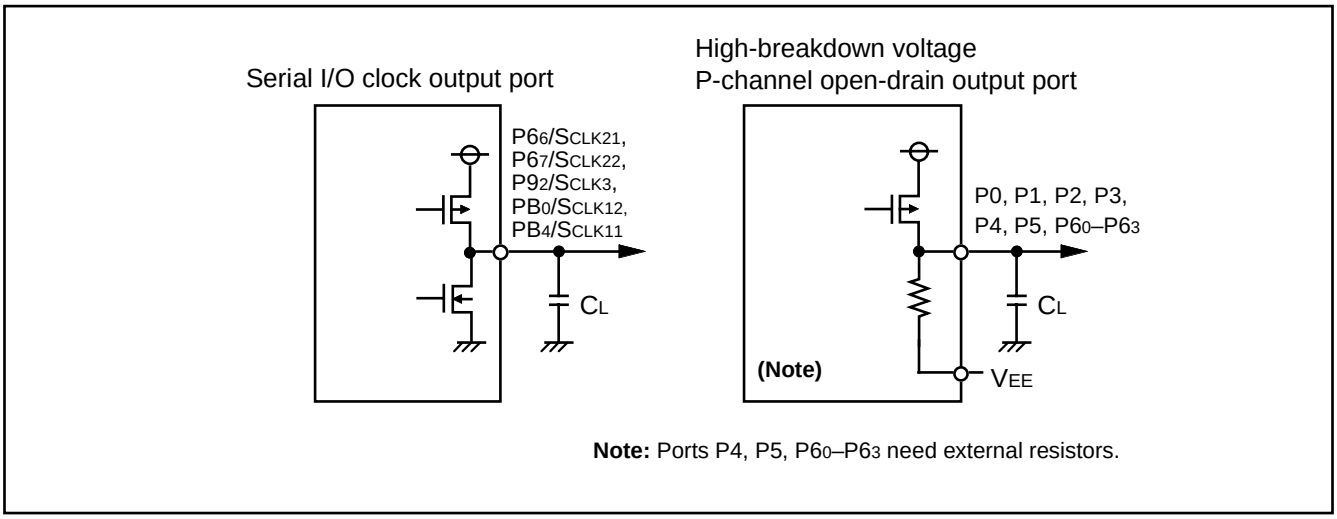


Fig. 102 Circuit for measuring output switching characteristics

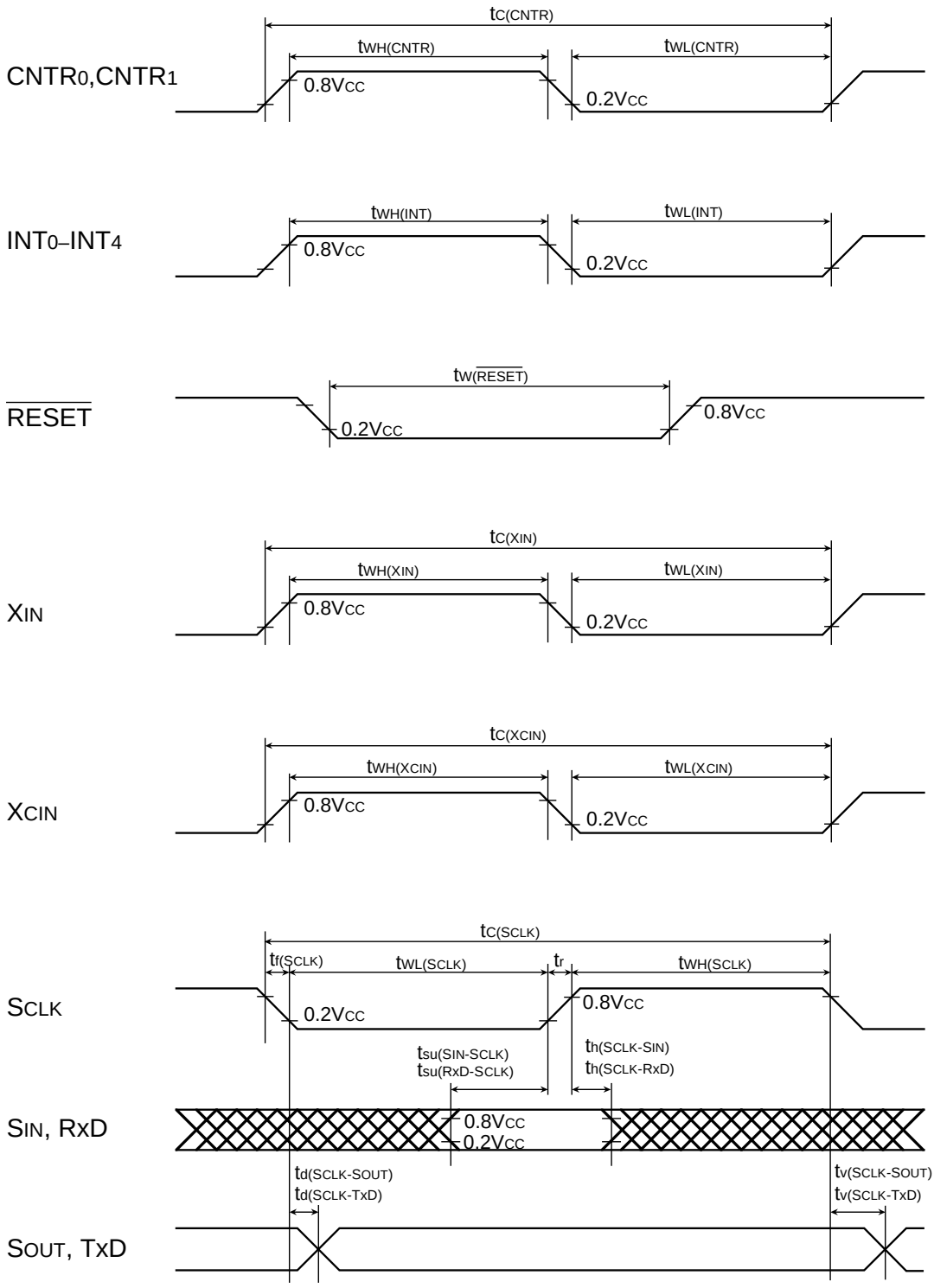


Fig. 103 Timing diagram

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

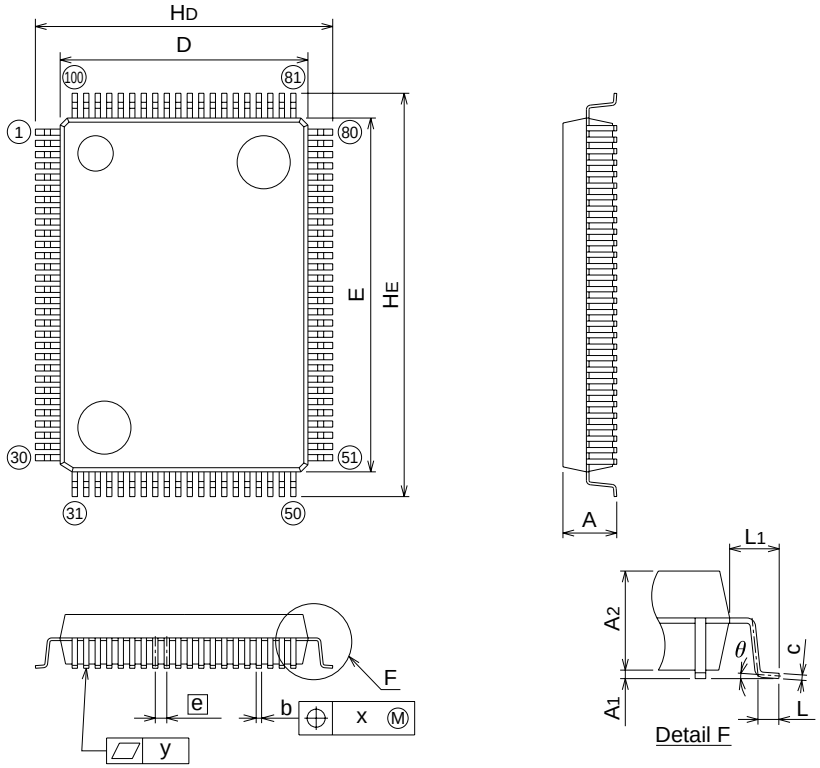
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

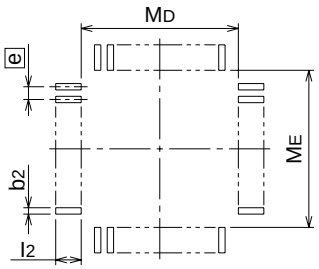
PACKAGE OUTLINE

100P6S-A

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	–	1.58	Alloy 42





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
l2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

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REVISION HISTORY	38B7 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
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