288pin Registered DIMM based on 4Gb D-die

78FBGA with Lead-Free & Halogen-Free (RoHS compliant)

CAUTION :
This document includes some items still under discussion in JEDEC
Therefore, those may be changed without pre-notice based on JEDEC progress
In addition, it is highly recommended that you not send specs without Samsung's permission

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC. Release	Aug. 2014	-	J.Y.Lee
1.1	- Addition of Data Output Timing (tDVWd , tDVWp) on page 33	Sep. 2014	-	J.Y.Lee
	- Change of [Table 21] Silicon pad I/O Capacitance on page 28			
	- Change of [Table 25] Timing Parameters by Speed Grade on page 32~38			
	- Change of Registering Clock Driver Specification on page 9			
1.11	- Correction of typo	Jan. 2015	-	J.Y.Lee
1.2	- Addition of VDDSPD tolerance on page 8	Mar. 2015	-	J.Y.Lee
1.3	- Change of IDD value on page 26	Apr. 2015	-	J.Y.Lee

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288pin Registered DIMM based on 4Gb D-die

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1. DDR4 Registered DIMM Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M393A8G40D40-CRB	64GB	8Gx72	TSV 4Gx4(K4AAG045WD-4CRB)*36	8	31.25mm

2. Key Features

Speed	DDR4-1600	DDR4-1866	DDR4-2133	Unit
	13-12-11	15-14-13	17-15-15	
tCK(min)	1.25	1.071	0.937	ns
CAS Latency	13	15	17	nCK
tRCD(min)	15	15	14.06	ns
tRP(min)	13.75	13.92	14.06	ns
tRAS(min)	35	34	33	ns
tRC(min)	48.75	47.92	47.06	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17
- Programmable Additive Latency(Posted CAS) : CL - 2, CL - 3 or CL - 5 clock
- Programmable CAS Write Latency(CWL) = 9,11 (DDR4-1600) , 10,11,12 (DDR4-1866) , 11,14 (DDR4-2133)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset

3. Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
TSV 4Gx4 (16Gb) based Module	A0-A17	A0-A9	BA0-BA1	A10/AP

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Registered DIMM — datasheet — **DDR4 SDRAM**

4. Registered DIMM Pin Configurations (Front side/Back side)

| Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1. VPP is 2.5V DC
2. Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.
3. Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM
4. The 5th VPP is required on all modules. DIMMs.

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5. Pin Description

Pin Name	Description	Pin Name	Description
A0–A17[1]	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0–SA2	I2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power supply
WE_n[4]	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input for activate input	ALERT_n	Register ALERT_n output
DQ0–DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0–CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t–DQS17_t	Data Buffer data strobes (positive line of differential pair)	VTT	SDRAM I/O termination supply
DQS0_c–DQS17_c	Data Buffer data strobes (negative line of differential pair)	RFU	Reserved for future use
CK0_t, CK1_t	Register clock input (positive line of differential pair)		
CK0_c, CK1_c	Register clocks input (negative line of differential pair)		

NOTE :
1. Address A17 is only valid for 16 Gb x4 based SDRAMs.
2. RAS_n is a multiplexed function with A16.
3. CAS_n is a multiplexed function with A15.
4. WE_n is a multiplexed function with A14.

6. ON DIMM Thermal Sensor
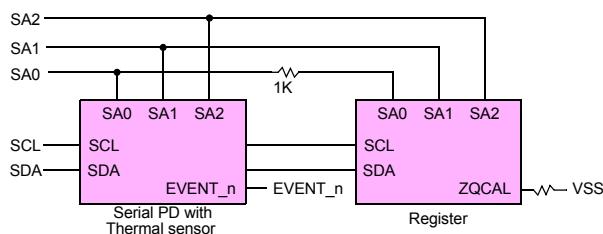
NOTE : 1. All Samsung RDIMM support Thermal sensor on DIMM
2. When the SPD and the thermal sensor are placed on the module, R1 is placed but R2 is not.
When only the SPD is placed on the module, R2 is placed but R1 is not.

[Table 1] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

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7. Input/Output Functional Description

Symbol	Type	Function
CK0_t, CK0_c, CK1_t, CK1_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE0, CKE1	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS0_n, CS1_n, CS2_n, CS3_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT0, ODT1	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
DQS0_t-DQS17_t, DQS0_c-DQS17_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
PAR[1]	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0, C1, C2. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Output (Input)	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. Using this signal or not is dependent on the system. If the SDRAM ALERT_n pins are not connected to the ALERT_n pin on the edge connector is must still be connected to VDD on DIMM.
RFU		Reserved for Future Use: No on DIMM electrical connection is present
NC		No Connect: No on DIMM electrical connection is present

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Symbol	Type	Function
VDD[2]	Supply	Power Supply: 1.2 V ± 0.06 V
VSS	Supply	Ground
VTT	Supply	VDD/2
VPP	Supply	SDRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VDDSPD	Supply	SPD and register supply voltage. Register requires the nominl volatge to be 2.5V±10%.
VREFCA	Supply	Reference voltage for CA

NOTE :
1. Input only pins (BG0-BG1, BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, C0, C1, C2 and RESET_n) do not supply termination.
2. For PC4 VDD is 1.2V. For PC4L VDD is TBD.

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8. Registering Clock Driver Specification

8.1 Timing & Capacitance values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		Units	Notes
			Min	**Max**		
fclock	Input Clock Frequency	application frequency	625	1080	MHz	
t_{CH}/t_{CL}	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	t_{CK}	
t_{ACT}	Inputs active time4 before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	8	-	t_{CK}	
t_{PDM}	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	ns	
t_{DIS}	output disable time	Rising edge of Yn_t to output float	0.5*tCK + tQSK1(min)	-	ps	
t_{EN}	output enable time	Output valid to rising edge of Yn_t	0.5*tCK - tQSK1(max)	-	ps	
C_I	Input capacitance, Data inputs	NOTE[1,2]	0.8	1.1	pF	
C_{CK}	Input capacitance, CK_t, CK_c	NOTE[1,2]	0.8	1.1		
C_{IR}	Input capacitance, DRST_n	$V_I=V_{DD}$ or V_{SS} ; $V_{DD}=1.2V$	0.5	2.0		

Note:
1. This parameter does not include package capacitance
2. Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0..DC2, DPAR, DCS0/1_n

8.2 Clock driver Characteristics

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		Units	Notes
			Min	**Max**		
t_{jit} (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x tCK	ps	
t_{STAB}	Stabilization time		-	5	us	
t_{CKsk}	Clock Output skew		-	10	ps	
$t_{jit}(per)$	Yn Clock Period jitter		-0.025 * tCK	0.025 * tCK	ps	
$t_{jit}(hper)$	Half period jitter		-0.032 * tCK	0.032 * tCK	ps	
t_{Qsk1}	Qn Output to clock tolerance		-0.125 * tCK	0.125 * tCK	ps	
t_{dynoff}	Maximum re-driven dynamic clock off-set		-	50	ps	

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9. Function Block Diagram:

9.1 64GB, 8Gx72 Module (Populated as 8 ranks of x4 DDR4 SDRAMs)

Input	Register Output
BG[1:0]	QABG[1:0] -> BG[1:0]: SDRAMs D[20:1] QBBG[1:0] -> BG[1:0]: SDRAMs D[36:21]
BA[1:0]	QABA[1:0] -> BA[1:0]: SDRAMs D[20:1] QBBA[1:0] -> BA[1:0]: SDRAMs D[36:21]
A[17:0]	QAA[17:0] -> A[17:0]: SDRAMs D[20:1] QBA[17:0] -> A[17:0]: SDRAMs D[36:21]
ACT_n	QAACT_n -> ACT_n: SDRAMs D[20:1] QBACT_n -> ACT_n: SDRAMs D[36:21]
C[2:0]	QAC[2:0] -> C[2:0]: SDRAMs D[20:1] QBC[2:0] -> C[2:0]: SDRAMs D[36:21]
PARITY	QAPAR -> PAR: SDRAMs D[20:1] QBPAR -> PAR: SDRAMs D[36:21]
CKE0	QACKE0 -> CKE: SDRAMs D[10:1] QBCKE0 -> CKE: SDRAMs D[28:21]
CKE1	QACKE1 -> CKE: SDRAMs D[20:11] QBCKE1 -> CKE: SDRAMs D[36:29]
ODT0	QAODT0 -> ODT: SDRAMs D[10:1] QBODT0 -> ODT: SDRAMs D[28:21]
ODT1	QAODT1 -> ODT: SDRAMs D[20:11] QBODT1 -> ODT: SDRAMs D[36:29]
CS0_n	QACS0_n -> CS_n: SDRAMs D[10:1] QBCS0_n -> CS_n: SDRAMs D[28:21]
CS1_n	QACS1_n -> CS_n: SDRAMs D[20:11] QBCS1_n -> CS_n: SDRAMs D[36:29]
CK0_t CK0_c CK1_t CK1_c	Y0_t -> CK_t: SDRAMs D[24:21], D[32:29] Y1_t -> CK_t: SDRAMs D[5:1], D[15:11] Y2_t -> CK_t: SDRAMs D[28:25], D[36:33] Y3_t -> CK_t: SDRAMs D[10:6], D[20:16] Y0_c -> CK_c: SDRAMs D[24:21], D[32:29] Y1_c -> CK_c: SDRAMs D[5:1], D[15:11] Y2_c -> CK_c: SDRAMs D[28:25], D[36:33] Y3_c -> CK_c: SDRAMs D[10:6], D[20:16]
RESET_n	QRST_n -> RESET_n: All SDRAMs
ALERT_n	ERROR_IN_n <- ALERT_n: All SDRAMs

Address, Command and Control lines

NOTE :
1. CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2. CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3. Unless otherwise noted resistors are 22Ω ± 5%.
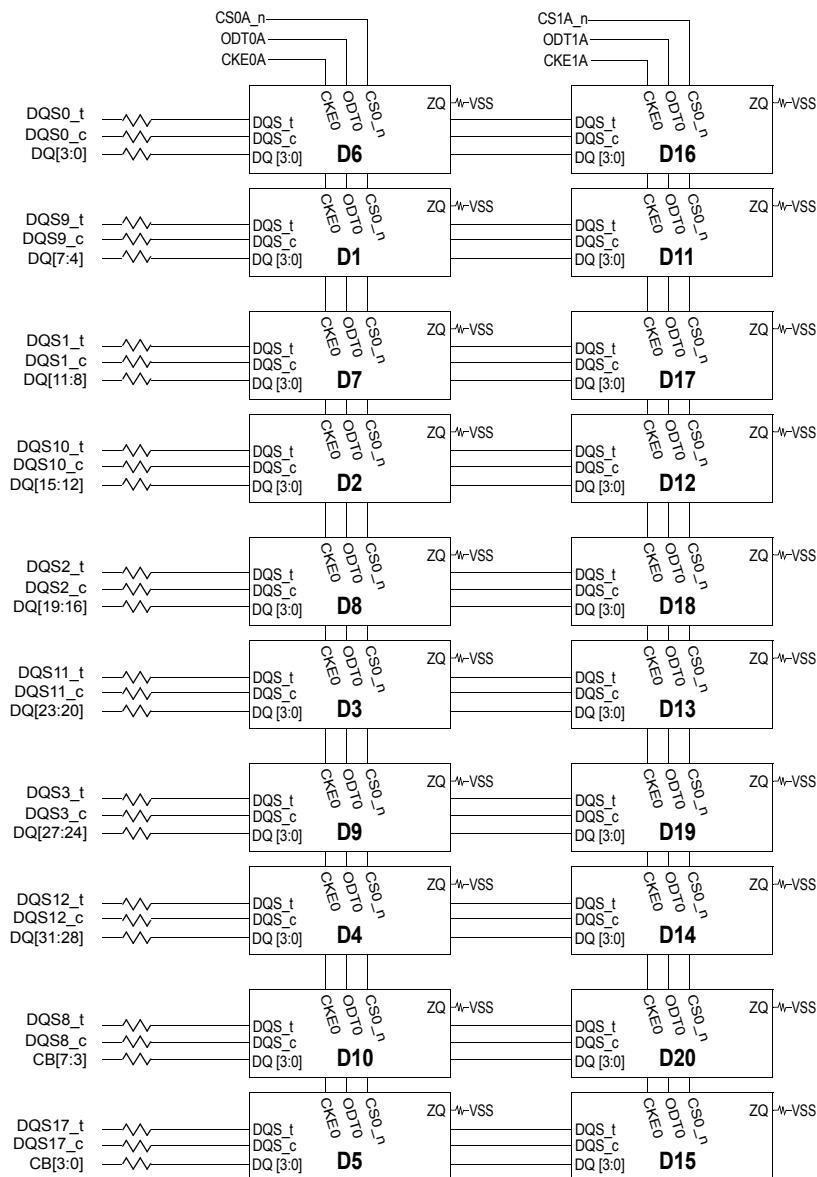
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NOTE :

1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.

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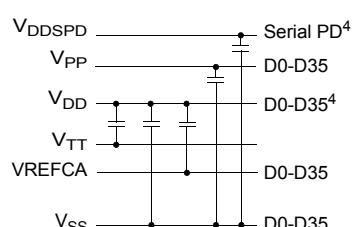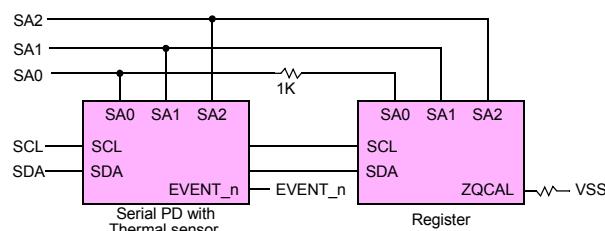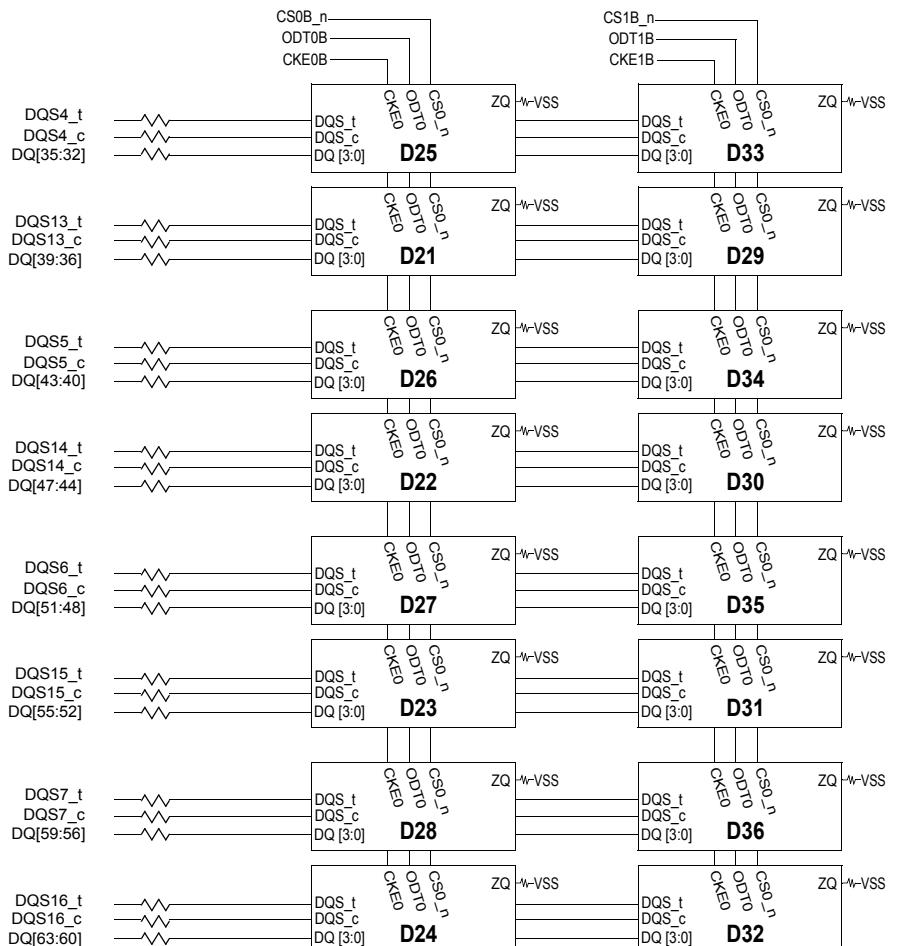
NOTE :
1. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
2. See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3. TEN pin of SDRAMs is tied to VSS.
4. VDDSPD is also applied to the register. VDD is also applied to the register and the data buffers.

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10. Absolute Maximum Ratings

10.1 Absolute Maximum DC Ratings

[Table 2] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1,3
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV

4. VPP must be equal or greater than VDD/VDDQ at all times.

11. AC & DC Operating Conditions

11.1 Recommended DC Operating Conditions

[Table 3] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.

2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

3. DC bandwidth is limited to 20MHz.

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12. AC & DC Input Measurement Levels

12.1 AC & DC Logic input levels for single-ended signals

[Table 4] Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133		Unit	NOTE
		Min.	Max.		
$V_{IH.CA}(DC75)$	DC input logic high	$V_{REFCA}+ 0.075$	V_{DD}	V	
$V_{IL.CA}(DC75)$	DC input logic low	V_{SS}	$V_{REFCA}-0.075$	V	
$V_{IH.CA}(AC100)$	AC input logic high	$V_{REF} + 0.1$	Note 2	V	1
$V_{IL.CA}(AC100)$	AC input logic low	Note 2	$V_{REF} - 0.1$	V	1
$V_{REFCA}(DC)$	Reference Voltage for ADD, CMD inputs	$0.49*V_{DD}$	$0.51*V_{DD}$	V	2,3

NOTE :
1. See "Overshoot and Undershoot Specifications" on section.
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3. For reference : approx. VDD/2 ± 12mV

12.2 AC and DC Input Measurement Levels : V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than ± 1% V_{DD}.
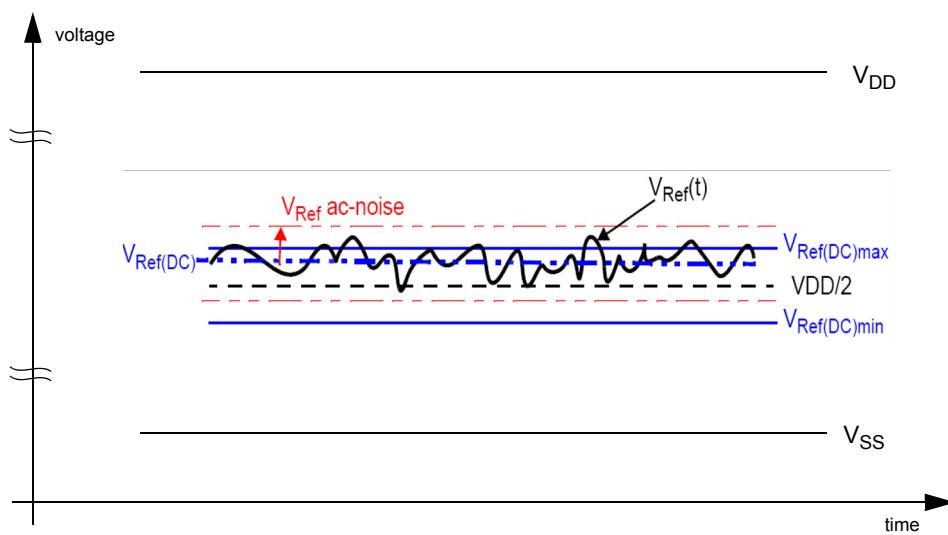
Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF}.

"V_{REF}" shall be understood as $V_{REF}(DC)$, as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

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12.3 AC and DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition
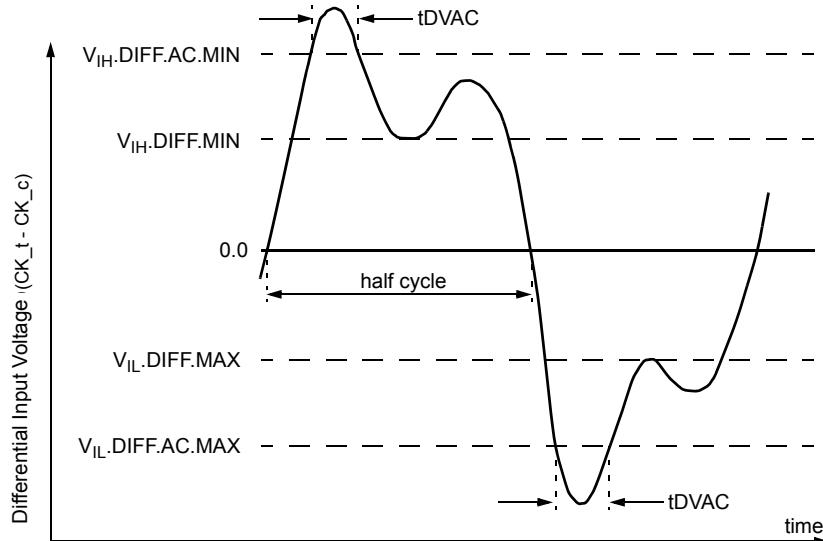
Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE :
1. Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2. Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

12.3.2 Differential swing requirements for clock (CK_t - CK_c)

[Table 5] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		unit	NOTE
		min	max		
V_{IHdiff}	differential input high	+0.150	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.150	V	1
$V_{IHdiff}(AC)$	differential input high ac	$2 \times (V_{IH}(AC) - V_{REF})$	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	$2 \times (V_{IL}(AC) - V_{REF})$	V	2

NOTE:
1. Used to define a differential signal slew-rate.
2. for CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}(AC)$ of ADD/CMD and V_{REFCA};
3. These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}(DC)$ max, $V_{IL.CA}(DC)$min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 6] Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $|V_{IH/Ldiff}(AC)|$ = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

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12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c
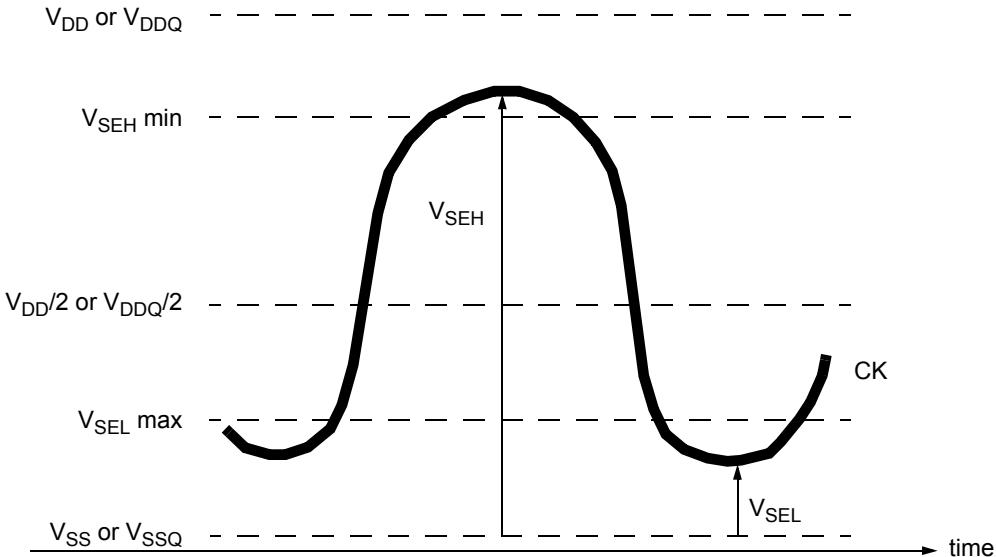
Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 7] Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		Unit	NOTE
		Min	Max		
V_{SEH}	Single-ended high-level for CK_t , CK_c	(VDD/2)+0.100	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t , CK_c	NOTE3	(VDD/2)-0.100	V	1, 2

NOTE :

1. For CK_t - CK_c use $V_{IH.CA}/V_{IL.CA}$(AC) of ADD/CMD;

2. V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};

3. These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

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12.4 Slew Rate Definitions

12.4.1 Slew Rate Definitions for Differential Input Signals (CK)

[Table 8] Differential Input Slew Rate Definition

Description	from	to	Defined by
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			
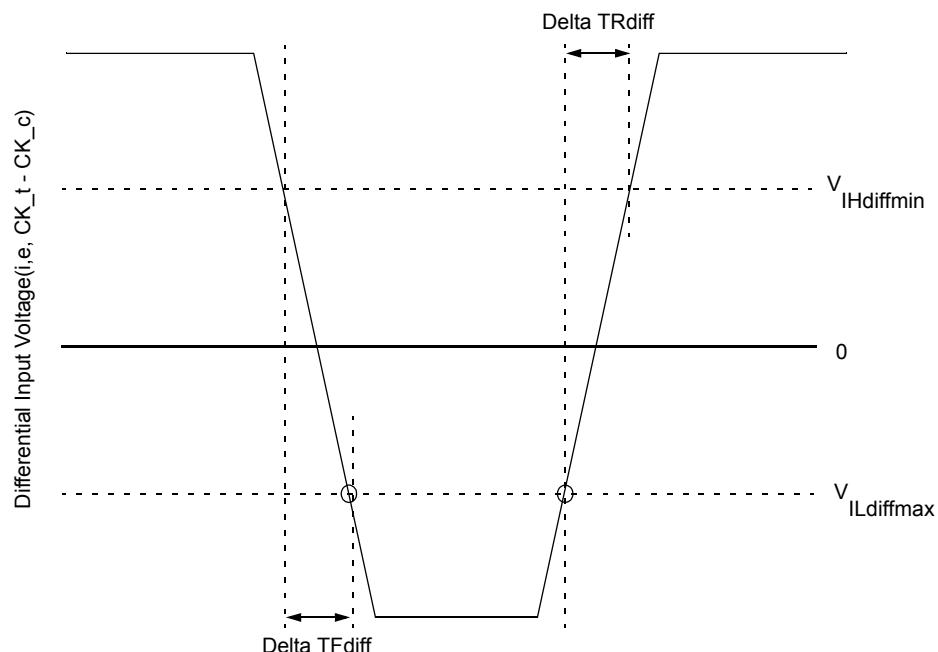
Figure 4. Differential Input Slew Rate Definition for CK_t, CK_c

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12.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 9. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.
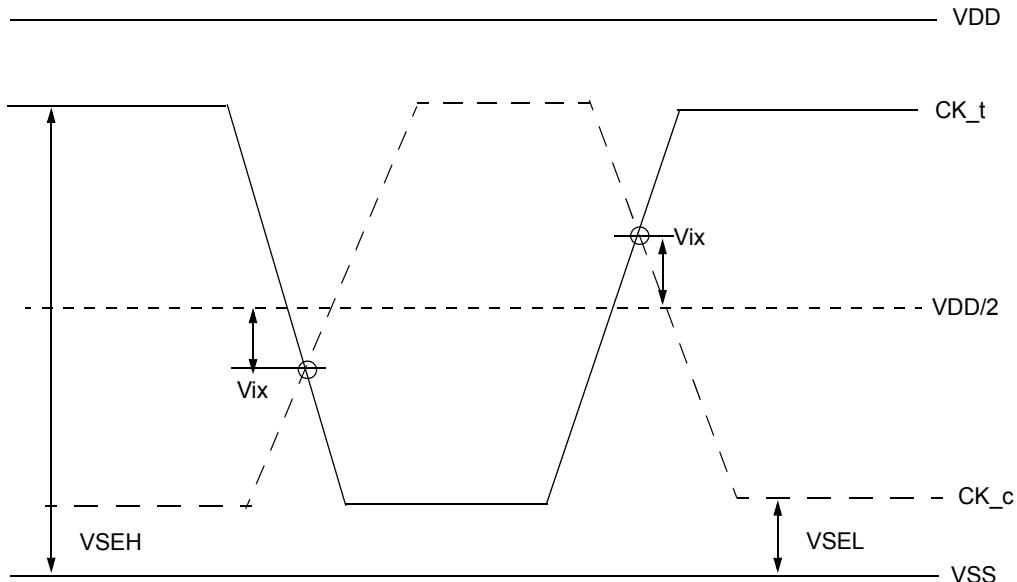
Figure 5. Vix Definition (CK)

[Table 9] Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	VSEL =< VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV =< VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

12.6 Single-ended AC & DC Output Levels

[Table 10] Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133	Units	NOTE
$V_{OH}(DC)$	DC output high measurement level (for IV curve linearity)	$1.1 \times V_{DDQ}$	V	
$V_{OM}(DC)$	DC output mid measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
$V_{OL}(DC)$	DC output low measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
$V_{OH}(AC)$	AC output high measurement level (for output SR)	$(0.7 + 0.15) \times V_{DDQ}$	V	1
$V_{OL}(AC)$	AC output low measurement level (for output SR)	$(0.7 - 0.15) \times V_{DDQ}$	V	1

NOTE :
1. The swing of $\pm 0.15 \times V_{DDQ}$ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$.

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12.7 Differential AC & DC Output Levels

[Table 11] Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133	Units	NOTE
$V_{OHdiff}(AC)$	AC differential output high measurement level (for output SR)	$+0.3 \times V_{DDQ}$	V	1
$V_{OLdiff}(AC)$	AC differential output low measurement level (for output SR)	$-0.3 \times V_{DDQ}$	V	1

NOTE :
1. The swing of $\pm 0.3 \times V_{DDQ}$ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to $V_{TT} = V_{DDQ}$ at each of the differential outputs.

12.8 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 12 and Figure 6.

[Table 12] Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	$V_{OL}(AC)$	$V_{OH}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TRse
Single ended output slew rate for falling edge	$V_{OH}(AC)$	$V_{OL}(AC)$	$[V_{OH}(AC)-V_{OL}(AC)]$ / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.
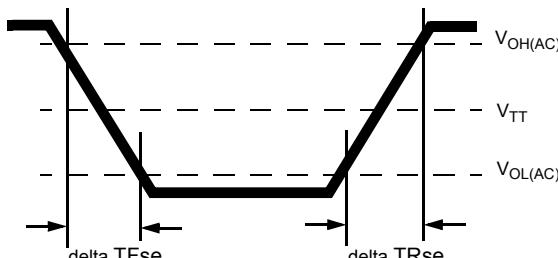
Figure 6. Single-ended Output Slew Rate Definition

[Table 13] Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		Units
		Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE :
1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

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12.9 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 14 and Figure 7.

[Table 14] Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	V_{OLdiff}(AC)	V_{OHdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TRdiff
Differential output slew rate for falling edge	V_{OHdiff}(AC)	V_{OLdiff}(AC)	[V_{OHdiff}(AC)-V_{OLdiff}(AC)] / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.
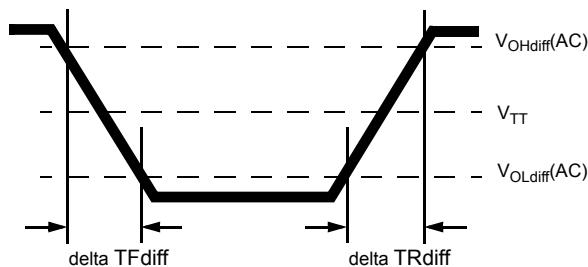
Figure 7. Differential Output Slew Rate Definition

[Table 15] Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		Units
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

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12.10 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 16] Single-ended AC & DC output levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE :
1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.
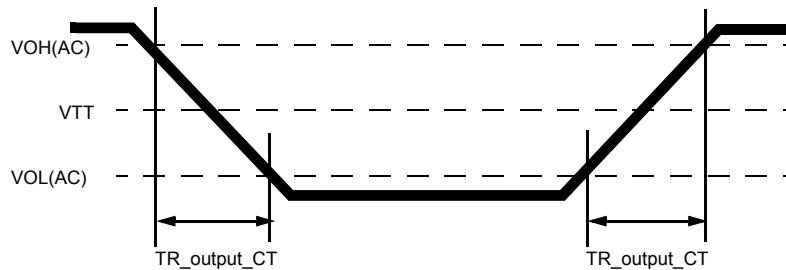
Figure 8. Output Slew Rate Definition of Connectivity Test Mode

[Table 17] Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

12.11 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 7.
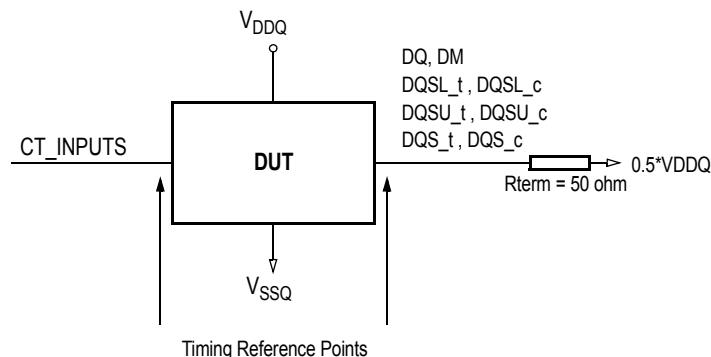
Figure 9. Connectivity Test Mode Timing Reference Load

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13. DIMM IDD specification definition

[Table 18] Basic IDD, IPP and IDDQ Measurement Conditions

| Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Logical Rank Activity:** Cycling with one logical rank active at a time; **Output Buffer and RTT:** Enabled in Mode **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Logical Rank Activity:** Cycling with one logical rank active at a time; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD2NA	**Precharge Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according ; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

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Symbol	Description
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:**Refer to Component Datasheet for detail pattern
IDD3NA	**Active Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless read data burst with different data between one burst and the next one according ; **DM_n**: stable at 1; **Bank Activity:** all banks of all logical ranks open, RD commands cycling through banks: 0,0,1,1,2,2,... and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4RA	**Operating Burst Read Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless write data burst with different data between one burst and the next one ; **DM_n**: stable at 1; **Bank Activity:** all banks open of all logical ranks, WR commands cycling through banks: 0,0,1,1,2,2,... and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at <u>HIGH</u>; **Pattern Details:** Refer to Component Datasheet for detail pattern
IDD4WA	**Operating Burst Write Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B1	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC_dlr between REF command to REF command; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP5B1	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5B2	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC_slr between REF command to REF command ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP5B2	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B2**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B1
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**

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Symbol	Description
IDD5F3	**Burst Refresh Current (2X REF)** tRFC=tRFC_x2, **Other conditions:** see IDD5B2
IPP5F3	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F3**
IDD5F4	**Burst Refresh Current (4X REF)** tRFC=tRFC_x4, **Other conditions:** see IDD5B1
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD5F5	**Burst Refresh Current (4X REF)** tRFC=tRFC_x4, **Other conditions:** see IDD5B2
IPP5F5	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F5**
IDD6N	**Self Refresh Current: Normal Temperature Range** T_{CASE}: 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL:** Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) T_{CASE}: 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL:** Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** T_{CASE}: 0 - TBD (~35-45)°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL:** Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** T_{CASE}: 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4]; **Partial Array Self-Refresh (PASR):** Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL:** Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** Refer to Component Datasheet for detail pattern; **BL:** 8[1]; **AL:** CL-2; **CS_n:** High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE :
1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]

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3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
              010] : 1866MT/s, 2133MT/s
              011] : 2400MT/s
 Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
 DLL disabled : set MR1 [A0 = 0]
 CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
             010] : 2400MT/s
 Read DBI enabled : set MR5 [A12 = 1]
 Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
                     01] : Reduced Temperature range
                     10] : Extended Temperature range
                     11] : Auto Self Refresh
5. IDD2NG should be measured after sync pules(NOP) input.

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14. IDD Table

These values are based on measurement at 1.26V @ 85'C. The spec value will be available later.

[Table 19] I_{DD} and I_{DDQ} Values

Symbol	M393A8G40D40 : 64GB(8Gx72) Module DDR4-2133 17-15-15 1.2V		Unit	NOTE
	IDD Max.	IPP Max.		
I_{DD0}	2500	54	mA	
I_{DD0A}	2730	54	mA	
I_{DD1}	2620	54	mA	
I_{DD1A}	2850	54	mA	
I_{DD2N}	2200	47	mA	
I_{DD2NA}	2480	47	mA	
I_{DD2NT}	2280	47	mA	
I_{DD2NL}	2120	47	mA	
I_{DD2NG}	2210	47	mA	
I_{DD2ND}	2170	47	mA	
I_{DD2N_par}	2270	47	mA	
I_{DD2P}	920	47	mA	
I_{DD2Q}	2160	47	mA	
I_{DD3N}	2470	47	mA	
I_{DD3NA}	2710	47	mA	
I_{DD3P}	1160	47	mA	
I_{DD4R}	3820	47	mA	
I_{DD4RA}	4110	47	mA	
I_{DD4RB}	3870	47	mA	
I_{DD4W}	4100	47	mA	
I_{DD4WA}	4360	47	mA	
I_{DD4WB}	4110	47	mA	
I_{DD4WC}	3890	47	mA	
I_{DD4W_par}	4040	47	mA	
I_{DD5B1}	8260	666	mA	
I_{DD5F2}	7220	557	mA	
I_{DD5F4}	5680	396	mA	
I_{DD5B2}	4330	263	mA	
I_{DD5F3}	3950	224	mA	
I_{DD5F5}	3500	175	mA	
I_{DD6N}	850	101	mA	
I_{DD6E}	1460	159	mA	
I_{DD6R}	540	69	mA	
I_{DD6A}	1460	159	mA	
I_{DD7}	5540	166	mA	
I_{DD8}	230	40	mA	

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[Table 20] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

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15. Input/Output Capacitance

[Table 21] Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		Unit	NOTE
		min	max		
C_{IO}	Input/output capacitance	0.55	1.6	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	pF	1,3,4
C_I	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	2.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.5	pF	1,3,12
C_{TEN}	Input capacitance of TEN	0.2	2.3	pF	1,3,13

NOTE:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.

2. DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS

3. This parameter applies to 3DS devices. It is meant to represent the silicon pad capacity of the master die.

4. Absolute value CK_T-CK_C

5. Absolute value of CIO(DQS_T)-CIO(DQS_C)

6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

7. CDI CTRL applies to ODT, CS_n and CKE

8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))

9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))

11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))

12. Maximum external load capacitance on ZQ pin: tbd pF.

13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case C_{TEN} might not be valid and system shall verify TEN signal with Vendor specific information.

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16. Electrical Characterisitics and AC timing

16.1 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding bin

[Table 22] DDR4-1600 Speed Bins and Operations

Speed Bin		DDR4-1600		Unit	NOTE
CL-nRCD-nRP		**13-12-11**		Unit	NOTE
Parameter	**Symbol**	**min**	**max**		
Internal read command to first data	tAA	16.25	21.00	ns	
ACT to internal read or write delay time	tRCD	15	-	ns	
PRE command period	tRP	13.75	-	ns	
ACT to PRE command period	tRAS	35	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	48.75	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings		13,14		nCK	
Supported nRCD Timings minimum		10		nCK	
Supported nRP Timings minimum		10		nCK	
Supported CWL Settings		9,11		nCK	
Supported AL Settings		10,11		nCK	12

[Table 23] DDR4-1866 Speed Bins and Operations

Speed Bin		DDR4-1866		Unit	NOTE
CL-nRCD-nRP		**15-14-13**		Unit	NOTE
Parameter	**Symbol**	**min**	**max**		
Internal read command to first data	tAA	16.07	21.00	ns	
ACT to internal read or write delay time	tRCD	15.00	-	ns	
PRE command period	tRP	13.92 (13.75[11])	-	ns	
ACT to PRE command period	tRAS	34	9 x tREFI	ns	
ACT to ACT or REF command period	tRC	47.92	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved	ns	1.2.3.4.6
	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 14	tCK(AVG)	Reserved	ns	1,2,3,4
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings		13,14,15,16		nCK	
Supported nRCD Timings minimum		10		nCK	
Supported nRP Timings minimum		10		nCK	
Supported CWL Settings		9,10,11,12		nCK	
Supported AL Settings		10,11,12,13		nCK	12

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[Table 24] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE
CL-nRCD-nRP			17-15-15		Unit	NOTE
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15.94	21.00	ns	
ACT to internal read or write delay time		tRCD	14.06	-	ns	
PRE command period		tRP	14.06 (13.75[11])	-	ns	
ACT to PRE command period		tRAS	33	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.06	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
CWL = 9,11	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
CWL = 10,12	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4
CWL = 11,14	CL = 17	tCK(AVG)	0.937	1.071	ns	1,2,3,4
CWL = 11,14	CL = 18	tCK(AVG)	0.937	1.071	ns	1,2,3,4
CWL = 11,14	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,7
Supported CL Settings			13,14,15,16,17,18,20		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12,14		nCK	
Supported AL Settings			11,12,13,14,15		nCK	12

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16.2 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-3DS-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.937 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-3DS-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-3DS-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. 13.75ns is minimum tRCD when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25ns
9. 13.92ns is minimum tRCD when operating by DDR4-1600L-3DS2B at tCK(AVG).min=1.071ns
10. 12.85ns is minimum tRCD when operating by DDR4-1866L-3DS2B at tCK(AVG).min=1.071ns
11. 13.75ns is minimum tRP when operating by DDR4-1600K-3DS2B at tCK(AVG). min=1.25ns
12. Not all CL settings support the listed AL settings for each speed bin. The AL settings are supported only for those CL settings where AL=CL-2 or AL=CL-3. For example, in DDR4-1866-3DSB, AL=12 is only supported for CL=14 and 15, and AL=13 is only supported for CL=15 and 16.18. DDR4-2133R-3DS4A and DDR4-2400U-3DS4A devices may optionally support tAAmin=17.14 ns or lower. SPD settings must be programmed to match. For example, DDR4-2133R-3DS4A devices capable of running with CAS Latency of 16 at average cycle times of 1.071 ns or larger must program 17.14 ns in SPD byes for tAAmin.

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17. Timing Parameters by Speed Grade

[Table 25] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.938	<1.071	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_-tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_-tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	125		107		94		ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	63		54		47		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	100		86		75		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	$^tERR(nper)min = ((1 + 0.68ln(n)) * ^tJIT(per)\_total\ min)$ $^tERR(nper)max = ((1 + 0.68ln(n)) * ^tJIT(per)\_total\ max)$						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.355 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(\1K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)		nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)		Max(4nCK,4.2ns)		Max(4nCK,3.7ns)			
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)		Max(4nCK,6.4ns)		Max(4nCK,6.4ns)			34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)			34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)		Max(4nCK,5.3ns)		Max(4nCK,5.3ns)			34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)			34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)			34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)			34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max(4nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	tWR+max(5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max(4nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	tWTR_S+max(5nCK,3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max(4nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	tWTR_L+max(5nCK,3.75ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + pre-charge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	tCK(avg)/2	13,18
DQ output hold time from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	tCK(avg)/2	13,17,18
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.63		0.63		0.64		UI	16,17,18
Data Valid Window per device, per pin: tQH - tDQSQ each device's output	tDVWp	0.66		0.66		0.69		UI	16,17,18
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	tCK	40
		NA	NA	NA	NA	NA	NA	tCK	41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential WRITE Pre-amble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
		NA	NA	NA	NA	NA	NA	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	0.33	TBD	0.33	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing locatino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	ps	37,38,39
DQS_t, DQS_c rising edge output vari-ance window per DRAM	tDQSCKI (DLL On)		370		330		310	ps	37,38,39
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)			
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)		tXS(min)		tXS(min)			
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)			
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid com-mand	tXPR	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min)+ 10ns)	-		
Exit Self Refresh to commands not requir-ing a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		
Valid Clock Requirement after Self Re-fresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Re-fresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Re-fresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing									

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4		4		4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	nCK	
Parity Latency	PL	4		4		4		nCK	
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
tREFI									

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Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34

[Table 26] Minimum Read and Write Command Timings for 4H devices

Logical Rank	Bank Group	Timing Parameter	DDR4-1600	DDR4-1866	DDR4-2133	Units	Note
Same	Same	Minimum Read to Read	5	5	6	nCK	1
		Minimum Write to Write					
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE				1,2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_L				1,3
	different	Minimum Read to Read	4	4	4	nCK	1
		Minimum Write to Write					
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE				1,2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_S				1,3
different	Same	Minimum Read to Read	4	4	5(4) (optional)	nCK	1
		Minimum Write to Write					
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE				1,2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_S				1,3
	different	Minimum Read to Read	4	4	5(4) (optional)	nCK	1
		Minimum Write to Write					
		Minimum Read to Write	CL - CWL + RBL / 2 + 1 tCK + tWPRE				1,2
		Minimum Read after Write	CWL + WBL / 2 + tWTR_S				1,3

Note:
1. These timings require extended calibrations times tZQinit and tZQCS (values TBD).
2. RBL : Read burst length associated with Read command
   RBL = 8 for fixed 8 and on-the-fly mode 8
   RBL = 4 for fixed BC4 and on-the-fly mode BC4
3. WBL : Write burst length associated with Write command
   WBL = 8 for fixed 8 and on-the-fly mode 8 or BC4
   WBL = 4 for fixed BC4 only

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[Table 27] Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density			Units	Note
			4Gb	8Gb	16Gb		
REF command to ACT or REF command time to same logical rank	tRFC_slr1 (1X mode)		260	350	TBD1	ns	
	tRFC_slr2 (2X mode)		160	260	TBD2	ns	
	tRFC_slr4 (4X mode)		110	160	TBD3	ns	
REF command to REF command to different logi-cal rank	tRFC_dlr1 (1X mode)		90	120	TBD1/3	ns	
	tRFC_dlr2 (2X mode)		55	90	TBD2/3	ns	
	tRFC_dlr4 (4X mode)		40	55	TBD3/3	ns	
Average periodic refresh interval in same logical rank	tREFI_slr1 (1X mode)	$0°C =< T_{CASE} =< 85°C$	7.8	7.8	TBD4	us	
		$85°C < T_{CASE} =< 95°C$	3.9	3.9	TBD4/2	us	
	tREFI_slr2 (2X mode)	$0°C =< T_{CASE} =< 85°C$	3.9	3.9	TBD4/2	us	
		$85°C < T_{CASE} =< 95°C$	1.95	1.95	TBD4/4	us	
	tREFI_slr4 (4X mode)	$0°C =< T_{CASE} =< 85°C$	1.95	1.95	TBD4/4	us	
		$85°C < T_{CASE} =< 95°C$	0.975	0.975	TBD4/8	us	

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NOTE :

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down
   IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in Device Operation.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM
39. Value is only valid for RZQ/7
40. 1tCK toggle mode with setting MR4:A11 to 0
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400 speed grade.
42. 1tCK mode with setting MR4:A12 to 0
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Device Operation.
   to Data Strobe Relationship". Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in See Device Operation Preamble".

45.DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.

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18. Physical Dimensions

18.1 4Gbx4(TSV) based 8Gx72 Module (8 Ranks) - M393A8G40D40

Units : Millimeters

Detail A

Detail B,E

Detail C

Detail D
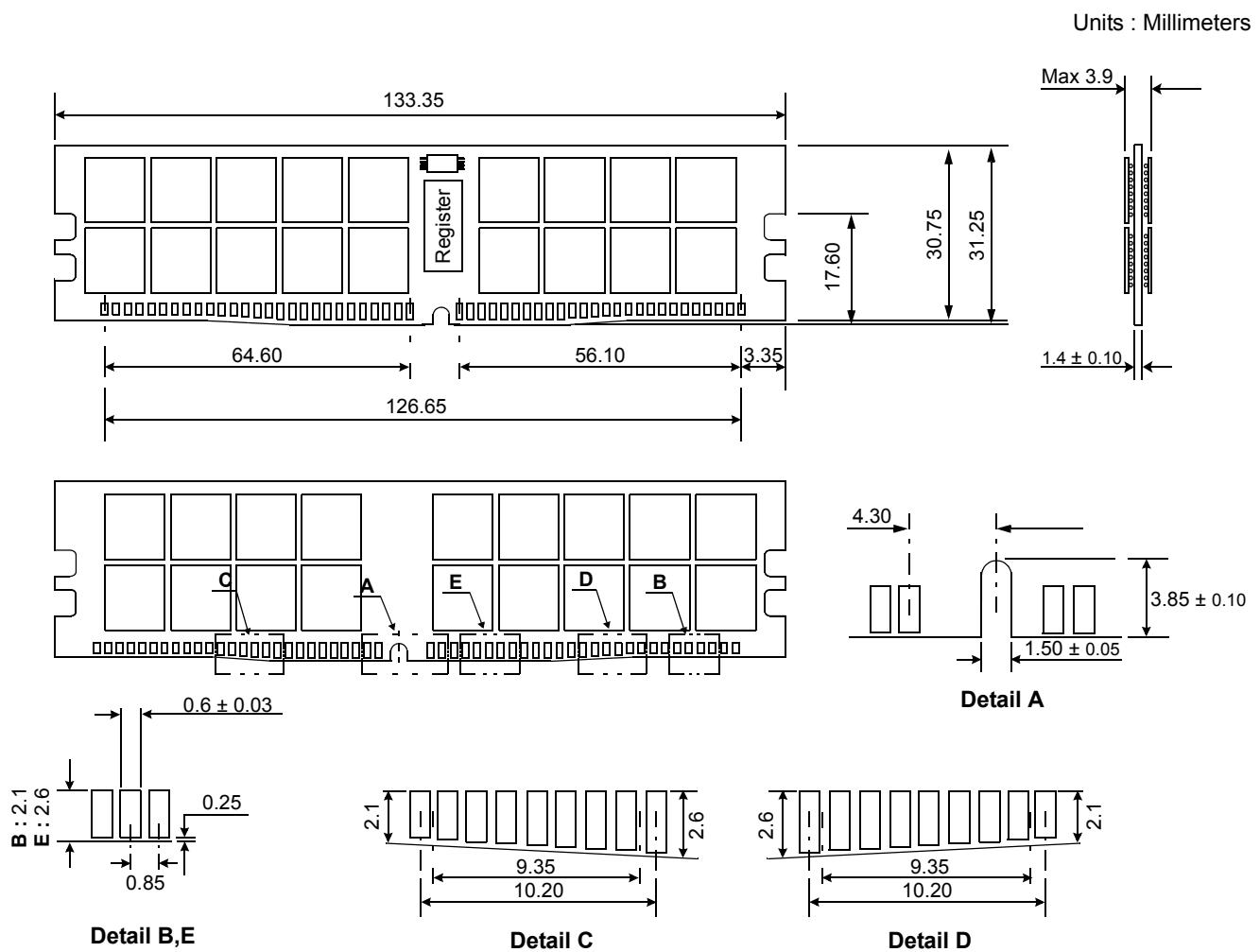
18.1.1 x72 DIMM, populated as Octal physical ranks of x4 DDR4 SDRAMs


——— Address, Command and Control lines
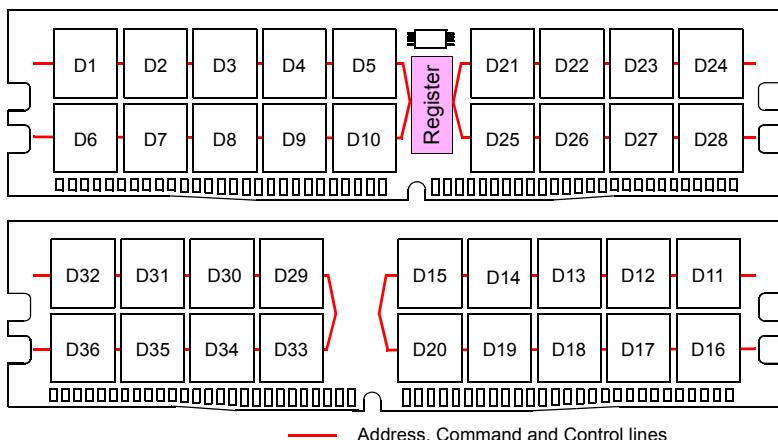
The used device is 4G x4(TSV) DDR4 SDRAM, FCFBGA.
DDR4 SDRAM Part NO : K4AAG045WD-4C**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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18.1.2 Heat Spreader Design Guide

1. FRONT PART

2. BACK PART
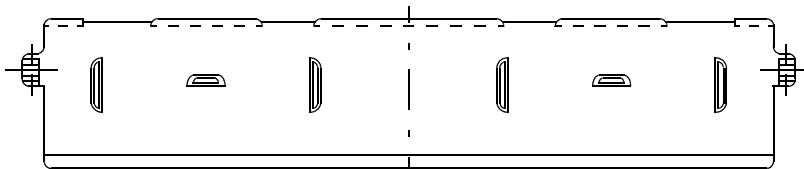
3. CLIP PART
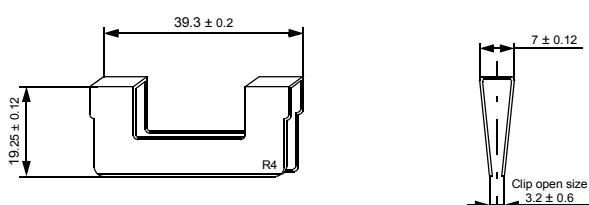
4. DDR4 RDIMM ASS'Y View

Reference thickness total (Maximum) : 7.30 (With Clip thickness)

H/S Assay

H/S, Clip Assay

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