288pin Registered DIMM based on 16Gb M-die

78FBGA with Lead-Free & Halogen-Free
(RoHS compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First version for target specification.	21st Sep, 2018	Target	T.Y.Lee J.Y.Bae
1.0	- Final datasheet. - Update IDD table 1. Update IDD and IPP values. 2. Remove symbol IDD5B2, IDD5F3, IDD5F5, IPP5B2, IPP5F3 and IPP5F5. - Update speed bins table. - Add Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns table. - Update Basic IDD, IPP and IDDQ Measurement Conditions table. 1. Correct typo. 2. Remove IDD4RB/IDDQ4RB/IDD4WB. 3. Add IDD5B2/IPP5B2/IDD5F3/IPP5F3/IDD5F5/IPP5F5 parameters. - Update DDR4-2933 Speed Bins and Operations table. - Correct CAS latency in Key features.	21st Feb, 2019	Final	T.Y.Lee J.Y.Bae

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1. DDR4 REGISTERED DIMM ORDERING INFORMATION

[Table 1] Ordering Information Table

Part Number	Density	Organization	Component Composition	Number of Rank	Height
M393ABG40M5B-CYF	256GB	32Gx72	3DS 4H 16Gx4 (K4ACG045WM-5C##)*36	8 (2 physical ranks / 4 logical ranks)	31.25mm

NOTE :
1) "##" - YF
2) YF(2933Mbps 24-21-21)
- Backward compatible to lower frequency.

2. KEY FEATURES

[Table 2] Speed bins

Speed	DDR4-2133	DDR4-2400	DDR4-2666	DDR-2933	Unit
	17-15-15	19-17-17	22-19-19	24-21-21	
tCK	0.937	0.833	0.750	0.682	ns
CAS Latency	17	19	22	24	nCK
tRCD	14.06	14.16	14.25	14.32	ns
tRP	14.06	14.16	14.25	14.32	ns
tRAS	33	32	32	32	ns
tRC	47.06	46.16	46.25	46.32	ns

- JEDEC standard 1.2V ± 0.06V Power Supply
- V_{DDQ} = 1.2V ± 0.06V
- 800 MHz f_{CK} for 1600Mb/sec/pin,933 MHz f_{CK} for 1866Mb/sec/pin, 1067MHz f_{CK} for 2133Mb/sec/pin, 1200MHz f_{CK} for 2400Mb/sec/pin,1333MHz f_{CK} for 2666Mb/sec/pin, 1467MHz f_{CK} for 2933Mb/sec/pin.
- 16 Banks (4 Bank Groups)
- Programmable $\overline{CAS}$ Latency: 11,12,13,14,15,16,17,18,20,22,24,25
- Programmable Additive Latency (Posted $\overline{CAS}$): CL - 2 or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency (CWL) = 9,11 (DDR4-1600), 10,11,12 (DDR4-1866), 11,14 (DDR4-2133), 12,16 (DDR4-2400), 14,18 (DDR4-2666) and 16, 20 (DDR4-2933)
- Burst Length: 8, 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset

3. ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
16Gx4(64Gb 3DS 4H) based Module	A0-A17	A0-A9	BA0-BA1	A10/AP

4. REGISTERED DIMM PIN CONFIGURATIONS (FRONT SIDE/BACK SIDE)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

NOTE:

1) VPP is 2.5V DC

2) Pin 230 is defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pin 230 is defined as SAVE_n for NVDIMMs.

3) Pins 1 and 145 are defined as NC for UDIMMs, RDIMMs and LRDIMMs. Pins 1 and 145 are defined as 12V for Hybrid /NVDIMM

4) The 5th VPP is required on all modules. DIMMs.

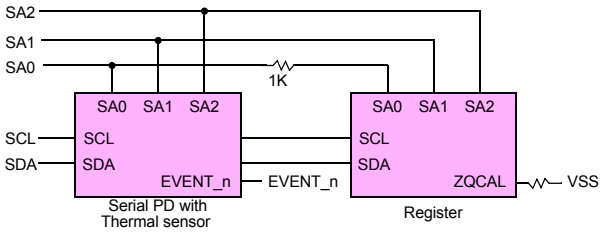
5. PIN DESCRIPTION

Pin Name	Description
A0-A17[1)]	Register address input
BA0, BA1	Register bank select input
BG0, BG1	Register bank group select input
RAS_n[2)]	Register row address strobe input
CAS_n[3)]	Register column address strobe input
WE_n[4)]	Register write enable input
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input
CKE0, CKE1	Register clock enable lines input
ODT0, ODT1	Register on-die termination control lines input
ACT_n	Register input for activate input
DQ0–DQ63	DIMM memory data bus
CB0–CB7	DIMM ECC check bits
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)
DQS0_c-DQS17_c	Data Buffer data strobes (negative line of differential pair)
CK0_t, CK1_t	Register clock input (positive line of differential pair)
CK0_c, CK1_c	Register clocks input (negative line of differential pair)

Pin Name	Description
SCL	I2C serial bus clock for SPD/TS and register
SDA	I2C serial bus data line for SPD/TS and register
SA0-SA2	I2C slave address select for SPD/TS and register
PAR	Register parity input
VDD	SDRAM core power supply
VPP	SDRAM activating power supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return (ground)
VDDSPD	Serial SPD/TS positive power supply
ALERT_n	Register ALERT_n output
RESET_n	Set Register and SDRAMs to a Known State
EVENT_n	SPD signals a thermal event has occurred
VTT	SDRAM I/O termination supply
RFU	Reserved for future use

NOTE :
1) Address A17 is only valid for 16 Gb x4 based SDRAMs.
2) RAS_n is a multiplexed function with A16.
3) CAS_n is a multiplexed function with A15.
4) WE_n is a multiplexed function with A14.

6. ON DIMM THERMAL SENSOR



NOTE :
1) All Samsung RDIMM support Thermal sensor on DIMM

[Table 3] Temperature Sensor Characteristics

Grade	Range	Temperature Sensor Accuracy			Units	NOTE
		Min.	Typ.	Max.		
B	75 < Ta < 95	-	+/- 0.5	+/- 1.0	°C	-
	40 < Ta < 125	-	+/- 1.0	+/- 2.0		-
	-20 < Ta < 125	-	+/- 2.0	+/- 3.0		-
Resolution		0.25			°C /LSB	-

7. INPUT/OUTPUT FUNCTIONAL DESCRIPTION

[Table 4] Input/Output Function Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0, C1, C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/ output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific data sheets to determine which DQ is used.

[Table 4] Input/Output Function Description

Symbol	Type	Function
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0 and C0-C2 (3DS devices). Command and address inputs shall have parity check performed when commands are latched via the rising edge of CK_t and when CS_n is low.
ALERT_n	Output/ Input	Alert : It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until on going DRAM internal recovery transaction is complete. During Connectivity Test mode this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present
VDDQ	Supply	DQ Power Supply: 1.2V +/- 0.06V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2V ± 0.06V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE:
1) Input only pins (BG0-BG1, BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT and RESET_n) do not supply termination.

8. REGISTERING CLOCK DRIVER SPECIFICATION

8.1 Timing & Capacitance values

Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		Units	Notes
			Min	Max	Min	Max	Min	Max		
fclock	Input Clock Frequency	application frequency	625	1080	625	1350	625	1620	MHz	
t_{CH}/t_{CL}	Pulse duration, CK_t, CK_c HIGH or LOW		0.4	-	0.4	-	0.4	-	t_{CK}	
t_{ACT}	Inputs active time4 before DRST_n is taken HIGH	DCKE0/1 = LOW and DCS0/1_n = HIGH	16	-	16	-	16	-	t_{CK}	
t_{PDM}	Propagation delay, single-bit switching, CK_t/ CK_c to output	1.2V Operation	1	1.3	1	1.3	1	1.3	ns	
t_{DIS}	output disable time	Rising edge of Yn_t to output float	0.5*tCK + tQSK1(min)	-	0.5*tCK + tQSK1(min)	-	0.5*tCK + tQSK1(min)	-	ps	
t_{EN}	output enable time	Output valid to rising edge of Yn_t	0.5*tCK - tQSK1(max)	-	0.5*tCK - tQSK1(max)	-	0.5*tCK - tQSK1(max)	-	ps	
C_I	Input capacitance, Data inputs		0.8	1.1	0.8	1.0	0.8	1.0	pF	1,2
C_{CK}	Input capacitance, CK_t, CK_c		0.8	1.1	0.8	1.0	0.8	1.0		1,2
C_{IR}	Input capacitance, DRST_n	$V_I=V_{DD}$ or V_{SS} ; V_{DD}=1.2V	0.5	2.0	0.5	2.0	0.5	2.0		

NOTE :
1) This parameter does not include package capacitance
2) Data inputs are DCKE0/1, DODT0/1, DA0..DA17, DBA0..DBA1, DBG0..DBG1, DACT_n, DC0..DC2, DPAR, DCS0/1_n

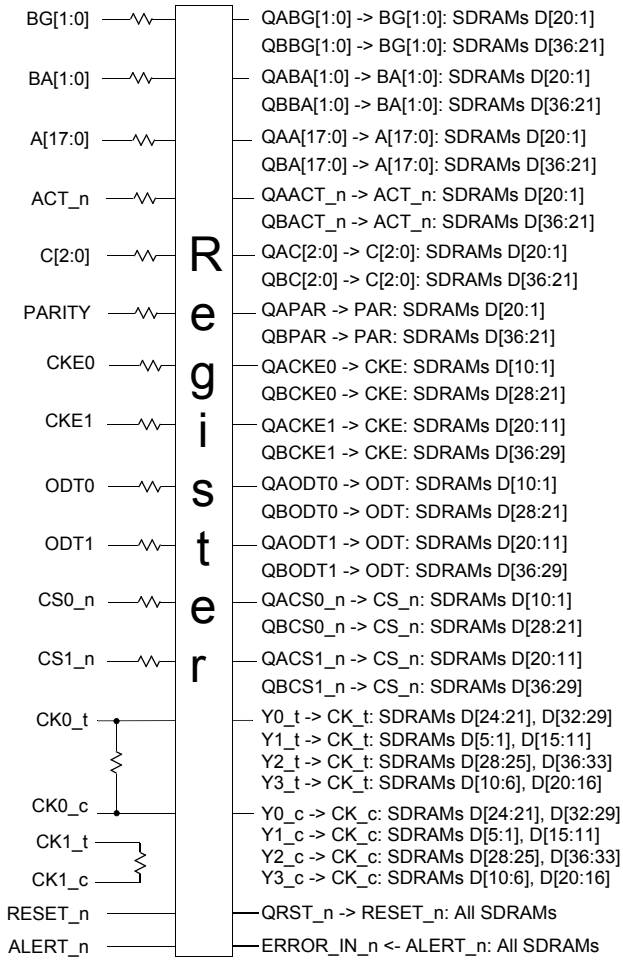
8.2 Clock driver Characteristics

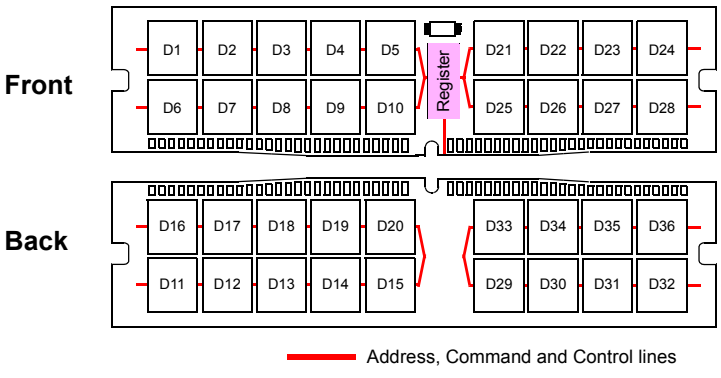
Symbol	Parameter	Conditions	DDR4-1600/1866/2133		DDR4-2400		DDR4-2666		DDR-2933		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{jit} (cc)	Cycle-to-cycle period jitter	CK_t/CK_c stable	0	0.025 x tCK	0	0.025 x tCK	0	0.025 x tCK	0	0.025 x tCK	ps
t_{STAB}	Stabilization time		-	5	-	5	-	5	-	5	us
t_{CKsk}	Clock Output skew		-	10	-	10	-	10	-	10	ps
t_{jit}(per)	Yn Clock Period jitter		-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	-0.025 * tCK	0.025 * tCK	ps
t_{jit}(hper)	Half period jitter		-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	-0.032 * tCK	0.032 * tCK	ps
t_{Qsk1}	Qn Output to clock tolerance		-0.125 * tCK	0.125 * tCK	-0.125 * tCK	0.125 * tCK	-0.1 * tCK	0.1 * tCK	-0.1 * tCK	0.1 * tCK	ps
t_{dynoff}	Maximum re-driven dynamic clock off-set		-	50	-	45	-	45	-	40	ps

9. FUNCTION BLOCK DIAGRAM:

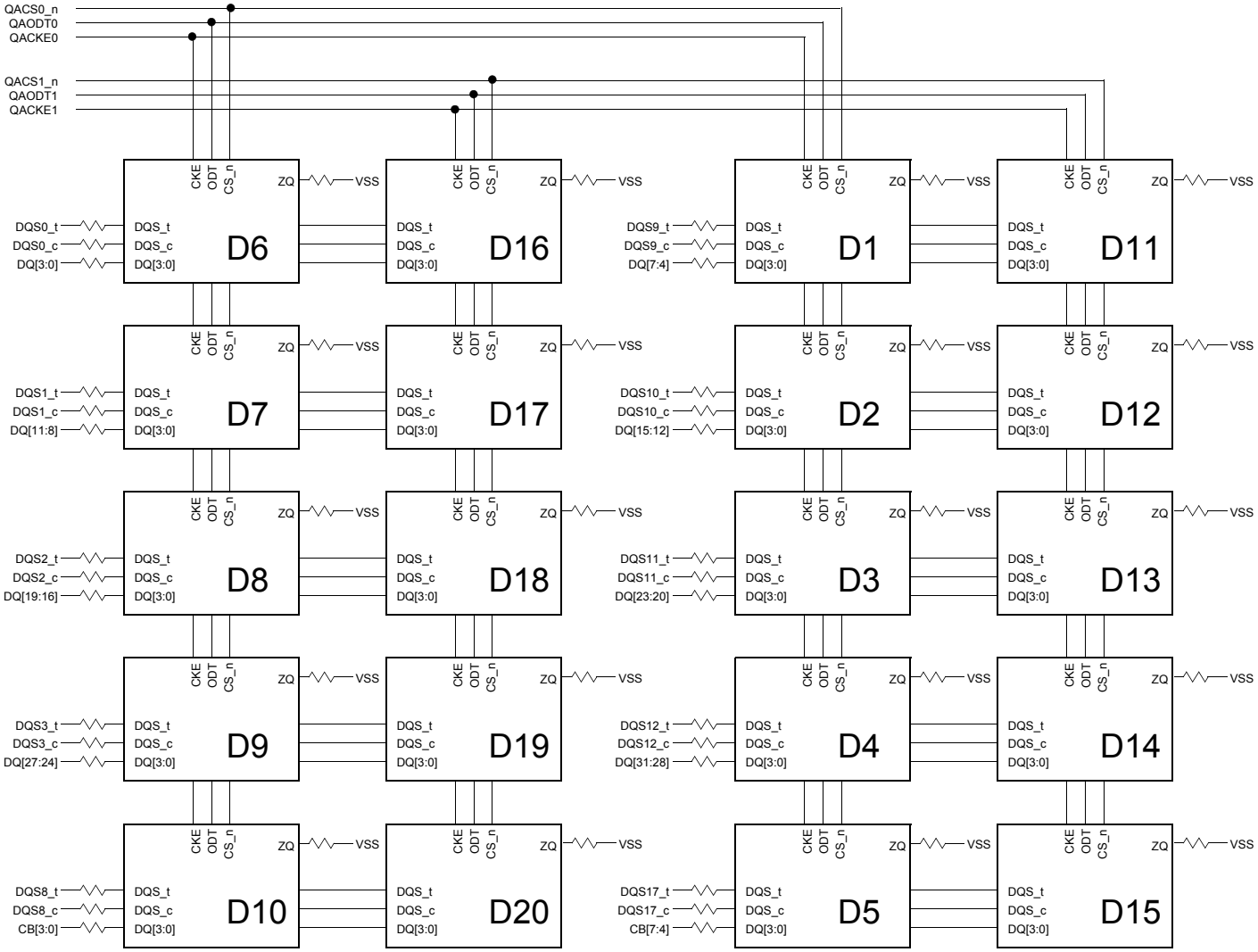
9.1 256GB, 32Gx72 Module

9.1.1 (PC4-RDIMM Populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAMs)

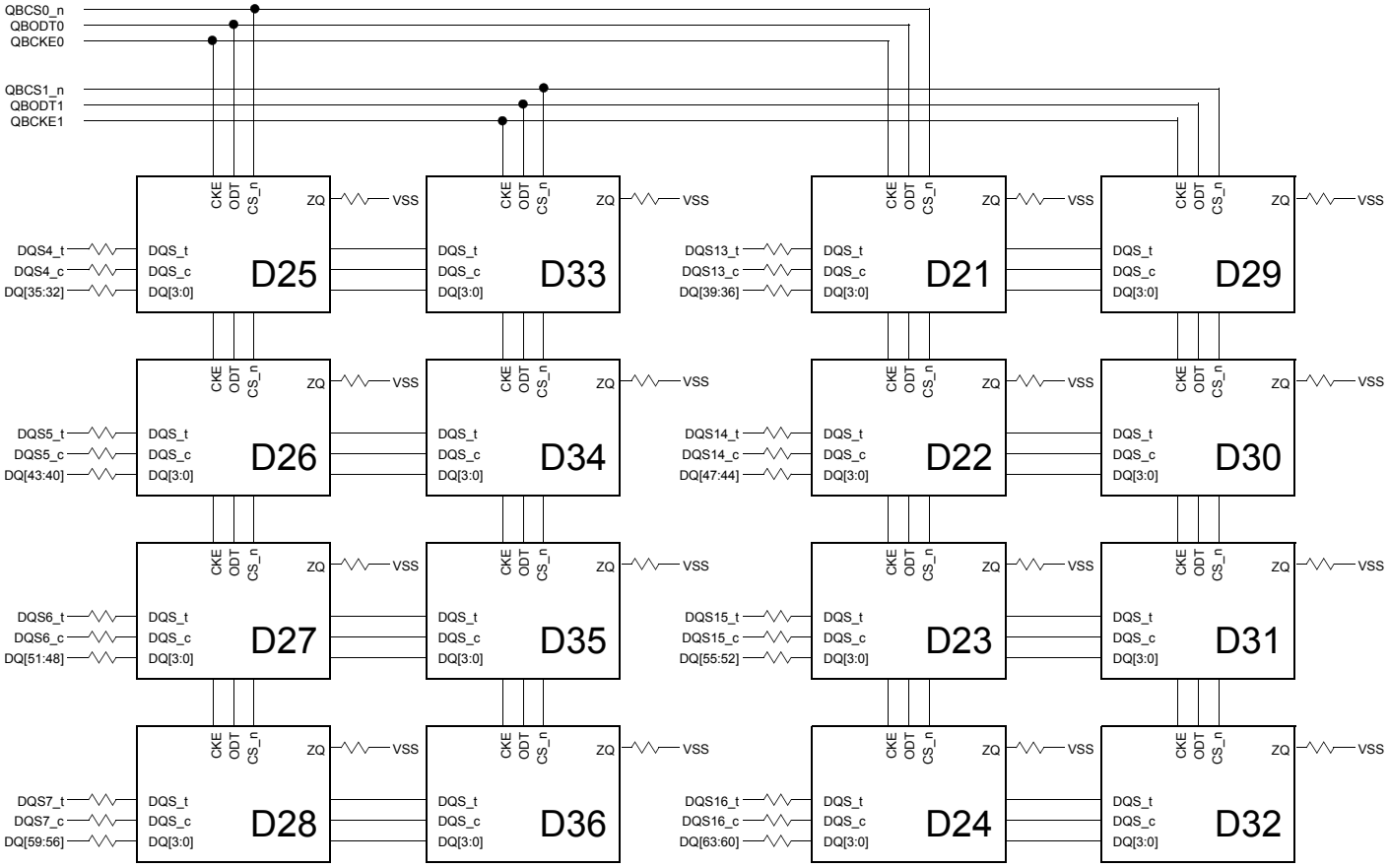


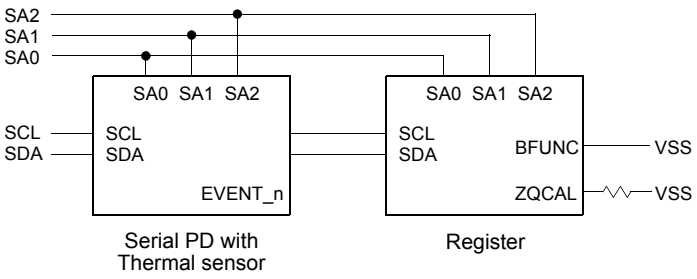


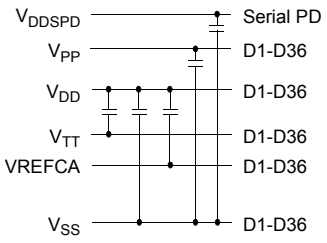
NOTE :
1) CK0_t, CK0_c terminated with 120Ω ± 5% resistor.
2) CK1_t, CK1_c terminated with 120Ω ± 5% resistor but not used.
3) Unless otherwise noted resistors are 22Ω ± 5%.



NOTE :
1) Unless otherwise noted, resistor values are 15Ω ± 5%.
2) See the Net Structure diagrams for all resistors associated with the command, address and Control bus.
3) ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.
4) DRAM TEN pin need to be tied to VSS.







NOTE :

1) Unless otherwise noted, resistor values are 15Ω ± 5%.
2) See the Net Structure diagrams for all resistors associated with the command, address and control bus.
3) ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.
4) DRAM TEN pin need to be tied to VSS.

10. ABSOLUTE MAXIMUM RATINGS

[Table 5] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	1,3,5
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE :

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) VDD and VDDQ must be within 300mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREFCA may be equal to or less than 300mV
4) VPP must be equal or greater than VDD/VDDQ at all times.
5) Overshoot area above 1.5 V is specified in 12.3.4, 12.3.5Clock Overshoot and Undershoot Specifications and 12.3.6.

11. AC & DC OPERATING CONDITIONS

[Table 6] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP	Peak-to-Peak Voltage	2.375	2.5	2.75	V	3

NOTE :

1) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3) DC bandwidth is limited to 20MHz.

12. AC & DC INPUT MEASUREMENT LEVELS

12.1 AC & DC Logic Input Levels for Single-Ended Signals

[Table 7] Single-ended AC & DC Input Levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933		Unit	NOTE
		Min.	Max.	Min.	Max.		
VIH.CA(DC75)	DC input logic high	V_{REFCA}+ 0.075	VDD	-	-	V	
VIH.CA(DC65)		-	-	V_{REFCA}+ 0.065	VDD		
VIL.CA(DC75)	DC input logic low	VSS	V_{REFCA}-0.075	-	-	V	
VIL.CA(DC65)		-	-	VSS	V_{REFCA}-0.065		
VIH.CA(AC100)	AC input logic high	V_{REF} + 0.1	Note 2	-	-	V	
VIH.CA(AC90)		-	-	V_{REF} + 0.09	Note 2		1
VIL.CA(AC100)	AC input logic low	Note 2	V_{REF} - 0.1	-	-	V	
VIL.CA(AC90)		-	-	Note 2	V_{REF} - 0.09		1
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2,3

NOTE :
1) See “Overshoot and Undershoot Specifications” on section12.3AC and DC Logic Input Levels for Differential Signals.
2) The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV)
3) For reference : approx. VDD/2 ± 12mV.

12.2 AC and DC Input Measurement Levels: V_{REF} Tolerances.

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA}).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table 7. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

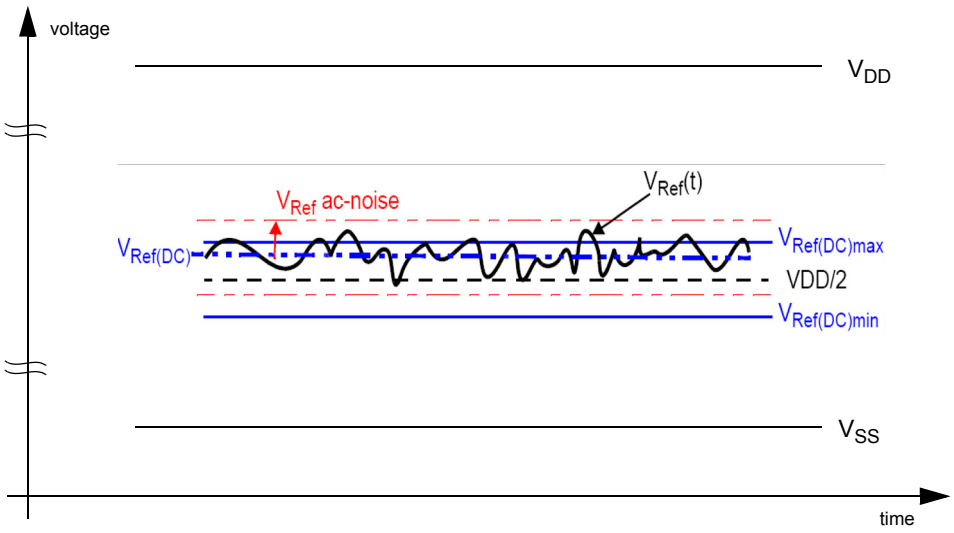


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

12.3 AC and DC Logic Input Levels for Differential Signals

12.3.1 Differential Signals Definition

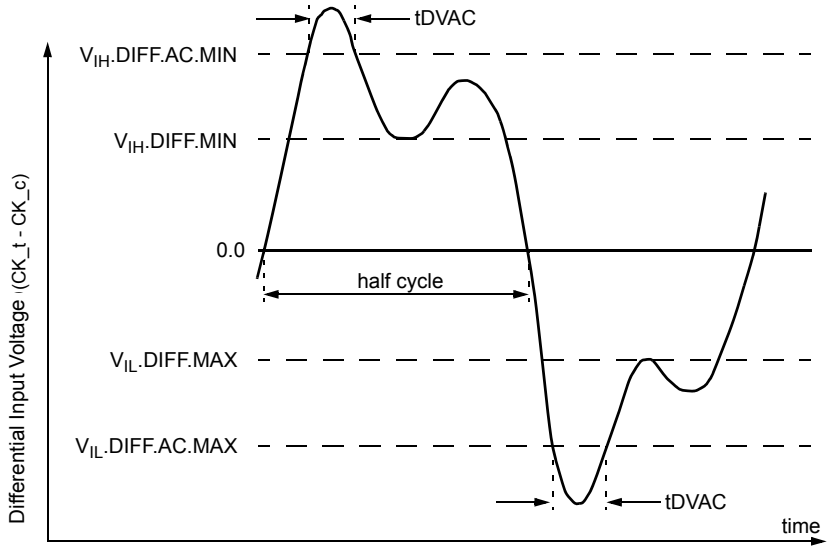


Figure 2. Definition of differential ac-swing and "time above ac-level" t_{DVAC}

NOTE:
1) Differential signal rising edge from VIL.DIFF.MAX to VIH.DIFF.MIN must be monotonic slope.
2) Differential signal falling edge from VIH.DIFF.MIN to VIL.DIFF.MAX must be monotonic slope.

12.3.2 Differential Swing Requirements for Clock (CK_t - CK_c)

[Table 8] Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600/1866/2133		DDR4 -2400/2666		DDR4-2933		unit	NOTE
		min	max	min	max	min	max		
V_{IHdiff}	differential input high	+0.150	NOTE 3	+0.135	NOTE 3	+0.125	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	-0.150	NOTE 3	-0.135	NOTE 3	-0.125	V	1
V_{IHdiff}(AC)	differential input high ac	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	2 x (V_{IH}(AC) - V_{REF})	NOTE 3	V	2
V_{ILdiff}(AC)	differential input low ac	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	NOTE 3	2 x (V_{IL}(AC) - V_{REF})	V	2

NOTE :
1) Used to define a differential signal slew-rate.
2) for CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD and V_{REFCA};
3) These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

[Table 9] Allowed Time Before Ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ |$V_{IH/Ldiff}$(AC)| = 200mV	
	min	max
> 4.0	120	-
4.0	115	-
3.0	110	-
2.0	105	-
1.8	100	-
1.6	95	-
1.4	90	-
1.2	85	-
1.0	80	-
< 1.0	80	-

12.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH.CA(AC) / VIL.CA(AC)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC100)/VIL.CA(AC100) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c.

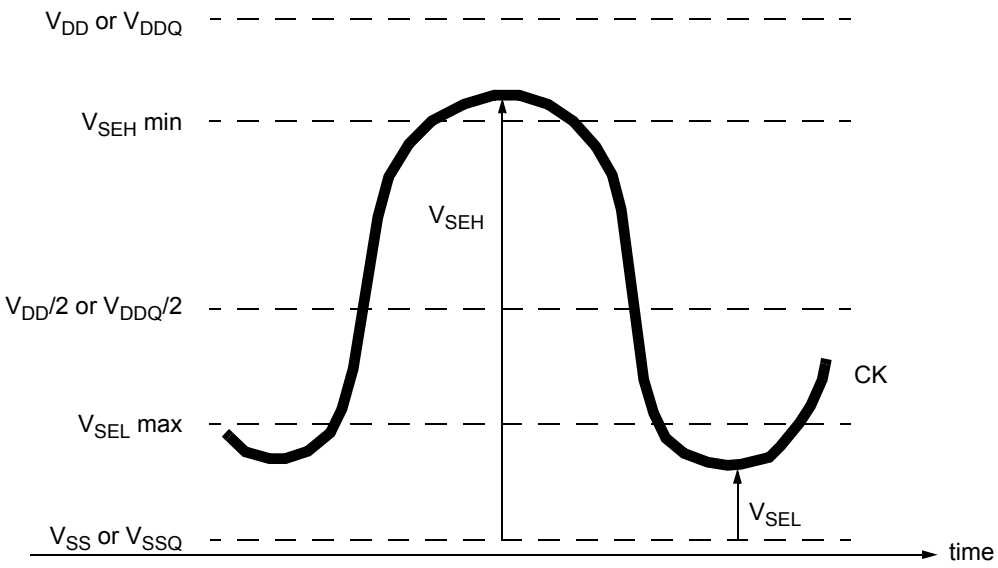


Figure 3. Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

[Table 10] Single-ended Levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t, CK_c	(VDD/2)+0.100	NOTE3	(VDD/2)+0.95	NOTE3	(VDD/2)+0.85	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t, CK_c	NOTE3	(VDD/2)-0.100	NOTE3	(VDD/2)-0.95	NOTE3	(VDD/2)-0.85	V	1, 2

NOTE :

1) For CK_t - CK_c use $V_{IH.CA}$/$V_{IL.CA}$(AC) of ADD/CMD;

2) V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};

3) These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits ($V_{IH.CA}$(DC) max, $V_{IL.CA}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

12.3.4 Address, Command and Control Overshoot and Undershoot specifications

[Table 11] AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Symbol	Specification						Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933		
Maximum peak amplitude above VAOS	VAOSP	0.06						V	
Upper boundary of overshoot area AAOS1	VAOS	VDD +0.24						V	1
Maximum peak amplitude allowed for undershoot	VAUS	0.30						V	
Maximum overshoot area per 1 tCK above VAOS	AAOS2	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	V-ns	
Maximum overshoot area per 1 tCK between VDD and VAOS	AAOS1	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	V-ns	
Maximum undershoot area per 1 tCK below VSS	AAUS	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	V-ns	
(A0-A13,A17,BG0-BG1,BA0-BA1,ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)									

NOTE :

1) The value of VAOS matches VDD absolute max as defined in Table 5 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 6 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VAOS remains at VDD absolute max as defined in Table 5.

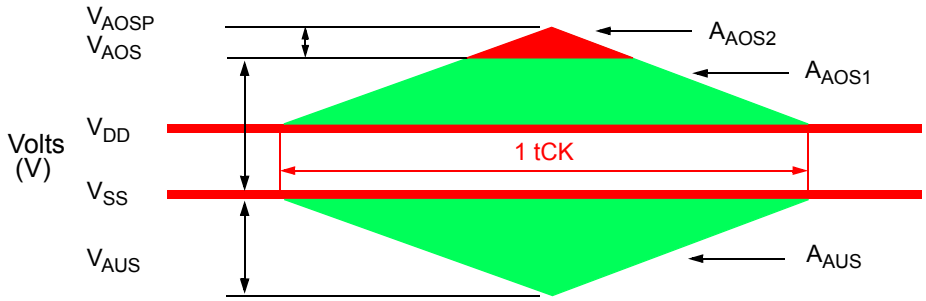


Figure 4. Address, Command and Control Overshoot and Undershoot Definition

12.3.5 Clock Overshoot and Undershoot Specifications

[Table 12] AC overshoot/undershoot specification for Clock

Parameter	Symbol	Specification						Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933		
Maximum peak amplitude above VCOS	VCOSP	0.06						V	
Upper boundary of overshoot area ADOS1	VCOS	VDD +0.24						V	1
Maximum peak amplitude allowed for undershoot	VCUS	0.30						V	
Maximum overshoot area per 1 UI above VCOS	ACOS2	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	V-ns	
Maximum overshoot area per 1 UI between VDD and VDOS	ACOS1	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	V-ns	
Maximum undershoot area per 1 UI below VSS	ACUS	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	V-ns	
(CK_t, CK_c)									

NOTE :
1) The value of VCOS matches VDD absolute max as defined in Table 5 Absolute Maximum DC Ratings if VDD equals VDD max as defined in Table 6 Recommended DC Operating Conditions. If VDD is above the recommended operating conditions, VCOS remains at VDD absolute max as defined in Table 5.

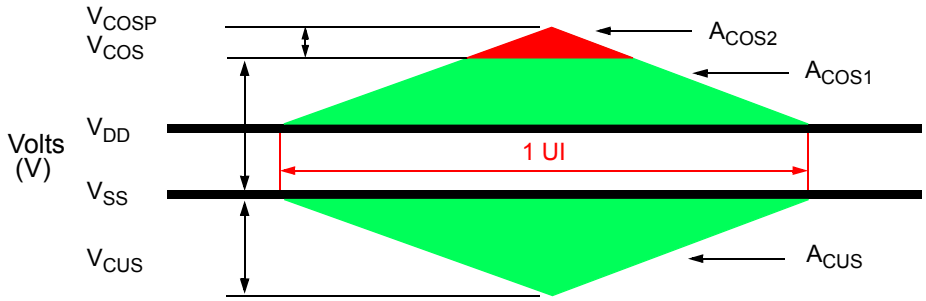


Figure 5. Clock Overshoot and Undershoot Definition

12.3.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

[Table 13] AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Symbol	Specification						Unit	NOTE
		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933		
Maximum peak amplitude above VDOS	VDOSP	0.16						V	
Upper boundary of overshoot area ADOS1	VDOS	VDDQ + 0.24						V	1
Lower boundary of undershoot area ADUS1	VDUS	0.30						V	2
Maximum peak amplitude below VDUS	VDUSP	0.10	0.10	0.10	0.10	0.10	0.10	V	
Maximum overshoot area per 1 UI above VDOS	ADOS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	V-ns	
Maximum overshoot area per 1 UI between VDDQ and VDOS	ADOS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI between VSSQ and VDUS1	ADUS1	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	V-ns	
Maximum undershoot area per 1 UI below VDUS	ADUS2	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	V-ns	

NOTE :
1) The value of VDOS matches (VIN, VOUT) max as defined in Table 5 Absolute Maximum DC Ratings if VDDQ equals VDDQ max as defined in Table 6 Recommended DC Operating Conditions. If VDDQ is above the recommended operating conditions, VDOS remains at (VIN, VOUT) max as defined in Table 5.
2) The value of VDUS matches (VIN, VOUT) min as defined in Table 5 Absolute Maximum DC Ratings

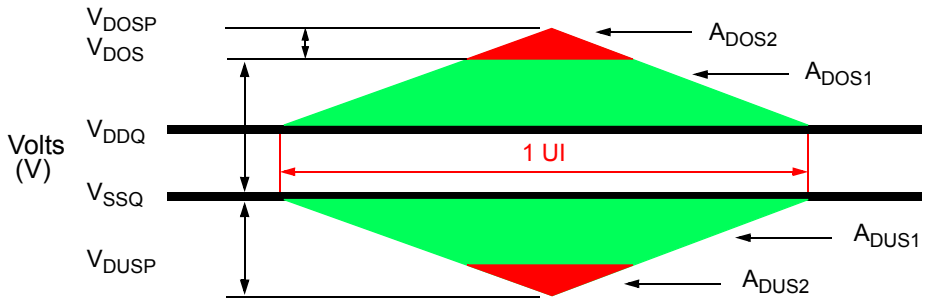


Figure 6. Data, Strobe and Mask Overshoot and Undershoot Definition

12.4 Slew Rate Definitions

12.4.1 Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 14 and Figure 7.

[Table 14] Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}]$ / DeltaTFdiff

NOTE :
1) The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.

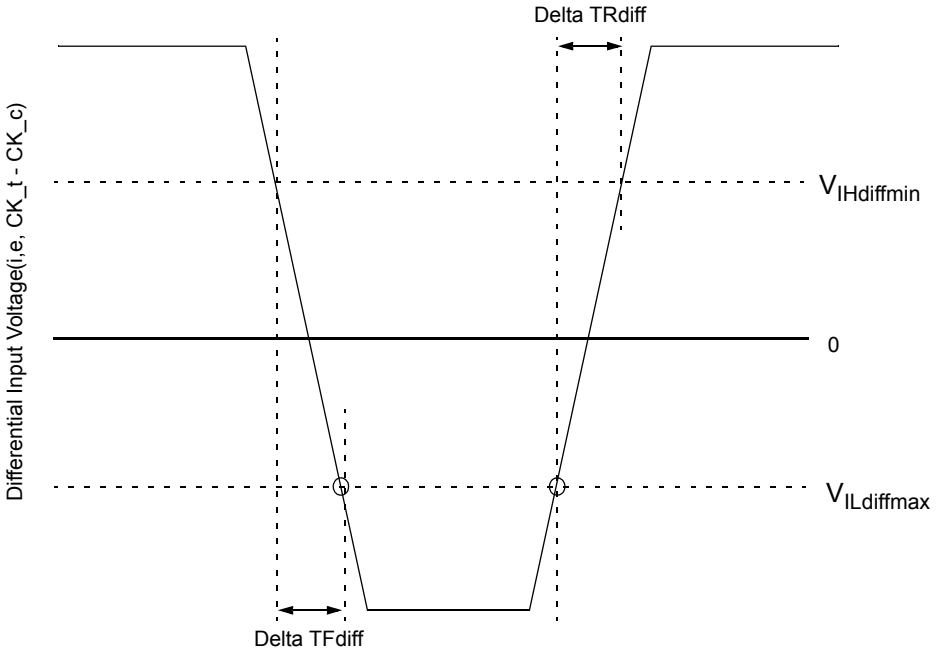


Figure 7. Differential Input Slew Rate Definition for CK_t, CK_c

12.4.2 Slew Rate Definition for Single-ended Input Signals (CMD/ADD)

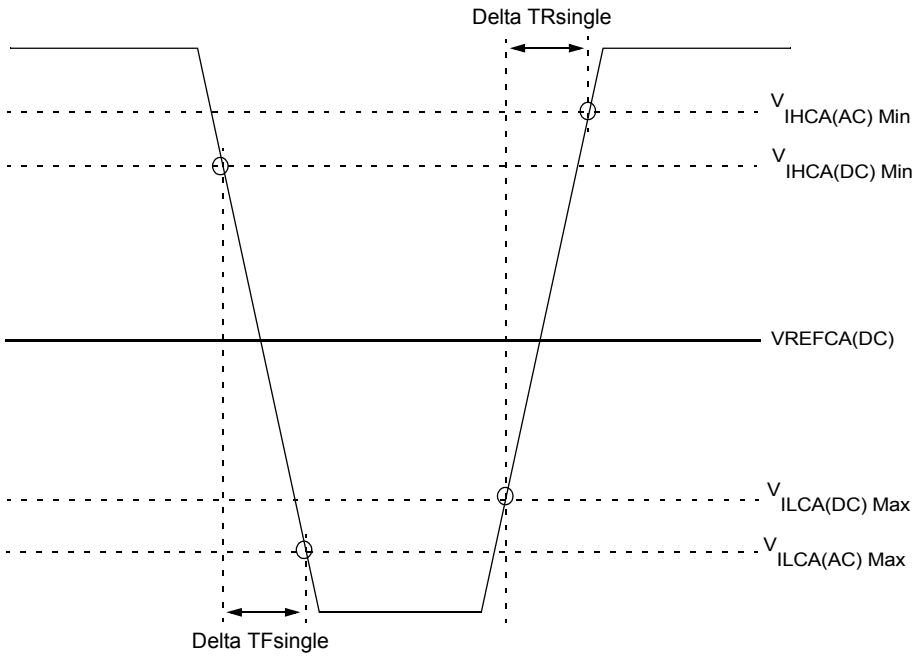


Figure 8. Single-ended Input Slew Rate definition for CMD and ADD

NOTE :
1) Single-ended input slew rate for rising edge = {VIHCA(AC)Min - VILCA(DC)Max} / Delta TR single.
2) Single-ended input slew rate for falling edge = {VIHCA(DC)Min - VILCA(AC)Max} / Delta TF single.
3) Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.
4) Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

12.5 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 15. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

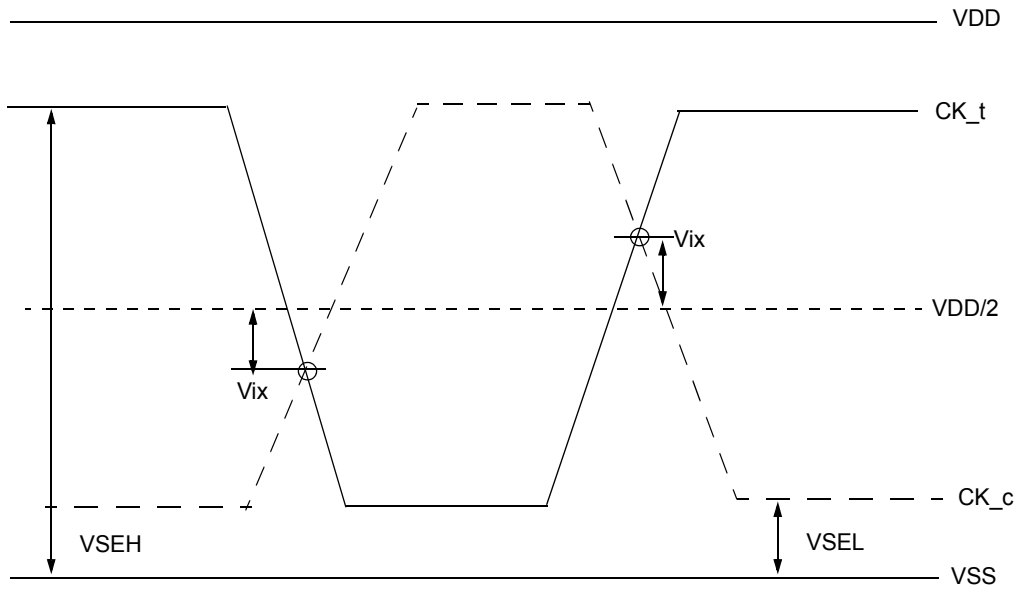


Figure 9. Vix Definition (CK)

[Table 15] Cross Point Voltage for Differential Input Signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145mV	VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	VDD/2 + 100mV =< VSEH =< VDD/2 + 145mV	VDD/2 + 145mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	-(VDD/2 - VSEL) + 25mV	(VSEH - VDD/2) - 25mV	120mV

Symbol	Parameter	DDR4-2400			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145 mV	VDD/2 - 145 mV =< VSEL =< VDD/2 - 100 mV	VDD/2 + 100 mV =< VSEH =< VDD/2 + 145 mV	VDD/2 + 145 mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120mV	- (VDD/2 - VSEL) + 25 mV	(VSEH - VDD/2) - 25 mV	120mV

Symbol	Parameter	DDR4-2666/2933			
		min		max	
-	Area of VSEH, VSEL	VSEL < VDD/2 - 145 mV	VDD/2 - 145 mV =< VSEL =< VDD/2 - 100 mV	VDD/2 + 100 mV =< VSEH =< VDD/2 + 145 mV	VDD/2 + 145 mV < VSEH
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-110 mV	- (VDD/2 - VSEL) + 30 mV	(VSEH - VDD/2) - 30 mV	110mV

12.6 CMOS rail to rail Input Levels

12.6.1 CMOS rail to rail Input Levels for RESET_n

[Table 16] CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :
1) After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2) Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3) RESET is destructive to data contents.
4) No slope reversal(ringback) requirement during its level transition from Low to High.
5) This definition is applied only “Reset Procedure at Power Stable”.
6) Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7) Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

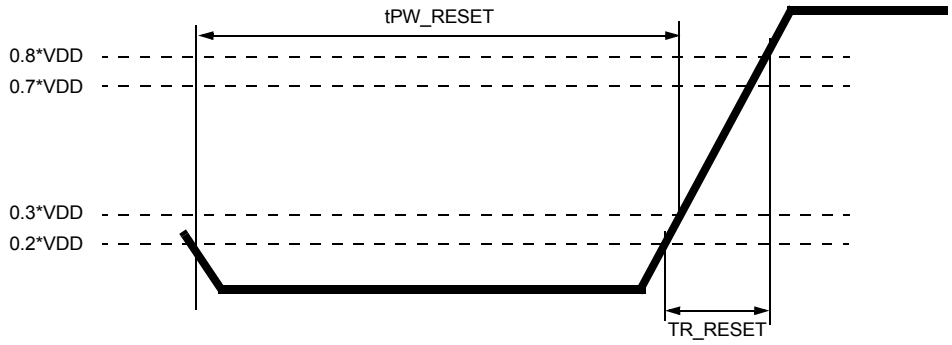


Figure 10. RESET_n Input Slew Rate Definition

12.7 AC and DC Logic Input Levels for DQS Signals

12.7.1 Differential signal definition

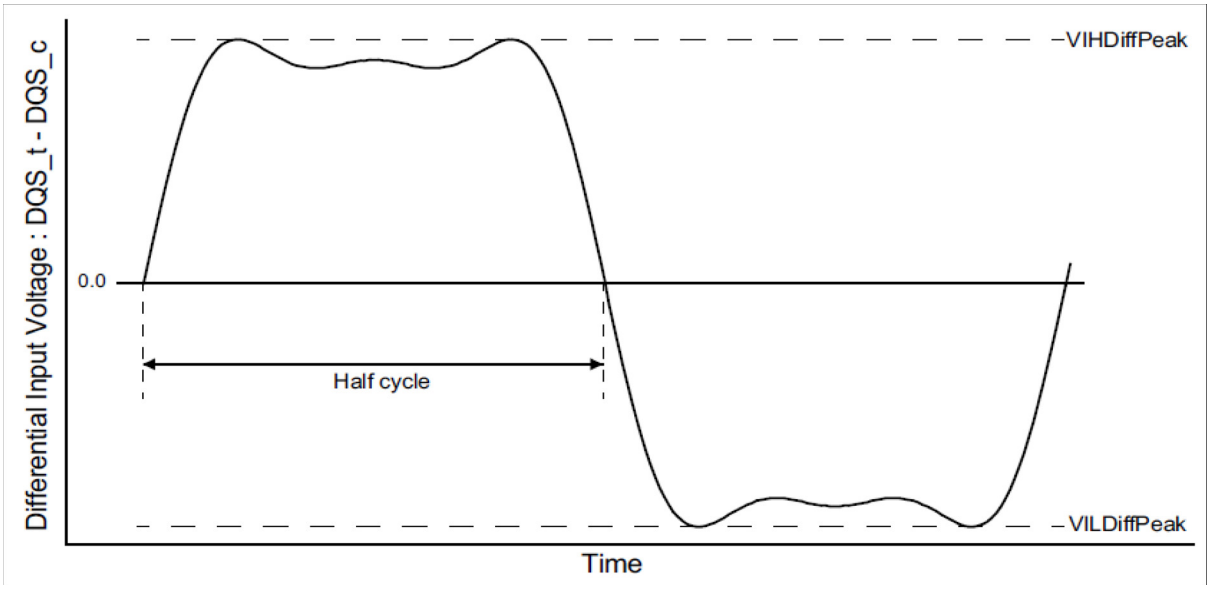


Figure 11. Definition of differential DQS Signal AC-swing Level

12.7.2 Differential swing requirements for DQS (DQS_t - DQS_c)

[Table 17] Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600, 1866, 2133		DDR4-2400		DDR4-2666		DDR4-2933		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	Note2	160	Note2	150	Note2	145	Note2	mV	1
VILDiffPeak	VIL.DIFF.Peak Voltage	Note2	-186	Note2	-160	Note2	-150	Note2	-145	mV	1

NOTE :

1) Used to define a differential signal slew-rate.
2) These values are not defined; however, the differential signals DQS_t - DQS_c, need to be within the respective limits Overshoot, Undershoot Specification for single-ended signals.

12.7.3 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

The Max(f(t)) or Min(f(t)) used to determine the midpoint which to reference the +/-35% window of the exempt non-monotonic signaling shall be the smallest peak voltage observed in all ui's.

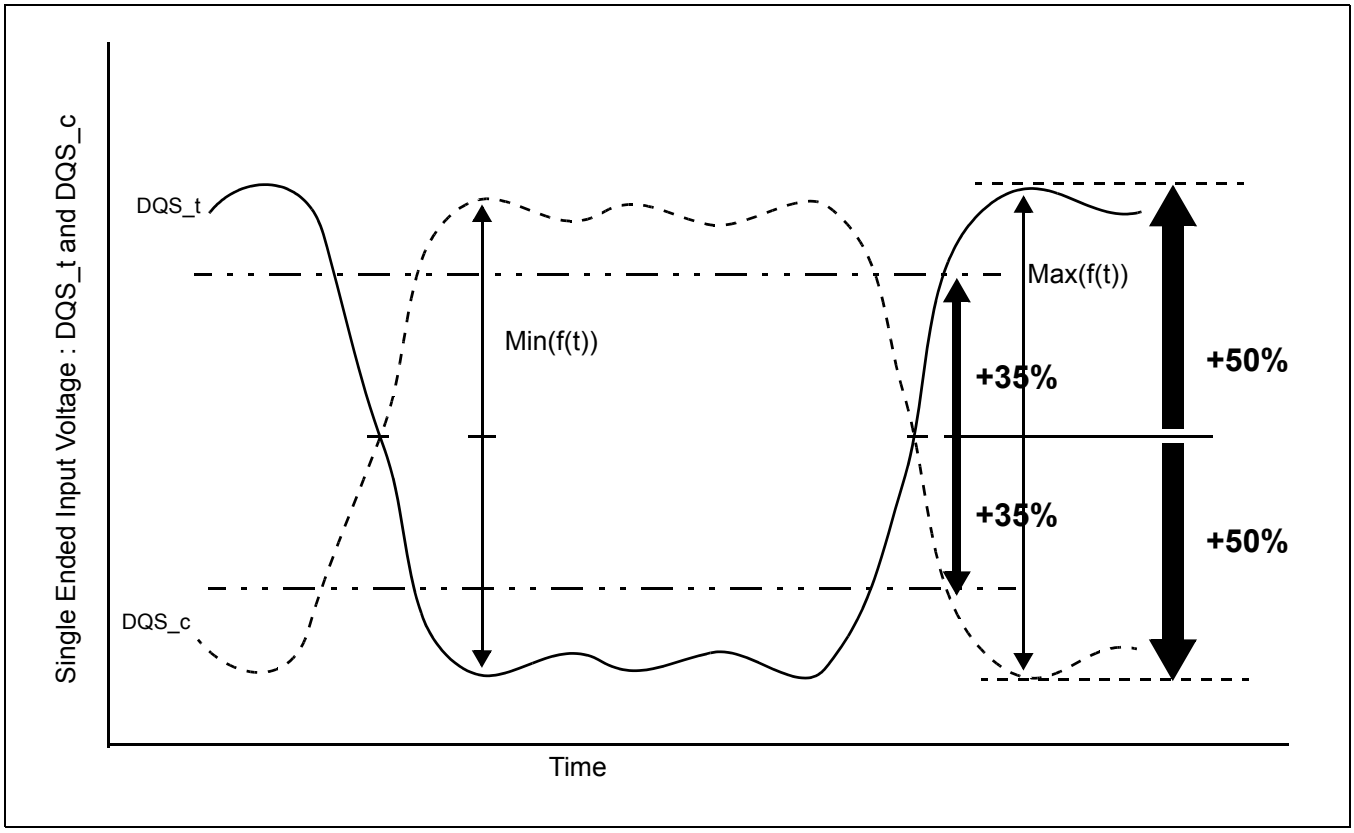


Figure 12. Definition of differential DQS Peak Voltage and rage of exempt non-monotonic signaling

12.7.4 Differential Input Cross Point Voltage

To achieve tight RxMask input requirements as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 18. The differential input cross point voltage VIX_DQS (VIX_DQS_FR and VIX_DQS_RF) is measured from the actual cross point of DQS_t, DQS_c relative to the VDQSmid of the DQS_t and DQS_c signals.
VDQSmid is the midpoint of the minimum levels achieved by the transitioning DQS_t and DQS_c signals, and noted by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
A non-monotonic transitioning signal's ledge is exempt or not used in determination of a horizontal tangent provided the said ledge occurs within +/- 35% of the midpoint of either VIH.DIFF.Peak Voltage (DQS_t rising) or VIL.DIFF.Peak Voltage (DQS_c rising), refer to Figure 12. A secondary horizontal tangent resulting from a ring-back transition is also exempt in determination of a horizontal tangent. That is, a falling transition's horizontal tangent is derived from its negative slope to zero slope transition (point A in Figure 13) and a ring-back's horizontal tangent derived from its positive slope to zero slope transition (point B in Figure 13) is not a valid horizontal tangent; and a rising transition's horizontal tangent is derived from its positive slope to zero slope transition (point C in Figure 13) and a ring-back's horizontal tangent derived from its negative slope to zero slope transition (point D in Figure 13) is not a valid horizontal tangent

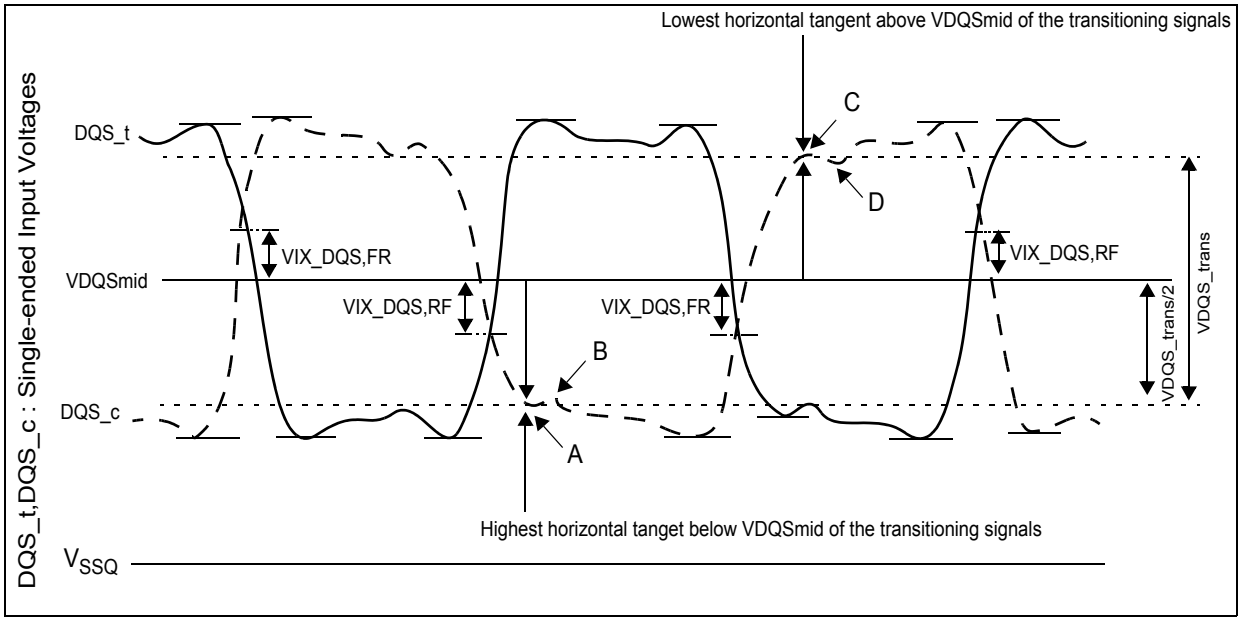


Figure 13. Vix Definition (DQS)

[Table 18] Cross point voltage for DQS differential input signals

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933		Unit	Note
		Min	Max	Min	Max		
Vix_DQS_ratio	DQS_t and DQS_c crossing relative to the midpoint of the DQS_t and DQS_c signal swings	-	25	-	25	%	1, 2
VDQSmid_to_Vcent	VDQSmid offset relative to Vcent_DQ(midpoint)	-	min (VIHdiff,50)	-	min (VIHdiff,50)	mV	3, 4, 5

NOTE :
1) Vix_DQS_Ratio is DQS VIX crossing (Vix_DQS_FR or Vix_DQS_RF) divided by VDQS_trans. VDQS_trans is the difference between the lowest horizontal tangent above VDQSmid of the transitioning DQS signals and the highest horizontal tangent below VDQSmid of the transitioning DQS signals.
2) VDQSmid will be similar to the VREFDQ internal setting value obtained during Vref Training if the DQS and DQs drivers and paths are matched.
3) The maximum limit shall not exceed the smaller of VIHdiff minimum limit or 50mV.
4) VIX measurements are only applicable for transitioning DQS_t and DQS_c signals when toggling data, preamble and high-z states are not applicable conditions.
5) The parameter VDQSmid is defined for simulation and ATE testing purposes, it is not expected to be tested in a system.

12.7.5 Differential Input Slew Rate Definition

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 13 and Figure 14.

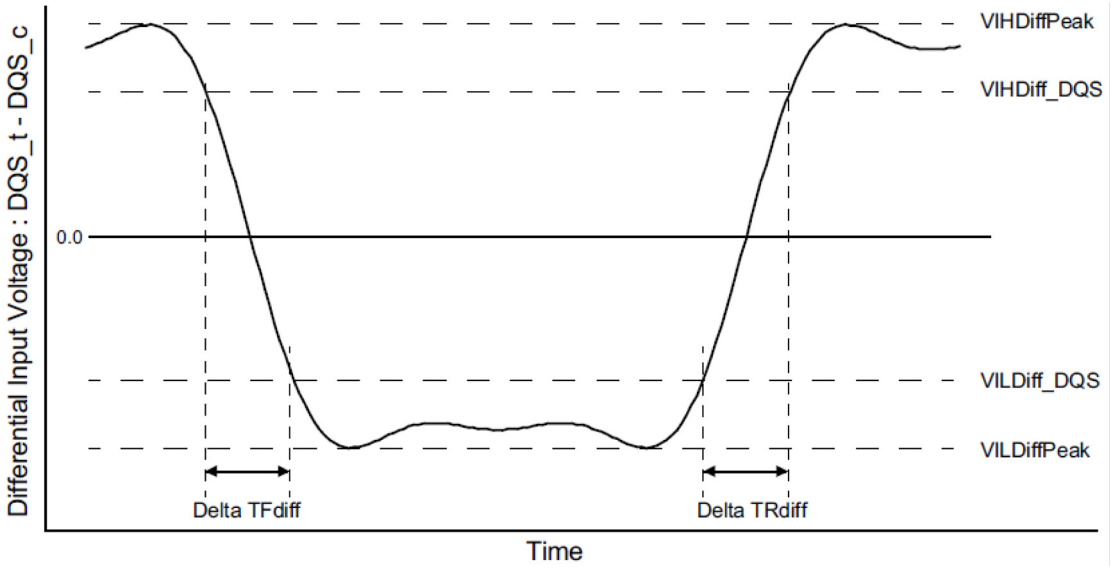


Figure 14. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :

1) Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope.
2) Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

[Table 19] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

[Table 20] Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
VIHDiff_DQS	Differential Input High	136	-	130	-	115	-	mV	
VILDiff_DQS	Differential Input Low	-	-136	-	-130	-	-115	mV	

[Table 21] Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933		Unit	NOTE
		Min	Max	Min	Max		
SRIdiff	Differential Input Slew Rate	3	18	2.5	18	V/ns	

13. AC AND DC OUTPUT MEASUREMENT LEVELS

13.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\ out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\ out|}$$ under the condition that RON_{Pu} is off

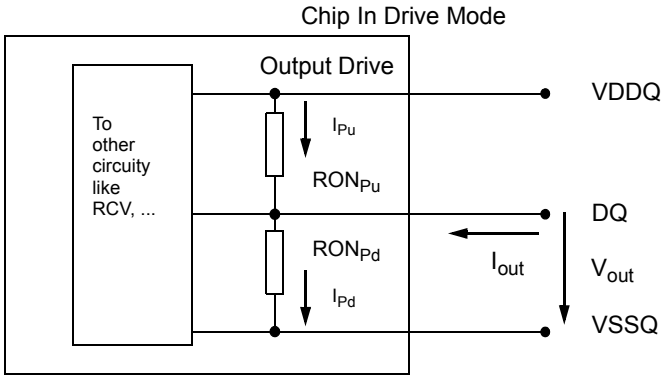


Figure 15. Output driver

[Table 22] Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

NOTE :

1) The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on 13.1.1Output Driver Temperature and Voltage Sensitivity.

2) Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.

3) Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} * 100$$

4) RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} * 100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} * 100$$

5) This parameter of x16 device is specified for Uper byte and Lower byte.

13.1.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

ΔT = T - T(@calibration); ΔV = VDDQ - VDDQ(@ calibration); VDD = VDDQ

[Table 23] Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
R_{ONPU}@ $V_{OH(DC)}$	0.6 - $dR_{ON}dTH \times \|\Delta T\| - dR_{ON}dVH \times \|\Delta V\|$	1.1 - $dR_{ON}dTH \times \|\Delta T\| + dR_{ON}dVH \times \|\Delta V\|$	$R_{ZQ}/6$
R_{ON}@ $V_{OM(DC)}$	0.9 - $dR_{ON}dTM \times \|\Delta T\| - dR_{ON}dVM \times \|\Delta V\|$	1.1 + $dR_{ON}dTM \times \|\Delta T\| + dR_{ON}dVM \times \|\Delta V\|$	$R_{ZQ}/6$
R_{ONPD}@ $V_{OL(DC)}$	0.6 - $dR_{ON}dTL \times \|\Delta T\| - dR_{ON}dVL \times \|\Delta V\|$	1.1 + $dR_{ON}dTL \times \|\Delta T\| + dR_{ON}dVL \times \|\Delta V\|$	$R_{ZQ}/6$

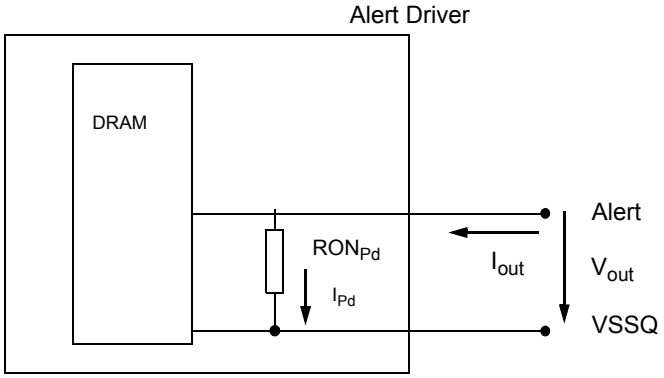
[Table 24] Output Driver Temperature and Voltage Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	%/mV
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV

13.1.2 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off



Resistor	Vout	Min	Max	Unit	NOTE
RON_{Pd}	VOLdc= 0.1* VDDQ	0.3	1.2	34Ω	1
	V_{OMdc} = 0.8* VDDQ	0.4	1.2	34Ω	1
	V_{OHdc} = 1.1* VDDQ	0.4	1.4	34Ω	1

NOTE:
1) VDDQ voltage is at VDDQ DC.

13.1.3 Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ}-V_{OUT}}{|Iout|}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{|Iout|}$$

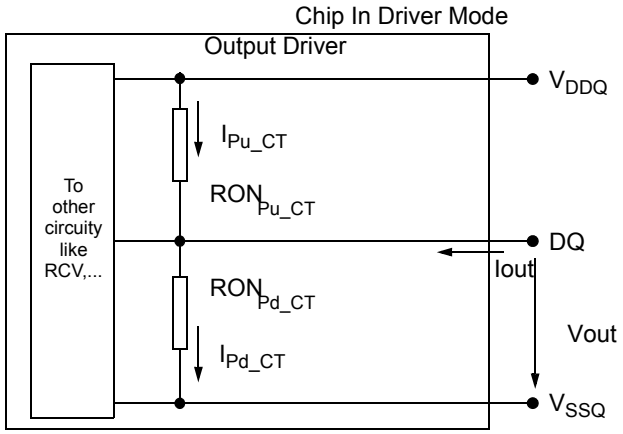


Figure 16. Output Driver

RON_{NOM_CT}	Resistor	Vout	Max	Units	NOTE
34Ω	RON_{Pd_CT}	VOB_{dc} = 0.2 x V_{DDQ}	1.9	34Ω	1
		VOL_{dc} = 0.5 x V_{DDQ}	2.0	34Ω	1
		VOM_{dc} = 0.8 x V_{DDQ}	2.2	34Ω	1
		VOH_{dc} = 1.1 x V_{DDQ}	2.5	34Ω	1
	RON_{Pu_CT}	VOB_{dc} = 0.2 x V_{DDQ}	2.5	34Ω	1
		VOL_{dc} = 0.5 x V_{DDQ}	2.2	34Ω	1
		VOM_{dc} = 0.8 x V_{DDQ}	2.0	34Ω	1
		VOH_{dc} = 1.1 x V_{DDQ}	1.9	34Ω	1

NOTE :
1) Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

13.2 Single-ended AC & DC Output Levels

[Table 25] Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE :
1) The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

13.3 Differential AC & DC Output Levels

[Table 26] Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE :
1) The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

13.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 27 and Figure 17.

[Table 27] Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE :
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

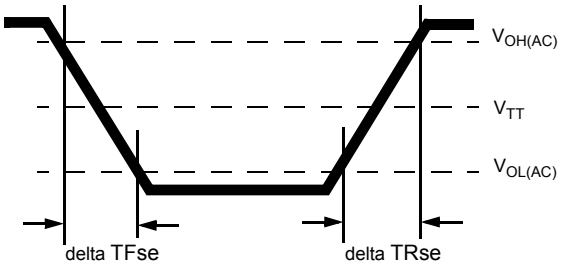


Figure 17. Single-ended Output Slew Rate Definition

[Table 28] Single-ended Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE :
1) In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

13.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 29 and Figure 18.

[Table 29] Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE:
1) Output slew rate is verified by design and characterization, and may not be subject to production test.

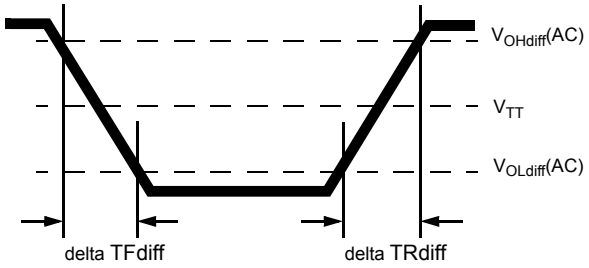


Figure 18. Differential Output Slew Rate Definition

[Table 30] Differential Output Slew Rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	8	18	8	18	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

13.6 Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

[Table 31] Single-ended AC & DC Output Levels of Connectivity Test Mode

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
$V_{OB(DC)}$	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
$V_{OL(AC)}$	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE :

1) The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.

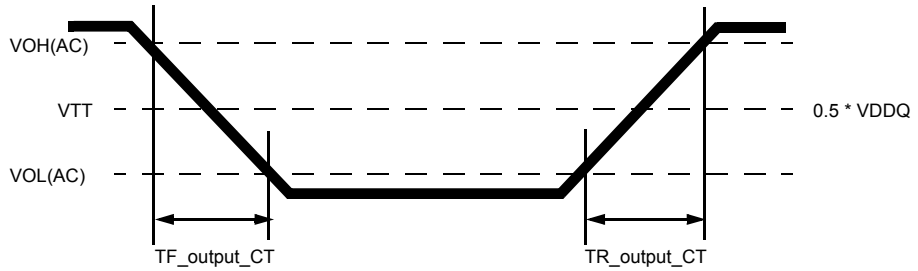


Figure 19. Output Slew Rate Definition of Connectivity Test Mode

[Table 32] Single-ended Output Slew Rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400/2666/2933		Unit	Notes
		Min	Max		
Output signal Falling time	TF_output_CT	-	10	ns/V	
Output signal Rising time	TR_output_CT	-	10	ns/V	

13.7 Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure 20.

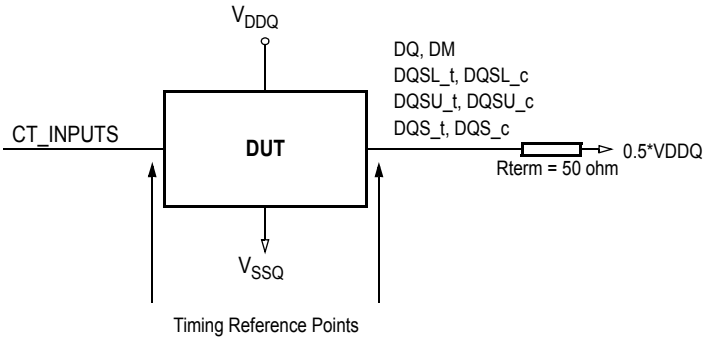


Figure 20. Connectivity Test Mode Timing Reference Load

14. IDD AND IDDQ SPECIFICATION PARAMETERS AND TEST CONDITIONS

14.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 21 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 22. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as VIN <= VILAC(max).
- "1" and "HIGH" is defined as VIN >= VIHAC(min).
- "MID-LEVEL" is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 37.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 35.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 36 through Table 43.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0_B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n} := {HIGH, HIGH, HIGH, HIGH, HIGH} ;apply invert of BG/BA changes when directed above.

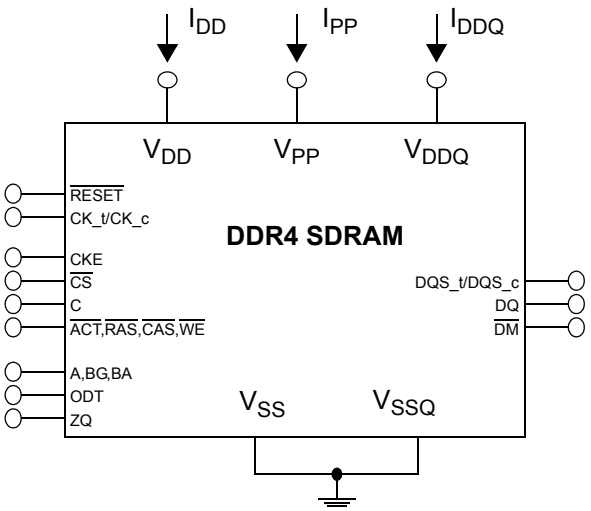


Figure 21. Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

NOTE :
1) DIMM level Output test load condition may be different from above.

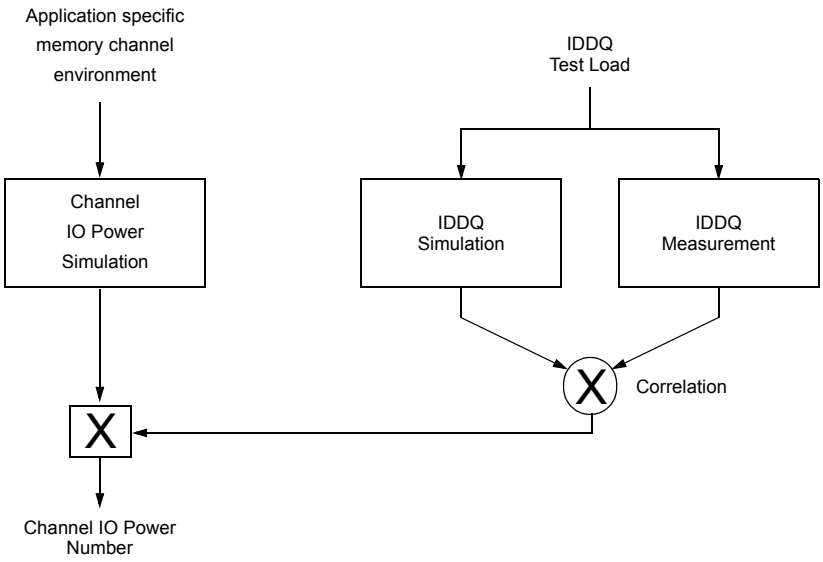


Figure 22. Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

[Table 33] Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	Unit
		17-15-15	19-17-17	22-19-19	24-21-21	
tCK		0.937	0.833	0.75	0.682	ns
CL		17	19	22	24	nCK
CWL		14	16	18	20	nCK
nRCD		15	17	19	21	nCK
nRC		51	56	62	68	nCK
nRAS		36	39	43	47	nCK
nRP		15	17	19	21	nCK
nFAW_slr	x4	16	16	16	16	nCK
nRRD_S_slr	x4	4	4	4	4	nCK
nRRD_L_slr	x4	6	6	7	8	nCK
nRFC_slr 16 Gb		587	661	734	807	nCK
nRFC_dlr 16 Gb		203	228	254	279	nCK

15. DIMM IDD SPECIFICATION DEFINITION

[Table 34] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 35; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 35); Logical Rank Activity: Cycling with one logical rank active at a time; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 35
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 36; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 36); Logical Rank Activity: Cycling with one logical rank active at a time; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 36
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 37; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 37
IDD2NA	**Precharge Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 38; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to Table 38; **Pattern Details:** see Table 38
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3],[5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 37; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 37

[Table 34] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD3NA	**Active Standby Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[2)]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 39; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 39; **DM_n**: stable at 1; **Bank Activity:** all banks of all logical ranks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 39); and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 39
IDD4RA	**Operating Burst Read Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 40; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 40; **DM_n:** stable at 1; **Bank Activity:** all banks open of all logical ranks, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 40); and through logical ranks; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 40
IDD4WA	**Operating Burst Write Current (AL=CL-2)** **AL = CL-2, Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3)], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3)], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B1	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 30; **BL:** 8[1)]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 42; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 42); Logical Rank Activity: REF command staggered nRFC_dlr between REF command to REF command; **Output Buffer and RTT:** Enabled in Mode Registers[2)]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 42
IPP5B1	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B1**
IDD5B2	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 30; **BL**: 8[1)]; **AL**: 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs**: partially toggling according to Table 41; **Data IO**: VDDQ; **DM_n**: stable at 1; **Bank Activity**: REF command every nRFC (see Table 41); Logical Rank **Activity**: REF command staggered nRFC_slr between REF command to REF command; **Output Buffer and RTT**: Enabled in Mode Registers[2)]; **ODT Signal**: stable at 0; **Pattern Details**: see Table 41
IPP5B2	**Burst Refresh Write IPP Current (1X REF)** **Same condition with I_{DD5B2}**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B1
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**
IDD5F3	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions: see IDD5B2**
IPP5F3	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F3**

[Table 34] Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B1
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD5F5	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B2
IPP5F5	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F5**
IDD6N	**Self Refresh Current: Normal Temperature Range** **T_{CASE}:** 0 - 85°C; **Low Power Auto Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range** **T_{CASE}:** 0 - 95°C; **Low Power Auto Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LE**VEL**
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** **T_{CASE}:** 0 - 45°C; **Low Power Auto Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** **T_{CASE}:** 0 - 95°C; **Low Power Auto Self Refresh (LP ASR)** : Auto[4]; Partial Array Self-Refresh (PASR): Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 37; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**: stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 30; **BL:** 8[1]; **AL:** CL-2; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 43; **Data IO:** read data bursts with different data between one burst and the next one according to Table 43; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 43; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 43
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current** **Place DRAM in MPSM**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE:

1) Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2) Output Buffer Enable
   - set MR1 [A12 = 0]: Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00]: Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011]: RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01]: RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000]
3) CAL enabled: set MR4 [A8:6 = 001]: 1600MT/s
   010]: 1866MT/s, 2133MT/s
   011]: 2400MT/s, 2666MT/s
   100]: 2933MT/s
   Gear Down mode enabled: set MR3 [A3 = 1]: 1/4 Rate
   DLL disabled: set MR1 [A0 = 0]
   CA parity enabled: set MR5 [A2:0 = 001]: 1600MT/s,1866MT/s, 2133MT/s
   010]: 2400MT/s, 2666MT/s
   011]: 2933MT/s
   Read DBI enabled: set MR5 [A12 = 1]
   Write DBI enabled: set MR5 [A11 = 1]
4) Low Power Array Self Refresh (LP ASR): set MR2 [A7:6 = 00]: Normal
   01]: Reduced Temperature range
   10]: Extended Temperature range
   11]: Auto Self Refresh
5) IDD2NG should be measured after sync pules (NOP) input.

[Table 35] IDD0, IDD0A and IPP0 Measurement-Loop Pattern [1)]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2)]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device
3) C[2:0] are used only for 3DS device
4) DQ signals are VDDQ.

[Table 36] IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[b)]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	0	1	**1**	**0**	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	**0**	**0**	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	**0**	3[b)]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	**0**	**1**	1	0	0	0	0	**0**	**0**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	1	1	**0**	**0**	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		8	7*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		11	11*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		13	13*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] =** 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use **BG[1:0][2)] = 2, BA[1:0] =** 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use **BG[1:0][2)] = 3, BA[1:0] =** 0 instead																

NOTE :

1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.

2) BG1 is don't care for x16 device.

3) C[2:0] are used only for 3DS device.

4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

[Table 37] IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	0
			3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, use **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 38] IDD2NT and IDDQ2NT Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																	
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																	
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																	
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																	
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																	
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																	
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																	
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																	For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																	
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																	
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																	
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																	
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																	
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																	
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																	

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 39] IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**RD**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Read Command.

[Table 40] IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**WR**	0	1	1	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**WR**	0	1	1	0	0	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead															
		3	12-15	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead															
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead															
		5	20-23	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead															
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead															
		7	28-31	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead															
		8	32-35	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Write Command.

[Table 41] IDD4WC Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**WR**	0	1	1	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC**
			1,2	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			5	**WR**	0	1	1	0	0	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC**
			6,7	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Write Command.

[Table 42] IDD5B Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**REF**	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
		1	1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			4	D#, D#	1	1	1	1	1	0	0	**3**[2)]	**3**	0	0	0	**7**	**F**	0	-
			4-7	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 1** instead																
			8-11	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 2** instead																
			12-15	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 3** instead																
			16-19	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 1** instead																
			20-23	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 2** instead																
			24-27	repeat pattern 1...4, use **BG[1:0]**[2)] **= 0, BA[1:0] = 3** instead																
			28-31	repeat pattern 1...4, use **BG[1:0]**[2)] **= 1, BA[1:0] = 0** instead																
			32-35	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 1** instead																
			40-43	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 2** instead																
			44-47	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 3** instead																
			48-51	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 1** instead																
			52-55	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 2** instead																
			56-59	repeat pattern 1...4, use **BG[1:0]**[2)] **= 2, BA[1:0] = 3** instead																
			60-63	repeat pattern 1...4, use **BG[1:0]**[2)] **= 3, BA[1:0] = 0** instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE :
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) DQ signals are VDDQ.

[Table 43] IDD7 Measurement-Loop Pattern[1)]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3)]	BG[1:0][2)]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4)]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**-**
			1	**RDA**	0	1	1	0	1	0		**0**	**0**	0	0	1	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRRD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**	0	**-**
			nRRD + 1	**RDA**	0	1	1	0	1	0		**1**	**1**	0	0	1	**0**	**0**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRRD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRRD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 3** instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0][2)] = 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0][2)] = 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE:
1) DQS_t, DQS_c are VDDQ.
2) BG1 is don't care for x16 device.
3) C[2:0] are used only for 3DS device.
4) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

16. IDD TABLE

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

[Table 44] I_{DD} and I_{DDQ} Values for M393ABG40M5B

Symbol	M393ABG40M5B : 256GB(32Gx72) Module		Unit	NOTE
	DDR4-2933			
	24-21-21			
	VDD 1.2V	VPP 2.5V		
	IDD Max.	IPP Max.		
I_{DD0}	6839	337	mA	
I_{DD0A}	7073	337	mA	
I_{DD1}	7086	339	mA	
I_{DD1A}	7437	341	mA	
I_{DD2N}	6436	324	mA	
I_{DD2NA}	6990	324	mA	
I_{DD2NT}	6414	321	mA	
I_{DD2NL}	6169	321	mA	
I_{DD2NG}	6417	321	mA	
I_{DD2ND}	6230	321	mA	
I_{DD2N_par}	6410	321	mA	
I_{DD2P}	4506	170	mA	
I_{DD2Q}	6270	321	mA	
I_{DD3N}	7517	360	mA	
I_{DD3NA}	7946	360	mA	
I_{DD3P}	5598	353	mA	
I_{DD4R}	9419	351	mA	
I_{DD4RA}	9950	350	mA	
I_{DD4RB}	9444	351	mA	
I_{DD4W}	9594	350	mA	
I_{DD4WA}	9931	342	mA	
I_{DD4WB}	9599	350	mA	
I_{DD4WC}	9136	342	mA	
I_{DD4W_par}	9873	353	mA	
I_{DD5B1}	30779	2646	mA	
I_{DD5F2}	23316	1910	mA	
I_{DD5F4}	20995	1644	mA	
I_{DD6N}	7003	677	mA	
I_{DD6E}	10570	1012	mA	
I_{DD6R}	5184	504	mA	
I_{DD6A}	6997	674	mA	
I_{DD7}	11104	526	mA	
I_{DD8}	3210	332	mA	

NOTE :

1) DIMM IDD SPEC is based on the condition that de-activated rank (IDLE) is IDD2N. Please refer to Table .
2) IDD current measure method and detail patterns are described on DDR4 component datasheet.
3) VDD and VDDQ are merged on module PCB (IDDQ values are not considered by Qoff condition)
4) DIMM IDD Values are calculated based on the component IDD spec and Register power.

[Table 45] DIMM Rank Status

SEC DIMM	Operating Rank	The other Rank
I_{DD0}	I_{DD0}	I_{DD2N}
I_{DD1}	I_{DD1}	I_{DD2N}
I_{DD2P}	I_{DD2P}	I_{DD2P}
I_{DD2N}	I_{DD2N}	I_{DD2N}
I_{DD2Q}	I_{DD2Q}	I_{DD2Q}
I_{DD3P}	I_{DD3P}	I_{DD3P}
I_{DD3N}	I_{DD3N}	I_{DD3N}
I_{DD4R}	I_{DD4R}	I_{DD2N}
I_{DD4W}	I_{DD4W}	I_{DD2N}
I_{DD5B}	I_{DD5B}	I_{DD2N}
I_{DD6}	I_{DD6}	I_{DD6}
I_{DD7}	I_{DD7}	I_{DD2N}
I_{DD8}	I_{DD8}	I_{DD8}

17. INPUT/OUTPUT CAPACITANCE

[Table 46] DDR4 3DS Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		DDR4-2933		Unit	NOTE
		min	max	min	max	min	max		
C_{IO}	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.0	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	-	0.05	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.7	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	-	0.05	pF	1,3,4
C_{I}	Input capacitance (CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	0.2	0.6	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,3,7,8
$C_{DI\_ADD\_CMD}$	Input capacitance delta (All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	pF	1,3,12

NOTE :

1) This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating.
2) DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3) This parameter applies to 3DS devices. It is meant to represent the silicon pad capacity of the master die.
4) Absolute value CK_T-CK_C
5) Absolute value of CIO(DQS_T)-CIO(DQS_C)
6) CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7) CDI CTRL applies to ODT, CS_n and CKE
8) CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_t)+CI(CLK_c))
9) CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10) CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_t)+CI(CLK_c))
11) CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_t)+CIO(DQS_c))
12) Maximum external load capacitance on ZQ pin: 5 pF.

18. ELECTRICAL CHARACTERISTICS & AC TIMINGS FOR DDR4-1600-3DS TO DDR4-2933-3DS

18.1 Refresh parameters

Typical platforms are designed with the assumption that no more than one physical rank is refreshed at the same time. In order to limit the maximum refresh current (IDD5B1) for a 3D stacked SDRAM, it will be required to stagger the refreshes to each device in a stack.

The tRFC time for a single logical rank is defined as tRFC_slr and is specified as the same value as for a monolithic DDR4 SDRAM of equivalent density. The minimum amount of stagger between refresh commands (=tREF_stagger) sent to different logical ranks is specified to be approximately tRFC_slr/3 - Table 47 below.

[Table 47] Refresh parameters by logical rank density

Parameter	Symbol		Logical Rank Density	Units
			16Gb	
REF command to ACT or REF command time to same logical rank	tRFC_slr1 (1X mode)		350	ns
	tRFC_slr2 (2X mode)		260	ns
	tRFC_slr4 (4X mode)		160	ns
REF command to REF command to different logical rank	tRFC_dlr1 (1X mode)		120	ns
	tRFC_dlr2 (2X mode)		90	ns
	tRFC_dlr4 (4X mode)		55	ns
Average periodic refresh interval in same logical rank	tREFI_slr1 (1X mode)	0°C = < T_{CASE} = < 85°C	7.8	us
		85°C < T_{CASE} = < 95°C	3.9	us
	tREFI_slr2 (2X mode)	0°C = < T_{CASE} = < 85°C	3.9	us
		85°C < T_{CASE} = < 95°C	1.95	us
	tREFI_slr4 (4X mode)	0°C = < T_{CASE} = < 85°C	1.95	us
		85°C < T_{CASE} = < 95°C	0.975	us

[Table 48] Timing Parameters by Speed Grade

Parameter	Sym-bol	DDR4-1600-3DS		DDR4-1866-3DS		DDR4-2133-3DS		DDR4-2400-3DS		DDR4-2666-3DS		DDR4-2933-3DS		Units	NOTE
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Row Activate to Row Activate Delay															
ACTIVATE to ACTIVATE command period to different bank group in the same logical rank	tRRD_S_slr	max(4nCK,5ns)	-	max(4nCK,4.2ns)	-	max(4nCK,3.7ns)	-	max(4nCK,3.3ns)	-	Max(4nCK,3ns)	-	Max(4nCK,2.7ns)	-	ns	
ACTIVATE to ACTIVATE command period to same bank group in the same logical rank	tRRD_L_slr	max(4nCK,6ns)	-	max(4nCK,5.3ns)	-	max(4nCK,5.3ns)	-	max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	Max(4nCK,4.9ns)	-	ns	
ACTIVATE to ACTIVATE command period to different logical ranks	tRRD_dlr	4	-	4	-	4	-	4	-	4	-	4	-	nCK	
Four Activate Window															
Four activate window to the same logical rank for 0.5KB page size	tFAW_slr_x4	Max(16nCK,20ns)	-	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	Max(16nCK,10.875ns)	-	ns	1
Four activate window to different logical ranks	tFAW_dlr	16	-	16	-	16	-	16	-	16	-	16	-	nCK	
Self-Refresh Timings															
Exit Self-Refresh to commands not requiring a locked DLL	tXS	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-	max(5nCK,tRFC_slr(min)+10ns)	-		2

NOTE :

1) For x4 devices only.
2) Upon exit from Self-Refresh, the 3D Stacked DDR4 SDRAM requires a minimum of one extra refresh command to all logical ranks before it is put back into Self-Refresh Mode.

18.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding bin

[Table 49] DDR4-1600 Speed Bins and Operations

Speed Bin			DDR4-1600		Unit	NOTE
CL-nRCD-nRP			13-12-11			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.25	21.00	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	13.75	-	ns	
ACT to PRE command period		tRAS	35	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	48.75	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	tCK(AVG)	1.25	1.5	ns	1,2,3,4
	CL = 14	tCK(AVG)	1.25	1.5	ns	1,2,3
Supported CL Settings			11,12,13,14		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,11		nCK	

[Table 50] DDR4-1866 Speed Bins and Operations

Speed Bin			DDR4-1866		Unit	NOTE
CL-nRCD-nRP			15-14-13			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.07	21.00	ns	
ACT to internal read or write delay time		tRCD	15	-	ns	
PRE command period		tRP	13.92 (13.75[13])	-	ns	
ACT to PRE command period		tRAS	34	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.92	-	ns	
CWL = 9,11	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,6
	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,6
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3
Supported CL Settings			11,12,13,14,15,16		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12		nCK	

[Table 51] DDR4-2133 Speed Bins and Operations

Speed Bin			DDR4-2133		Unit	NOTE
CL-nRCD-nRP			17-15-15			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15.95	21.00	ns	
ACT to internal read or write delay time		tRCD	14.06	-	ns	
PRE command period		tRP	14.06 (13.75[13])	-	ns	
ACT to PRE command period		tRAS	33	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	47.06	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 14	tCK(AVG)	Reserved			1,2,3,4,7
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	tCK(AVG)	0.937	<1.071		1,2,3,4
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,7
Supported CL Settings			11,12,13,14,15,16,17,18		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12,14		nCK	

[Table 52] DDR4-2400 Speed Bins and Operations

Speed Bin			DDR4-2400		Unit	NOTE
CL-nRCD-nRP			19-17-17			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	15.83	21.00	ns	
ACT to internal read or write delay time		tRCD	14.16	-	ns	
PRE command period		tRP	14.16	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.16	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	1.25	1.5	ns	1,2,3,4,8
	CL = 14	tCK(AVG)	1.25	1.5	ns	1,2,3,8
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,8
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4,8
	CL = 17	tCK(AVG)	0.937	<1.071		1,2,3,4,8
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,8
CWL = 12,16	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	tCK(AVG)	0.833	<0.937		1,2,3,4
	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4
	CL = 22	tCK(AVG)	Reserved		ns	1,2,3,4,8
Supported CL Settings			11,12,13,14,15,16,17,18,19,20		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9,10,11,12,14,16		nCK	

[Table 53] DDR4-2666 Speed Bins and Operations

Speed Bin			DDR4-2666		Unit	NOTE
CL-nRCD-nRP			22-19-19			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.5	21.5	ns	
ACT to internal read or write delay time		tRCD	14.25	-	ns	
PRE command period		tRP	14.25	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.25	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 14	tCK(AVG)	1.25	1.5	ns	1,2,3,8
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 15	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.833	<0.937	ns	1,2,3,9
CWL = 14,18	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 22	tCK(AVG)	0.75	0.833	ns	1,2,3,4,9
	CL = 24	tCK(AVG)	0.75	0.833	ns	1,2,3,9
Supported CL Settings			11,12,13,14,15,16,17,18,19,20,22,24		nCK	
Supported nRCD Timings minimum			12		nCK	
Supported nRP Timings minimum			12		nCK	
Supported CWL Settings			9,10,11,12,14,16,18		nCK	

[Table 54] DDR4-2933 Speed Bins and Operations

Speed Bin			DDR4-2933		Unit	NOTE
CL-nRCD-nRP			24-21-21			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	16.37	21.50	ns	
ACT to internal read or write delay time		tRCD	14.32	-	ns	
PRE command period		tRP	14.32	-	ns	
ACT to PRE command period		tRAS	32	9 x tREFI	ns	
ACT to ACT or REF command period		tRC	46.32	-	ns	
CWL = 9,11	CL = 13	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 14	tCK(AVG)	1.25	1.5	ns	1,2,3,4,10
CWL = 10,12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 15	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
CWL = 11,14	CL = 16	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 20	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
CWL = 12,16	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 22	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
CWL = 14,18	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 24	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
CWL = 14,18	CL = 22	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 24	tCK(AVG)	0.682	<0.75	ns	1,2,3,4,10
	CL = 25	tCK(AVG)	0.682	<0.75	ns	1,2,3,4,10
Supported CL Settings			14, 16, 18, 20, 22, 24, 25		nCK	
Supported nRCD Timings minimum			10		nCK	
Supported nRP Timings minimum			10		nCK	
Supported CWL Settings			9, 10, 11, 12, 14,16, 18, 20		nCK	

18.3 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-3DS-1600, 1866, 2133, 2400, 2666 and 2933 Speed Bin Tables are valid only when Gear_Down mode is disabled.

1) The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2) tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.937 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 12 calculation.
3) tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071ns or 0.937 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4) 'Reserved' settings are not allowed. User must program a different value.
5) 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6) Any DDR4-3DS-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7) Any DDR4-3DS-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8) Any DDR4-3DS-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9) Any DDR4-3DS-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10) Any DDR4-3DS-2933 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11) 13.75ns is minimum tRCD when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25ns
12) 12.85ns is minimum tRCD when operating by DDR4-1866L-3DS2B at tCK(AVG).min=1.071ns
13) 17.14 ns is the minimum tAA when operating in DDR4-1866N-3DS2B at tCK(AVG).min=1.071ns.
14) 13.75ns is minimum tRP when operating by DDR4-1600K-3DS2B at tCK(AVG).min=1.25ns

19. ELECTRICAL CHARACTERISTICS & AC TIMING

19.1 Reference Load for AC Timing and Output Slew Rate

Figure 23 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

Ron nominal of DQ, DQS_t and DQS_c drivers uses 34 ohms to specify the relevant AC timing parameter values of the device.

The maximum DC High level of Output signal = 1.0 * VDDQ,

The minimum DC Low level of Output signal = {34 /(34 + 50)} *VDDQ = 0.4* VDDQ

The nominal reference level of an Output signal can be approximated by the following:

The center of maximum DC High and minimum DC Low = {(1 + 0.4) / 2} * VDDQ = 0.7 * VDDQ

The actual reference level of Output signal might vary with driver Ron and reference load tolerances. Thus, the actual reference level or midpoint of an output signal is at the widest part of the output signal's eye. Prior to measuring AC parameters, the reference level of the verification tool should be set to an appropriate level.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

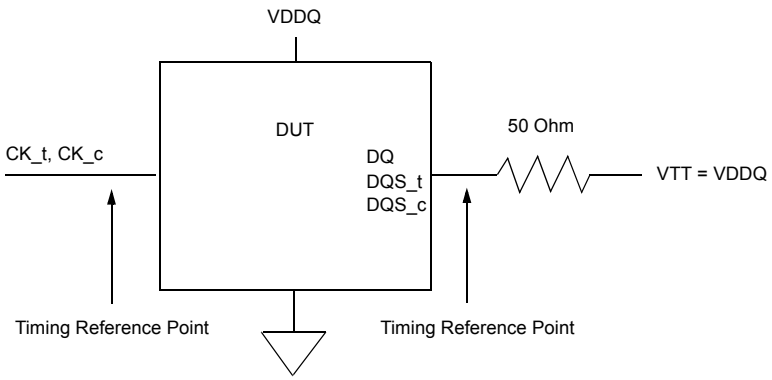


Figure 23. Reference Load for AC Timing and Output Slew Rate

19.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

[Table 55] tREFI by device density

Parameter	Symbol		16Gb	Units	NOTE
All Bank Refresh to active/refresh cmd time	tRFC		350	ns	
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	µs	
		85 °C < T_{CASE} ≤ 95°C	3.9	µs	1

NOTE :

1) Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

19.3 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the DDR4 SDRAM device.

19.3.1 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject t o production test.

19.3.2 Definition for tCK(avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK(abs)j \right) / N \qquad N = 200$$

19.3.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj \right) / \{ N \times tCK(avg) \} \quad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCLj \right) / \{ N \times tCK(avg) \} \quad N = 200$$

19.3.4 Definition for tERR(nper)

tERR is defined as the cumulative error across n consecutive cycles of n x tCK(avg). tERR is not subject to production test.

20. TIMING PARAMETERS BY SPEED GRADE

[Table 56] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2933

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing															
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	<1.5	1.071	<1.25	0.937	<1.071	0.833	<0.937	0.750	<0.833	0.682	<0.750	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN : tCK(avg)min + tJIT(per)min_tot MAX : tCK(avg)max + tJIT(per)max_tot												tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	-38	38	-34	34	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	-19	19	-17	17	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	-30	30	-27	27	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	-	125	-	107	-	94	-	83	-	75	-	68	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	-	60	-	55	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	-55	55	-50	50	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	-73	73	-66	66	-60	60	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	-73	73	-66	66	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	-78	78	-71	71	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	-83	83	-75	75	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	-87	87	-79	79	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	-91	91	-83	83	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	-94	94	-85	85	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	-96	96	-88	88	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	-110	110	-99	99	-90	90	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	-101	101	-92	92	ps	
Cumulative error across 13 cycles	tERR(13per)	-172	172	-147	147	-129	129	-114	114	-103	103	-93	93	ps	
Cumulative error across 14 cycles	tERR(14per)	-175	175	-150	150	-131	131	-116	116	-104	104	-95	95	ps	
Cumulative error across 15 cycles	tERR(15per)	-178	178	-152	152	-133	133	-118	118	-106	106	-97	97	ps	
Cumulative error across 16 cycles	tERR(16per)	-180	189	-155	155	-135	135	-120	120	-108	108	-98	98	ps	
Cumulative error across 17 cycles	tERR(17per)	-183	183	-157	157	-137	137	-122	122	-110	110	-100	100	ps	
Cumulative error across 18 cycles	tERR(18per)	-185	185	-159	159	-139	139	-124	124	-112	112	-101	101	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	MIN : tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) MAX : tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)												ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	115	-	100	-	80	-	62	-	55	-	48	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	140	-	125	-	105	-	87	-	80	-	73	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	145	-	138	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	385	-	365	-	ps	
Command and Address Timing															
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 6.250 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	max(5 nCK, 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK, 6ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK, 5ns)		Max(4nCK, 4.2ns)		Max(4nCK, 3.7ns)		Max(4nCK, 3.3ns)	-	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK, 5ns)		Max(4nCK, 4.2ns)		Max(4nCK, 3.7ns)		Max(4nCK, 3.3ns)	-	Max(4nCK, 3ns)	-	Max(4nCK, 2.7ns)	-	nCK	34

[Table 56] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2933

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK, 7.5ns)		Max(4nCK, 6.4ns)		Max(4nCK, 6.4ns)		Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK, 6ns)		Max(4nCK, 5.3ns)		Max(4nCK, 5.3ns)		Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK, 6ns)		Max(4nCK, 5.3ns)		Max(4nCK, 5.3ns)		Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	Max(4nCK, 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,35ns)		Max(28nCK,30ns)		Max(28nCK,30ns)		Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,25ns)		Max(20nCK,23ns)		Max(20nCK,21ns)		Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,20ns)		Max(16nCK,17ns)		Max(16nCK,15ns)		Max(16nCK,13ns)	-	Max(16nCK,12ns)	-	Max (16nCK, 10.875ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	Max (2nCK, 2.5ns)	-	ns	1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC_DM	tWR+max (4nCK,3.75 ns)	-	tWR+max (5nCK,3.75 ns)	-	tWR+max (5nCK,3.75 ns)	-	tWR+max (5nCK,3.75 ns)	-	tWR+max (5nCK,3.75 ns)	-	tWR+max (5nCK,3.75 ns)	-	ns	1, 28
Delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+ max (4nCK,3.75 ns)	-	tWTR_S+ max (5nCK,3.75 ns)	-	tWTR_S+ max (5nCK,3.75 ns)	-	tWTR_S+ max (5nCK,3.75 ns)	-	tWTR_S+ max (5nCK,3.75 ns)	-	tWTR_S+ max (5nCK,3.75 ns)	-	ns	2, 29, 34
Delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (4nCK,3.75 ns)	-	tWTR_L+max (5nCK,3.75 ns)	-	tWTR_L+max (5nCK,3.75 ns)	-	tWTR_L+max (5nCK,3.75 ns)	-	tWTR_L+max (5nCK,3.75 ns)	-	tWTR_L+max (5nCK,3.75 ns)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-	nCK	50
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-		
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))												nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS falling edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47
CS_n to Command Address Latency															
CS_n to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	max(3 nCK, 3.748 ns)	-	nCK	
Mode Register Set command cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing															
DQS_t, DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	-	0.18	-	0.19	tCK(avg)/2	13,18,39,49
DQ output hold time per group, per access from DQS_t, DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	0.74	-	0.72	-	tCK(avg)/2	13,17,18,39,49
Data Valid Window per device, per UI: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	0.64	-	0.64	-	UI	17,18,39,49
Data Valid Window, per pin, per UI: (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	0.72	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	-	170	-	165	ps	39
Data Strobe Timing															

[Table 56] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2933

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
DQS_t, DQS_c differential READ Pre-amble (1 clock preamble)	tRPRE	0.9	NOTE44	0.9	NOTE44	0.9	NOTE44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	40
DQS_t, DQS_c differential READ Preamble (2 clock preamble)	tRPRE2	NA	NA	NA	NA	NA	NA	1.8	NOTE 44	1.8	NOTE 44	1.8	NOTE 44	tCK	41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	
DQS_t, DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t, DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble (1 clock preamble)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
DQS_t, DQS_c differential WRITE Preamble (2 clock preamble)	tWPRE2	NA		NA		NA		1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	-330	175	-310	170	-280	165	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	-	170	-	165	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	42
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (2 clock preamble)	tDQSS2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	tCK	43
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	-175	175	-170	170	-165	165	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	370	-	330	-	310	-	290	-	270	-	265	ps	37,38,39
MPSM Timing															
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	$t_{MOD(min)}$ + $t_{CPDED(min)}$	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) +tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCP-DED(min)	-	$t_{MOD(min)}$ +$t_{CP-DED(min)}$	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	tCKSRX(min)	-	$t_{CKSRX(min)}$	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	$t_{XS(min)}$	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) +tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	tXMP(min) + tXS-DLL(min)	-	$t_{XMP(min)}$ + $t_{XSDLL(min)}$	-		
CS setup time to CKE	tMPX_S	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	tIS(min) + tIH(min)	-	$t_{IS(min)}$ + $t_{IH(min)}$	-		
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	tXP(min)	-	$t_{XP(min)}$	-		
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	tXMP-10ns	12	t_{XMP}-10ns	ns	51
Calibration Timing															
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing															
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	max (5nCK,tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	

[Table 56] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2933

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK	
Power Down Timing															
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK,5ns)	-	max(3nCK,5ns)	-	max(3nCK,5ns)	-	max(3nCK,5ns)	-	max(3nCK,5ns)	-	max(3nCK,5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing															
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	max(16nCK,10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		tMOD		tMOD			
ODT Timing															
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.28	0.72	0.26	0.74	tCK(avg)	
Write Leveling Timing															
First DQS_t/DQS_c rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_c crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_c crossing to rising CK_t, CK_c crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	0	2	0	2	ns	
CA Parity Timing															

[Table 56] Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2933

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-2933		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	72	144	80	160	88	176	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	-	64	-	71	-	78	nCK	
Parity Latency	PL	4		4		4		5		5		6		nCK	
CRC Error Reporting															
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	6	10	6	10	nCK	
Geardown timing															
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-	-	-	-	-	-	-	-	tXPR	-	tXPR	-		
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-	-	-	-	-	-	-	-	tXS	-	tXS	-		
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	-	-	-	-	-	-	tMOD + 4tCK	-	tMOD + 4tCK	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-	-	-	-	-	-	-	-	tMOD	-	tMOD	-		27
Geardown setup time	tGEAR_setup	-	-	-	-	-	-	-	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	-	-	-	-	-	-	2	-	2	-	nCK	
tREFI															
tRFC1 (min)	16Gb	350	-	350	-	350	-	350	-	350	-	350	-	ns	34
tRFC2 (min)	16Gb	260	-	260	-	260	-	260	-	260	-	260	-	ns	34
tRFC4 (min)	16Gb	160	-	160	-	160	-	160	-	160	-	160	-	ns	34

NOTE :

1) Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2) A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3) Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4) tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK following rounding algorithm defined in "20.1 Rounding Algorithms".
5) WR in clock cycles as programmed in MR0.
6) tREFI depends on TOPER.
7) CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8) For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12) The max values are system dependent.
13) DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER.
14) The deterministic component of the total timing.
15) DQ to DQ static offset relative to strobe per group.
16) This parameter will be characterized and guaranteed by design.
17) When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock).
18) DRAM DBI mode is off.
19) DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22) There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23) tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24) tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25) Total jitter includes the sum of deterministic and random jitter terms for a specified BER.
26) The deterministic jitter component out of the total jitter. This parameter is characterized and guaranteed by design.
27) This parameter has to be even number of clocks
28) When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29) When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30) When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31) After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32) After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33) Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34) Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35) This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36) DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2.
37) applied when DRAM is in DLL ON mode.
38) Assume no jitter on input clock signals to the DRAM.
39) Value is only valid for RONNOM = 34 ohms.
40) 1tCK toggle mode with setting MR4:A11 to 0.
41) 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666 and 2933 speed grade.
42) 1tCK mode with setting MR4:A12 to 0.
43) 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666 and 2933 speed grade.
44) The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. See Figure “Clock to Data Strobe Relationship” in Operation datasheet. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode which is illustrated in “Read Preamble” section.
45) DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point
46) last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High
47) VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48) The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See Figure “Clock to Data Strobe Relationship” in Operation datasheet.
49) Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.
50) For MR7 commands, the minimum delay to a subsequent non-MRS command is 5nCK.
51) tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

20.1 Rounding Algorithms

Software algorithms for calculation of timing parameters are subject to rounding errors from many sources. For example, a system may use a memory clock with a nominal frequency of 933.33... MHz, or a clock period of 1.0714... ns. Similarly, a system with a memory clock frequency of 1066.66... MHz yields mathematically a clock period of 0.9375... ns. In most cases, it is impossible to express all digits after the decimal point exactly, and rounding must be done because the DDR4 SDRAM specification establishes a minimum granularity for timing parameters of 1 ps.

Rules for rounding must be defined to allow optimization of device performance without violating device parameters. These algorithms rely on results that are within correction factors on device testing and specification to avoid losing performance due to rounding errors.

These rules are:

- Clock periods such as tCKAVGmin are defined to 1 ps of accuracy; for example, 0.9375... ns is defined as 937 ps and 1.0714... ns is defined as 1071 ps.
- Using real math, parameters like tAAmin, tRCDmin, etc. which are programmed in systems in numbers of clocks (nCK) but expressed in units of time (in ns) are divided by the clock period (in ns) yielding a unitless ratio, a correction factor of 2.5% is subtracted, then the result is set to the next higher integer number of clocks:

nCK = ceiling [(parameter_in_ns / application_tCK_in_ns) - 0.025]

- Alternatively, programmers may prefer to use integer math instead of real math by expressing timing in ps, scaling the desired parameter value by 1000, dividing by the application clock period, adding an inverse correction factor of 97.4%, dividing the result by 1000, then truncating down to the next lower integer value:

nCK = truncate [{(parameter_in_ps x 1000) / (application_tCK_in_ps) + 974} / 1000]

- Either algorithm yields identical results

20.2 The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal with BER of 1e-16; any input signal encroaching within the Rx Mask is subject to being invalid data. The Rx Mask is the receiver property for each DQ input pin and it is not the valid data-eye.

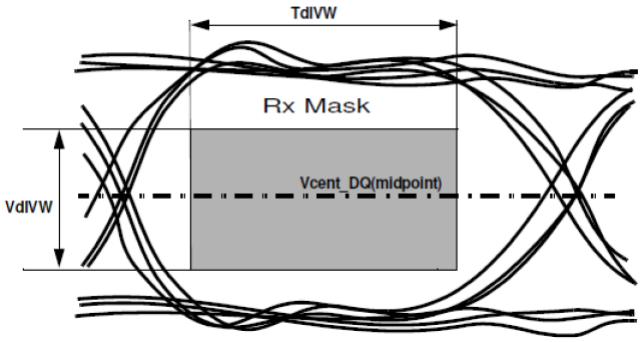


Figure 24. DQ Receiver(Rx) compliance mask

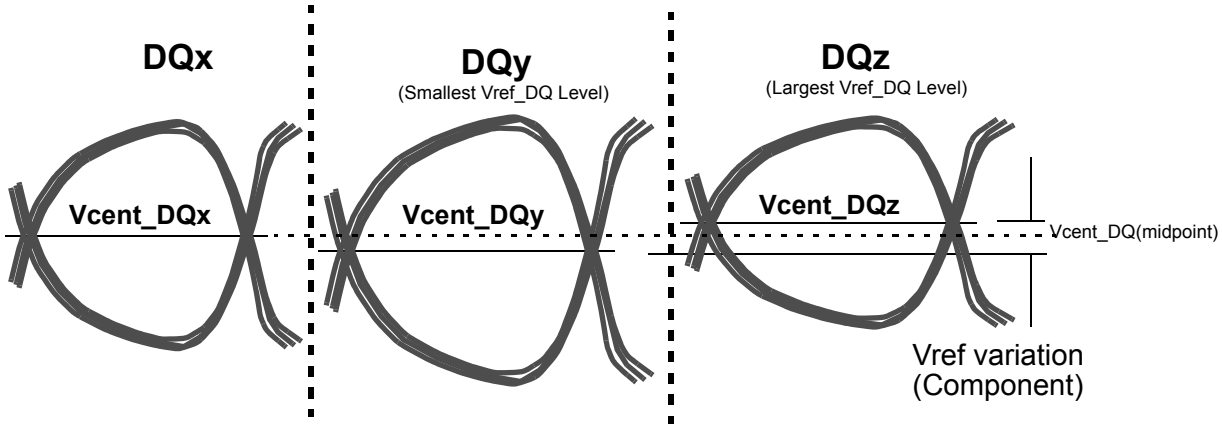
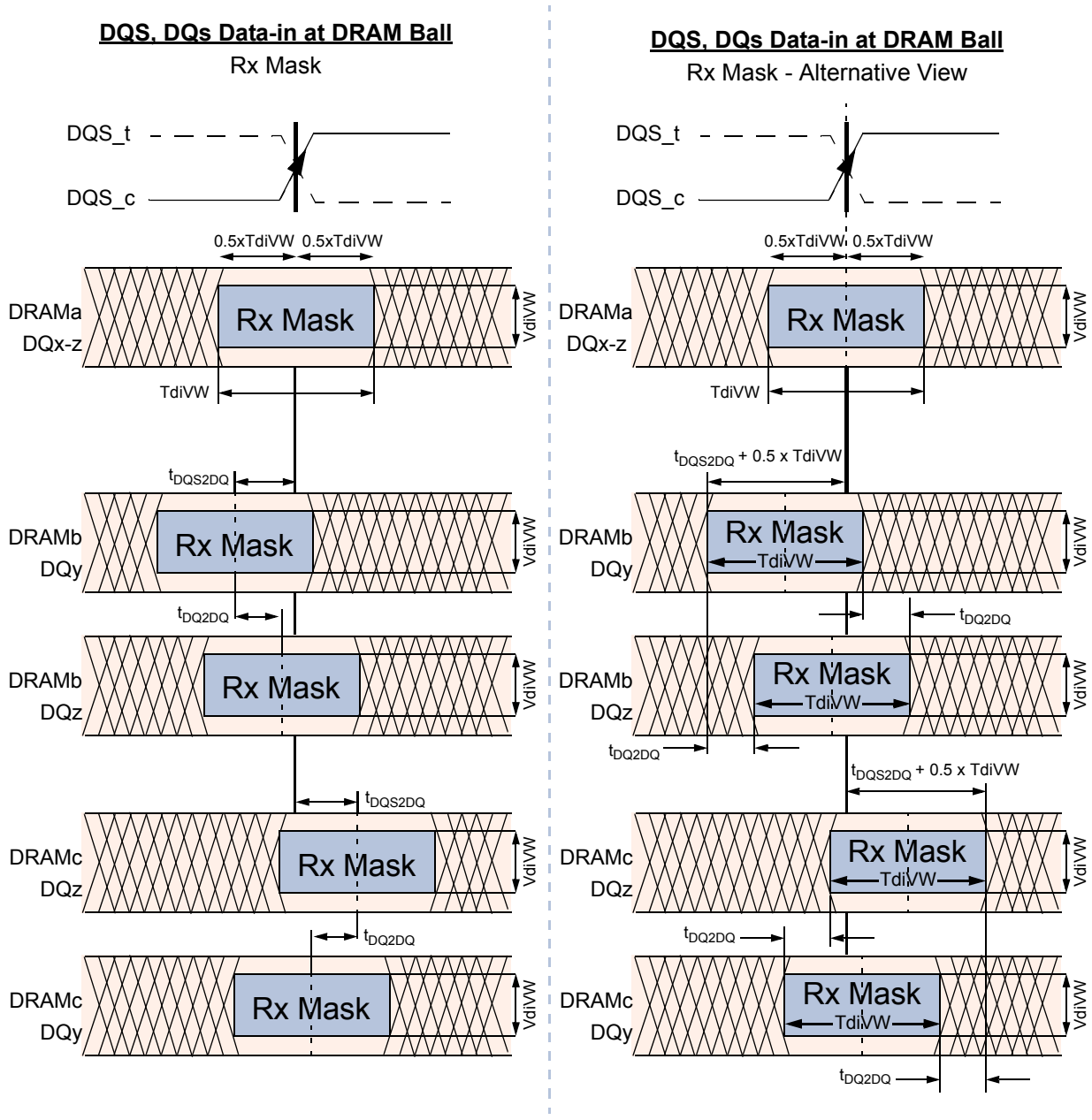


Figure 25. Vcent_DQ Variation to Vcent_DQ(midpoint)

The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values.

Vcent_DQ is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 25. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.



NOTE : DQx represents an optimally centered mask.
DQy represents earliest valid mask.
DQz represents latest valid mask.

NOTE : DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with early skews (negative t_{DQS2DQ}).
DRAMc represents a DRAM with delayed skews (positive t_{DQS2DQ}).

NOTE : Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch.
TdiPW is not shown; composite data-eyes shown would violate TdiPW.
VCENT DQ(midpoint) is not shown but is assummed to be midpoint of VdiVW..

Figure 26. DQS to DQ and DQ to DQ Timings at DRAM Balls

All of the timing terms in Figure 26 are measured at the VdIVW voltage levels centered around Vcent_DQ and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 27 below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1

srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

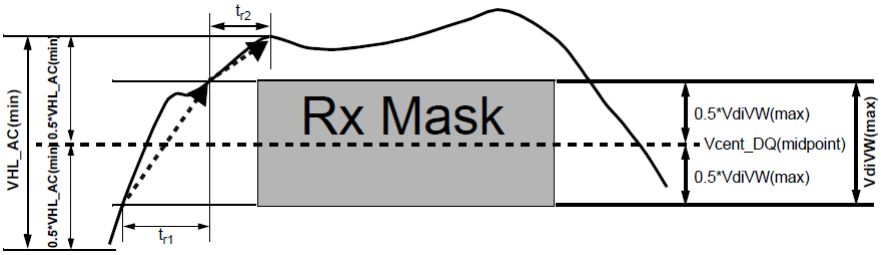


Figure 27. Slew Rate Conditions For Rising Transition

The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure 28 below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1

srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)

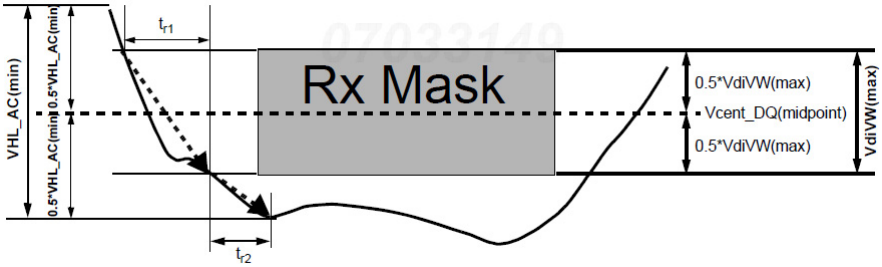


Figure 28. Slew Rate Conditions For Falling Transition

[Table 57] DRAM DQs In Receive Mode;

Symbol	Parameter	1600/1866/2133		2400		2666		2933		Unit	NOTE
		min	max	min	max	min	max	min	max		
VdIVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	115	mV	1,2,10
TdIVW	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	UI*	1,2,10
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	145	-	mV	3,4,10
TdIPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	UI*	5,10
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	UI*	6, 10
tDQ2DQ	Rx Mask DQ to DQ offset	-	0.1	-	0.1	-	0.105	-	0.115	UI*	7
srr1, srf1	Input Slew Rate over VdIVW if tCK >0.937ns	1.0	9	1.0	9	1.0	9	1.0	9	V/ns	8,10
	Input Slew Rate over VdIVW if 0.937ns > tCK >= 0.625ns	-	-	1.25	9	1.25	9	1.25	9	V/ns	8,10
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2*srf1	9	0.2*srf1	9	0.2*srr1	9	0.2*srr1	9	V/ns	9,10

*** UI=tck(avg)min/2**

NOTE :

1) Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(midpoint) after VrefDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER = e-16 when the RxMask is not violated.
2) Defined over the DQ internal Vref range 1.
3) See Overshoot and Undershoot Specifications.
4) DQ input pulse signal swing into the receiver must meet or exceed VIHL AC(min). VIHL_AC(min) is to be achieved on an UI basis when a rising and falling edge occur in the same UI, i.e. a valid TdiPW.
5) DQ minimum input pulse width defined at the Vcent_DQ(midpoint).
6) DQS to DQ offset is skew between DQS and DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls over process, voltage, and temperature.
7) DQ to DQ offset is skew between DQs within a nibble (x4) or word (x8, x16) at the DDR4 SDRAM balls for a given component over process, voltage, and temperature.
8) Input slew rate over VdIVW Mask centered at Vcent_DQ(midpoint). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7 V/ns of each other.
9) Input slew rate between VdIVW Mask edge and VIHL_AC(min) points.
10) All Rx Mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW(min), VdiVW(max), and minimum slew rate limits, then either TdiVW(min) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.

20.3 Command, Control, and Address Setup, Hold, and Derating

The total tIS (setup time) and tIH (hold time) required is calculated to account for slew rate variation by adding the data sheet tIS (base) values, the VIL(AC)/VIH(AC) points, and tIH (base) values, the VIL(DC)/VIH(DC) points; to the ΔtIS and ΔtIH derating values, respectively. The base values are derived with single-end signals at 1V/ns and differential clock at 2V/ns. Example: tIS (total setup time) = tIS (base) + ΔtIS.

For a valid transition, the input signal has to remain above/below VIH(AC)/VIL(AC) for the time defined by tVAC.

Although the total setup time for slow slew rates might be negative (for example, a valid input signal will not have reached VIH(AC)/ VIL(AC) at the time of the rising clock transition), a valid input signal is still required to complete the transition and to reach VIH(AC)/ VIL(AC). For slew rates that fall between the values listed in derating tables, the derating values may be obtained by linear interpolation.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)max that does not ring back above VIL(DC)max. Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC)max and the first crossing of VIH(AC)min that does not ring back below VIH(DC)min. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC)min and the first crossing of VIL(AC)minthat does not ring back above VIL(DC)max.

[Table 58] Command, Address, Control Setup and Hold Values

DDR4	1600	1866	2133	2400	2666	2933	Unit	Reference
tIS(base, AC100)	115	100	80	62	-	-	ps	VIH/L(ac)
tIH(base, DC75)	140	125	105	87	-	-	ps	VIH/L(dc)
tIS(base, AC 90)	-	-	-	-	55	48	ps	VIH/L(ac)
tIH(base, DC 65)	-	-	-	-	80	73	ps	VIH/L(dc)
tIS/tIH @ VREF	215	200	180	162	145	138	ps	

NOTE :
1) Base ac/dc referenced for 1V/ns slew rate and 2 V/ns clock slew rate.
2) Values listed are referenced only; applicable limits are defined elsewhere.

[Table 59] Command, Address, Control Input Voltage Values

DDR4	1600	1866	2133	2400	2666	2933	Unit	Reference
VIH.CA(AC)min	100	100	100	100	90	90	mV	VIH/L(ac)
VIH.CA(DC)min	75	75	75	75	65	65	mV	VIH/L(dc)
VIL.CA(DC)max	-75	-75	-75	-75	-65	-65	mV	VIH/L(dc)
VIL.CA(AC)max	-100	-100	-100	-100	-90	-90	mV	VIH/L(ac)

NOTE :
1) Command, Address, Control input levels relative to VREFCA.
2) Values listed are referenced only; applicable limits are defined elsewhere.

[Table 60] Derating values DDR4-1600/1866/2133/2400 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																
		CK_t, CK_c Differential Slew Rate														
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	76	54	76	55	77	56	79	58	82	60	86	64	94	73	111	89
	6	73	53	74	53	75	54	77	56	79	58	83	63	92	71	108	88
	5	70	50	71	51	72	52	74	54	76	56	80	60	88	68	105	85
	4	65	46	66	47	67	48	69	50	71	52	75	56	83	65	100	81
	3	57	40	57	41	58	42	60	44	63	46	67	50	75	58	92	75
	2	40	28	41	28	42	29	44	31	46	33	50	38	58	46	75	63
	1.5	23	15	24	16	25	17	27	19	29	21	33	25	42	33	58	50
	1	-10	-10	-9	-9	-8	-8	-6	-6	-4	-4	0	0	8	8	25	25
	0.9	-17	-14	-16	-14	-15	-13	-13	-10	-11	-8	-7	-4	1	4	18	21
	0.8	-26	-19	-25	-19	-24	-18	-22	-16	-20	-14	-16	-9	-7	-1	9	16
	0.7	-37	-26	-36	-25	-35	-24	-33	-22	-31	-20	-27	-16	-18	-8	-2	9
	0.6	-52	-35	-51	-34	-50	-33	-48	-31	-46	-29	-42	-25	-33	-17	-17	0
	0.5	-73	-48	-72	-47	-71	-46	-69	-44	-67	-42	-63	-38	-54	-29	-38	-13
	0.4	-104	-66	-103	-66	-102	-65	-100	-63	-98	-60	-94	-56	-85	-48	-69	-31

NOTE :
1) VIH/L(ac) = +/-100mV, VIH/L(dc) = +/-75mV; relative to VREFCA.

[Table 61] Derating values DDR4-2666/2933 tIS/tIH - ac/dc based

ΔtIS, ΔIH derating in [ps] AC/DC based [1]																	
		CK_t, CK_c Differential Slew Rate															
		10V/ns		8V/ns		6V/ns		4V/ns		3.0V/ns		2.0V/ns		1.5V/ns		1V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD, ADDR, CNTL Input Slew rate V/ns	7	68	47	69	47	70	48	72	50	73	52	77	56	85	63	100	78
	6	66	45	67	46	68	47	69	49	71	50	75	54	83	62	98	77
	5	63	43	64	44	65	45	66	46	68	48	72	52	80	60	95	75
	4	59	40	59	40	60	41	62	43	64	45	68	49	75	56	90	71
	3	51	34	52	35	53	36	54	38	56	40	60	43	68	51	83	66
	2	36	24	37	24	38	25	39	27	41	29	45	33	53	40	68	55
	1.5	21	13	22	13	23	14	24	16	26	18	30	22	38	29	53	44
	1	-9	-9	-8	-8	-8	-8	-6	-6	-4	-4	0	0	8	8	23	23
	0.9	-15	-13	-15	-12	-14	-11	-12	-9	-10	-7	-6	-4	1	4	16	19
	0.8	-23	-17	-23	-17	-22	-16	-20	-14	-18	-12	-14	-8	-7	-1	8	14
	0.7	-34	-23	-33	-22	-32	-21	-30	-20	-28	-18	-25	-14	-17	-6	-2	9
	0.6	-47	-31	-47	-30	-46	-29	-44	-27	-42	-25	-38	-22	-31	-14	-16	1
	0.5	-67	-42	-66	-41	-65	-40	-63	-38	-61	-36	-58	-33	-50	-25	-35	-10
	0.4	-95	-58	-95	-57	-94	-56	-92	-54	-90	-53	-86	-49	-79	-41	-64	-26

NOTE :
1) VIH/L(ac) = +/-90 mV, VIH/L(dc) = +/- 65 mV; relative to VREFCA

20.4 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

[Table 62] Function Matrix (By ORG. V:Supported, Blank:Not supported)

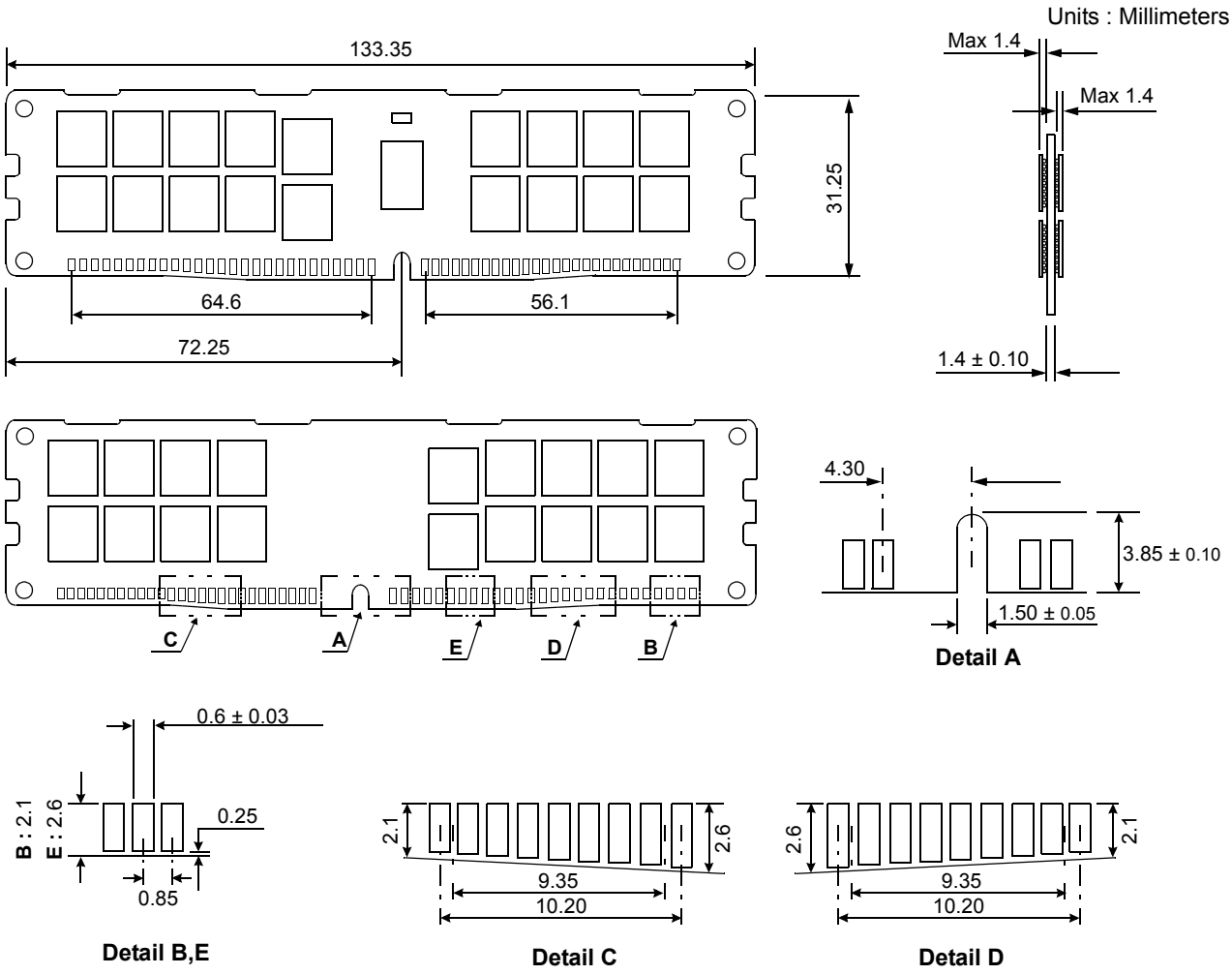
Functions	x4	NOTE
Write Leveling	V	
Temperature controlled Refresh	V	
Low Power Auto Self Refresh	V	
Fine Granularity Refresh	V	
Multi Purpose Register	V	
Data Mask		
Data Bus Inversion		
TDQS		
ZQ calibration	V	
DQ Vref Training	V	
Per DRAM Addressability	V	
Mode Register Readout	V	
CAL	V	
WRITE CRC	V	
CA Parity	V	
Control Gear Down Mode	V	
Programmable Preamble	V	
Maximum Power Down Mode	V	
Boundary Scan Mode		
Additive Latency	V	
3DS	V	

[Table 63] Function Matrix (By Speed. V:Supported, Blank:Not supported)

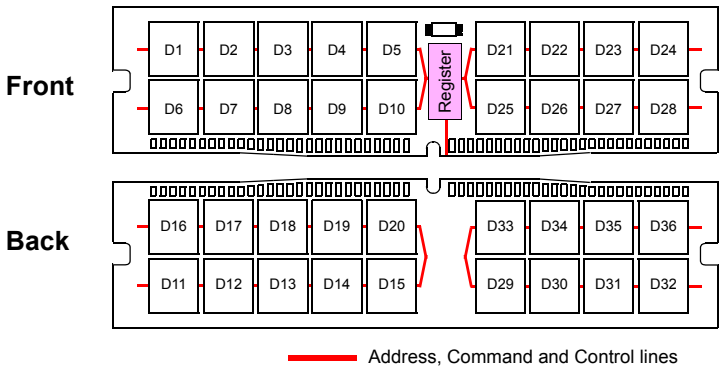
Functions	DLL Off mode	DLL On mode			NOTE
	equal or slower than 250Mbps	1600/1866/2133 Mbps	2400Mbps	2666/2933Mbps	
Write Leveling	V	V	V	V	
Temperature controlled Refresh	V	V	V	V	
Low Power Auto Self Refresh	V	V	V	V	
Fine Granularity Refresh	V	V	V	V	
Multi Purpose Register	V	V	V	V	
Data Mask	V	V	V	V	
Data Bus Inversion	V	V	V	V	
TDQS		V	V	V	
ZQ calibration	V	V	V	V	
DQ Vref Training	V	V	V	V	
Per DRAM Addressability		V	V	V	
Mode Register Readout	V	V	V	V	
CAL		V	V	V	
WRITE CRC		V	V	V	
CA Parity		V	V	V	
Control Gear Down Mode				V	
Programmable Preamble (= 2tCK)			V	V	
Maximum Power Down Mode		V	V	V	
Boundary Scan Mode	V	V	V	V	
3DS	V	V	V	V	

21. PHYSICAL DIMENSIONS

21.1 16Gbx4(3DS 4H) based 32Gx72 Module (M393ABG40M5B)



21.1.1 x72 DIMM, populated as 2 physical ranks / 4 logical ranks of x4 DDR4 SDRAMs



The used device is 16G x4(3DS 4H) DDR4 SDRAM, FBGA.
DDR4 SDRAM Part NO : K4ACG045WM-5C**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

22. PRODUCT REGULATORY COMPLIANCE

22.1 Product Regulatory Compliance And Certifications

[Table 64] Samsung Module products comply with the following:

Category	Certifications	Region or Country	Standard
RoHS	CE	E.U. (Europe)	EN50581:2012

For more details are available at the following internet address:
https://www.samsung.com/semiconductor/about-us/global-compliance/

MANUFACTURER'S DECLARATION FOR CE CERTIFICATION

Hereby, Samsung Electronics declares that the product above is in compliance with Directive 2011/65/EU.

EU Compliance Contact information
Samsung Electronics (UK) Ltd, Euro QA Lab, Yateley, GU46 6GG. UK

Waste Electrical and Electronic Equipment

This symbol on the product or on its packaging indicates that this product must not be disposed of with your other household waste. Instead, it is your responsibility to dispose of your waste equipment by handing it over to a designated collection point for the recycling of waste electrical and electronic equipment. The separate collection and recycling of your waste equipment at the time of disposal will help to conserve natural resources and ensure that it is recycled in a manner that protects human health and the environment. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service, or the shop where you purchased the product.