MOS INTEGRATED CIRCUIT

M 4027

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

- POWER SUPPLY V_{DD}= 12V, V_{CC}= 5V, V_{BB}= -5V (ALL WITH ± 10% TOLERANCE)
- ALL INPUTS ARE LOW CAPACITANCE AND TTL COMPATIBLE
- INPUT LATCHES FOR ADDRESSES, CHIP SELECT AND DATA IN
- INPUTS PROTECTED AGAINST STATIC CHARGE
- THREE-STATE TTL COMPATIBLE OUTPUT
- OUTPUT DATA LATCHED AND VALID INTO NEXT CYCLE
- ECL COMPATIBLE ON V_{BB} POWER SUPPLY (-5.7V)
- LOW POWER CONSUMPTION: ACTIVE POWER UNDER 470 mW
  STANDBY POWER UNDER 27 mW
- ORGANIZATION 4096 x 1 BIT IN 16-PIN STD PACKAGE
- FUNCTIONAL AND PIN COMPATIBLE WITH MK4027
- ACCESS TIME: TYPE M 4027-2 150 ns
  TYPE M 4027-3 200 ns
  TYPE M 4027-4 250 ns

The M 4027 is a 4096 word by 1 bit dynamic N-channel silicon gate MOS RAM. The M 4027 uses a single transistor cell utilizing a dynamic storage technique and dynamic control circuitry with low power dissipation. A unique multiplexing and latching technique for the address inputs permits the M 4027 to be mounted in a standard 16-pin package. The M 4027 incorporates several flexible operating modes. In addition to the usual read and write cycles, read modify write, page mode and RAS-only refresh cycles are available with the M 4027. Page-mode timing is very useful in systems requiring Direct Memory Access (DMA). The device is available in 16-lead dual in-line plastic or ceramic package (metal-seal), and ceramic package (frit-seal).

ABSOLUTE MAXIMUM RATINGS*

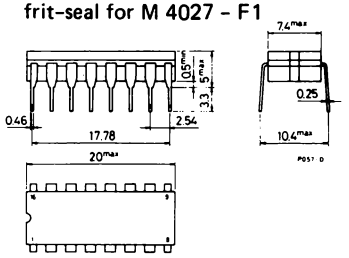
	Voltage on any pin relative to V_{BB}	-0.5 to +20	V
	Voltage on V_{DD}, V_{CC} relative to V_{SS}	-1 to +15	V
	V_{BB}-V_{SS} (V_{DD}-$V_{SS} > 0$)	0	V
T_{op}	Operating temperature	0 to +70	°C
T_{stg}	Storage temperature for ceramic package	-65 to +150	°C
	for plastic package	-55 to +125	°C
I_o	Short circuit output current	50	mA
P_{tot}	Total power dissipation	1	W

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

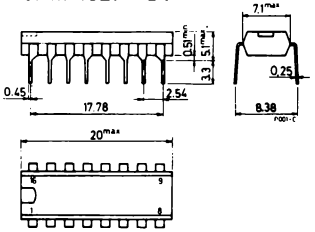
ORDERING NUMBERS: M 4027-2/3/4 B1 for dual in-line plastic package
M 4027-2/3/4 D1 for dual in-line ceramic package, metal-seal
M 4027-2/3/4 F1 for dual in-line ceramic package, frit-seat

MECHANICAL DATA (dimensions in mm)

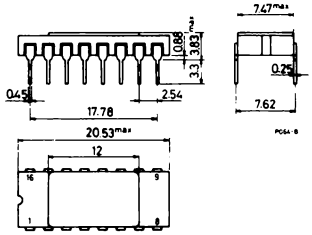
Dual in-line ceramic package
frit-seal for M 4027 - F1



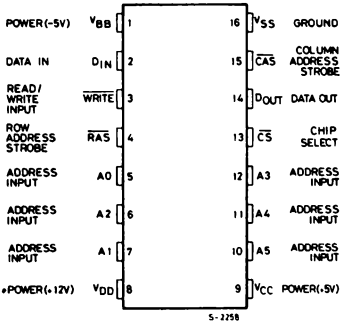
Dual in-line plastic package
for M 4027 - B1



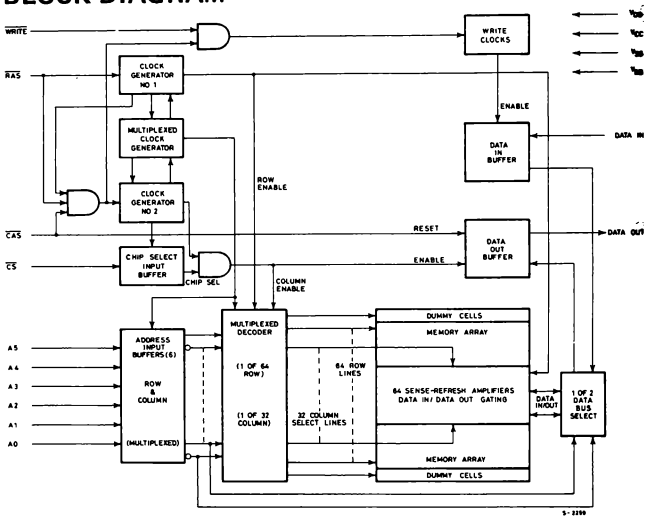
Dual in-line ceramic package
metal-seal for M 4027 - D1



PIN CONNECTIONS



BLOCK DIAGRAM



RECOMMENDED DC OPERATING CONDITIONS[1] (T_{amb}= 0 to 70°C)[4]

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply voltage	10.8	12	13.2	V	2
V_{CC}	Supply voltage	4.5	5	5.5	V	2, 3
V_{SS}	Supply voltage	0	0	0	V	2
V_{BB}	Supply voltage	-4.5	-5	-5.7	V	2
V_{IHC}	Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V	2
V_{IH}	Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.2		7	V	2
V_{IL}	Input low voltage, all inputs	-1		0.8	V	2

DC ELECTRICAL CHARACTERISTICS[1] (T_{amb}= 0 to 70°C)[4] (V_{DD}= 12V ± 10%, V_{CC}= 5V ± 10%, V_{SS}= 0V, V_{BB}= - 5.7 to -4.5V)

Parameter		Values			Unit	Notes
		Min.	Typ.	Max.		
I_{DD1}	Average V_{DD} power supply current			35	mA	5
I_{DD2}	Standby V_{DD} power supply current			2	mA	8
I_{DD3}	Average V_{DD} power supply current during "$\overline{RAS}$ only" cycles			25	mA	
I_{CC}	V_{CC} power supply current				mA	6
I_{BB}	Average V_{BB} power supply current			150	µA	
$I_{I(L)}$	Input leakage current (any input)			10	µA	7
$I_{O(L)}$	Output leakage current			10	µA	8, 9
V_{OH}	Output high voltage (I_{SOURCE}= -5 mA)	2.4			V	
V_{OL}	Output low voltage (I_{SINK}= 3.2 mA)			0.4	V	

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS[1, 10, 15]

(T_{amb} = 0 to 70°C)[4], (V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = 0V, V_{BB} = -5.7 to -4.5V)

Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random read or write cycle time	320		375		380		ns	
t_{RWC}	Read write cycle time	320		375		395		ns	
t_{RMW}	Read modify write cycle time	320		405		470		ns	
t_{RAC}	Access time from row address strobe		150		200		250	ns	11-13
t_{CAC}	Access time from column address strobe		100		135		165	ns	12-13
t_{OFF}	Output buffer turn-off delay		40		50		60	ns	
t_{RP}	Row address strobe precharge time	100		120		120		ns	
t_{RAS}	Row address strobe pulse width	150	10000	200	10000	250	10000	ns	
t_{RSH}	Row address strobe hold time	100		135		165		ns	
t_{CAS}	Column address strobe pulse width	100		135		165		ns	
t_{CSH}	Column address strobe hold time	150		200		250		ns	
t_{RCD}	Row to column strobe delay	20	50	25	65	35	85	ns	14
t_{ASR}	Row address set-up time	0		0		0		ns	
t_{RAH}	Row address hold time	20		25		35		ns	
t_{ASC}	Column address set-up time	-10		-10		-10		ns	
t_{CAH}	Column address hold time	45		55		75		ns	
t_{AR}	Column address hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CSC}	Chip select set-up time	-10		-10		-10		ns	
t_{CH}	Chip select hold time	45		55		75		ns	
t_{CHR}	Chip select hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_T	Transition time (rise and fall)	3	35	5	50	5	50	ns	15
t_{RCS}	Read command set-up time	0		0		0		ns	
t_{RCH}	Read command hold time	0		0		0		ns	
t_{WCH}	Write command hold time	45		55		75		ns	
t_{WCR}	Write command hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write command pulse width	45		55		75		ns	
t_{RWL}	Write command to row strobe lead time	50		70		85		ns	
t_{CWL}	Write command to column strobe lead time	50		70		85		ns	
t_{DS}	Data in set-up time	0		0		0		ns	16

AC CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS (cont.)

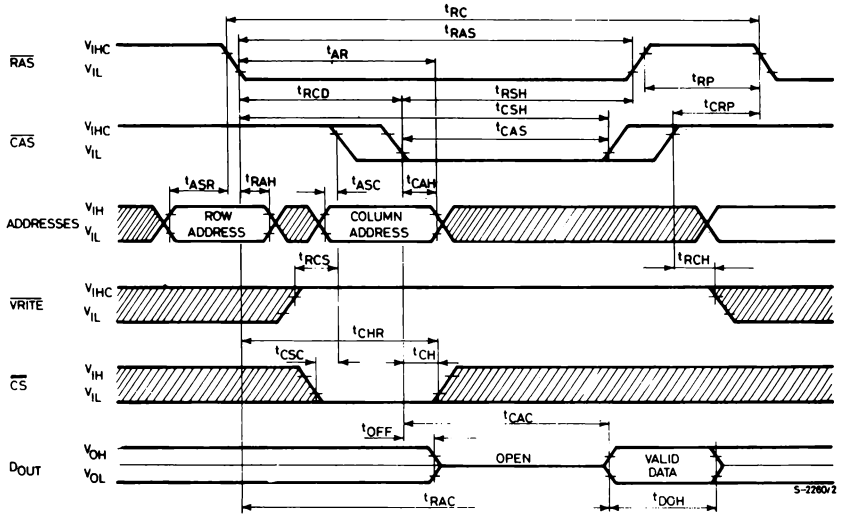
Parameter		Types						Unit	Notes
		M 4027-2		M 4027-3		M 4027-4			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{DH}	Data in hold-time	45		55		75		ns	16
t_{DHR}	Data in hold time referenced to $\overline{RAS}$	95		120		160		ns	
t_{CRP}	Column to row strobe precharge time	0		0		0		ns	
t_{CP}	Column precharge time	60		80		110		ns	
t_{RFSH}	Refresh period		2		2		2	ms	
t_{WCS}	Write command set-up time	0		0		0		ns	17
t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ delay	60		80		90		ns	17
t_{RWD}	RAS to WRITE delay	110		145		175		ns	17
t_{DOH}	Data out hold time	10		10		10		μs	

CAPACITANCES (T_{amb}= 0 to 70°C, V_{DD}= 12V ± 10%; V_{SS}= 0V; V_{BB}= -5.7 to -4.5V)

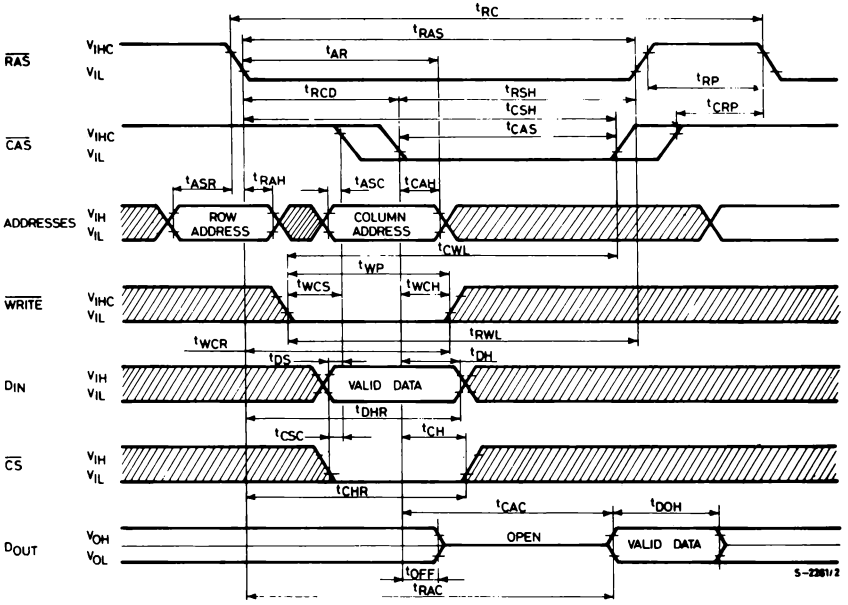
Parameter		Values		Unit	Notes
		Typ.	Max.		
C_{I1}	Input capacitance (A_0-A_5), D_{IN}, $\overline{CS}$	4	5	pF	18
C_{I2}	Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	8	10	pF	18
C_O	Output capacitance (D_{OUT})	5	7	pF	8-18

1. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
2. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.
4. T_{amb} is specified for operation at frequencies to $t_{RC} \geqslant t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all AC parameters are met.
5. Current is proportional to cycle rate. I_{DD1} (max) is measured at the cycle rate specified by t_{RC} (min).
6. I_{CC} depends on output loading. The V_{CC} supply is connected to the output buffer only.
7. All device pins at 0 volts except V_{BB} which is at -5V and the pin under test which is at +10V.
8. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
9. $0V \leqslant V_{out} \leqslant +10V$.
10. AC measurements assume t_T= 5 ns.
11. Assumes that $t_{RCD} \leqslant t_{RCD}$ (max).
12. Assumes that $t_{RCD} \geqslant t_{RCD}$ (max).
13. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
14. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
15. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
16. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in a read/write or read/modify/write cycle only. If $t_{WCS} \geqslant t_{WCS}$ (min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geqslant t_{CWD}$ (min) and $t_{RWD} \geqslant t_{RWD}$ (min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.
18. Effective capacitance is calculated from the equation: $C = \frac{\Delta Q}{\Delta V}$ with ΔV = 3 volts.

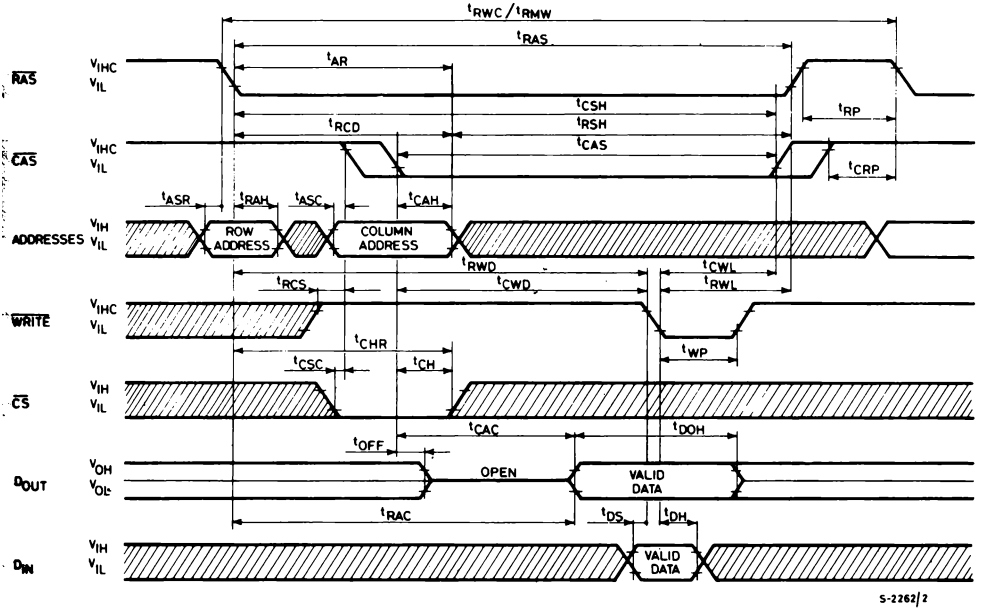
READ CYCLE



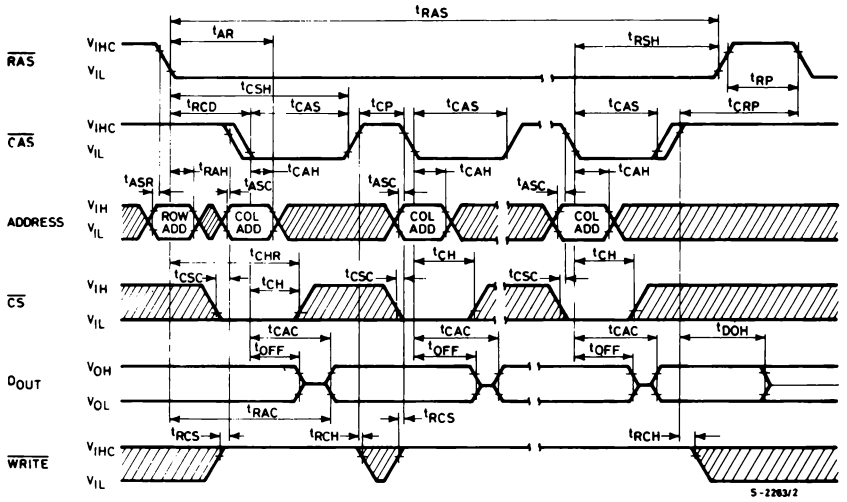
WRITE CYCLE
(early write)



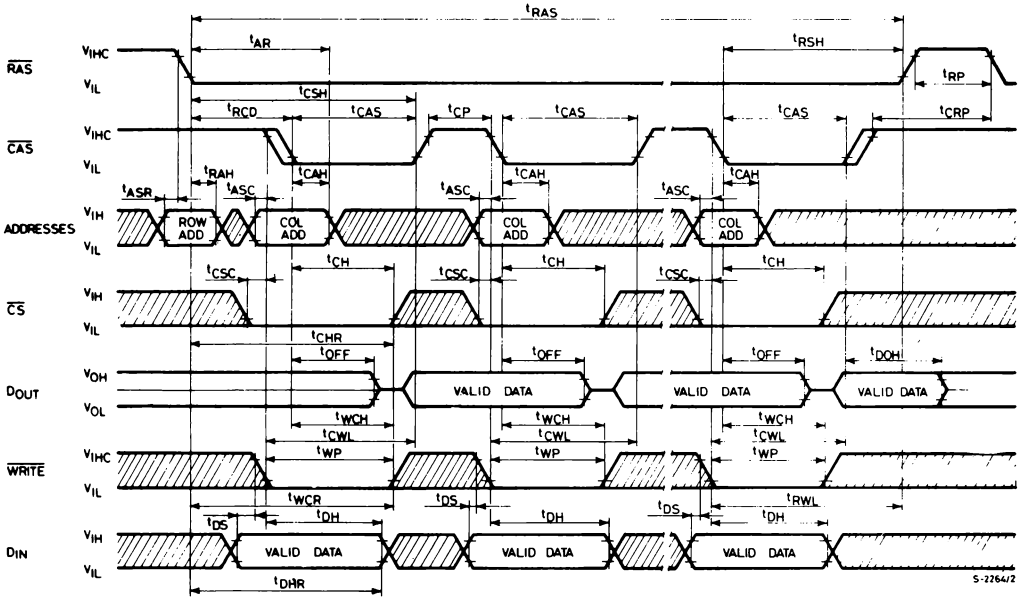
READ WRITE/READ MODIFY-WRITE CYCLE



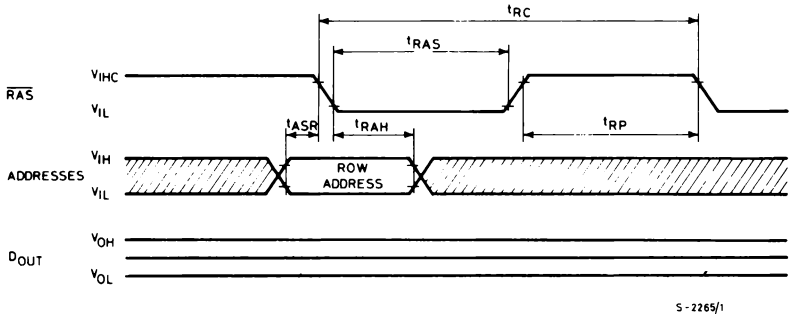
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



RAS ONLY REFRESH CYCLE



ADDRESSING

The 12 address bits required to decode one of 4096 cell locations within the M 4027 are multiplexed onto the 6 address inputs and latched into the on-chip row and column address latches.
Row Address Strobe ($\overline{RAS}$) latches the six row address bits onto the chip. Column Address Strobe ($\overline{CAS}$) latches the six column address bits plus Chip Select ($\overline{CS}$) onto the chip.
Since the internal circuitry allows the columns information to be externally applied to the chip before it is actually required, the hold time requirements for column address and $\overline{CS}$ are also referenced to $\overline{RAS}$. However, this gated $\overline{CAS}$ feature allows the systems designer to compensate for timing skews that may be encountered in the multiplexing operation.
Since the Chip Select signal is not required until $\overline{CAS}$ time, which is well into the memory cycle, its decoding time does not add to system access or cycle time.
Additional timing margin is gained because column address is not required until $\overline{CAS}$ makes its negative transition.
The timing is further simplified by the positive transition of $\overline{CAS}$ not being referenced to the positive transition of $\overline{RAS}$. In fact, $\overline{CAS}$ need not go HIGH until the beginning of the next cycle.

DATA INPUT/OUTPUT

Data to be written into selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active.
The later of this signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In into the latch. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is activated prior to $\overline{CAS}$, the Data In is strobe by $\overline{CAS}$, and set-up time and hold time are referenced to $\overline{CAS}$. If the Data In input is not available at $\overline{CAS}$ time or the cycle is a read-write or read-modify-write, the $\overline{WRITE}$ signal must be delayed until after $\overline{CAS}$. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than to $\overline{CAS}$. (To illustrate this feature, Data In is referenced to $\overline{WRITE}$ in the timing diagram depicting the read-write and page mode write cycles while the "early write" cycle diagram shows Data In referenced to $\overline{CAS}$)
Note that if the chip is unselected ($\overline{CS}$ high at $\overline{CAS}$ time) $\overline{WRITE}$ commands are not executed and, consequently, data stored in the memory is unaffected. Data is retrieved from the memory in read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of memory cycle in which $\overline{CAS}$ is active. Data read from the selected cell will be available at the output within the specified access time.

DATA OUTPUT CONTROL

At the beginning of a memory cycle, the state of the Data Out latch and buffer depend on the previous memory cycle.
Changes in the condition of Data Out latch are initiated by $\overline{CAS}$. The negative transition of $\overline{CAS}$ causes the Data Output (D_{OUT}) to unconditionally go to its open-circuit state. If will remain open-circuited until after the access D_{OUT} time, the will assume the proper state for the type of cycle performed.
If the cycle is a read, read-modify-write, or a delayed write and the chip is selected, then the D_{OUT} latch and buffer will contain the data from the selected cell. This output data is the same polarity (not inverted) as the input data. If the cycle is a write cycle ($\overline{WRITE}$ active low before $\overline{CAS}$ goes low) and the chip is selected, then D_{OUT} will contain the input data.
Once the D_{OUT} goes active, it will remain active until the next negative transition of $\overline{CAS}$.
If the cycle is a $\overline{CAS}$ only cycle (no $\overline{RAS}$ signal), then D_{OUT} will assume the open - circuit state.
The same istrue for normal cycles (both $\overline{RAS}$ and $\overline{CAS}$ present-when the chip is unselected D_{OUT} remains in the open-circuit state until the next negative transition of $\overline{CAS}$.
$\overline{RAS}$ only refresh cycles (no $\overline{CAS}$) have no effect on the D_{OUT}.
However, when $\overline{RAS}$ only refresh cycles are continued for extended periods of time, D_{OUT} may eventually go open-circuit.
If the chip unselected, it will not accept a write command and the D_{OUT} will remain in the open-circuit state.

INPUT/OUTPUT LEVELS

All inputs, including the two address strobes, interface directly with TTL.
The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements.
The 3-state output buffer is a low impedance to V_{CC} for a logic "1" and a low impedance to V_{SS} for a logic "0".
The output resistance to V_{CC} (logic "1" state) is 420 ohm maximum and 135 ohm tipically.
The output resistance to V_{SS} (logic "0" state) is 125 ohm maximum and 35 ohm tipically.
The separate V_{CC} pin allows the output buffer to be powered from supply voltage of the logic to which chip is interfaced.
During battery stand-by operation, the V_{CC} pin may be unpowered without effecting the M 4027 refresh operation.
This allows all system logic, except $\overline{RAS}$ timing circuitry and refresh address logic, to be turned off during battery stand-by to save power.

REFRESH

Refresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 64 row address every two millisecond or less.
Any cycle in which a $\overline{RAS}$ signal occurs, accomplished a refresh operation. A read cycle will refresh the selected row, regardless of the state of the Chip Select ($\overline{CS}$) input.
A write or read-modify-write cycle also refreshes the selected row, but the chip should be unselected to prevent writing data into the selected cell.
If, during a refresh cycle, the M 4027 receives a $\overline{RAS}$ signal but no $\overline{CAS}$ signal, the state of the output will not be affected. However, if "$\overline{RAS}$-only" refresh cycles (when $\overline{RAS}$ is the only signal applied to the chip) are contained for extended periods, the output buffer may eventually lose proper data and go open-circuit.
The output buffer will regain activity with the first cycle in which a $\overline{CAS}$ signal is applied to the chip.

POWER DISSIPATION/STANDBY MODE

Most of the circuitry used in the M 4027 and most of the power drawn is the result of an address strobe edge. Because the power is not drawn during the time the strobe is active, the dynamic power is a function of operating frequency rather than active duty cycle.
Tipically, the power is 170 mW at 1 μsec cycle rate for M 4027 with a worse case power of less than 470 mW at 320 μsec cycle time.
To reduce the overall system power, the Row Address Strobe ($\overline{RAS}$) should be decoded and supplied to only the selected chips.
The $\overline{CAS}$ must be supplied to all chips (to turn off the unselected output).
Those chips that did not receive a $\overline{RAS}$, however, will not dissipate any power on the $\overline{CAS}$ edges, except for that required to turn off the outputs.
If the $\overline{RAS}$ signal is decoded and supplied only the selected chips, then the chip select ($\overline{CS}$) input of all chips can be at a logic 0.
Then chips that receive a $\overline{CAS}$ but no $\overline{RAS}$ will be unselected (output open-circuited) regardless of the Chip Select input.
For refresh cycles, however, either the $\overline{CS}$ input for all chips must be high or the $\overline{CAS}$ input must be held high to prevent several "wire-OR" outputs from turning on with opposing force. Note that the M 4027 will dissipate considerably less power when the refresh operation is accomplished with a "$\overline{RAS}$-only" cycle as opposed to a normal $\overline{RAS}/\overline{CAS}$ memory cycle.

PAGE MODE OPERATION

The "Page mode" feature of the M 4027 allows for successive memory operations at multiple column location of the same row address with increased speed without an increase in power.
This is done by strobing the row address into the chip and keeping the $\overline{RAS}$ signal at logic 0 throughout all successive memory cycles in which the row address is common.
This "Page Mode" of operation will not dissipate the power associated with the negative going edge of $\overline{RAS}$. The time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times. The chip select input ($\overline{CS}$) is operative in page made cycles just as in normal cycles. It is not necessary that the chip be selected during the first operation in sequence of page cycles. Likewise, the $\overline{CS}$ input can be used to select or disable any cycle(s) in a series of page cycles.
This feature allows the page boundary to be extended beyond the 64 column location in a single chip. The page boundary can be extended by applying $\overline{RAS}$ to multiple 4K memory blocks and deconding $\overline{CS}$ to select the proper block.

POWER UP

The M 4027 requires no particular power supply sequencing so long as the Absolute Maximum Rating Conditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, SGS-ATES recommends sequencing of power supplies such that V_{BB} is applied first and removed last. V_{BB} should never be more positive than V_{SS} when power is applied to V_{DD}.
Under system failure condiction in which one or more supplied exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and Data Out to the inactive state. After power is applied to the device, the M 4027 requires several cycles before proper device operation is achieved.
Any 8 cycles which perform refresh are adequate for this purpose.