# MOS INTEGRATED CIRCUIT

# M 4116

PRELIMINARY DATA

## 16384-BIT DYNAMIC RANDOM ACCESS MEMORY

- RECOGNIZED INDUSTRY STANDARD 16-PIN CONFIGURATION
- 150ns ACCESS TIME, 320ns CYCLE (M 4116-2)
  200ns ACCESS TIME, 375ns CYCLE (M 4116-3)
  250ns ACCESS TIME, 410ns CYCLE (M 4116-4)
- ± 10% TOLERANCE ON ALL POWER SUPPLIES (+12V, ±5V)
- LOW POWER: 462 mW ACTIVE, 20 mW STANDBY (MAX)
- OUTPUT DATA CONTROLLED BY $\overline{CAS}$ AND UNLATCHED AT END OF CYCLE TO ALLOW TWO DIMENSIONAL CHIP SELECTION AND EXTENDED PAGE BOUNDARY
- COMMON I/O CAPABILITY USING "EARLY WRITE" OPERATION
- READ-MODIFY-WRITE, $\overline{RAS}$-ONLY REFRESH, AND PAGE-MODE CAPABILITY
- ALL INPUTS TTL COMPATIBLE, LOW CAPACITANCE, AND PROTECTED AGAINST STATIC CHARGE
- 128 REFRESH CYCLES
- MOSTEK 4116 PIN TO PIN REPLACEMENT
- ECL COMPATIBLE ON $V_{BB}$ POWER SUPPLY (-5.7V)

The M 4116 is a new generation MOS dynamic random access memory circuit organized as 16384 words by 1 bit. The technology used to fabricate the M 4116 is double-poly N-channel silicon gate.
This process, coupled with the use of a single transistor dynamic storage cell, provides the maximum possible circuit density and reliability, while maintaining high performance capability. The use of dynamic circuitry through-out, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin.
Multiplexed address inputs permits the M 4116 to be packaged in a standard 16-pin DIP. The device is available in 16-lead dual in-line ceramic package.

## ABSOLUTE MAXIMUM RATINGS*

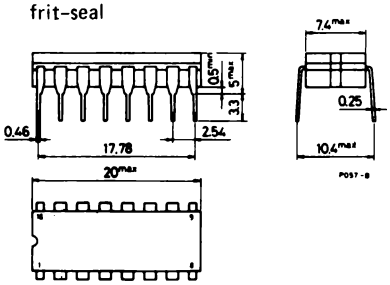
| | | | |
|---|---|---|---|
| | Voltage on any pin relative to $V_{BB}$ | -0.5 to +20 | V |
| | Voltage on $V_{DD}$, $V_{CC}$ supplies relative to $V_{SS}$ | -1 to +15 | V |
| | $V_{BB}$-$V_{SS}$ ($V_{DD}$-$V_{SS} > 0V$) | 0 | V |
| $T_{op}$ | Operating temperature | 0 to +70 | °C |
| $T_{stg}$ | Storage temperature for ceramic package | -65 to +150 | °C |
| | for plastic package | -55 to +125 | °C |
| $I_o$ | Short circuit output current | 50 | mA |
| $P_{tot}$ | Total power dissipation | 1 | W |

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

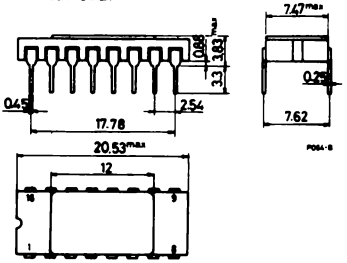
**ORDERING NUMBERS:** M 4116-2/3/4 D1 for dual in-line ceramic package, metal-seal
M 4116-2/3/4 F1 for dual in-line ceramic package, frit-seal

## MECHANICAL DATA (dimensions in mm)

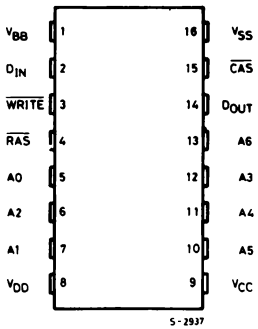
Dual in-line ceramic package
frit-seal




Dual in-line ceramic package
metal-seal



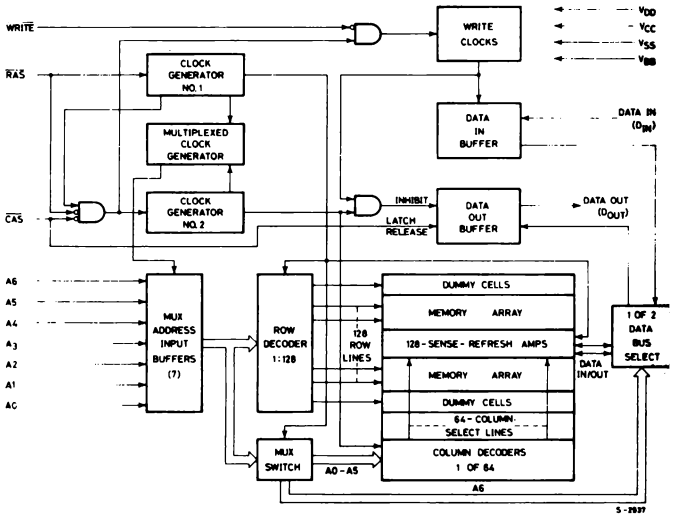

## PIN CONNECTIONS




**PIN NAMES**

| | |
|---|---|
| $A_0$-$A_6$ | ADDRESS INPUTS |
| $\overline{CAS}$ | COLUMN ADDRESS STROBE |
| $D_{IN}$ | DATA IN |
| $D_{OUT}$ | DATA OUT |
| $\overline{RAS}$ | ROW ADDRESS STROBE |
| $\overline{WRITE}$ | READ/WRITE INPUT |
| $V_{BB}$ | POWER (-5V) |
| $V_{CC}$ | POWER (+5V) |
| $V_{DD}$ | POWER (+12V) |
| $V_{SS}$ | GROUND |

## BLOCK DIAGRAM



## RECOMMENDED DC OPERATING CONDITIONS ($T_{amb}$= 0 to 70°C)[1]

| Parameter | | Types | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Supply voltage | 10.8 | 12 | ] 13.2 | V | 2 |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V | 2,3 |
| $V_{SS}$ | Supply voltage | 0 | 0 | 0 | V | 2 |
| $V_{BB}$ | Supply voltage | -4.5 | -5 | -5.7 | V | 2 |
| $V_{IHC}$ | Input high voltage on $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 2.7 | – | 7 | V | 2 |
| $V_{IH}$ | Input high voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | 2.4 | – | 7 | V | 2 |
| $V_{IL}$ | Input low voltage, all inputs | -1 | – | 0.8 | V | 2 |

## DC ELECTRICAL CHARACTERISTICS ($T_{amb}$= 0 to 70°C)[1], $V_{DD}$= 12V±10% $V_{CC}$= 5V±10%; $V_{BB}$= -5.7 to -4.5V; $V_{SS}$= 0V)

| Parameter | | Test conditions | Types | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | M 4116-2/3 | | M 4116-4 | | | |
| | | | Min. | Max. | Min. | Max. | | |
| $I_{DD1}$ | Average operating current | $\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC}$= $t_{RC}$ (min) | | 35 | | 35 | mA | 4 |
| $I_{CC1}$ | Average operating current | | | | | | | 5 |
| $I_{BB1}$ | Average operating current | | | 200 | | 200 | µA | |
| $I_{DD2}$ | Standby current | $\overline{RAS}$ = $V_{IHC}$ $D_{OUT}$= High impedance | | 1.5 | | 1.5 | mA | |
| $I_{CC2}$ | Standby current | | -10 | 10 | -10 | 10 | µA | |
| $I_{BB2}$ | Standby current | | | 100 | | | µA | |
| $I_{DD3}$ | Refresh average current | Refresh mode: $\overline{RAS}$ cycling $\overline{CAS}$ = $V_{IHC}$ $t_{RC}$= $t_{RC}$ (min) | | 27 | | 27 | mA | 4 |
| $I_{CC3}$ | Refresh average current | | -10 | 10 | -10 | 10 | µA | |
| $I_{BB3}$ | Refresh average current | | | 200 | | | µA | |
| $I_{DD4}$ | Page mode average current | Page mode: $\overline{RAS}$ = $V_{IL}$ $\overline{CAS}$ cycling $t_{PC}$= $t_{PC}$ (min) | | 27 | | 27 | mA | 4 |
| $I_{CC4}$ | Page mode average current | | | | | | | 5 |
| $I_{BB4}$ | Page mode average current | | | 200 | | | µA | |
| $I_{I(L)}$ | Input leakage current | $V_{BB}$= -5V 0V ≤ $V_{IN}$ ≤ +7V, all other pins not under test = 0 volts | -10 | 10 | -10 | 10 | µA | |
| $I_{O(L)}$ | Output leakage current | $D_{OUT}$ in disabled 0V ≤ $V_{OUT}$ ≤ +5.5V | -10 | 10 | -10 | 10 | µA | |
| $V_{OH}$ | Output high voltage | $I_{OUT}$= -5 mA | 2.4 | | 2.4 | | V | 3 |
| $V_{OL}$ | Output low voltage | $I_{OUT}$= 4.2 mA | | 0.4 | | 0.4 | V | 3 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDIT.

($T_{amb}$ = 0 to 70°C)[1], $V_{DD}$ = 12V ± 10%; $V_{CC}$ = 5V ± 10%; $V_{SS}$ = 0V, $V_{BB}$ = -5.7 to -4.5V)

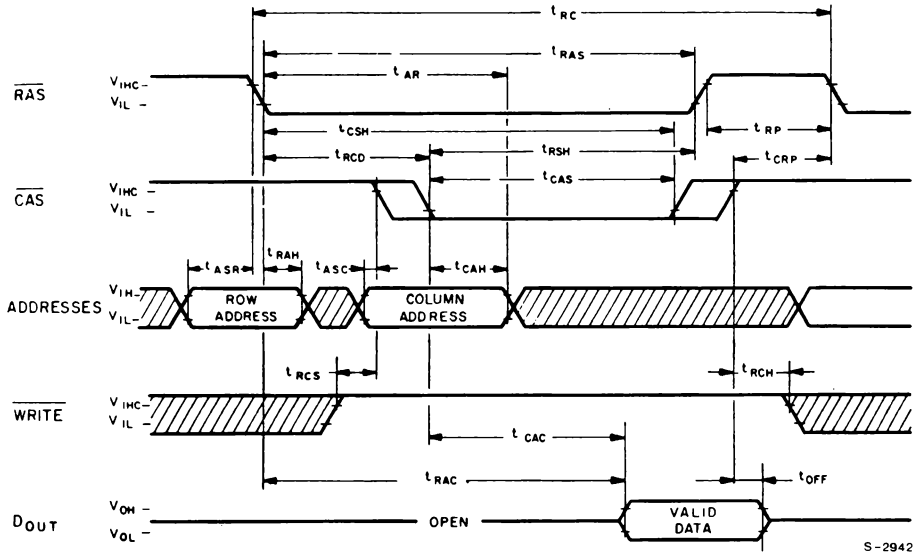
| Parameter | | Types | | | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | M 4116-2 | | M 4116-3 | | M 4116-4 | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| $t_{RC}$ | Random read or write cycle time | 320 | | 375 | | 410 | | ns | 9 |
| $t_{RWC}$ | Read-write cycle time | 320 | | 375 | | 425 | | ns | 9 |
| $t_{RMW}$ | Read modify write cycle time | 320 | | 405 | | 500 | | ns | 9 |
| $t_{PC}$ | Page mode cycle time | 170 | | 225 | | 275 | | ns | 9 |
| $t_{RAC}$ | Access time from $\overline{RAS}$ | | 150 | | 200 | | 250 | ns | 10, 12 |
| $t_{CAC}$ | Access time from $\overline{CAS}$ | | 100 | | 135 | | 165 | ns | 11, 12 |
| $t_{OFF}$ | Output buffer turn-off delay | 0 | 40 | 0 | 50 | 0 | 60 | ns | 13 |
| $t_T$ | Transition time (rise and fall) | 3 | 35 | 3 | 50 | 3 | 50 | ns | 8 |
| $t_{RP}$ | $\overline{RAS}$ precharge time | 100 | | 120 | | 150 | | ns | |
| $t_{RAS}$ | $\overline{RAS}$ pulse width | 150 | 10000 | 200 | 10000 | 250 | 10000 | ns | |
| $t_{RSH}$ | $\overline{RAS}$ hold time | 100 | | 135 | | 165 | | ns | |
| $t_{CSH}$ | $\overline{CAS}$ hold time | 150 | | 200 | | 250 | | ns | |
| $t_{RCD}$ | $\overline{RAS}$ to CAS delay time | 20 | 50 | 25 | 65 | 35 | 85 | ns | 14 |
| $t_{CAS}$ | $\overline{CAS}$ pulse width | 100 | | 135 | | 165 | | ns | |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ precharge time | -20 | | -20 | | -20 | | ns | |
| $t_{ASR}$ | Row address set-up time | 0 | | 0 | | 0 | | ns | |
| $t_{RAH}$ | Row address hold time | 20 | | 25 | | 35 | | ns | |
| $t_{ASC}$ | Column address set-up time | -10 | | -10 | | -10 | | ns | |
| $t_{CAH}$ | Column address hold time | 45 | | 55 | | 75 | | ns | |
| $t_{AR}$ | Column address hold time referenced to $\overline{RAS}$ | 95 | | 120 | | 160 | | ns | |
| $t_{RCS}$ | Read command set-up time | 0 | | 0 | | 0 | | ns | |
| $t_{RCH}$ | Read command hold time | 0 | | 0 | | 0 | | ns | |
| $t_{WCH}$ | Write command hold time | 45 | | 55 | | 75 | | ns | |
| $t_{WCR}$ | Write command hold time referenced to $\overline{RAS}$ | 95 | | 120 | | 160 | | ns | |
| $t_{WP}$ | Write command pulse width | 45 | | 55 | | 75 | | ns | |
| $t_{RWL}$ | Write command to $\overline{RAS}$ lead time | 50 | | 70 | | 85 | | ns | |
| $t_{CWL}$ | Write command to $\overline{CAS}$ lead time | 50 | | 70 | | 85 | | ns | |
| $t_{DS}$ | Data-in set-up time | 0 | | 0 | | 0 | | ns | 15 |
| $t_{DH}$ | Data-in hold time | 45 | | 55 | | 75 | | ns | 15 |
| $t_{DHR}$ | Data-in hold time referenced to $\overline{RAS}$ | 95 | | 120 | | 160 | | ns | |
| $t_{CP}$ | $\overline{CAS}$ precharge time (for page mode cycle only) | 60 | | 80 | | 100 | | ns | |
| $t_{REF}$ | Refresh period | | 2 | | 2 | | 2 | ns | |
| $t_{WCS}$ | $\overline{WRITE}$ command set-up time | -20 | | -20 | | -20 | | ns | 16 |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WRITE}$ delay | 60 | | 80 | | 90 | | ns | 16 |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WRITE}$ delay | 110 | | 145 | | 175 | | ns | 16 |

Notes:
1. $T_{amb}$ is specified here for operation at frequencies to $t_{RC} \geq t_{RC\,(min)}$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible, however, provided AC operating parameters are met.
2. All voltages referenced to $V_{SS}$.
3. Output voltage will swing from $V_{SS}$ to $V_{CC}$ when activated with no current loading. For purposes of maintaining data in standby mode, $V_{CC}$ may be reduced to $V_{SS}$ without affecting refresh operations or data retention. However, the $V_{OH}$ (min) specification is not guaranteed in this mode.
4. $I_{DD1}$, $I_{DD3}$ and $I_{DD4}$ depend on cycle rate.
5. $I_{CC1}$ and $I_{CC4}$ depend upon output loading. During read out of high level data $V_{CC}$ is connected through a low impedance to data out. At all other times $I_{CC}$ consists of leakage currents only.
6. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
7. AC measurements assume $t_T$ = 5 ns.
8. $V_{IHC}$ (min) or $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IHC}$ or $V_{IH}$ and $V_{IL}$.
9. The specifications for $t_{RC}$ (min) and $t_{RWC}$ (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_{amb} \leq 70°C$) is assured.
10. Assumes that $t_{RCD} \leq t_{RCD}$ (max). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds the value shown.
11. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
12. Measured with a load equivalent to 2 TTL loads and 100 pF.
13. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
14. Operation within the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
15. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. $t_{WCS}$, $t_{CWD}$ and $t_{RWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
17. Effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta v}$ with $\Delta v$ = 3 volts and power supplies at nominal levels.
18. $\overline{CAS}$ = $V_{IHC}$ to disable $D_{OUT}$.

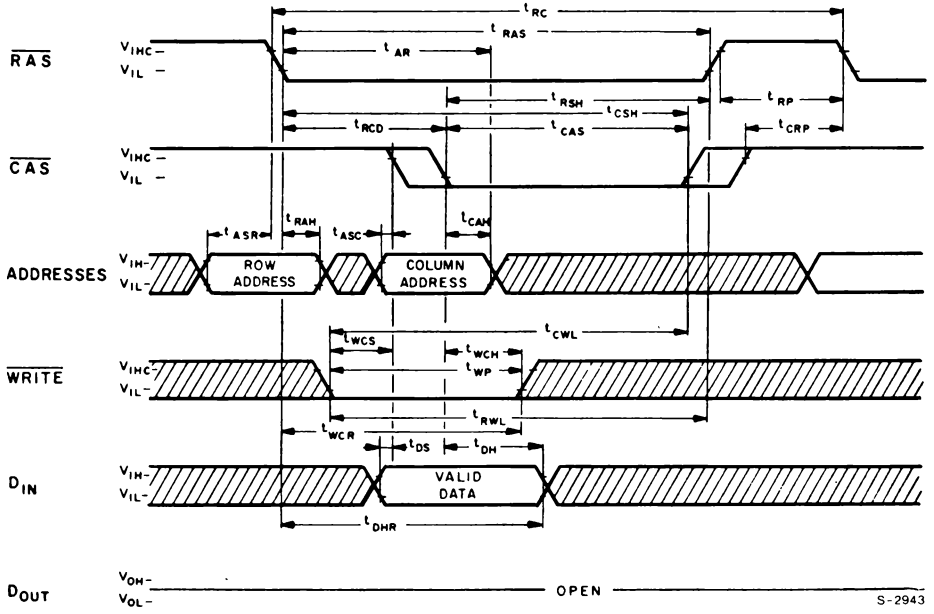
## CAPACITANCES ($T_{amb}$ = 0 to 70°C; $V_{DD}$ = 12V ± 10%; $V_{SS}$ = 0V; $V_{BB}$ = -5.7 to -4.5V)

| | Parameter | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|
| $C_{I1}$ | Input capacitance ($A_0$-$A_6$) DIN | | 4 | 5 | pF | 17 |
| $C_{I2}$ | Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ | | 8 | 10 | pF | 17 |
| $C_o$ | Output capacitance ($D_{OUT}$) | | 5 | 7 | pF | 17, 18 |

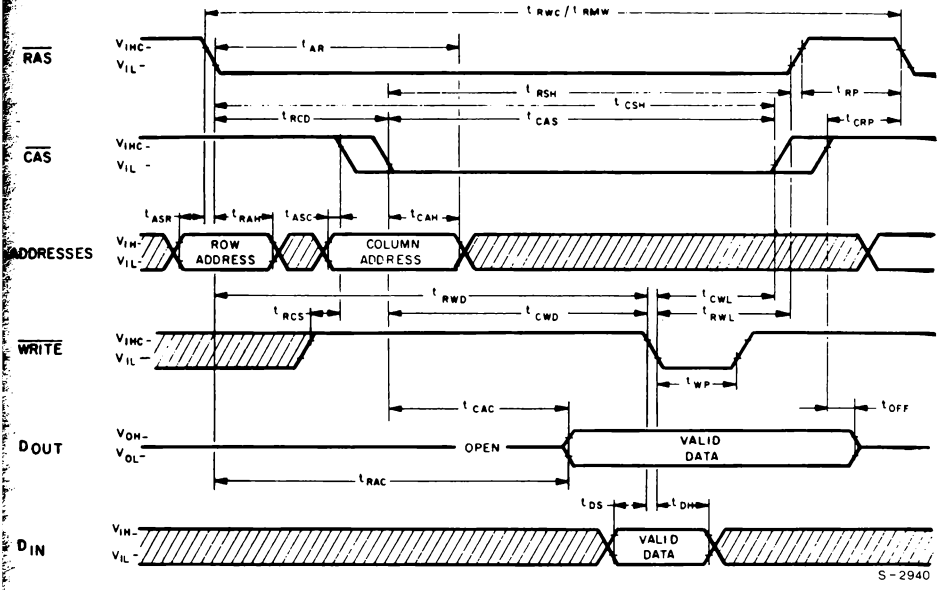
## READ CYCLE



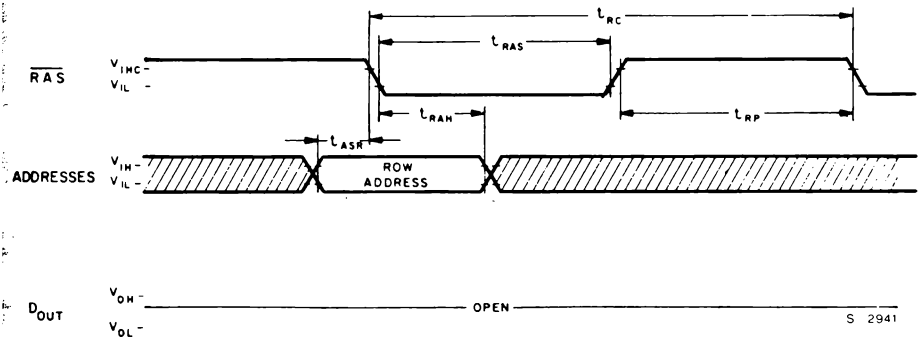

## WRITE CYCLE (EARLY WRITE)



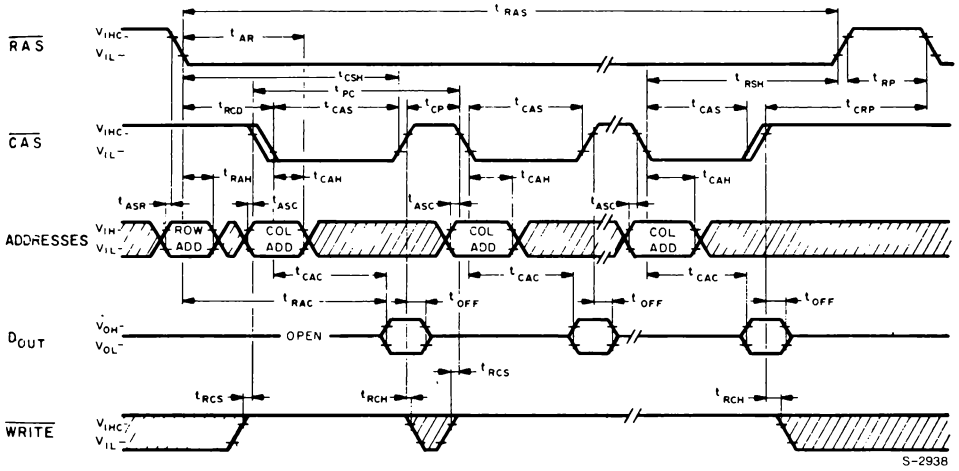
## EAD-WRITE/READ-MODIFY-WRITE CYCLE



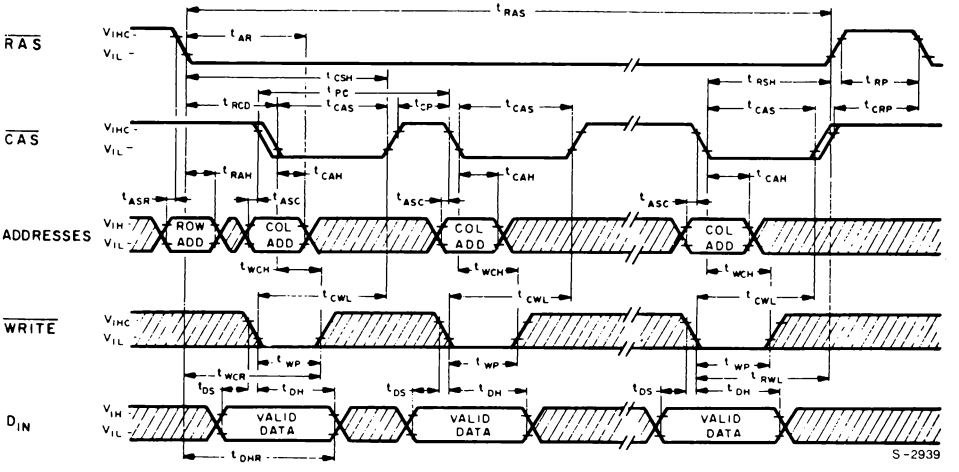

## RAS-ONLY" REFRESH CYCLE



## PAGE MODE READ CYCLE




## PAGE MODE WRITE CYCLE



## DESCRIPTION

System oriented features include ±10% tolerance on all power supplies, direct interfacing capability with high performance logic families such as Schottky TTL, maximum input noise immunity to minimize false triggering" of the inputs (a common cause of soft errors), on-chip address and data registers which eliminate the need for interface registers, and two chip select methods to allow the user to determine the appropriate speed/power characteristics of his memory system. The M 4116 also incorporates several flexible timing/operating modes. In addition to the usual read, write, and read-modify-write cycles, the M 4116 is capable of delayed write cycles, page-mode operation and RAS-only refresh. Proper control of the clock inputs ($\overline{RAS}$, $\overline{CAS}$ and $\overline{WRITE}$) allows common I/O capability, two dimensional chip selection, and extended page boundaries (when operating in page mode).

## ADDRESSING

The 14 address bits required to decode 1 of the 16,384 cell locations within the M 4116 are multiplexed into the 7 address inputs and latched into the on-chip address latches by externally applying two negative going TTL-level clocks. The first clock, the Row Address Strobe ($\overline{RAS}$), latches the 7 row address bits into the chip. The second clock, the Column Address Strobe ($\overline{CAS}$), subsequently latches the 7 column address bits into the chip. Each of these signals, $\overline{RAS}$ and $\overline{CAS}$, triggers a sequence of events which are controlled by different delayed internal clocks. The two clock chains are linked together logically in such a way that the address multiplexing operation is done outside of the critical path timing sequence for read data access. The later events in the $\overline{CAS}$ clock sequence are inhibited until the occurrence of a delayed signal derived from the $\overline{RAS}$ clock chain. This "gated $\overline{CAS}$" feature allows the $\overline{CAS}$ clock to be externally activated as soon as the Row Address Hold Time specification ($t_{RAH}$) has been satisfied and the address inputs have been changed from Row address to Column address information. Note that $\overline{CAS}$ can be activated at any time after $t_{RAH}$ and it will have no effect on the worst case data access time ($t_{RAC}$) up to the point in time when the delayed row clock no longer inhibits the remaining sequence of column clocks. Two timing end-points result from the internal gating of $\overline{CAS}$ which are called $t_{RCD}$ (min) and $t_{RCD}$ (max). No data storage or reading errors will result if $\overline{CAS}$ is applied to the M 4116 at a point in time beyond the $t_{RCD}$ (max) limit. However, access time will then be determined exclusively by the access time from $\overline{CAS}$ ($t_{CAC}$) rather than from $\overline{RAS}$ ($t_{RAC}$), and access time from $\overline{RAS}$ will be lengthened by the amount that $t_{RCD}$ exceeds the $t_{RCD}$ (max) limit.

## DATA INPUT/OUTPUT

Data to be written into a selected cell is latched into an on-chip register by a combination of $\overline{WRITE}$ and $\overline{CAS}$ while $\overline{RAS}$ is active. The later of the signals ($\overline{WRITE}$ or $\overline{CAS}$) to make its negative transition is the strobe for the Data In ($D_{IN}$) register. This permits several options in the write cycle timing. In a write cycle, if the $\overline{WRITE}$ input is brought low (active) prior to $\overline{CAS}$, the $D_{IN}$ is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the input data is not available at $\overline{CAS}$ time or if it is desired that the cycle be a read-write cycle, the $\overline{WRITE}$ signal will be delayed until after $\overline{CAS}$ has made its negative transition. In this "delayed write cycle" the data input set-up and hold times are referenced to the negative edge of $\overline{WRITE}$ rather than $\overline{CAS}$. (To illustrate this feature, $D_{IN}$ is referenced to $\overline{WRITE}$ in the timing diagrams depicting the read-write and page-mode write cycles while the "early write" cycle diagram shows $D_{IN}$ referenced to $\overline{CAS}$).

Data is retrieved from the memory in a read cycle by maintaining $\overline{WRITE}$ in the inactive or high state throughout the portion of the memory cycle in which $\overline{CAS}$ is active (low). Data read from the selected cell will be available at the output within the specified access time.

## DATA OUTPUT CONTROL

The normal condition of the Data Output ($D_{OUT}$) of the M 4116 is the high impedance (open-circuit) state. That is to say, anytime $\overline{CAS}$ is at a high level, the $D_{OUT}$ pin will be floating. The only time the output will turn on and contain either a logic 0 or logic 1 is at access time during a read cycle. $D_{OUT}$ will remain valid from access time until $\overline{CAS}$ is taken back to the inactive (high level) condition.

## DATA OUTPUT CONTROL (continued)

If the memory cycle in progress is a read, read-modify write, or a delayed write cycle, then the data output will go from the high impedance state to the active condition, and at access time will contain the data read from the selected cell. This output data is the same polarity (not inverted) as the input data. Once having gone active, the output will remain valid until CAS is taken to the precharge (logic 1) state, whether or not $\overline{RAS}$ goes into precharge.
If the cycle in progress is an "early-write" cycle ($\overline{WRITE}$ active before $\overline{CAS}$ goes active), then the output pin will maintain the high impedance state throughout the entire cycle. Note that with this type of output configuration, the user is given full control of the $D_{OUT}$ pin simply by controlling the placement of $\overline{WRITE}$ command during a write cycle, and the pulse width of the Column Address Strobe during read operations. Note also that even through data is not latched at the output, data can remain valid from access time until the beginning of a subsequent cycle without paying any penalty in overall memory cycle time (stretching the cycle).
This type of output operation results in some very significant system implications.

**Common I/O Operation** – If all write operations are handled in the "early write" mode, then $D_{IN}$ can be connected dorectly to $D_{OUT}$ for a common I/O data bus.
$D_{OUT}$ will remain valid during a read cycle from $t_{CAC}$ until $\overline{CAS}$ goes back to a high level (precharge), allowing data to be valid from one cycle up until a new memory cycle begins with no penalty in cycle time. This also makes the RAS/CAS clock timing relationship very flexible.
Two Methods of Chip Selection - Since $D_{OUT}$ is not latched, $\overline{CAS}$ is not required to turn off the outputs of unselected memory devices in a matrix. This means that both $\overline{CAS}$ and/or $\overline{RAS}$ can be decoded for chip selection. If both $\overline{RAS}$ and $\overline{CAS}$ are decoded, then a two dimensional (X, Y) chip select array can be realized.
Extended Page Boundary - Page-mode operation allows for successive memory cycles at multiple column locations of the same row address. By decoding $\overline{CAS}$ as a page cycle select signal, the page boundary can be extended beyond the 128 column location in a single chip. (See page-mode operation).

## OUTPUT INTERFACE CHARACTERISTICS

The three state data output buffer presents the data output pin with a low impedance to $V_{CC}$ for a logic 1 and a low impedance to $V_{SS}$ for a logic 0. The effective resistance to $V_{CC}$ (logic 1 state) is 420Ω maximum and 135Ω typically. The resistance to $V_{SS}$ (logic 0 state) is 95Ω maximum and 35Ω typically. The separate $V_{CC}$ pin allows the output buffer to be powered from the supply voltage of the logic to which the chip is interfaced. During battery standby operation, the $V_{CC}$ pin may have power removed without affecting the M 4116 refresh operation. This allows all system logic except the $\overline{RAS}$ timing circuitry and the refresh address logic to be turned off during battery standby to conserve power.

## PAGE MODE OPERATION

The "Page Mode" feature of the M 4116 allows for successive memory operations at multiplie column locations of the same row address with increased speed without an increase in power. This is done by strobing the row address into the chip and maintaining the $\overline{RAS}$ signal at a logic 0 throughout all successive memory cycles in which the row address is common. This "page-mode" of operation will not dissipate the power associated with the negative going edge of RAS. Also, the time required for strobing in a new row address is eliminated, thereby decreasing the access and cycle times.
The page boundary of a single M 4116 is limited to the 128 column locations determined by all combinations of the 7 column address bits. However, in system applications which utilize more than 16,384 data words, (more than one 16K memory block), the page boundary can be extended by using $\overline{CAS}$ rather than $\overline{RAS}$ as the chip select signal. $\overline{RAS}$ is applied to all devices to latch the row address into each device and the $\overline{CAS}$ is decoded and serves as a page cycle select signal. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ signals will execute a read or write cycle.

## EFRESH

efresh of the dynamic cell matrix is accomplished by performing a memory cycle at each of the 128 w addresses within each 2 millisecond time interval. Although any normal memory cycle will perform e refresh operation, this function is most easily accomplished with "$\overline{RAS}$-only" cycles. $\overline{RAS}$-only fresh results in a substantial reduction in operating power. This reduction in power is reflected in the $_{D\,3}$ specification.

## OWER CONSIDERATIONS

ost of the circuitry used in the M 4116 is dynamic and most of the power drawn is the result of an address strobe edge. Consequently, the dynamic power is primarily a function of operating frequency rather an active duty cycle. This current characteristic of the M 4116 precludes inadverten burn out of the vice in the event that the clock inputs become shorted to ground due to system malfunction.
lthough no particular power supply noise restriction exists other than the supply voltages remain within e specified tolerance limits, adequate decoupling should be provided to suppress high frequency noise sulting from the transient current of the device. This insures optimum system performance and reibility. Bulk capacitance requirements are minimal since the M 4116 draws very little steady state (DC) rrent.
n system applications requiring lower power dissipations, the operating frequency (cycle rate) of the 4116 can be reduced and the (guaranteed maximum) average power dissipation of the device will be wered in accordance with the $I_{DD1}$ (max) spec limit equation.

ote : The M 4116-4 is guaranteed to have a maximum $I_{DD1}$ requirement of 35 mA @ 410 ns cycle with an ambient temperature range from 0° to 70°C. A lower operating frequency, for example 1 microsecond cycle, results in a reduced maximum $I_{DD1}$ requirement of under 20 mA with an ambient temperature range from 0° to 70°C.

lthough $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the M 4116 overall sysm power is minimized if the Row Address Strobe ($\overline{RAS}$) is used for this purpose. All unselected devices those which do not receive a $\overline{RAS}$) will remain in a low power (standby) mode regardless of the state f $\overline{CAS}$.

## OWER UP

he M 4116 requires no particular power supply sequencing so long as the Absolute Maximum Rating onditions are observed. However, in order to insure compliance with the Absolute Maximum Ratings, GS-ATES recommends sequencing of power supplies such that $V_{BB}$ is applied first and removed last. $V_{BB}$ should never be more positive than $V_{SS}$ when power is applied to $V_{DD}$.
nder system failure conditions in which one or more supplies exceed the specified limits significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state (high level).
fter power is applied to be device, the M 4116 requires several cycles before proper device operation is chieved. Any 8 cycles which perform refresh are adequate for this purpose.