M50734SP/FP
M50734SP/FP-10

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M50734SP is a microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP (flat package type also available). This microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M50734SP-10 and the M50734SP are noted below.

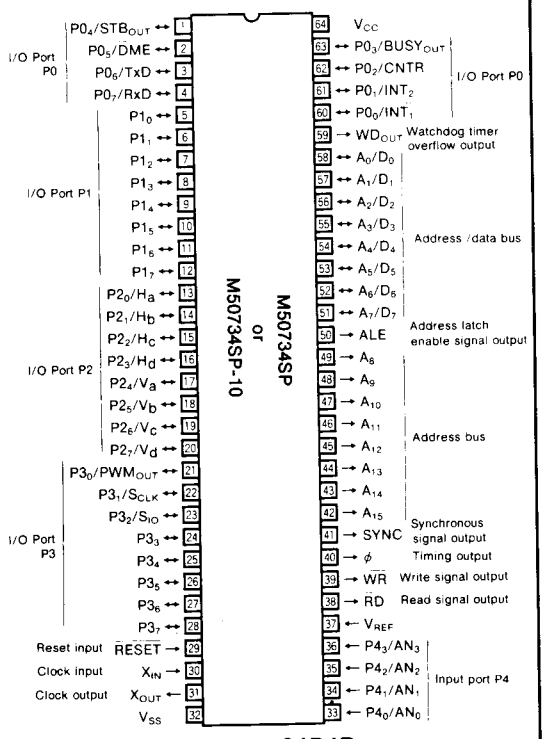
Type name	maximum value of clock generating frequency
M50734SP	8MHz
M50734SP-10	10MHz

The differences between the M50734SP and the M50734FP, and M50734SP-10 and M50734FP-10 are the package outline, the voltage input pins for A-D, and power dissipation ability (absolute maximum ratings).

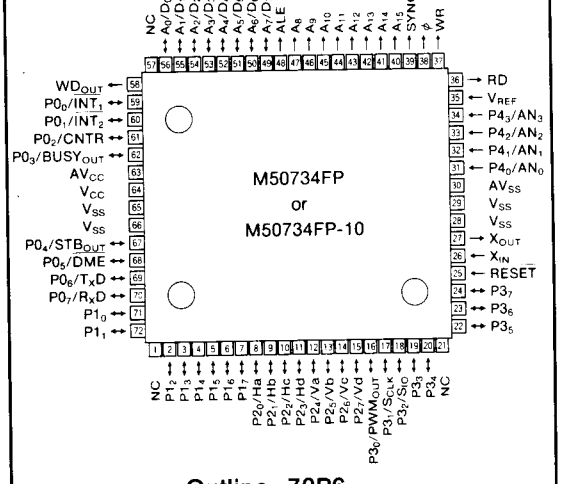
FEATURES

- Number of basic instructions 69
- Memory size (internal memories are not provided)
  - Memory area programmable memory .....64K bytes
  - data memory .....64K bytes
- Instruction execution time (minimum instructions)
  - ..... 1μs (at 8MHz frequency M50734SP)
  - ..... 0.8μs (at 10MHz frequency, M50734SP-10)
- Single power supply .....5V±10%
- Power dissipation
  - normal operation mode (at 8MHz frequency) 30mW
  - (at 10MHz frequency) 35mW
- Subroutine nesting ..... 128 levels (Max.)
- Interrupt .....11 types, 5 vectors
- Timers
  - 16-bit timer/event counter (general purpose) 1
  - 8-bit timer (general purpose) 3
  - 8-bit timer (watchdog timer) 1
  - 8-bit timer (strobe timer) 1
  - 8-bit timer (baud rate timer) 1
  - 8-bit counter (control for stepper motor) 2
- Stepper motor control circuit
  - ..... 1 channel for the X or Y direction
- Programmable I/O ports (Ports P0, P1, P2, P3) 32
- Input port (Port P4) 4
- Serial I/O
  - 8-bit clock synchronous 1
  - 8-bit UART 1
  - Baud rate (at 7.37MHz frequency) ...75bps~57600bps
  - (at 9.83MHz frequency) ...75bps~76800bps
- A-D converter ..... 8-bit successive approximation
- PWM function 1
- Multiplex-type bus
  - Address bus 16
  - Data bus (multiplexed with lower address bus) 8

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B



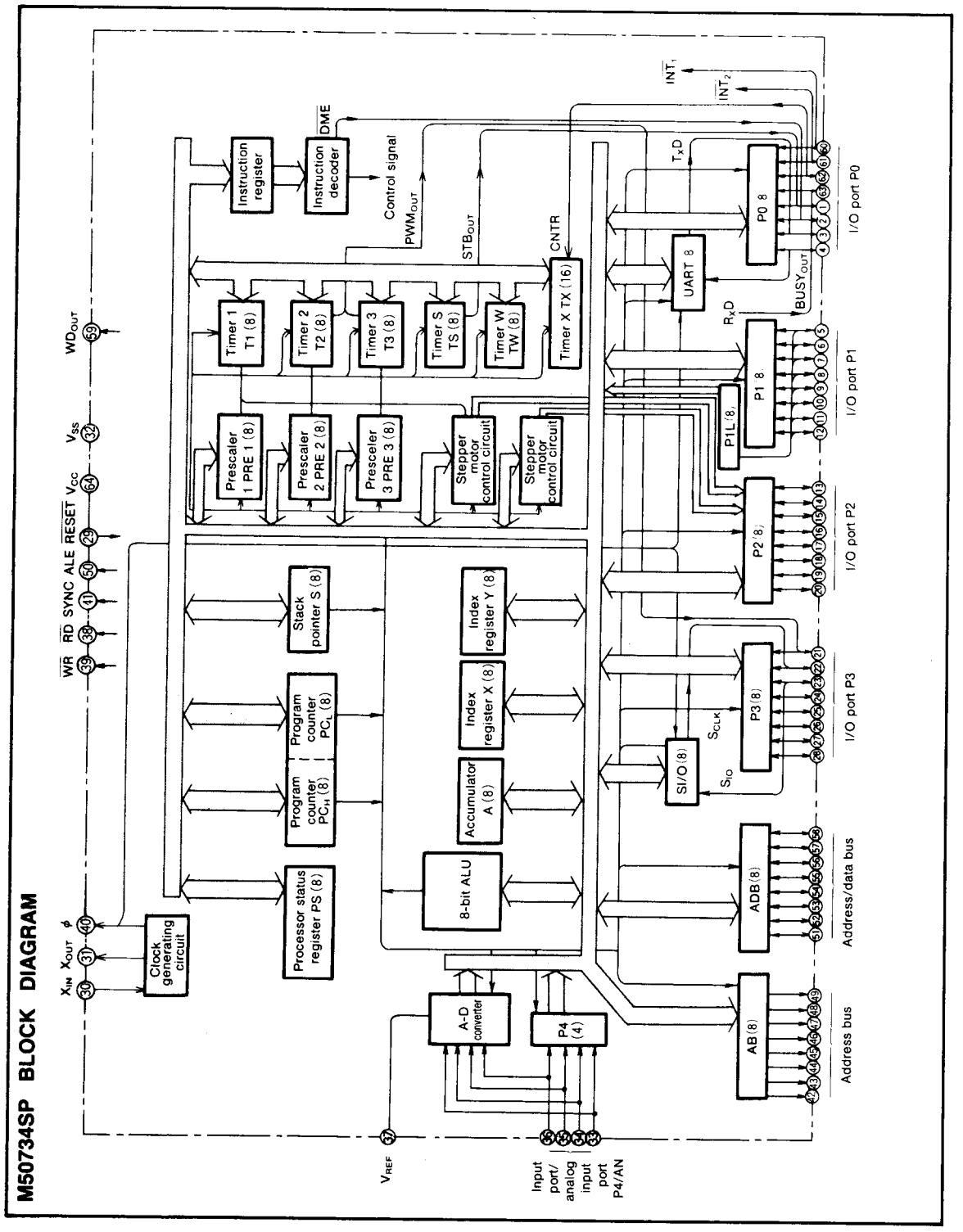
Outline 72P6

NC : No connection

APPLICATION

Printer/plotter, Electronic typewriter, PPC, FAX, Portable word processor, Robotics

M50734SP BLOCK DIAGRAM



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FUNCTIONS OF M50734SP and M50734SP-10

Parameter			Functions
Number of basic instructions			69
Instruction execution time	M50734SP		1μs (minimum instructions, at 8MHz frequency)
	M50734SP-10		0.8μs (minimum instructions, at 10MHz frequency)
Clock frequency	M50734SP		8MHz
	M50734SP-10		10MHz
Memory size			64K bytes (up to 128k bytes with $\overline{DME}$ signal)
Input/output ports	P0, P1, P2, P3	I/O	8-bit×4 (all pins of P0, P2, and part of P3 have double functions)
	P4	input	4-bit×1 (P4 is in common with analog input)
UART	M50734SP		1 (built-in baud rate generator 75~57600bps)
	M50734SP-10		1 (built-in baud rate generator 75~76800bps)
Clock synchronized serial I/O			8-bit×1
Timers	Timer X		16-bit×1
	Timer 1		8-bit×1 (with 8-bit prescaler)
	Timer 2		8-bit×1 (with 8-bit prescaler)
	Timer 3		8-bit×1 (with 8-bit prescaler)
	Timer S		8-bit×1 (with 1/4 frequency divider)
	Timer W		8-bit×1 (with 1/1024 frequency divider)
A-D converter			Four analog inputs, 8-bit successive approximation
Subroutine nesting			128 levels (max.)
Interrupt			Three external interrupts, four timer interrupts Two counter interrupts, one UART interrupt
Clock generating circuit			Built-in (externally connected to a ceramic resonater or a quartz crystal resonator)
Supply voltage			5V±10%
Power dissipation	at normal operation		30mW (M50734SP) 35mW (M50734SP-10)
	at wait mode		5mW
	at stop mode		5μW
Operating temperature range			−10~70℃
Device structure			CMOS sillicon gate process
Package	M50734SP, M50734SP-10		64-pin shrink plastic molded DIP
	M50734FP, M50734FP-10		72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and V_{SS}
AV_{CC}, AV_{SS}	Voltage input for A-D		This is the power supply input pin for the A-D converter. For M50734SP and M50734SP-10, this is not provided.
V_{REF}	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin. Clock oscillating frequency f(X_{IN}) divided by 4 signal is outputed.
SYNC	Synchronous signal output	Output	Synchronous signal is outputed when the op code is fetched, and is used to control the program's single-step operation.
$\overline{RD}$	Read signal output	Output	Control signal for read access to ROM, RAM and peripherals.
$\overline{WR}$	Write signal output	Output	Control signal for write access to RAM and peripherals.
ALE	Address latch enable signal output	Output	Address latch signal for address A_0~A_7.
A_{15}~A_8	Address bus	Output	The contents of the high-order 8 bits of the address bus are output (CMOS output).
A_7/D_7~ A_0/A_0	Address/Data bus	I/O	The contents of the lower-order 8 bits of the address bus and 8 bits of the address bus are output (CMOS output).
WD_{OUT}	Watchdog timer overflow output	Output	When the watchdog timer overflows, this pin is set to "H". Cleared only at reset.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with CMOS tri-state output. Each port has double function, and can switch by software.
$\overline{INT_1}$($P0_0$)	Interrupt input	Input	This is an interrupt input pin.
$\overline{INT_2}$($P0_1$)	Interrupt input	Input	This is an interrupt input pin.
CNTR($P0_2$)	Timer I/O	I/O	This is an output pin for the timer X.
$BUSY_{OUT}$($P0_3$)	Busy signal output	Output	When the falling edge is inputed to $\overline{INT_1}$ pin, this port is set by hardware.
STB_{OUT}($P0_4$)	Strove pulse output	Output	This pin is used for the strobe input to the external driver IC.
$\overline{DME}$($P0_5$)	Data memory enable output	Output	This pin is used for external memory expansion.
TxD($P0_6$)	Transmission output	Output	This is an output pin for UART.
RxD($P0_7$)	Receive input	Input	This is an input pin for UART.
$P1_0$ ~ $P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port with CMOS tri-state output. It is also used as "latch input" to read data when a low level signal is inputed to $\overline{INT_1}$ pin.
$P2_0$ ~ $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with CMOS tri-state output. By software selection, it can also be used as an output port for the decoder logic of a stepper motor control circuit.
$P3_0$ ~ $P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port with CMOS tri-state output. The function of the $P3_0$~$P3_2$ can be selected by software.
$P4_0/AN_0$~ $P4_3/AN_3$	Input port P4/ Analog input port AN	Input	Port P4 is a 4-bit input port, and is used as a 4-bit analog input port for A-D converter.

BASIC FUNCTION BLOCKS

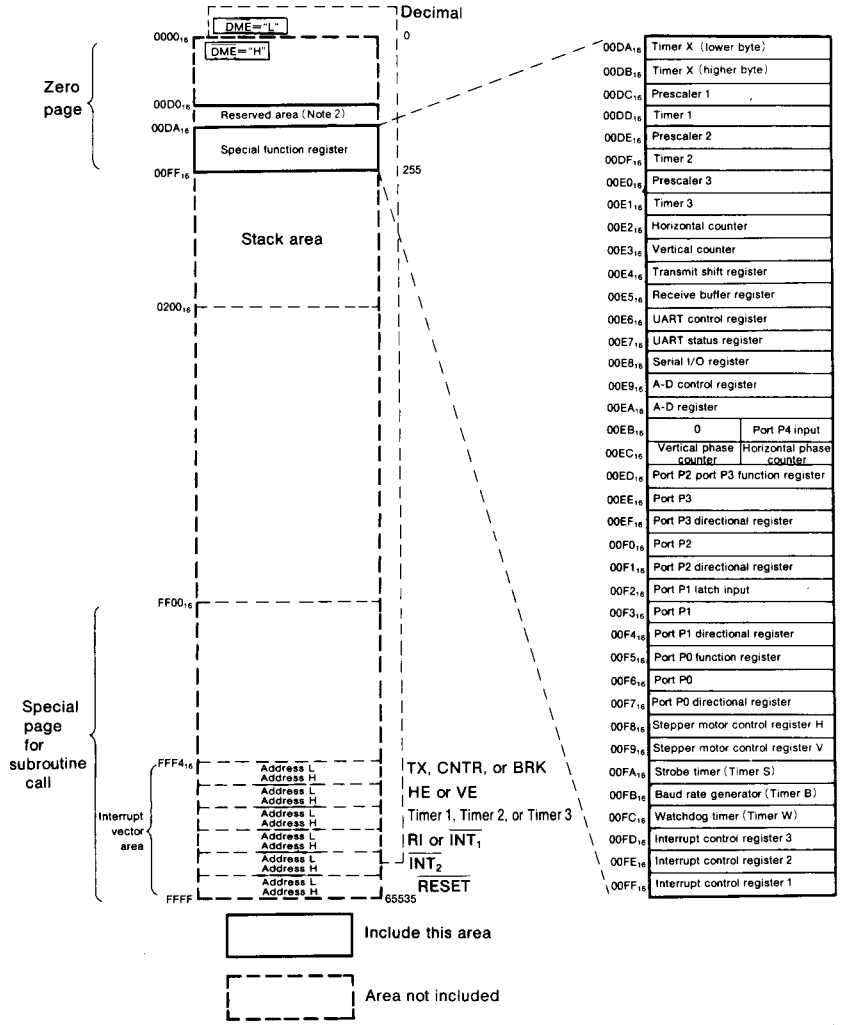
MEMORY

A memory map of the M50734SP is shown in Figure 1. Since the M50734SP contains no internal memory, the ROM and RAM must be connected externally. The addressable memory space is 64K bytes however, by using the $\overline{DME}$ signal, up to 128K bytes can be accessed.

The special address area is contained between addresses $FF00_{16}$ to $FFFF_{16}$. By using this special page addressing mode, subroutines located in this area can be called with only 2 bytes. The reset and interrupt vector addresses are contained within addresses $FFF4_{16}$ to $FFFF_{16}$.

The zero page address area is contained between 0000_{16} and $00FF_{16}$. Addresses within this area can be accessed with 1 byte. Frequently accessed addresses, such as in RAM, input/output ports and timers, are allocated to the zero page area.

Addresses 0100_{16} to $01FF_{16}$ are used mainly as the stack, and addresses 0200_{16} to $FEFF_{16}$ are used memories for the program and data.



Note 1 : When the $\overline{DME}$ signal is "L", an additional memory space of 64K bytes can be obtained. However the space can be used only for data memory such as ROM, RAM or peripherals.

2 : This area is reserved for system expansion.

Fig.1 Memory map

CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 2.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the microcomputer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.
In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

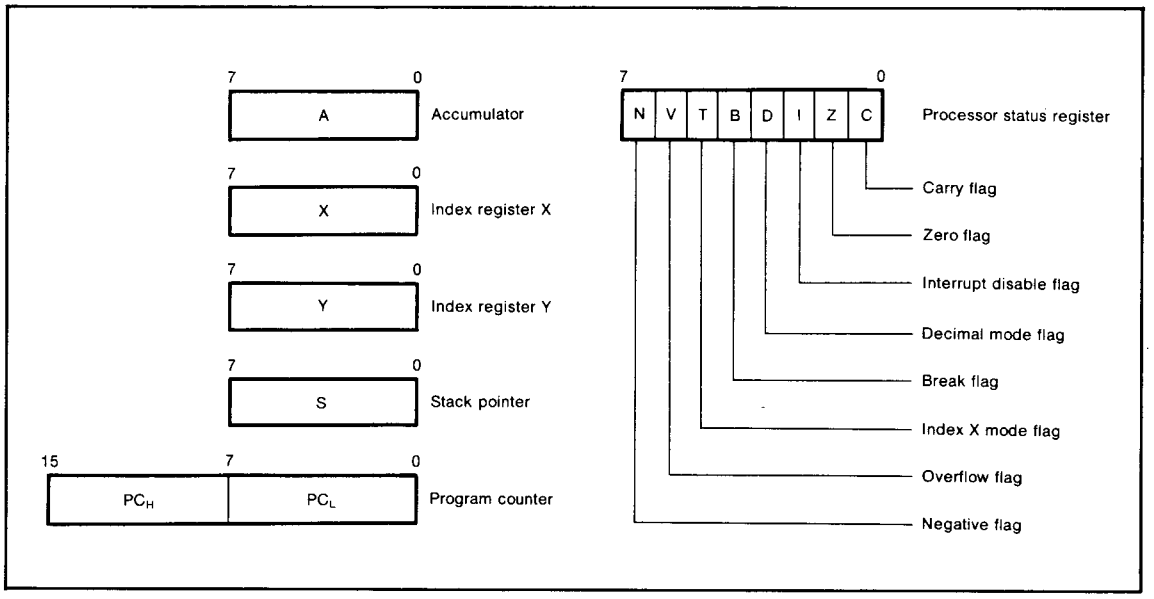


Fig.2 Register structure

STACK POINTER (S)

The stack pointer is an 8-bit register that contains the address of the next location in the stack. It is mainly used during interrupts and subroutine calls. The stack pointer is not automatically initialized after reset and should be initialized by the program using the TXS instruction.

When an interrupt occurs, the higher 8 bits of the program counter is pushed onto the stack first, the stack pointer is decremented by one, and then the lower 8 bits of the program counter is pushed onto the stack. Next the contents of the processor status register is pushed onto the stack. As each byte is pushed onto the stack. When the return from interrupt instruction (RTI) is executed, the program counter and processor status register data is pulled off the stack in reverse order from above.

The Accumulator is never pushed onto the stack automatically, so a Push Accumulator instruction (PHA) is provided to execute this function. Restoring the Accumulator to its previous value is accomplished by the Pull Accumulator instruction (PLA). It is executed in the reverse order of the PHA instruction.

The contents of the Processor Status Register (PS) are pushed and pulled to and from the stack with the PHP and PLP instructions, respectively.

During a subroutine call, only the program counter is pushed onto the stack. Therefore, any registers that should not be destroyed should be pushed onto the stack manually. To return from a subroutine call, the RTS instruction is used.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break flag (B)

When the BRK instruction is executed, the same operations are performed as in an interrupt. The address of the interrupt vector of the BRK instruction is the same as that of the lowest priority interrupt. The contents of the B flag can be checked to determine which condition caused the interrupt. If the BRK instruction caused the interrupt, the break flag will be "1", otherwise it will be "0".

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (ie., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or −128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is reset by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or resetting the negative flag.

INTERRUPTS

The M50734SP can be interrupted from 11 sources. The interrupts are vector interrupts, and their priorities and vector table is shown in Table 1. When the interrupt enable bit is set to "1", the interrupt request bit is set to "1" and the interrupt disable flag to "0", all interrupts except the reset and BRK instructions are acknowleded. The reset is treated as a nonmaskable interrupt of the highest priority.
This is shown in Figure 3.

Table 1. Interrupt vector address and priority

Interrupt source	Priority	Vector address
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{\text{INT}_2}$	2	$FFFD_{16}$, $FFFC_{16}$
R1 or $\overline{\text{INT}_1}$	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1, timer 2 or timer 3	4	$FFF9_{16}$, $FFF8_{16}$
HE or VE	5	$FFF7_{16}$, $FFF6_{16}$
Timer X, CNTR or BRK	6	$FFF5_{16}$, $FFF4_{16}$

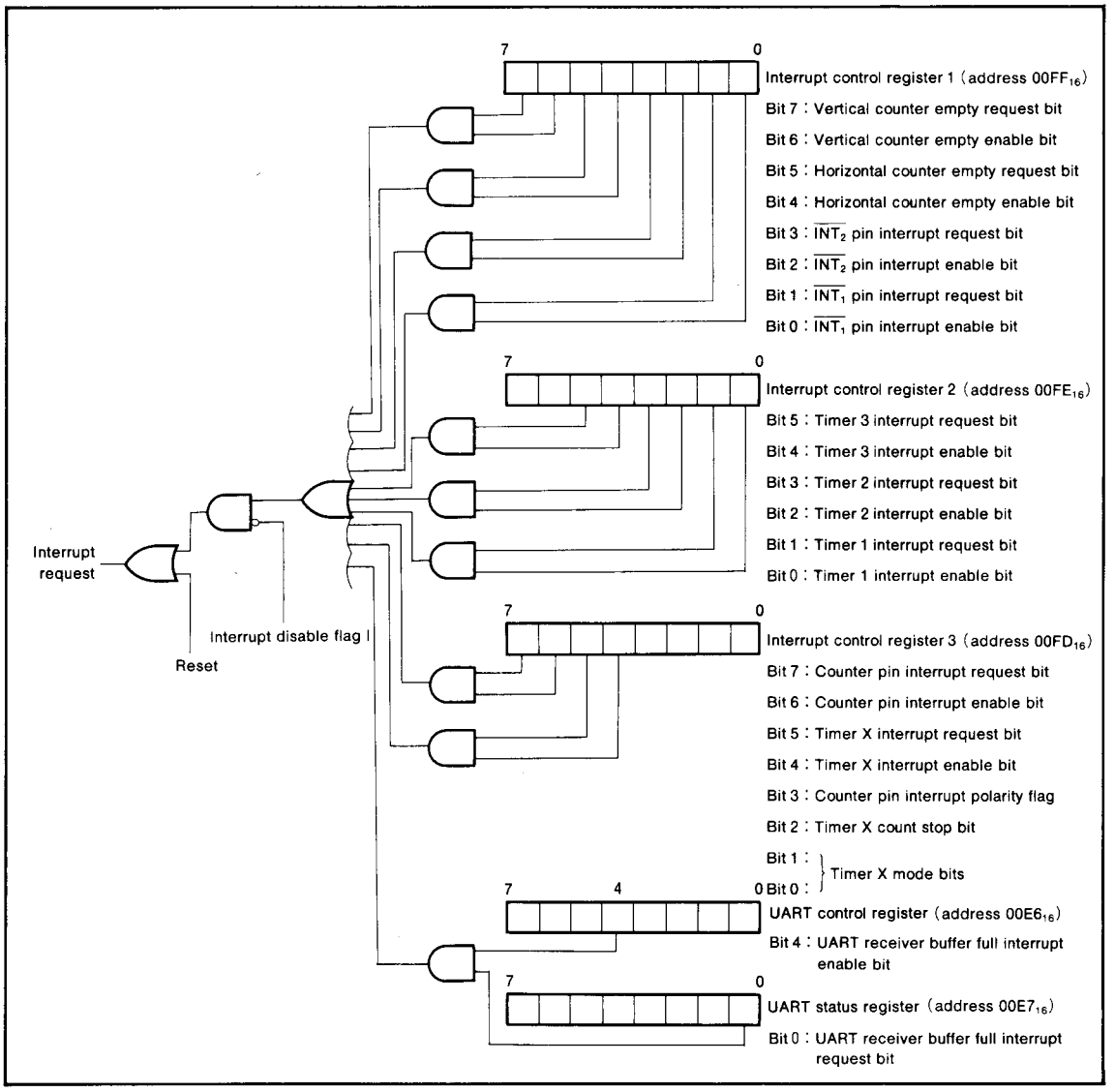


Fig.3 Interrupt control

TIMER (VCU)

The M50734SP provides a versatile control unit consisting of the timers and counters shown in Figure 4.
Each of the timers is described blow.

1. Timer X

The 16-bit timer X consists of timers X_H, X_L and their reload latches. This timer has four modes which are selected by bit 0 and bit 1 (timer X operation mode bits) of the interrupt control register 3 (address $00FD_{16}$). Figure 5 shows the structure of timer X and Figure 6 shows the structure of the interrupt control register 3.
Timer X can select the count source, either the oscillation frequency divided by 16 or the event clock which is input from the CNTR pin.
The timers are of the countdown type and the frequency ratio is 1/(n+1)(n:0~65535, decimal).

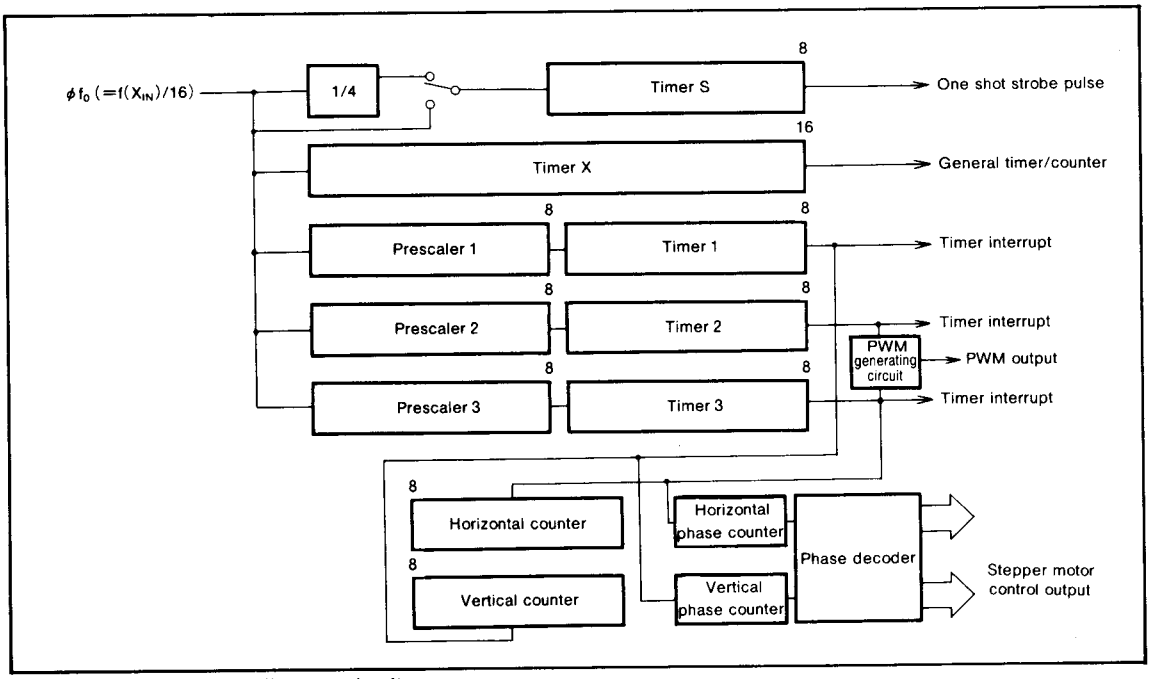


Fig.4 Structure of versatile control unit

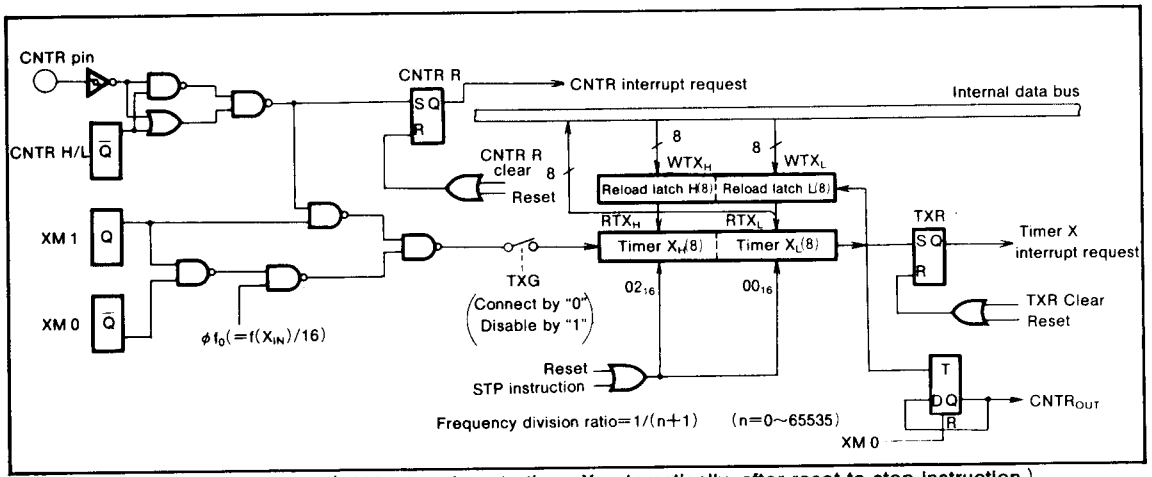


Fig.5 Block diagram of timer X (0200_{16} is written to timer X automatically, after reset to stop instruction.)

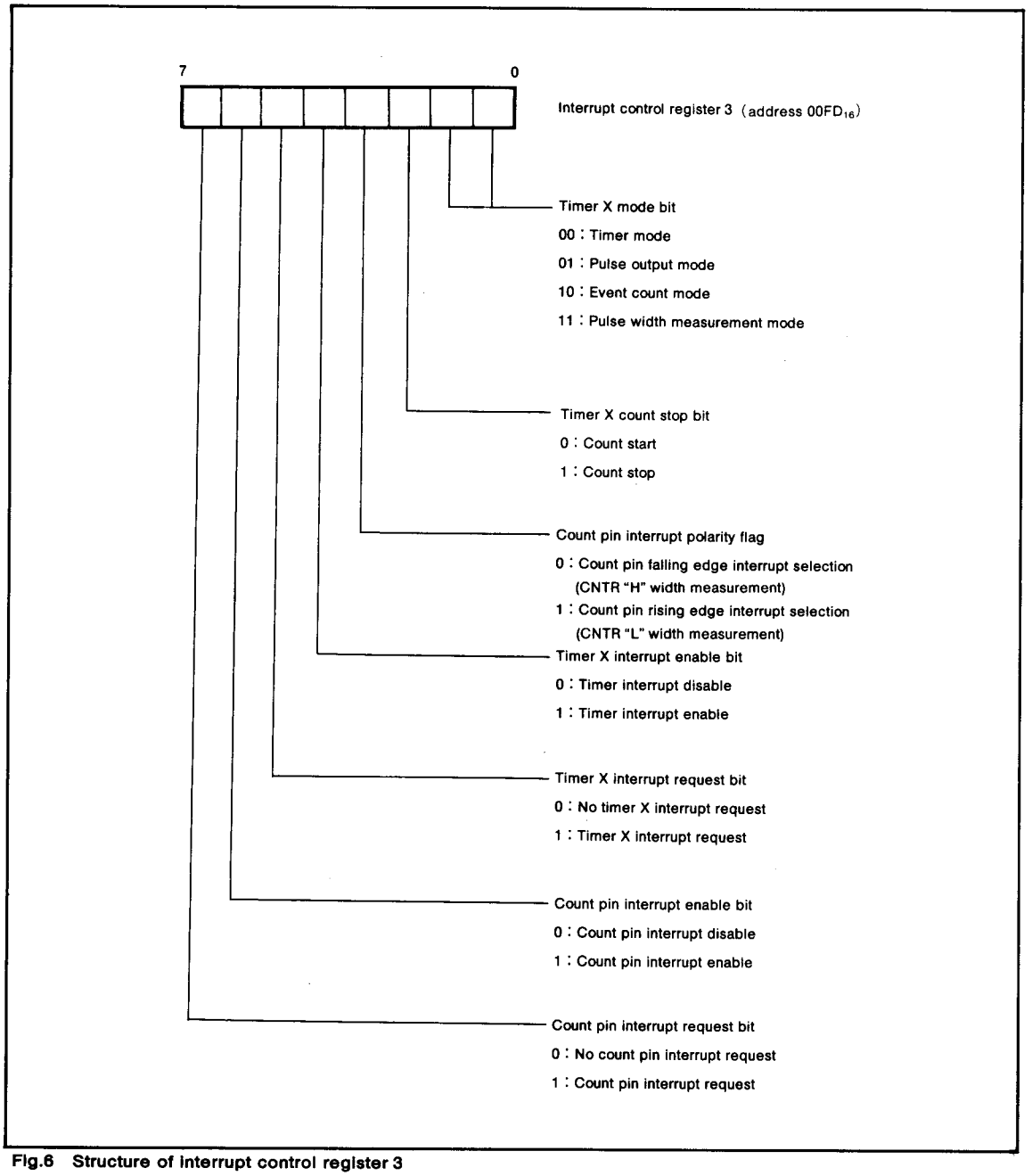


Fig.6 Structure of interrupt control register 3

The four modes of timer X are described below.

(1) Timer mode [00]

In this mode the oscillation frequency, divided by 16, is counted. When the contents of the timer reaches "0", the interrupt request bit is set to "1". At the next cycle, the contents of the timer latch are reloaded and the count continues. After resetting, this mode is set automatically.

(2) Pulse output mode (01)
Every time the contents of the timer reach "0", the output signal from the $P0_7$/CNTR pin changes polarity.
If this mode is used, bit 2 of port P0 function register and bit 2 of the port P0 directional register must be set to "1".

(3) Event counter mode (10)
The operation is the same as in the timer mode except that the input signal from pin $P0_7$/CNTR is counted. However, if this mode is used, bit 2 of port P0 directional register must be set to "0". The counter pin interrupt request bit is set by the event input signal. Therefore the counter pin interrupt enable bit must be set to "0" to prevent an interrupt.

(4) Pulse width measurement mode (11)
The oscillation frequency, divided by 16, is counted while the level of pin $P0_7$/CNTR is either low or high. The level of pin $P0_7$/CNTR is selected by interrupt control register 3, bit 3.
When the contents of the timer X reach "0", the interrupt request bit is set to "1". At the next cycle, the latches contents are reloaded and counting continues.
If this mode is used, the counter pin interrupt must be enabled and the timer X interrupt prohibited.

2. Timer 1, Timer 2, Timer 3

Timer 1, timer 2 and timer 3 each consist of an 8-bit prescaler, an 8-bit timer, a prescaler reload latch and a timer reload latch. The structure of timer 1, timer 2 and timer 3 is shown in Figure 7.
The count source for timer 1, timer 2 and timer 3 is the oscillation frequency divided by 16. These timers are of the countdown type and the frequency, ratio of the prescaler and timer is $1/(n+1)$ (n:0~255, decimal).
Timer 1 and timer 3 are also used to determine the step rate by connecting with the stepping motor control circuit and as timers for the PWM pulse output signal.

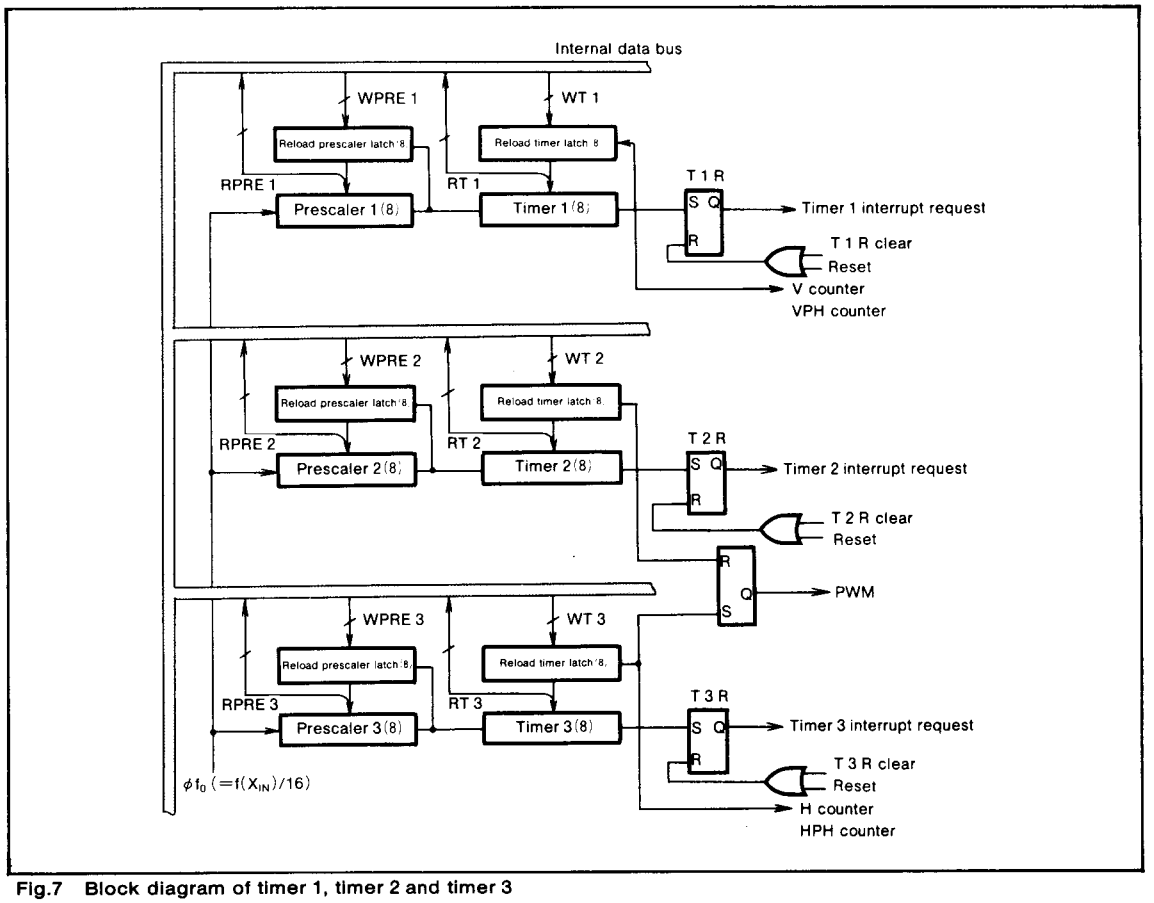


Fig.7 Block diagram of timer 1, timer 2 and timer 3

3. Timer S

The structure of timer S is shown in Figure 8. Timer S has no reload latch. Whether or not a 1/4 frequency divider should be put before the timer, is determined by bit 2 of the port P2 and port P3 function register (P2P3FR).

If the 1/4 frequency divider is bypassed, the clock produced by dividing the oscillation frequency by 16 becomes the count source for timers S. If it is built in, the oscillation frequency, divided by 16, (then divided by 4 once more), becomes the clock. This timer is of the countdown type and the frequency ratio is 1/(s+1)(s:0~255, decimal).

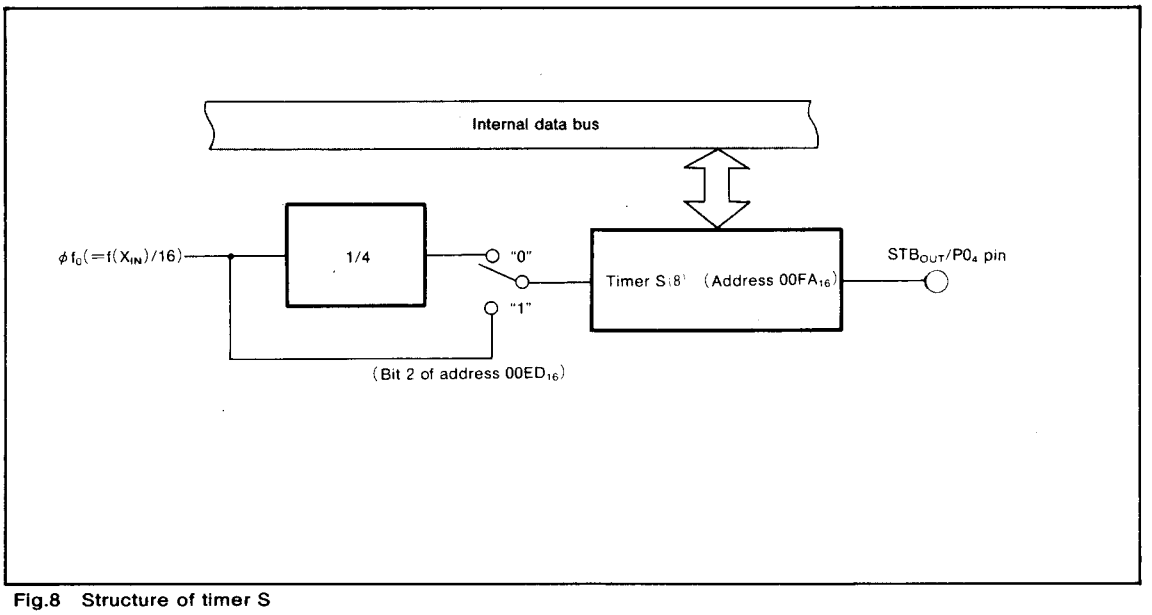


Fig.8 Structure of timer S

WATCHDOG TIMER

As shown in Figure 9, the watchdog timer is composed of a 10-bit prescaler and 8-bit timer counter. Timer W can be read from or written to by software. After a reset, this timer is set to FF_{16}. Every timer the prescaler overflows, timer W is decremented. When the contents of timer W (N_W) changes "00", the WD_{OUT} pin changes from "L" to "H".

If the oscillation frequency is 8MHz, the time (T_W) until the timer W underflows can be set by the following equation:

$T_W = 16/f(X_{IN}) \times 1024 \times (N_W \pm 1/2)$ $(1 \leq N_W \leq 255$, decimal)

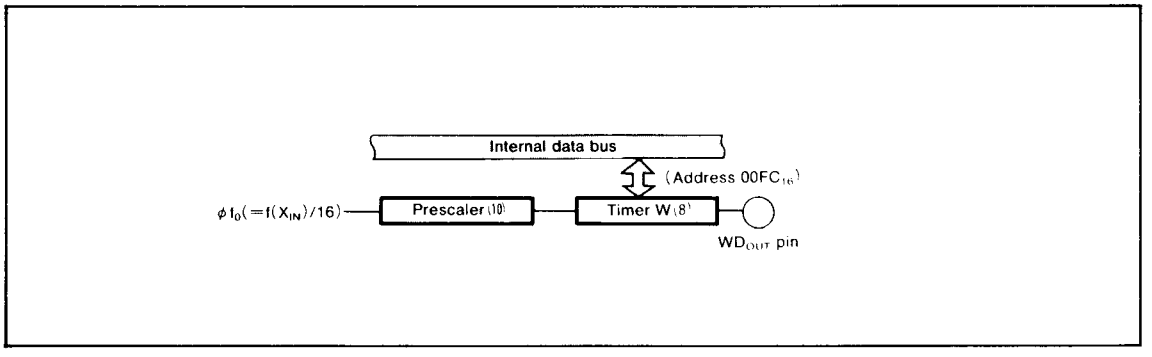


Fig.9 Structure of the watchdog timer

STEPPER MOTOR CONTROL CIRCUIT

Two identical circuits for the control of two stepper motors (for a horizontal and vertical direction) are built in to the M50734SP and can operate independently. The block diagram is shown in Figure 10.

The horizontal and vertical counters are both 8-bit binary counters which contain the number of steps. The horizontal phase counter (HPHC) and vertical phase counter (VPHC) are both 3-bit binary counters and perform phase decoding. The two stepping motor control registers are 4-bit registers controlling, start/stop, single-step, direction and 2-2 or 2-1 phase drive. The functions of these registers and the relation between the phase counter and the phase output signals are shown in Figure 11.

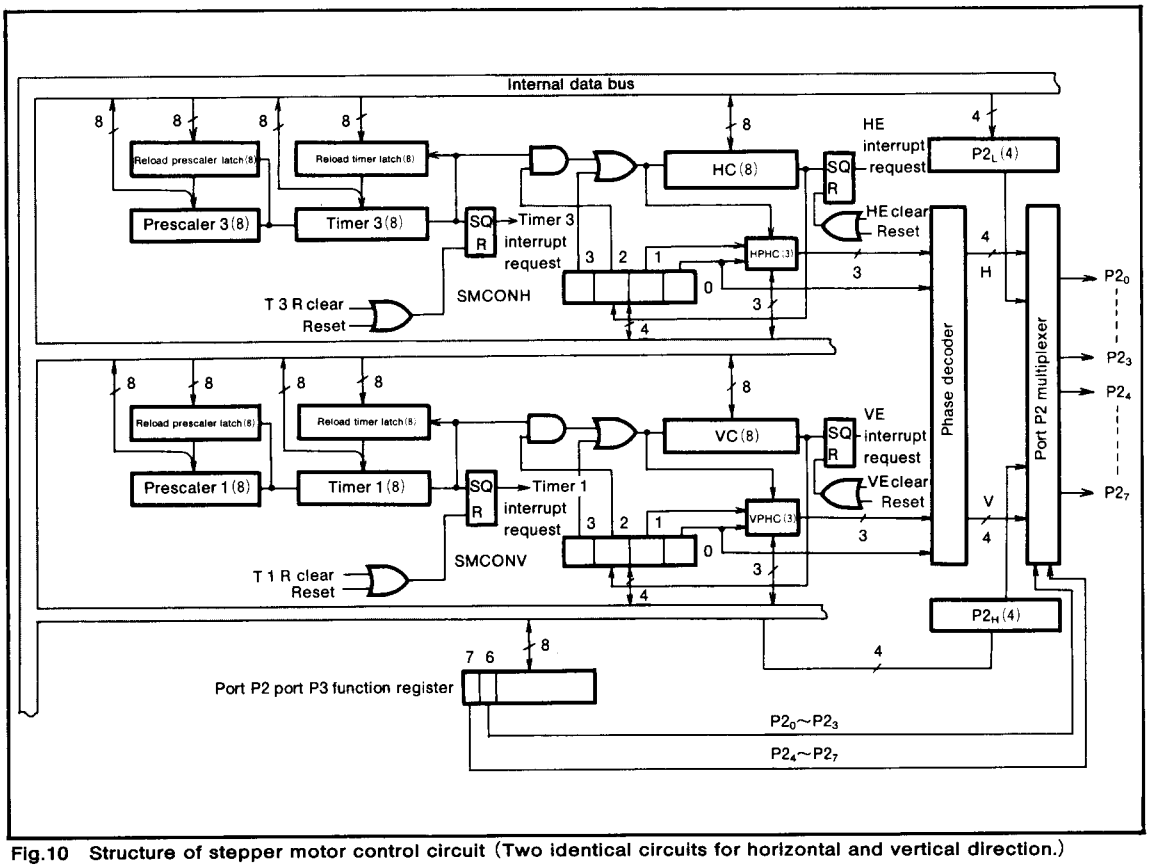


Fig.10 Structure of stepper motor control circuit (Two identical circuits for horizontal and vertical direction.)

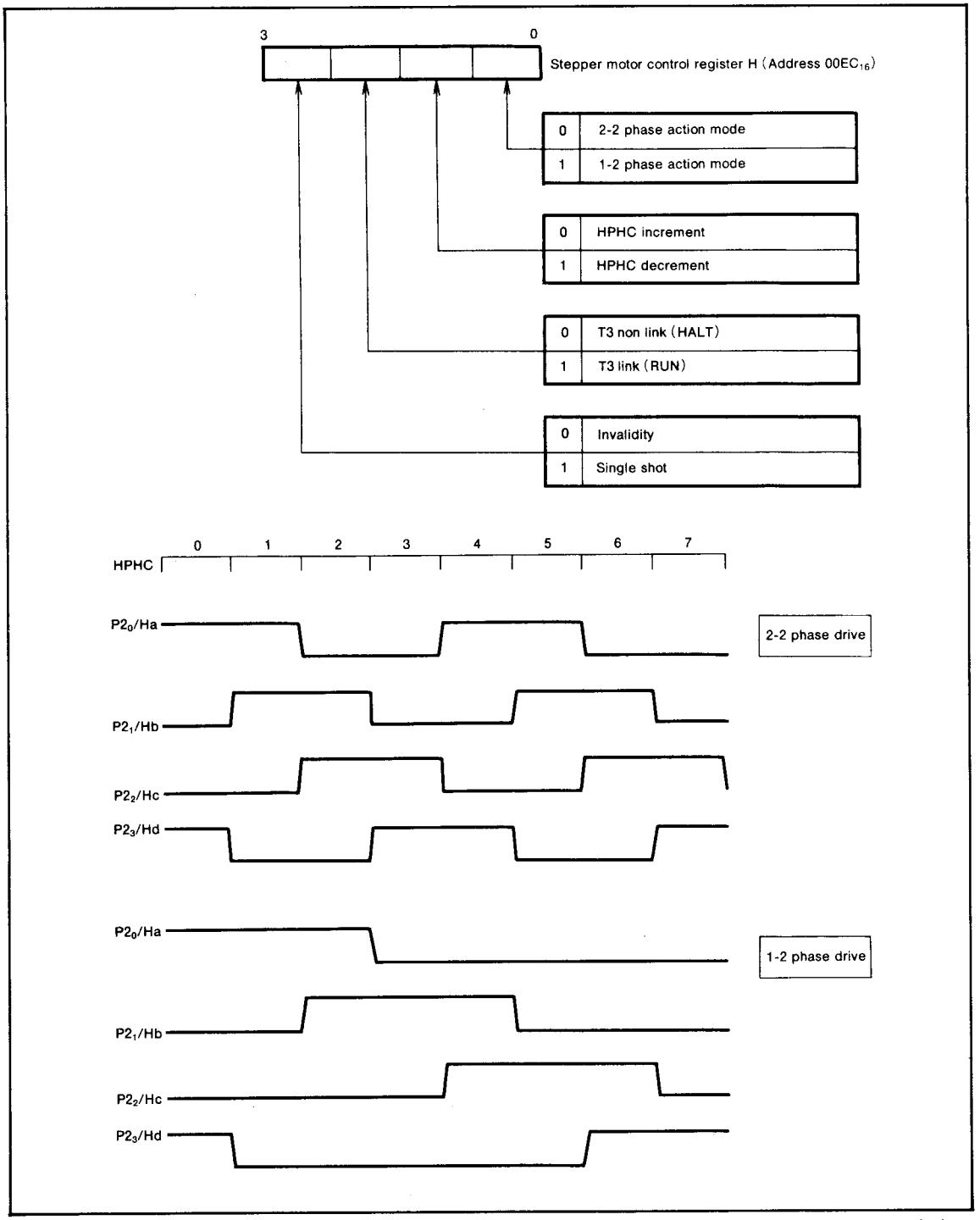


Fig.11 Bit functions of the stepper motor control register and relation between horizontal phase counter and phase output signals

PWM (Pulse width modulation)

The M50734SP includes a control circuit which generates pulses of various duty cycles utilizing timer 2 and 3.The PWM signal is internally generated as shown in Figure 12.

W3 is the time interval (time from reload to zero) of timer 3 and W2 the time interval of timer 2.

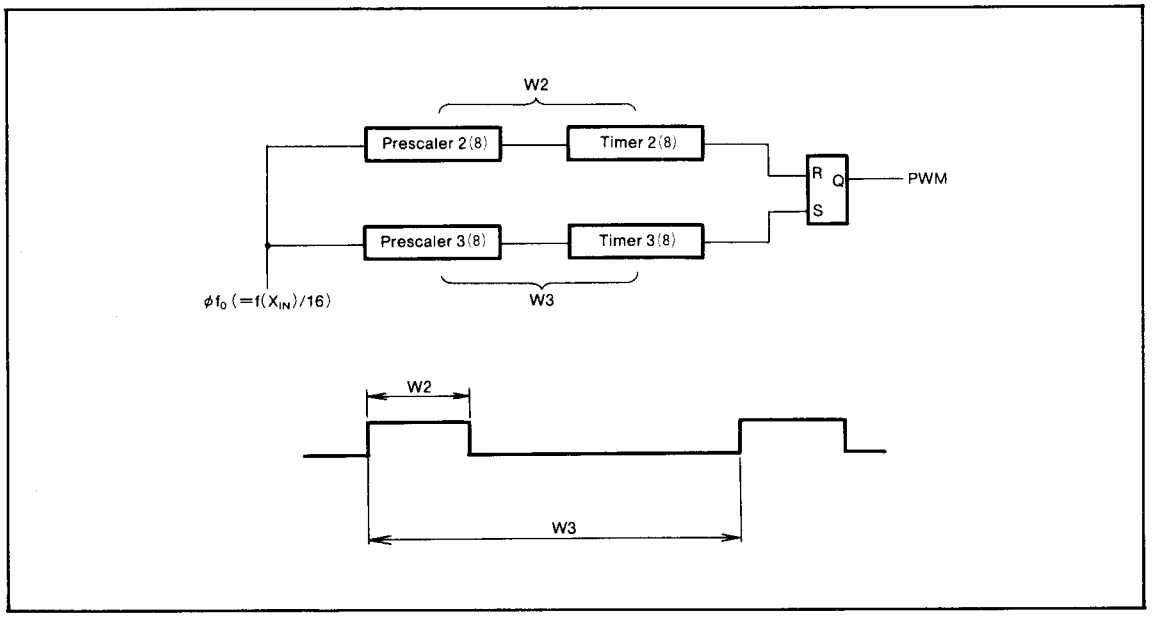


Fig.12 PWM signal generation

UART

The M50734SP has an 8-bit duplex UART. The block diagram is shown in Figure 13, and the bit structure of the UART control register and UART status register is shown in Figure 14. The UART control register can be read from or written to by software, but the UART status register can only be read.

Transmit/receive character length and parity addition are set by bit 0, 1 and 2 of the UART control register.

The four possible transmit/receive formats are as follows:

(1) 7-bit (no parity)
(2) 7-bit + parity (odd or even selectable)
(3) 8-bit (no parity).
(4) 8-bit + parity (odd and even selectable)

Each bit of the UART control register and UART status register is described in detail below.

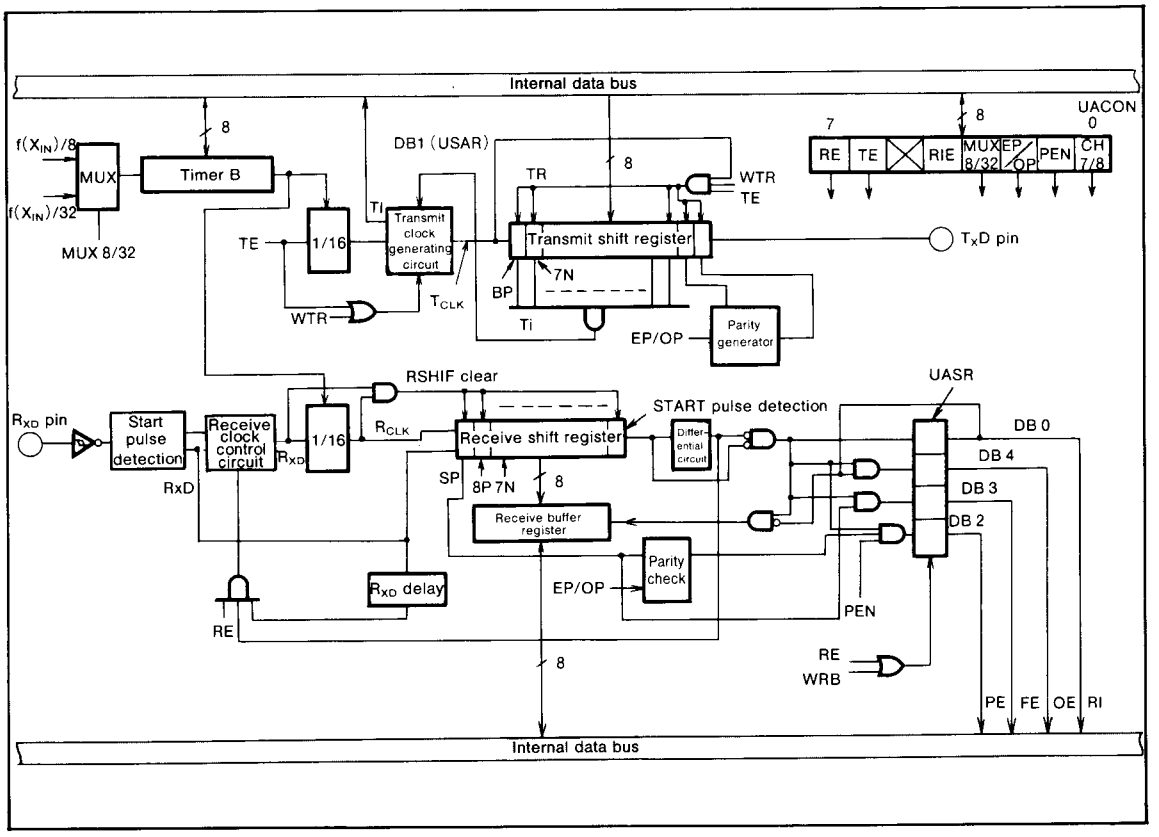


Fig.13 UART (timer B frequency ratio : 1/(B+1))

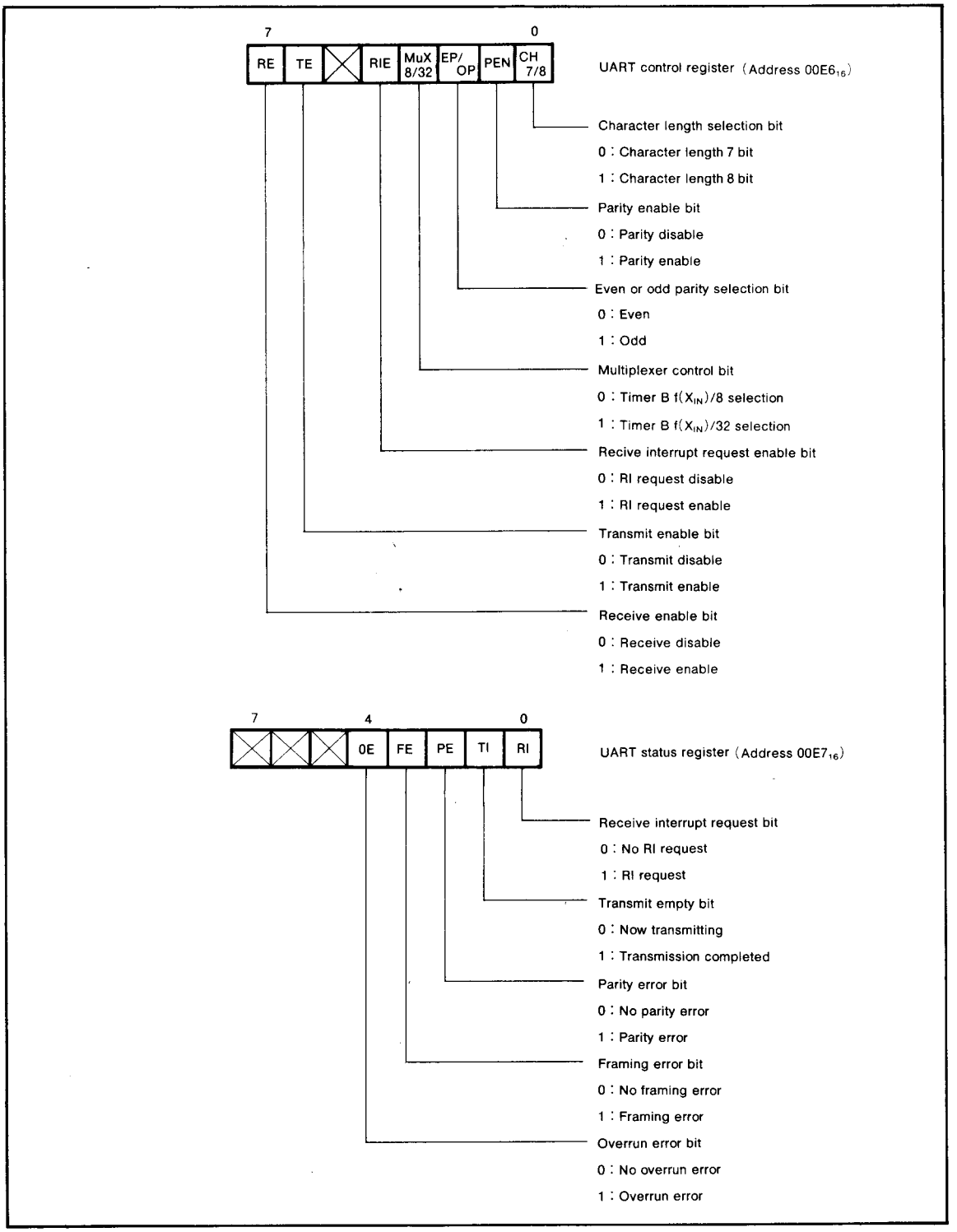


Fig.14 Bit structure of UART control register and UART status register

Character length selection bit (CH7/8)
If this bit is "0", the 7-bit character mode is selected;
If it is set to "1", the 8-bit character mode is selected.
It can be read from and written to by software.

Parity enable bit (PEN)
If this bit is "1", parity is added to the characters of the signal being transmitted or received. If this bit is to "0", parity is not added, and in the receive state a parity error can not occur.
If can be read from or written to by software.

Even or odd parity select bit (EP/OP)
If this bit is "0", even parity is selected, if set to "1", odd parity is selected. It can be read from or written to by software.

Multiplexer control bit (MuX 8/32)
This bit selects the count source of timer B. If it is "0", the oscillation frequency, divided by 8, is selected; if it is "1", the oscillation frequency divided by 32 is selected.
It can be read from or written to by software.

Receive interrupt request enable bit (RIE)
If this bit is "1", the receive interrupt request flag (RI) can be set; if it is cleared to "0", interrupts are inhibited. Even if the interrupts are inhibited, the RI flag remains as is.
It can be read from or written to by software.

Transmit enable bit (TE)
If this bit is "0", the transmit clock goes "H", the transmit interrupt bit is cleared "0" and goes to the initial state. When set to "1", transmission will start. It can be read from or written to by software.

Receive enable bit (RE)
If this bit is "0", the receive interrupt request bit (RI) parity error bit (PE), framing error bit (FE) and overrun error bit (OE) are cleared to the initial state. If it is "1", it will be in the receive enable state, and when the start bit is input into the $P0_7$/RxD pin, the receive operation will start.
This bit can be read from or written to by software.

Receive interrupt request bit (RI)
This bit is set to "1" when a receive interrupt request occurs. It is cleared to "0" when the receive enable bit (RE) is set to "0" or when data is written to the receive buffer register.

Transmit empty bit (TI)
This bit is cleared to "0" when the transmit enable bit (TE) is set to "0" or when data is written to the transmit shift register (TR). When the transmission is completed, it is set to "1".

Parity error bit (PE)
This bit is set to "1" when the parity odd or even selection bit is "0" and the number of is in the received data is even, or the parity odd or even selection bit is set to "1" and the number of "1"'s in the receive data is odd.
It is cleared to "0" when the receive enable bit (RE) is set to "0" or data is written to the receive buffer register.

Framing error bit (FE)
This bit is cleared to "0" when the receive enable bit (RE) is set to "0" or data is written to the receive buffer register. When a framing error occurs, this bit is set to "1". A framing error occurs when transmitting data from the receive shift register to the receive buffer register and the stop bit of the receive data does not exist.

Overrun error bit (OE)
This bit is cleared to "0" when the receive enable bit is set to "0" or data is written to the receive buffer register. When an overrun error occurs, this bit is set to "1".
An overrun error occurs when the next data is transmitted from the receive shift register to the receive buffer register while the receive interrupt request bit (RI) is "1".
The receive and transmit operations are shown in Figure 15 and Figure 16.

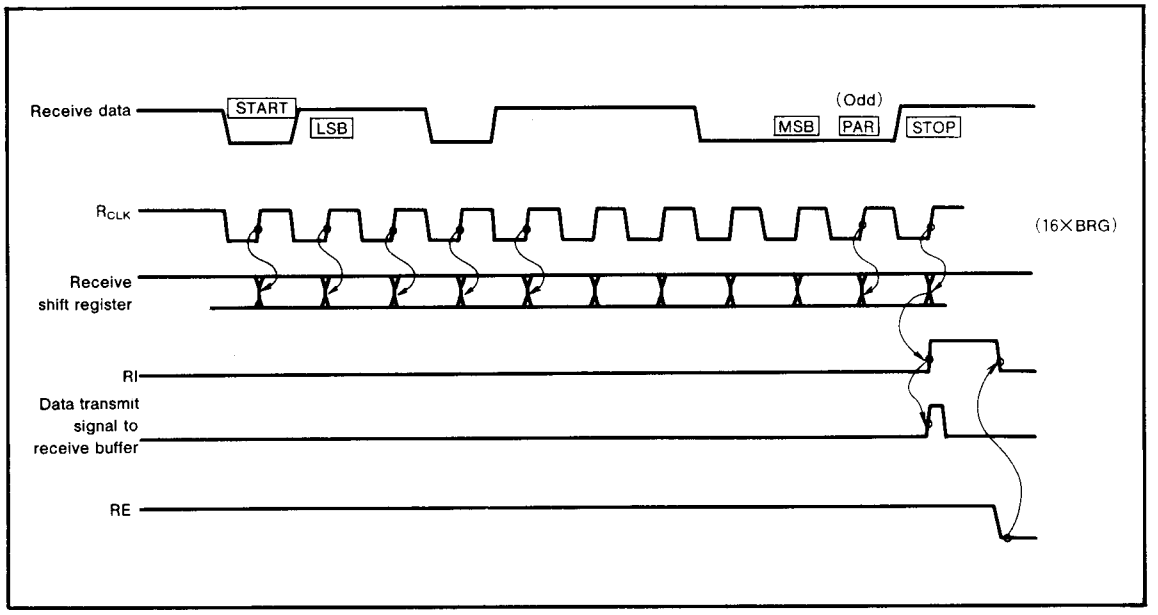


Fig.15 Receive operation (8-bit+1 parity mode)

(Each receive data bit is read by a master slave flip-flop when the R_{CLK} signal is "L". When the R_{CLK} signal goes from "L" to "H", it is transferred to the slave flip-flop and latched. When the start bit "0" (which is latched first), overflows from the last bit of the 11 bit shift register, it is detected as the stop bit and the RI bit is set.)

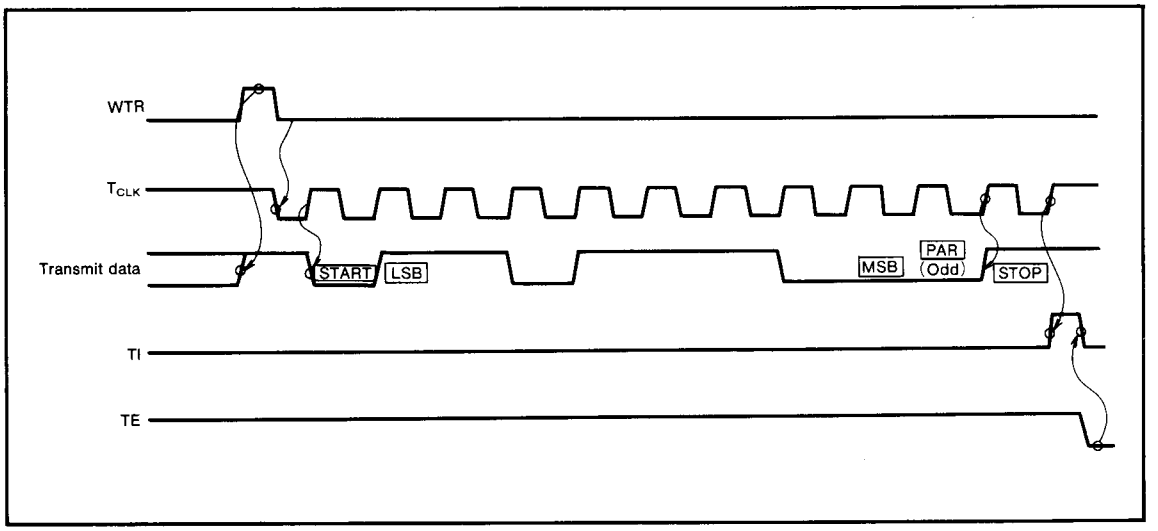


Fig.16 Transmit operation (8-bit+1 parity mode)

(When the T_{CLK} signal goes from "L" to "H", the transmit data is shifted. After the stop bit is transferred, the TI bit is set to "1" The TI bit is cleared when TE is set to "0" or when data is written to the transmit shift register (TR).)

CLOCKED SERIAL I/O

The M50734SP has one 8-bit clock serial I/O. Its structure and transmit/receive operation are shown in Figure 17. Data is transferred at a transmit speed of 1/4 the oscillation frequency.

Data is transferred and received beginning at the most significant bit.

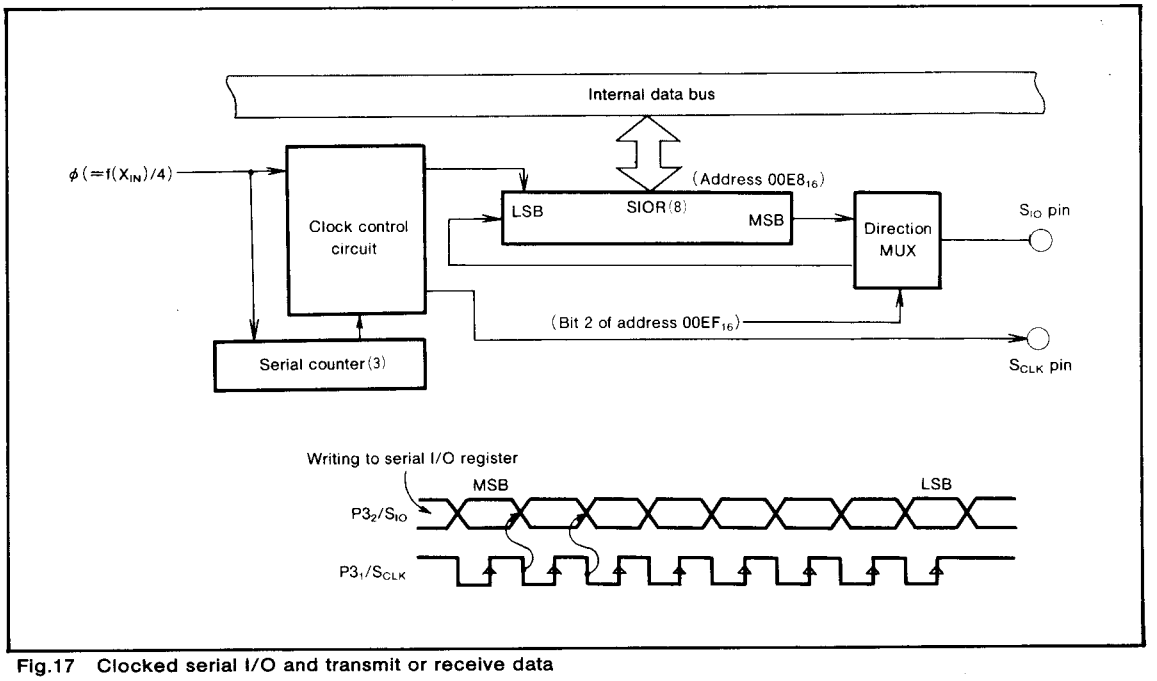


Fig.17 Clocked serial I/O and transmit or receive data

A-D CONVERTER

The A-D conversion circuit is shown in Figure 18. With the A-D analog input pins $P4_0/AN_0 \sim P4_3/AN_3$ are in common with the input pins of the data bus. The A-D control register (address $00E9_{16}$) is a 3-bit register. One of four analog input pins is selected by bit 0 and 1. The relation between bit 0, 1 and the selected analog input pin is shown in Figure 19. The A-D conversion speed is 36μs (at 8MHz frequency) with an absolute conversion precision of $\pm$ 3LSB.

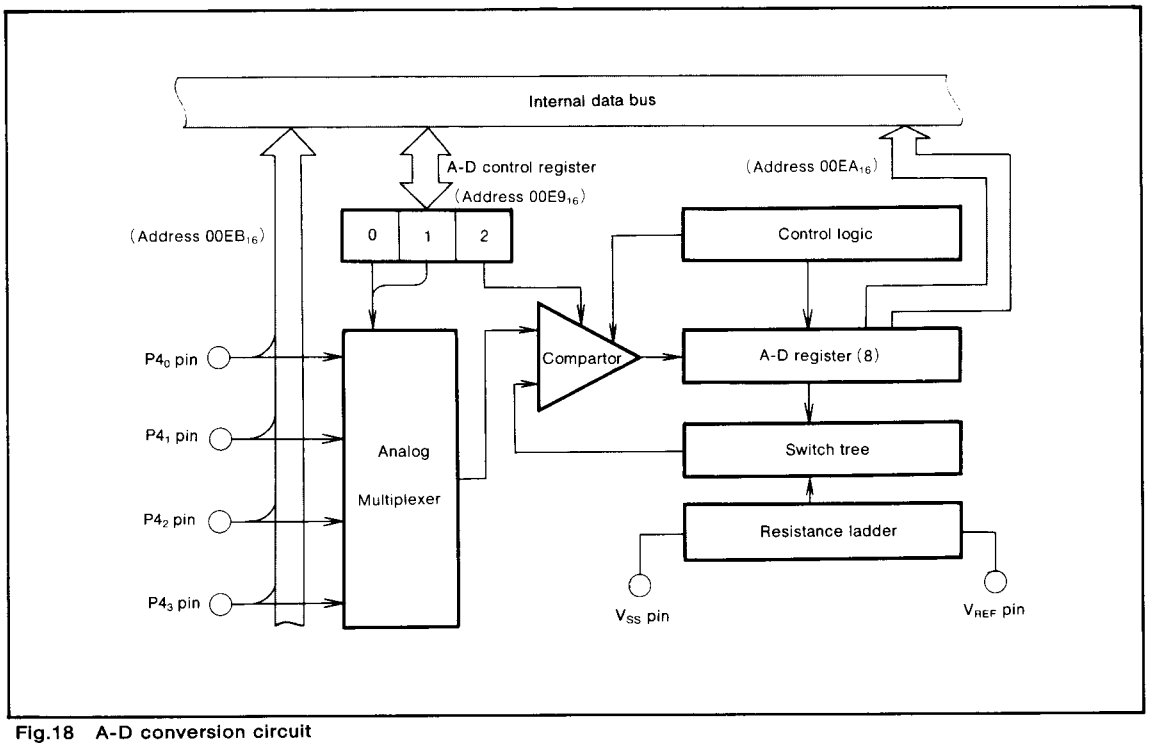


Fig.18 A-D conversion circuit

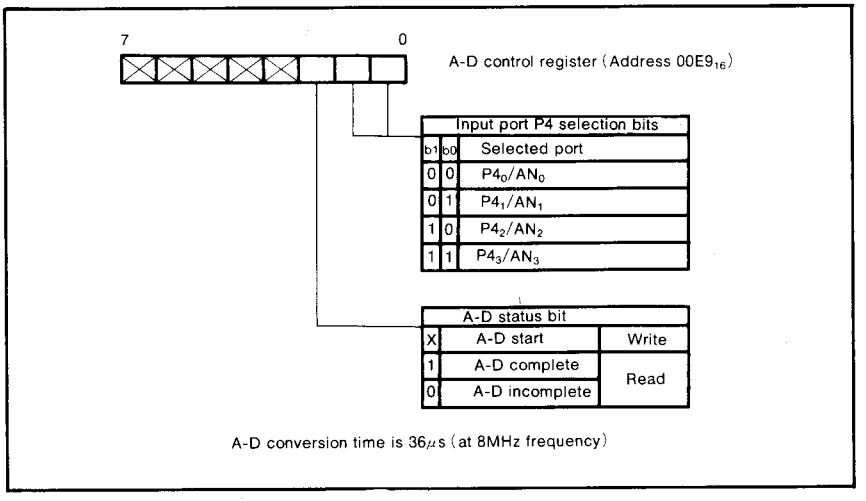


Fig.19 Structure of A-D control register

RESET CIRCUIT

The M50734SP is reset according to the sequence shown in Figure 20. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 22.

An example of the reset circuit is shown in Figure 21.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

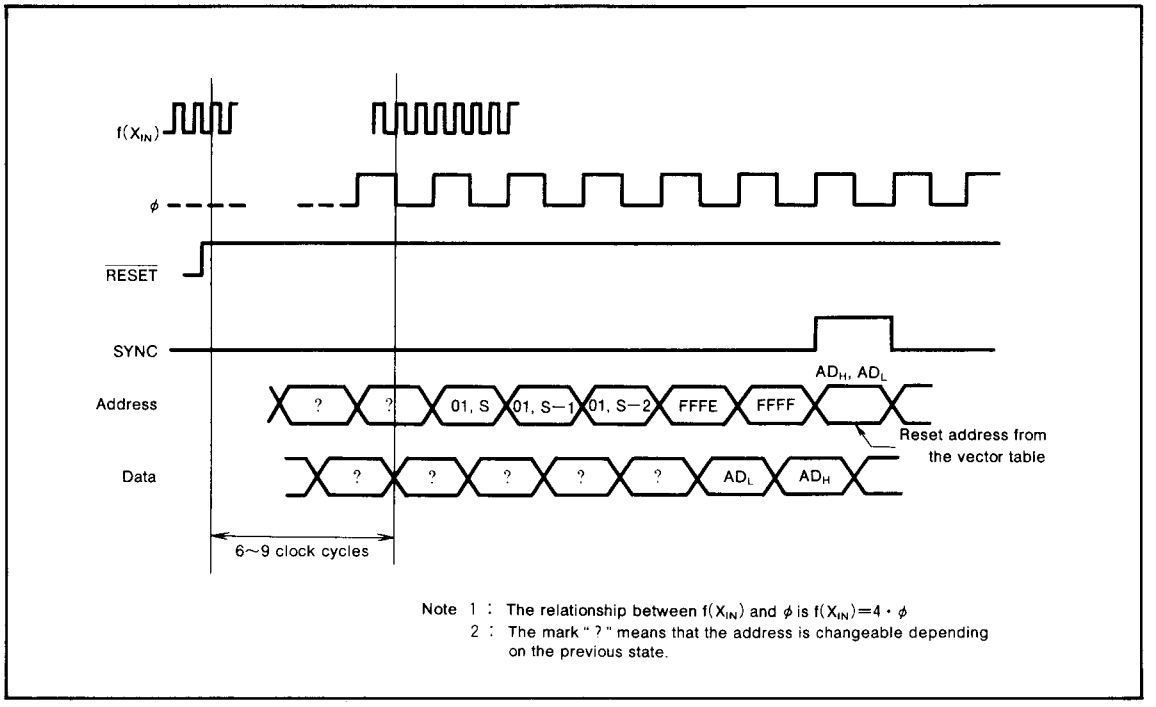


Fig.20 Timing diagram at reset

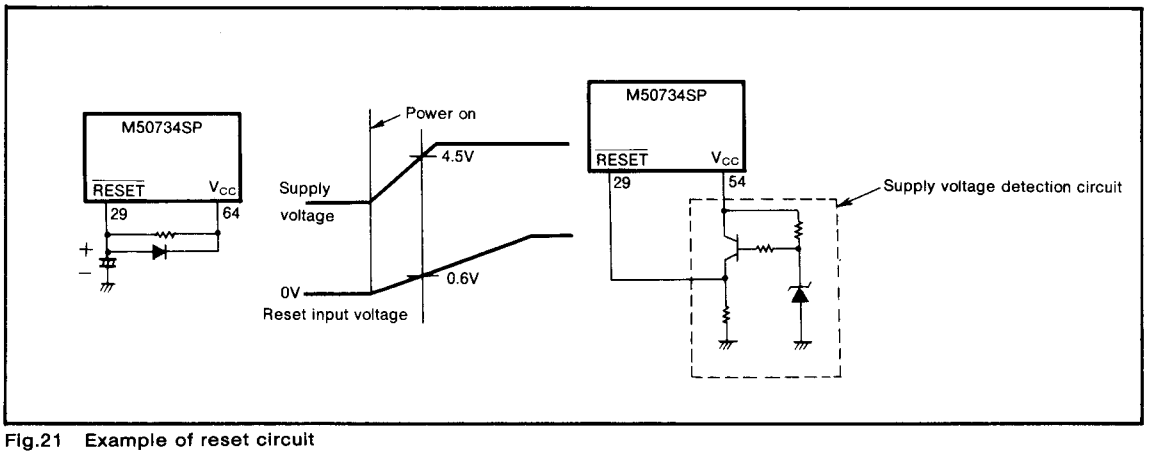


Fig.21 Example of reset circuit

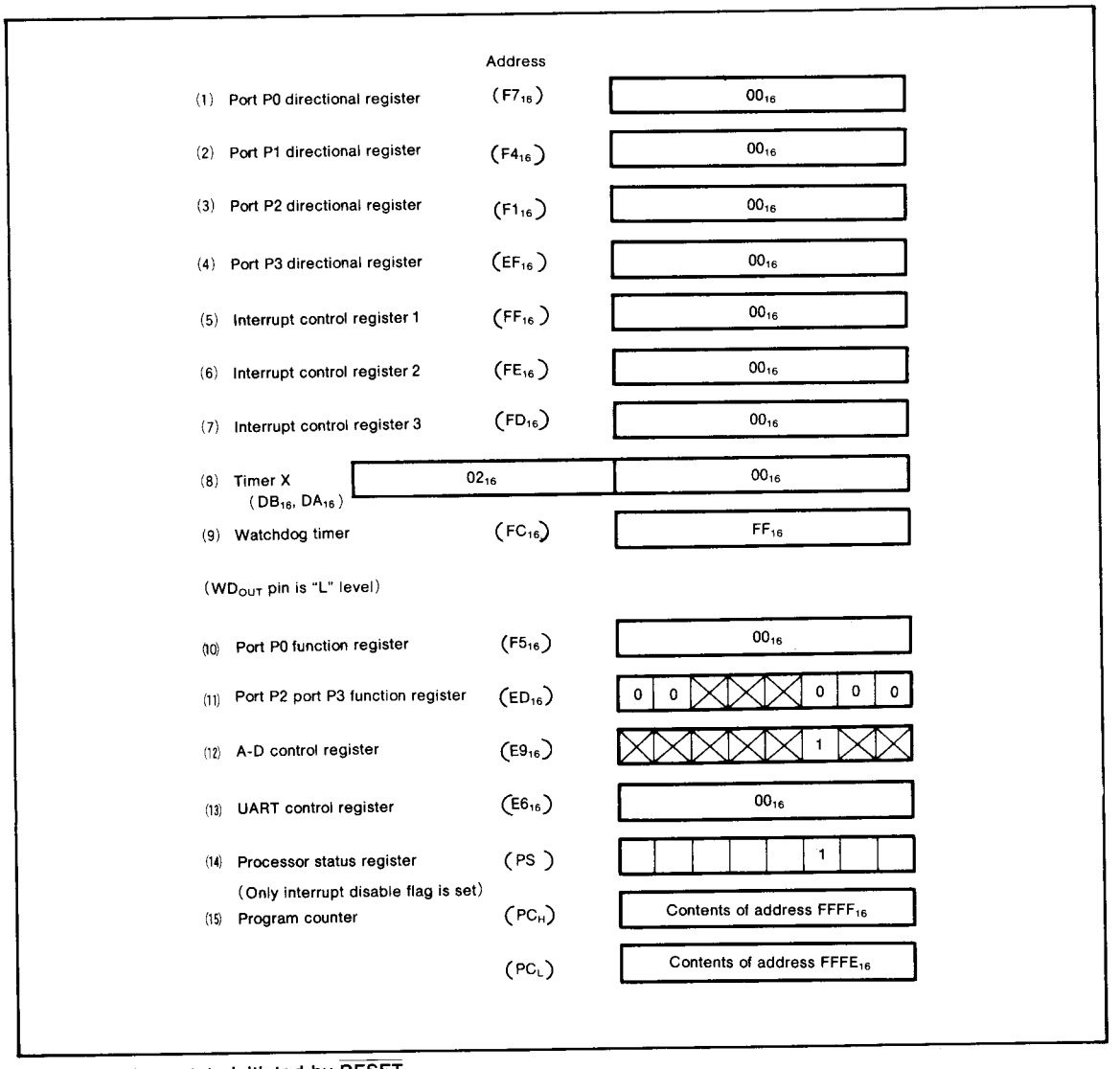


Fig.22 Register state initiated by $\overline{\text{RESET}}$

I/O PORTS

(1) Port P0

Port P0 is a CMOS three state 8-bit input/output port. As shown in the memory map of Figure 1, it is located at address $00F6_{16}$ on the zero page. Port P0 has a directional register (address $00F7_{16}$) to program each individual bit either for input or output. Those pins set to "1" are for output and those programmed to "0" are for input.

This port also has a double function which can be selected for individual bits by the port P0 function register (address $00F5_{16}$). If the contents of the port P0 function register are "0", this port is used as a normal port; if they are "1", this port is used as a special port for functions such as interrupt input, UART input/output etc.

The structure of the port P0 function register is shown in Figure 23.

(2) Port P1

Port P1 is a CMOS tri-state 8-bit input/output port. The I/O function can be selected in the same way as for port P0. An 8-bit input latch (address $00F2_{16}$) of the transparent type, is built into port P1. Therefore, port P1 can be used either by reading address $00F3_{16}$, for non-latched data, or address $00F2_{16}$, for latched data.

(3) Port P2

This port is a CMOS three state 8-bit input/output port. It can be set to input/output in the same way as port P0. By software 2 channels (1 channel=4-bit) from the stepping motor control circuit can be output simultaneously. Four-phase outputs can be selected by bit 6 and bit 7 of the port P2 port P3 function register (address $00ED_{16}$). The structure of the port P2 and P3 function register is shown in Figure 24.

(4) Port P3

Port P3 is an 8-bit CMOS three state input/output port. The pins of port P3 can be set to input/output in the same way as port P0. Ports P3, $P3_1$ and $P3_2$ have double functions, which are determined by bits 0 and 1 of the port P2 and port P3 function register (address $00ED_{16}$).

(5) Port P4

Port P4 is a 4-bit input port. It can be used not only a as 4-bit digital input port, but also as an analog input port for the A-D converter.

If it is used as a digital input port, the contents of address $00EB_{16}$ are read.

The 4 high-order bits of address $00EB_{16}$ are usually "0".

If port P4 is used as analog input, the ports are multiplexed by the A-D control register and A-D conversion is executed. When digital input is performed during A-D conversion, care is necessary as the precision of A-D conversion can sometimes be affected.

(6) WD_{OUT} pin

This pin is set after the contents of the watchdog timer W resetting. It can not be cleared by software, only by reset.

(7) ϕ pin

The oscillation frequency, divided by 4, is output from this pin.

(8) Address bus and data bus

The 8 high order bits of the address bus are output directly from $A_{15} \sim A_8$. Addresses and data of $A_7/D_7 \sim A_0/D_0$ are multiplexed. When ϕ is "H", the 8 low order bits are output, and when ϕ is "L", data can be transferred between $A_7/D_7 \sim A_0/D_0$ and external memory. The 8 low order address bits must be latched in an external latch with the ALE signal.

(9) $\overline{RD}$ pin

While $\overline{RD}$ is "L", the M50734SP can read external memory.

(10) $\overline{WR}$ pin

While $\overline{WR}$ is "L", the M50734SP can write to external memory.

(11) ALE pin

The ALE pin outputs the ALE signal to latch the low order address bits. The ALE signal is always generated once during a every machine cycle.

The 8 low order bits of the address bus start output when ALE signal changes from low to high. A transparent latch is used to allow an address set-up time. The address is latched when the ALE signal changes from high to low.

(12) SYNC pin

The SYNC signal controls single step operation of the M50734SP. It is synchronized with the ϕ signal and is output when an op code is fetched.

(13) V_{REF} pin

V_{REF} serves as reference voltage for the A-D converter.

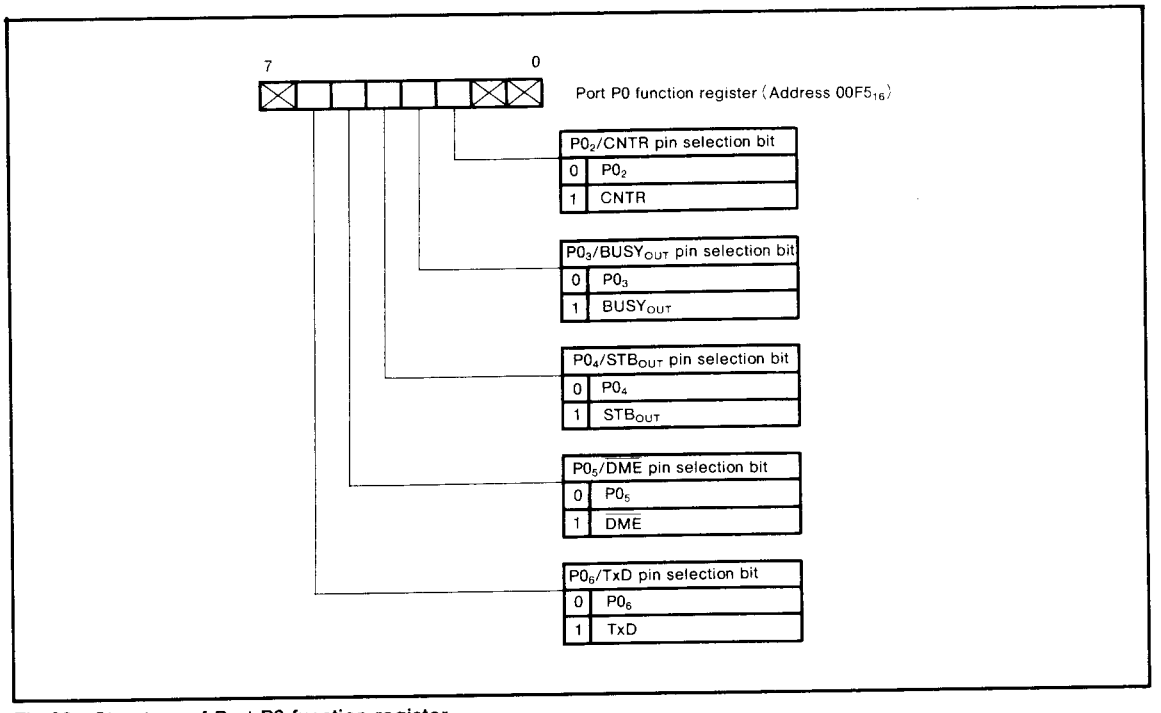


Fig.23 Structure of Port P0 function register

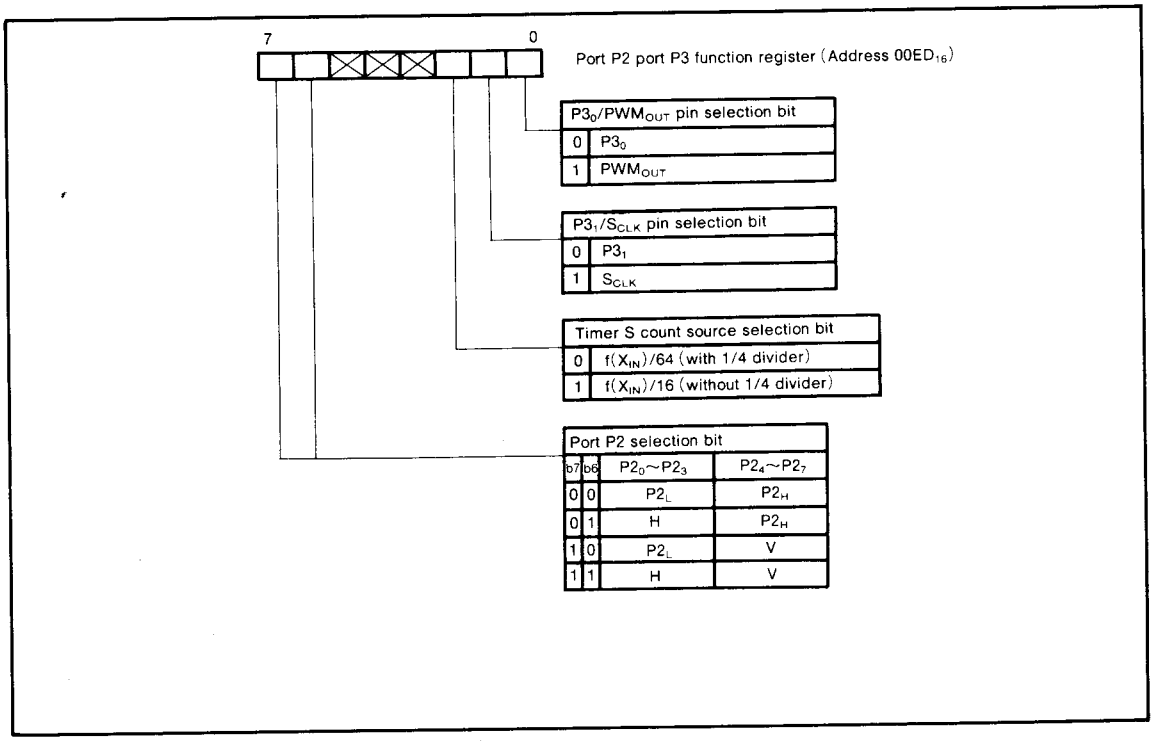


Fig.24 Structure of Port P2 and P3 function register

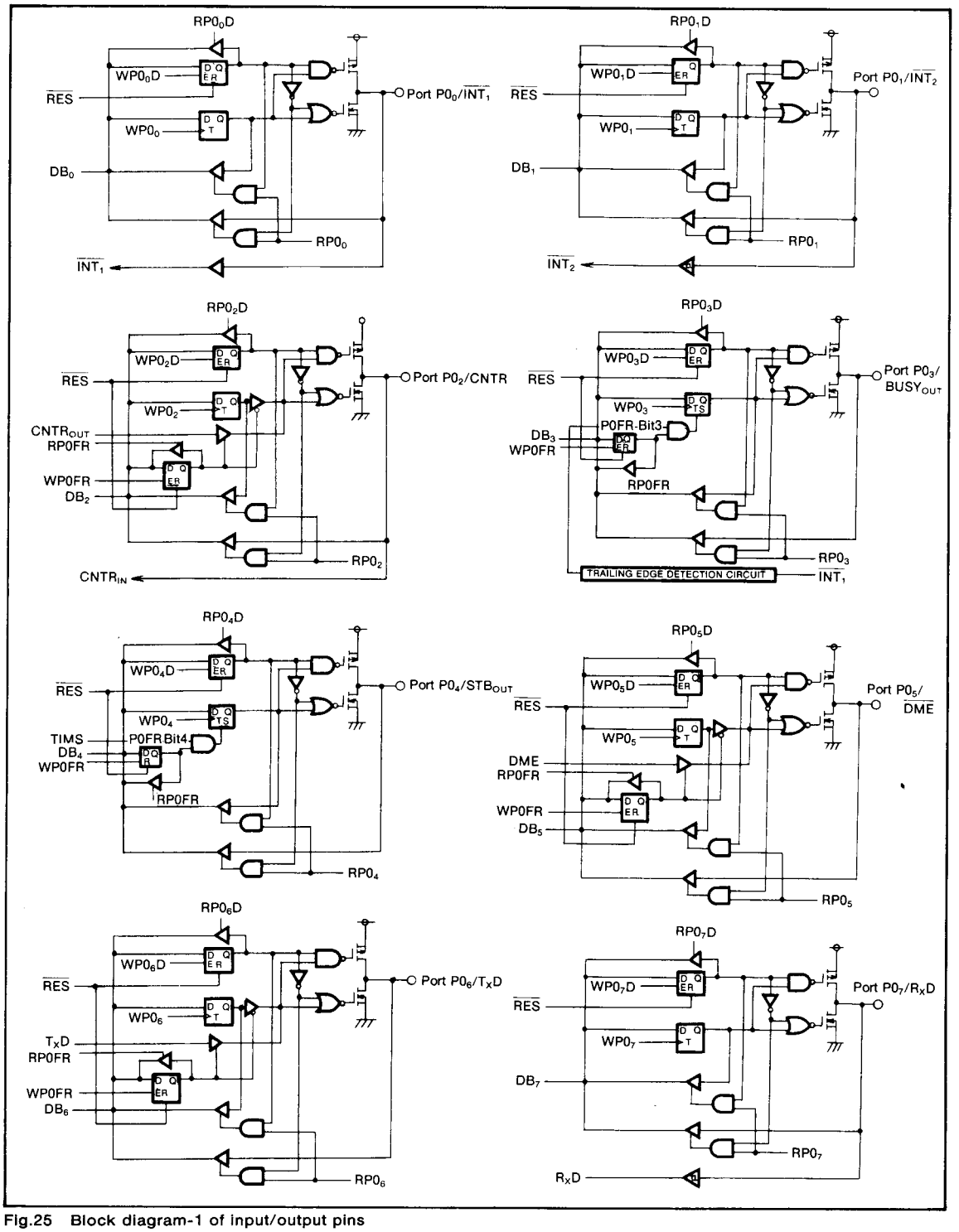


Fig.25 Block diagram-1 of input/output pins

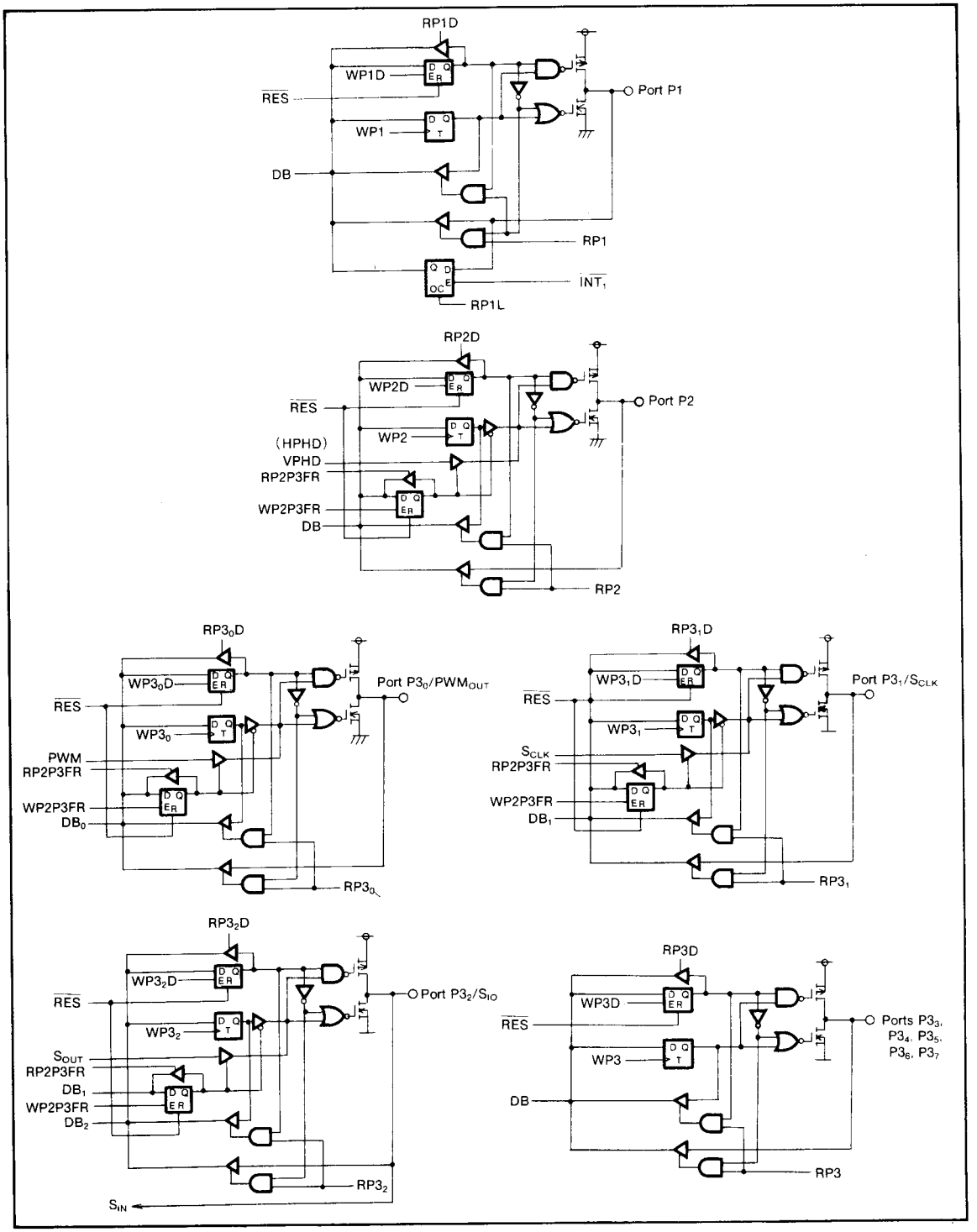


Fig.26 Block diagram-2 of input/output pins

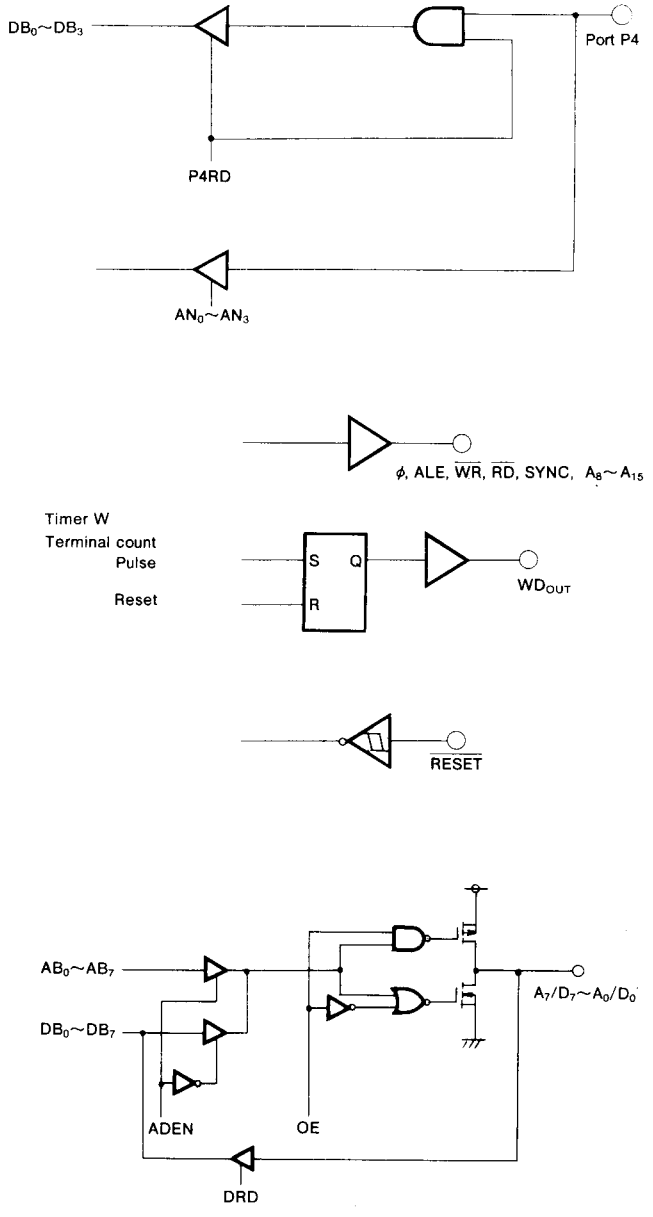


Fig.27 Block diagram-3 of input/output pins

CLOCK GENERATING CIRCUIT

The built-in clock generating ciruit is shown in Figure 28. When a STP instruction is executed, the oscillation stops at the "H" state of the internal clock ϕ. Moreover, timer X is set to 0200_{16}, and the oscillation output divided by 16 is connected to timer X. This connection is cleared when timer X overflows, or by resetting as discussed in the timer section.

The oscillation restarts after an interrupt is accepted, but the internal clock ϕ remains at "H" until timer X overflows. This is necessary because the oscillation needs a set-up period if a ceramic or a crystal oscillator is used. When the WIT instruction is executed, the internal clock ϕ stops at "H" but the oscillator will not stop. This wait state is cleared after an interrupt is accepted. Since the oscillation does not stopp, the following instruction will be executed immediately and not after a fixed time as for the STP instruction. The corresponding interrupt enable bit must be set to "1" before the STP or WIT instruction is executed.

When the STP state is cleared, timer X counts the oscillation frequency divided by 16. Therefore, timer X count stop bit (bit 2 of address $00FD_{16}$) must be set to "0" before the STP instruction is executed.

An example of ceramic oscillation (or quartz crystal oscillation) is shown in Figure 29. The value of the capacitance differs depending on the oscillator. Therefore, adjust the value as recommended by the each oscillator manufactures. An example where the clock signal is supplied from outside is shown in Figure 30. X_{IN} is the clock input, and X_{OUT} is open.

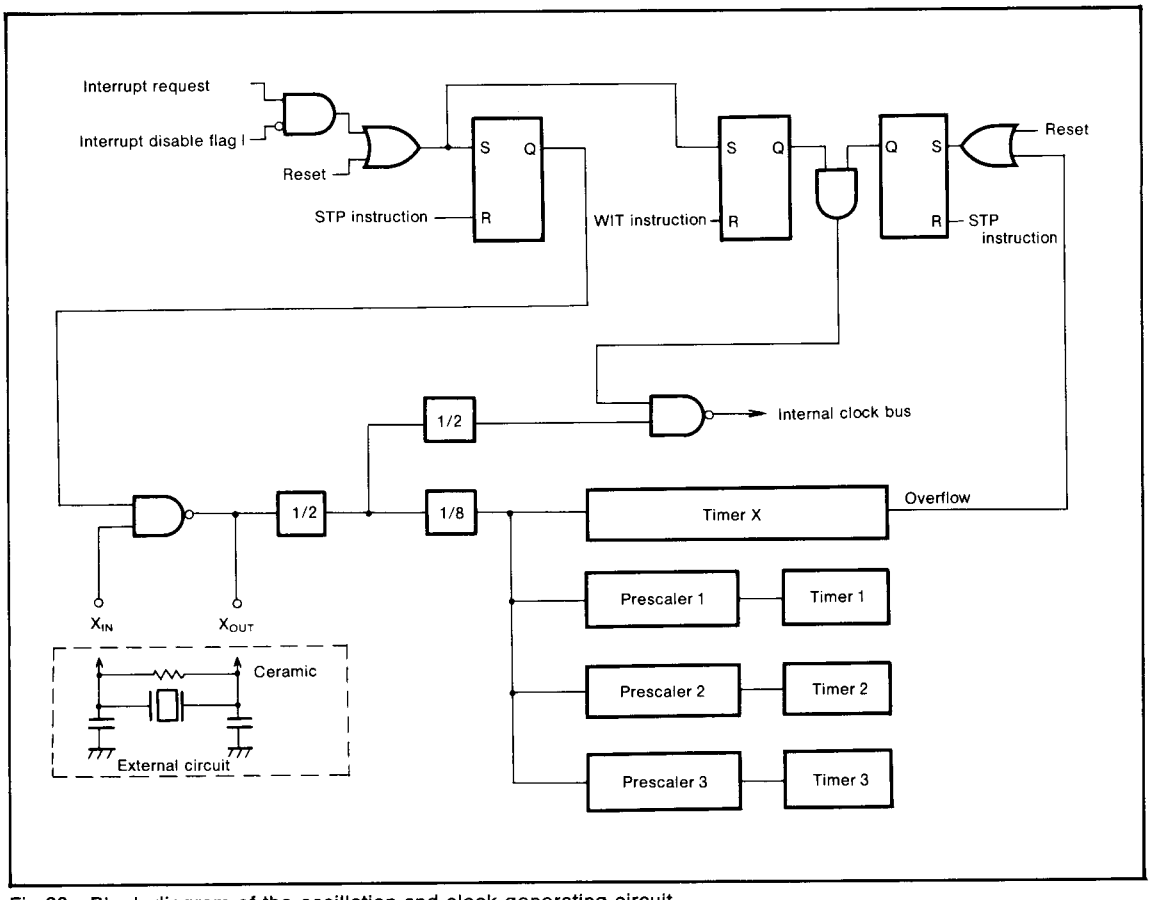


Fig.28 Block diagram of the oscillation and clock generating circuit

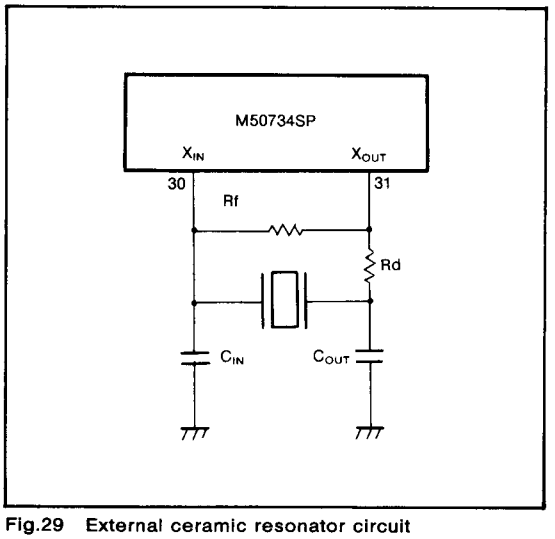


Fig.29 External ceramic resonator circuit

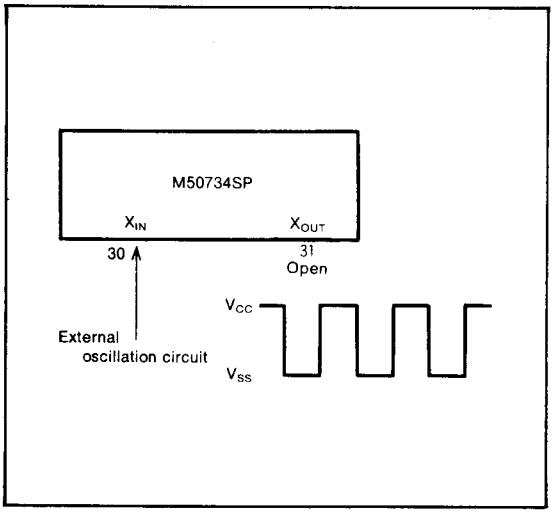


Fig.30 External clock input circuit

STANDBY MODE

The M50734SP can stop oscillation, preserving the contents of all registers, input/output ports and so on except timer X. Therefore, it can begin operation again in the same state as before it stopped; power dissipation is greatly reduced. The STP instruction is used to stop the oscillation. When the STP instruction is executed, it stops at the address fetch state of the next instruction. After RESET or an $\overline{INT_1}$, $\overline{INT_2}$ or CNTR interrupt is accepted, the oscillation starts again. Therefore, before the STP instruction is executed, one of the above interrupts must be enabled and the TXG (interrupt control register 3 (ICON 3), pin 2) must be cleared.

After the oscillation has been restarted by any means other than $\overline{RESET}$, the internal clock will start after timer X has counted 8208 cycles. When a ceramic oscillator is used, this time is needed to avoid instability at the oscillation rise. The block diagram of the standby mode is shown in Figure 31.

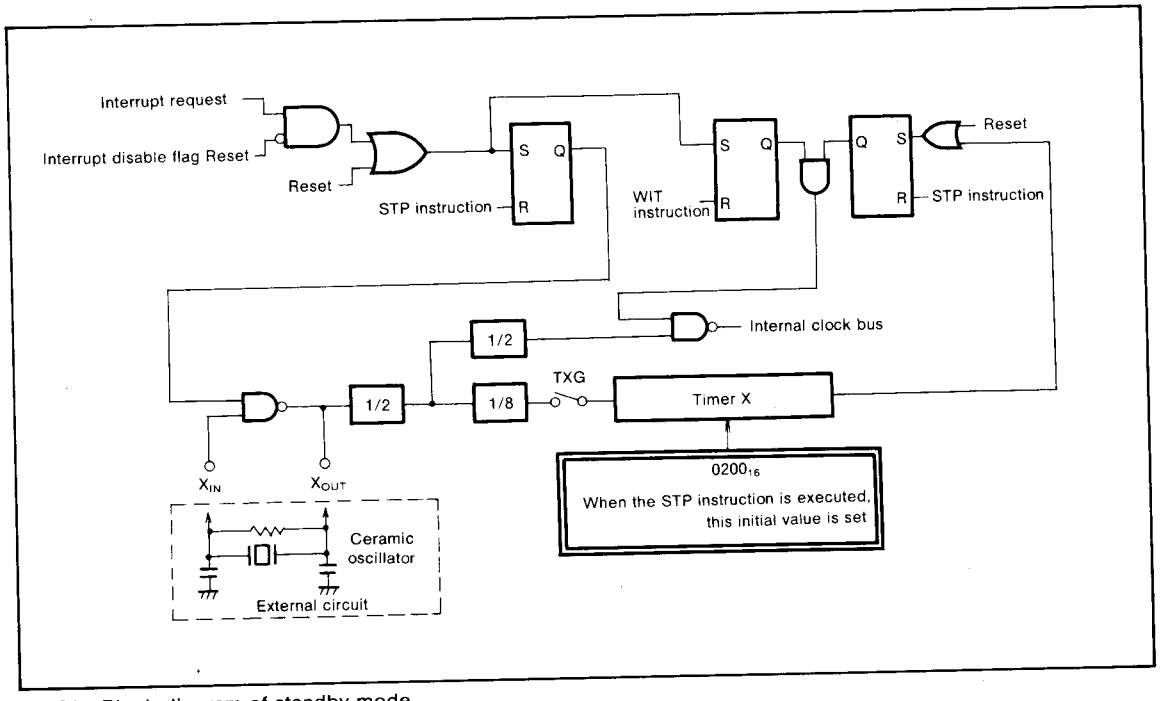


Fig.31 Block diagram of standby mode

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer X is used at event counter mode, the contents of the timer X must be read after the TXG flag is cut off. If the TXG flag is not cut off, the plural reading data of the contents of the timer X must be compared and used as real data of the timer X.
When the timer X at the other modes, other timers and prescalers are used, the contents of data can be read at optional time.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, SED, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Notes on the stepper motor control circuit
① The single-shot must not be used while the horizontal or vertical counter and the phase counter are linked with timers, because they can not rewrite data.
② When the stepper motor control register is set and reset, the bit set and bit reset instructions must be used.

(7) The area of addresses $00D0_{16} \sim 00D9_{16}$ can not be used, because those area are reserved for system expansion.

(8) When the port P0 function register is set and reset, CLB, SEB, and STA instructions must be used.

(9) When using the M50734SP/FP-10 at 10MHz clock frequency, the SFR ICON1 (address $00FF_{16}$) should be read using the LDA ICON1 instruction in zero page addressing mode.

M50734SP ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_{REF}	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Onput voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}, X_{OUT}		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

Note 1 : 300mW for QFP types.

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 8MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	2.0		V_{CC}+0.3	V
V_{IH}	"H" input voltage, R_XD, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}+0.3	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	−0.3		0.8	V
V_{IL}	"L" input voltage, R_XD, CNTR $\overline{INT_1}$, $\overline{INT_2}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	−0.3		0.16V_{CC}	V
V_{REF}	Standard voltage input	0.5V_{CC}		V_{CC}	V
V_{IA}	Analog input voltage, $P4_0$~$P4_3$	−0.3		V_{CC}+0.3	V
$I_{OL(perk)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			5	mA
$I_{OL(avg)}$	"L" average output current (Note1), $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_3~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC ALE, WD_{OUT}			2	mA
$I_{OH(peak)1}$	"H" peak output current, $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−5	mA
$I_{OH(peak)2}$	"H" peak output current, $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA
$I_{OH(avg)1}$	"H" average output current, (Note1) $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−2	mA
$I_{OH(avg)2}$	"H" average output current, (Note1) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA

Note 1 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.

2 : The total of $I_{OL(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of $I_{OL(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be 80mA max

The total of $I_{OH(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7 and A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be −60mA max

The total of $I_{OH(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be −80mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	I_{OH} = −200μA	2.4			V
		I_{OH} = −10μA	V_{CC}−0.7			
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	I_{OL} = 1.6mA			0.5	V
I_I	Input leak current, P_0~$P4_3$, $\overline{RESET}$	$V_{SS} \leq V_I \leq V_{CC}$	−5		5	μA
I_{OZ}	Three state leak current, all input/output pin	V_{SS} + 0.5V ≦ V_O ≦ V_{CC} − 0.5V	−5		5	μA
$V_{T+}-V_{T-}$	Hysteresis width, $\overline{INT_1}$, $\overline{INT_2}$, CNTR, R_XD, $\overline{RESET}$	When used as function except port		0.6		V
I_{OH}	"H" output current, $P2_0$~$P2_7$	V_{OH} = 1.5V	−1		−10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		6	15	mA
		Wait mode (Output transistors cut-off)		1	3	
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A/D supply current	During executing A/D convert			6	mA

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input set-up time	Fig.32	80			ns
$t_{SU(P0-\phi)}$	Port P0 input set-up time		250			ns
$t_{SU(P1-\phi)}$	Port P1 input set-up time		250			ns
$t_{SU(P2-\phi)}$	Port P2 input set-up time		250			ns
$t_{SU(P3-\phi)}$	Port P3 input set-up time		250			ns
$t_{SU(P4-\phi)}$	Port P4 input set-up time		250			ns
$t_{SU(P1-\overline{INT_1})}$	Port P1 latch input set-up time		250			ns
$t_{SU(S_{IN}-S_{CLK})}$	Serial input set-up time		250			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{h(\phi-P0)}$	Port P0 input hold time		50			ns
$t_{h(\phi-P1)}$	Port P1 input hold time		50			ns
$t_{h(\phi-P2)}$	Port P2 input hold time		50			ns
$t_{h(\phi-P3)}$	Port P3 input hold time		50			ns
$t_{h(\phi-P4)}$	Port P4 input hold time		50			ns
$t_{h(\overline{INT_1}-P1)}$	Port P1 latch input hold time		50			nS
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		50			ns
$t_{WL(\overline{INT_1})}$	$\overline{INT_1}$ input "L" pulse width		250			ns
$t_{WL(\overline{INT_2})}$	$\overline{INT_2}$ input "L" pulse width		1			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1			μs
$t_{WH(\overline{INT_1})}$	$\overline{INT_1}$ input "H" pulse width		1			μs
$t_{WH(\overline{INT_2})}$	$\overline{INT_2}$ input "H" pulse width		1			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1			μs
$t_{C(X_{IN})}$	External clock input cycle time		125			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width		45			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width		45			ns
$t_{W(\overline{RESET})}$	$\overline{RESET}$ input "L" pulse width		2			μs

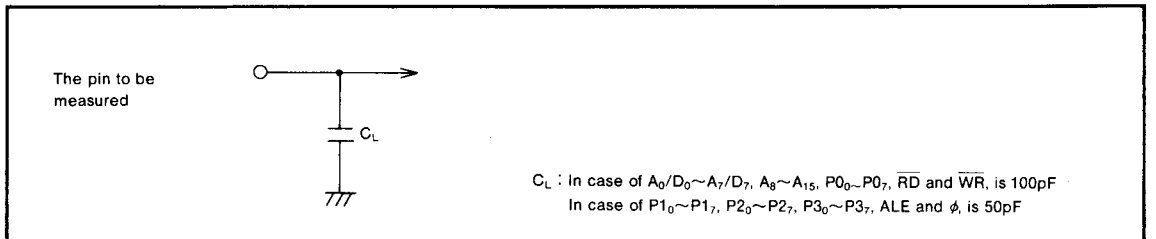


Fig.32 Measurement circuit diagram

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
※$t_{C(\phi)}$	Cycle time (Note 6)	Fig.32	500			ns
※$t_{WH(\phi)}$	ϕ clock pulse width (High level) (Note 2)		220			ns
※$t_{WL(\phi)}$	ϕ clock pulse width (Low level) (Note 2)		220			ns
$t_{r(\phi)}$	ϕ clock rising edge time				30	ns
$t_{f(\phi)}$	ϕ clock falling edge time				30	ns
※$t_{d(\phi-ALE)}$	Address strobe pulse delay time (Note 4)				60	ns
※$t_{W(ALE)}$	Address strobe pulse width (Note 3)		100			ns
$t_{d(A-ALE)}$	Address-ALE delay time		30			ns
$t_{v(ALE-A)}$	Address effective time after ALE		30			ns
$t_{d1(\phi-A)}$	Address delay time 1				130	ns
※$t_{d2(\phi-A)}$	Address delay time 2 (Note 1)				150	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
※$t_{W(RD)}$	$\overline{RD}$, $\overline{WR}$ pulse width (Note 2)		220			ns
$t_{d(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ delay time				20	ns
$t_{v(\phi-RD)}$	$\overline{RD}$, $\overline{WR}$ effective time after ϕ				10	ns
$t_{d(AZ-RD)}$	address floating-$\overline{RD}$ delay time		0			ns
$t_{d(\phi-D)}$	Data delay time (write cycle)				150	ns
※$t_{v(\phi-D)}$	Data effective time after ϕ (Note 5)		40			ns
$t_{d(\phi-P0)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P1)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2)}$	Port P2 data output delay time				250	ns
$t_{d(\phi-P3)}$	Port P3 data output delay time				250	ns
$t_{d(\phi-S_{CLK})}$	Serial clock delay time				60	ns
$t_{v(\phi-S_{CLK})}$	Serial clock effective time after ϕ				40	ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				150	ns
$t_{v(S_{CLK}-S_{OUT})}$	Serial output effective time after serial clock		0			ns
$t_{d(\overline{INT_1}-BSY)}$	Busy output delay time				250	ns

※ This timing is changed by $t_C(X_{IN})$, The timing of this list is the value in $t_C(X_{IN})$ = 125ns

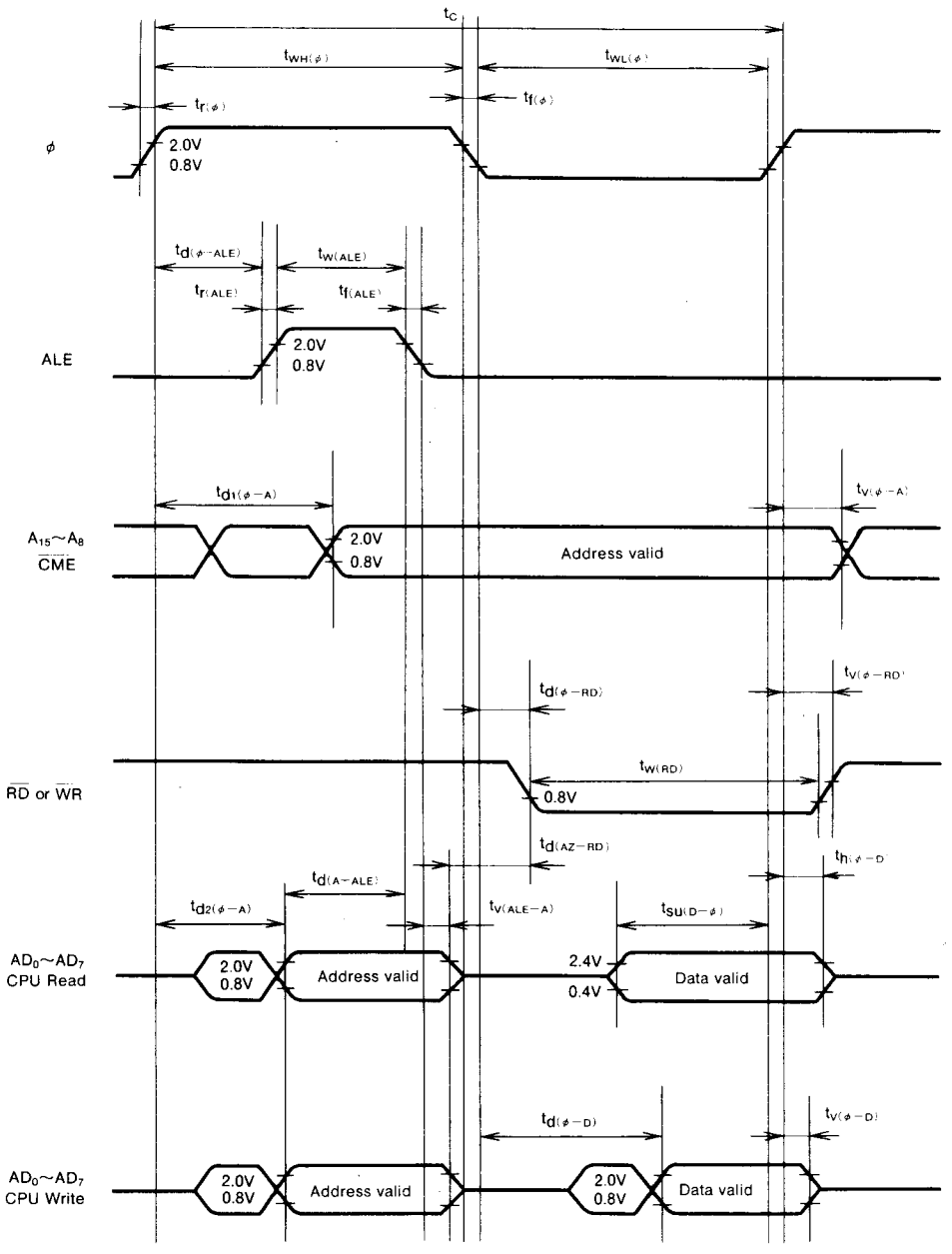
Note 1 : This value is defined as follows : $t_{dz}(\phi-A)=t_C(\phi)/8+8.75$
2 : This value is defined as follows : $t_W(RD)=t_C(\phi)/2-30$
3 : This value is defined as follows : $t_W(ALE)=t_C(\phi)/4-25$
4 : This value is defined as follows : $t_d(\phi-ALE)=t_C(\phi)/8-2.5$
5 : This value is defined as follows : $t_v(\phi-D)=t_C(\phi)/8-22.5$
6 : This value is defined as follows : $t_C(\phi)=4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz, unless otherwise noded)

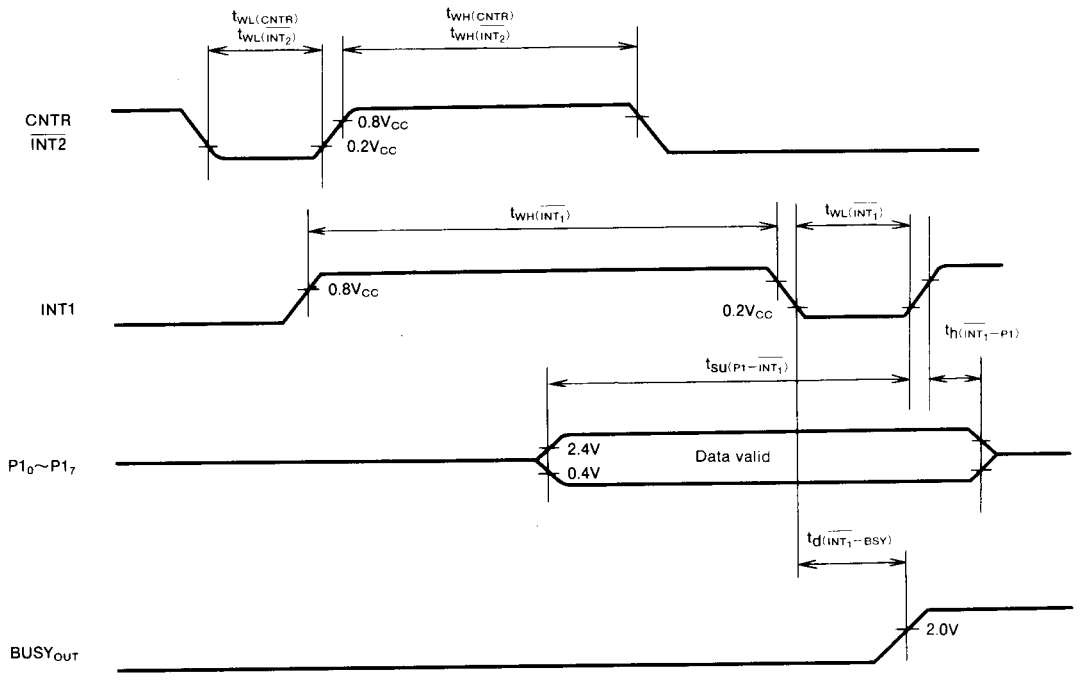
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	V_{CC}=V_{REF}=5.12V		±1 1/2	±3	LSB
R_{LADDER}	Ladder resistance value		1			KΩ
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0 \leqq V_I \leqq V_{REF}$			50	μA

M50734SP TIMING DIAGRAM

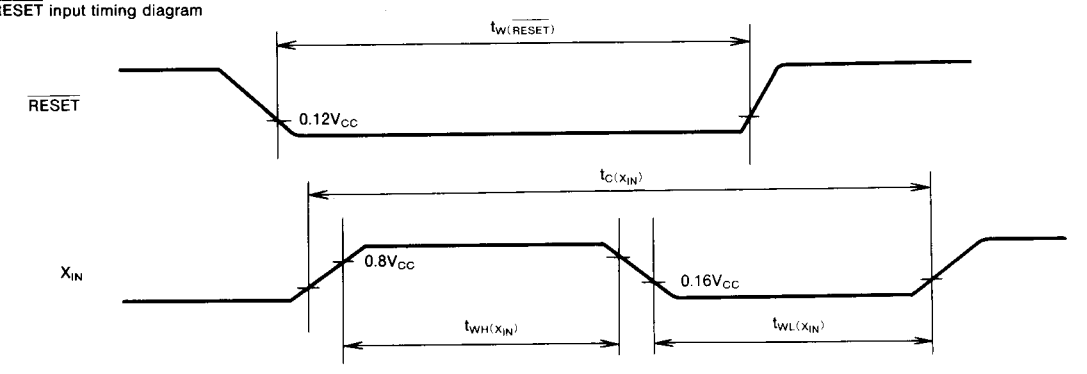
Bus timing diagram



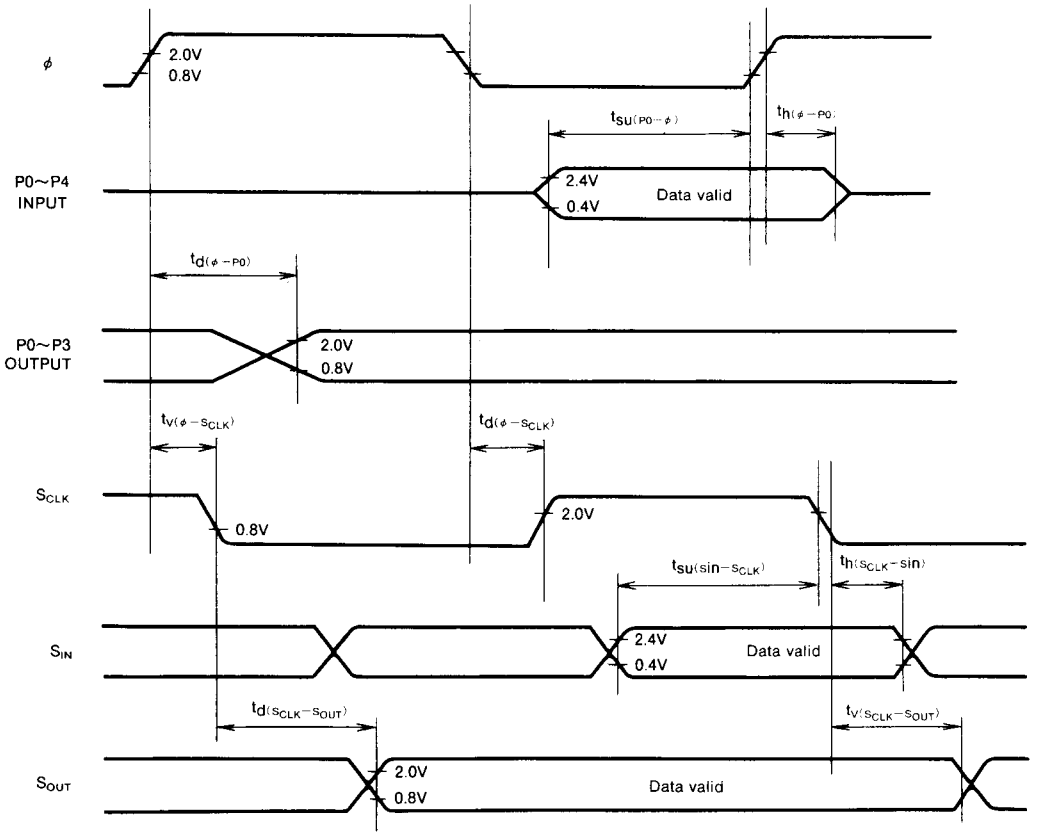
Port P1 latch input timing diagram



X_{IN}, $\overline{RESET}$ input timing diagram



Port P0~P4 input/output, serial I/O timing diagram



M50734SP-10 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}. Output transistors are at "off" state.	−0.3~7	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}		−0.3~7	V
V_{REF}	Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7, V_{REF}		−0.3~V_{CC}+0.3	V
V_O	Onput voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}, X_{OUT}		−0.3~V_{CC}+0.3	V
P_d	Power dissipation	T_a=25°C	1000	mW
T_{opr}	Operating temperature		−10~70	°C
T_{stg}	Storage temperature		−40~125	°C

RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70°C, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	2.0		V_{CC}+0.3	V
V_{IH}	"H" input voltage, R_XD, CNTR, $\overline{INT_1}$, $\overline{INT_2}$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}+0.3	V
V_{IL}	"L" input voltage, $P0_0$~$P0_7$ (During using as a port), $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, AD_0~AD_7	−0.3		0.8	V
V_{IL}	"L" input voltage, R_XD, CNTR $\overline{INT_1}$, $\overline{INT_2}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage, $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage, X_{IN}	−0.3		0.16V_{CC}	V
V_{REF}	Standard voltage input	0.5V_{CC}		V_{CC}	V
V_{IA}	Analog input voltage, $P4_0$~$P4_3$	−0.3		V_{CC}+0.3	V
$I_{OL(perk)}$	"L" peak output current, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			5	mA
$I_{OL(avg)}$	"L" average output current (Note1), $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, AD_0~AD_7, A_3~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			2	mA
$I_{OH(peak)1}$	"H" peak output current, $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−5	mA
$I_{OH(peak)2}$	"H" peak output current, $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA
$I_{OH(avg)1}$	"H" average output current, (Note1) $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE, WD_{OUT}			−2	mA
$I_{OH(avg)2}$	"H" average output current, (Note1) $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$			−10	mA

Note 1 : $I_{OL(avg)}$, $I_{OH(avg)}$ is the average current in 100ms.

2 : The total of $I_{OL(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7, A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be 80mA max

The total of $I_{OL(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be 80mA max

The total of $I_{OH(peak)}$, of $P0_0$~$P0_7$, AD_0~AD_7 and A_8~A_{15}, $\overline{RD}$, $\overline{WR}$, ϕ, SYNC, ALE and WD_{OUT} should be −60mA max

The total of $I_{OH(peak)}$, of $P1_0$~$P1_7$, $P2_0$~$P2_7$ and $P3_0$~$P3_7$ should be −80mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10~70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage all output pin except X_{OUT} pin	I_{OH} = −200μA	2.4			V
		I_{OH} = −10μA	V_{CC}−0.7			
V_{OL}	"H" output voltage all output pin except X_{OUT} pin	I_{OL} = 1.6mA			0.5	V
I_I	Input leak current, $P0_0$~$P4_3$, $\overline{RESET}$	$V_{SS} \leq V_I \leq V_{CC}$	−5		5	μA
I_{OZ}	Three state leak current, all input/output pin	V_{SS} + 0.5V ≤ V_O ≤ V_{CC} − 0.5V	−5		5	μA
$V_{T+}-V_{T-}$	Hysteresis width, $\overline{INT_1}$, $\overline{INT_2}$, CNTR, R_XD, $\overline{RESET}$	When used as function except port		0.6		V
I_{OH}	"H" output current, $P2_0$~$P2_7$	V_{OH} = 1.5V	−1		−10	mA
I_{CC}	Supply current	During operating (Output transistors cut-off)		7	18	mA
		Wait mode (Output transistors cut-off)		1	4	
		Stop mode (Output transistors cut-off)		1	20	μA
I_{ACC}	A-D supply current	During executing A-D conversion			6	mA

TIMING REQUIREMENTS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(D-\phi)}$	Data input set-up time	Fig.33	60			ns
$t_{SU(P0-\phi)}$	Port P0 input set-up time		250			ns
$t_{SU(P1-\phi)}$	Port P1 input set-up time		250			ns
$t_{SU(P2-\phi)}$	Port P2 input set-up time		250			ns
$t_{SU(P3-\phi)}$	Port P3 input set-up time		250			ns
$t_{SU(P4-\phi)}$	Port P4 input set-up time		250			ns
$t_{SU(P1-\overline{INT_1})}$	Port P1 latch input set-up time		250			ns
$t_{SU(S_{IN}-S_{CLK})}$	Serial input set-up time		250			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{h(\phi-P0)}$	Port P0 input hold time		50			ns
$t_{h(\phi-P1)}$	Port P1 input hold time		50			ns
$t_{h(\phi-P2)}$	Port P2 input hold time		50			ns
$t_{h(\phi-P3)}$	Port P3 input hold time		50			ns
$t_{h(\phi-P4)}$	Port P4 input hold time		50			ns
$t_{h(\overline{INT_1}-P1)}$	Port P1 latch input hold time		50			nS
$t_{h(S_{CLK}-S_{IN})}$	Serial input hold time		50			ns
$t_{WL(\overline{INT_1})}$	$\overline{INT_1}$ input "L" pulse width		250			ns
$t_{WL(\overline{INT_2})}$	$\overline{INT_2}$ input "L" pulse width		1			μs
$t_{WL(CNTR)}$	CNTR input "L" pulse width		1			μs
$t_{WH(\overline{INT_1})}$	$\overline{INT_1}$ input "H" pulse width		1			μs
$t_{WH(\overline{INT_2})}$	$\overline{INT_2}$ input "H" pulse width		1			μs
$t_{WH(CNTR)}$	CNTR input "H" pulse width		1			μs
$t_{C(X_{IN})}$	External clock input cycle time		100			ns
$t_{WL(X_{IN})}$	External clock input "L" pulse width		35			ns
$t_{WH(X_{IN})}$	External clock input "H" pulse width		35			ns
$t_{W(\overline{RESET})}$	$\overline{RESET}$ input "L" pulse width		2			μs

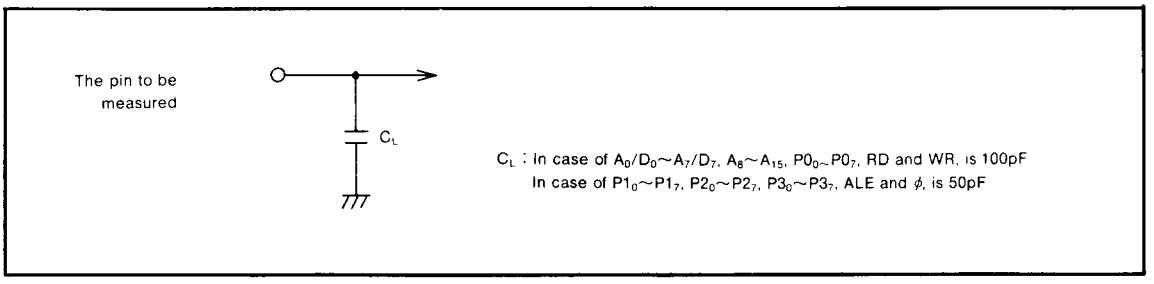


Fig.33 Measurement circuit diagram

SWITCHING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = −10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
※$t_{C(\phi)}$	Cycle time (Note 6)	Fig.33	400			ns
※$t_{WH(\phi)}$	ϕ clock pulse width (High level) (Note 2)		170			ns
※$t_{WL(\phi)}$	ϕ clock pulse width (Low level) (Note 2)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				30	ns
$t_{f(\phi)}$	ϕ clock falling edge time				30	ns
※$t_{d(\phi-ALE)}$	Address strobe pulse delay time (Note 4)				47.5	ns
※$t_{W(ALE)}$	Address strobe pulse width (Note 3)		75			ns
$t_{d(A-ALE)}$	Address-ALE delay time		10			ns
$t_{V(ALE-A)}$	Address effective time after ALE		30			ns
$t_{d1(\phi-A)}$	Address delay time 1				120	ns
※$t_{d2(\phi-A)}$	Address delay time 2 (Note 1)				140	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
※$t_{W(RD)}$	RD, WR pulse width (Note 2)		170			ns
$t_{d(\phi-RD)}$	RD, WR delay time				20	ns
$t_{V(\phi-RD)}$	RD, WR effective time after ϕ				10	ns
$t_{d(AZ-RD)}$	Address floating-RD delay time		0			ns
$t_{d(\phi-D)}$	Data delay time (write cycle)				150	ns
※$t_{V(\phi-D)}$	Data effective time after ϕ (Note 5)		27			ns
$t_{d(\phi-P0)}$	Port P0 data output delay time				250	ns
$t_{d(\phi-P1)}$	Port P1 data output delay time				250	ns
$t_{d(\phi-P2)}$	Port P2 data output delay time				250	ns
$t_{d(\phi-P3)}$	Port P3 data output delay time				250	ns
$t_{d(\phi-S_{CLK})}$	Serial clock delay time				60	ns
$t_{V(\phi-S_{CLK})}$	Serial clock effective time after ϕ				40	ns
$t_{d(S_{CLK}-S_{OUT})}$	Serial output delay time				150	ns
$t_{V(S_{CLK}-S_{OUT})}$	Serial output effective time after serial clock		0			ns
$t_{d(\overline{INT_1}-BSY)}$	Busy output delay time				250	ns

※ This timing is changed by $t_C(X_{IN})$. The timing of this list is the value in $t_C(X_{IN})$ = 100ns

Note 1 : This value is defined as follows : $t_{d2(\phi-A)}=t_C(\phi)/8+77.5$ ($t_C(\phi)\geqq 500ns$)
$t_{d2(\phi-A)}=140ns$ ($400ns\leqq t_C(\phi)\leqq 500ns$)

2 : This value is defined as follows : $t_W(RD)=t_C(\phi)/2-30$

3 : This value is defined as follows : $t_W(ALE)=t_C(\phi)/4-25$

4 : This value is defined as follows : $t_d(\phi-ALE)=t_C(\phi)/8-2.5$

5 : This value is defined as follows : $t_V(\phi-D)=t_C(\phi)/8-22.5$

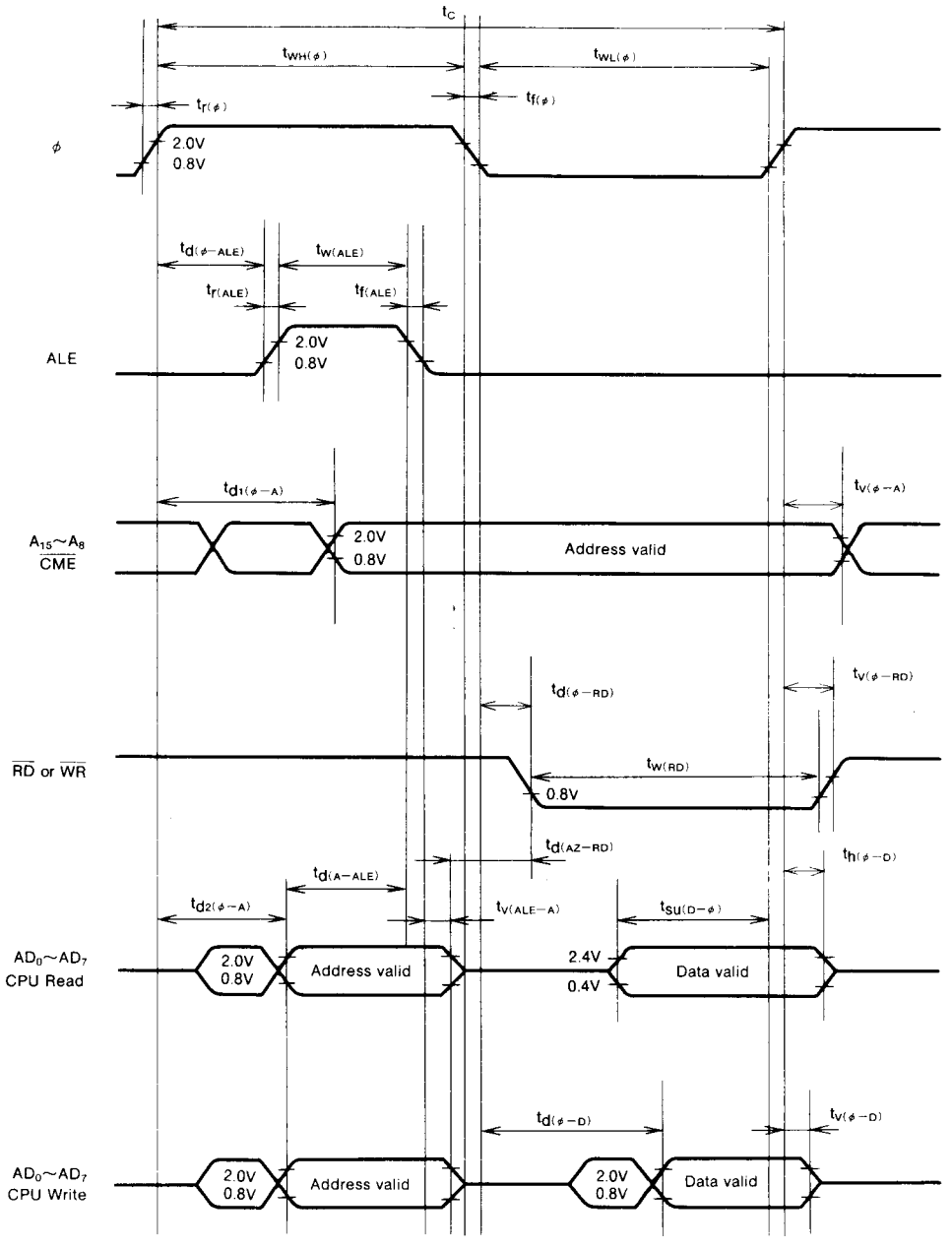
6 : This value is defined as follows : $t_C(\phi)=4t_C(X_{IN})$

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=10MHz, unless otherwise noded)

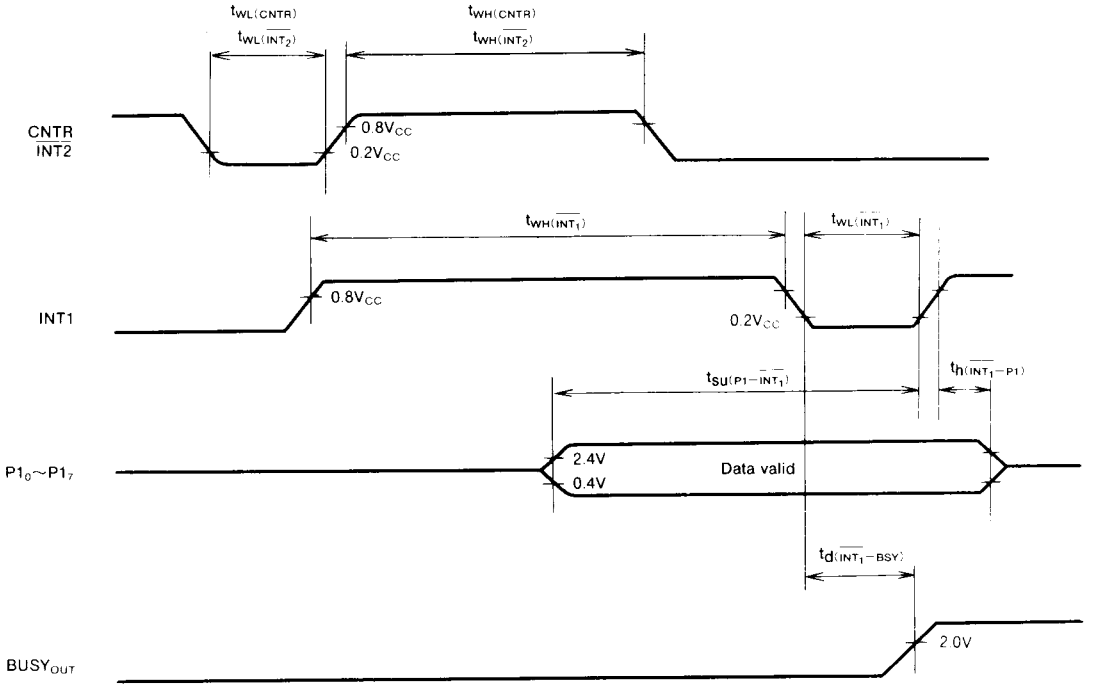
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution		8			Bits
—	Absolute accuracy	$V_{CC}=V_{REF}$=5.12V		±1 1/2	±3	LSB
R_{LADDER}	Ladder resistance value		1			KΩ
t_{CONV}	Conversion time				36	μs
$I_{I(AD)}$	Input current in A-D convert	$0\leqq V_I\leqq V_{REF}$			50	μA

M50734SP-10 TIMING DIAGRAM

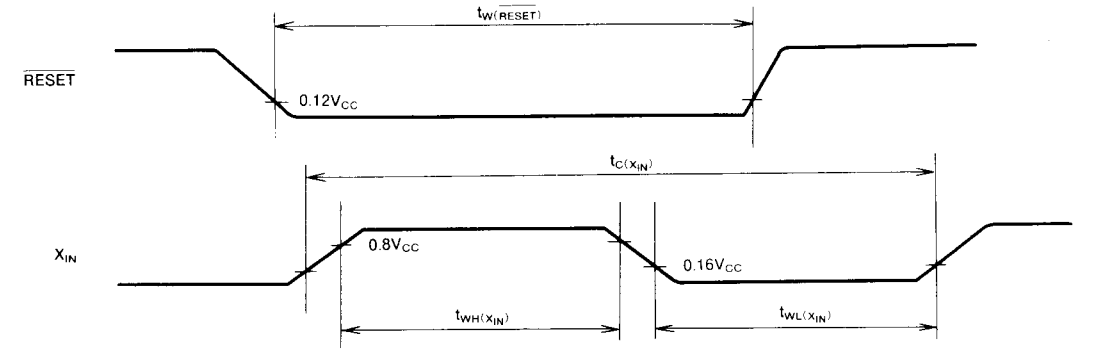
Bus timing diagram



Port P1 latch input timing diagram



X_{IN}, $\overline{RESET}$ input timing diagram



Port P0~P4 input/output, serial I/O timing diagram