M50752-PGYS

PIGGYBACK for M50752-XXXSP, M50757-XXXSP

DESCRIPTION

The M50752-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50757-XXXSP/M50752-XXXSP. The M50752-PGYS, being housed in a piggyback-type 52-pin shrink DIP, is compatible with the M50752-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2732K or the M5L2764K EPROM may be used.

The M50752-PGYS simplifies the development of programs for the M50757-XXXSP/M50752-XXXSP and is excellent for making prototypes.

DISTINCTIVE FEATURES

- Differences with the M50752-XXXSP/M50757-XXXSP are:

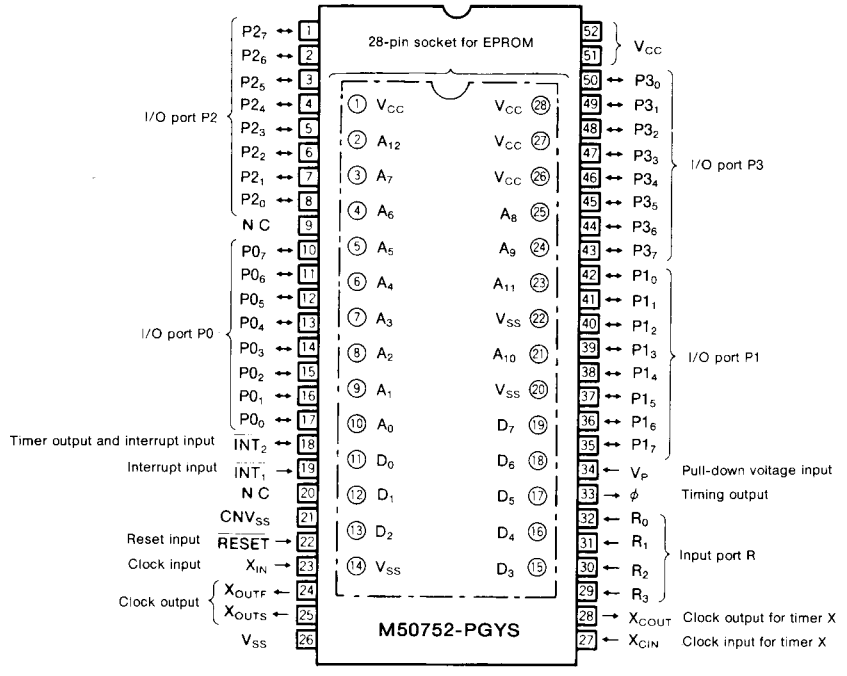
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2732K or the M5L2764K.

APPLICATION

Development of programs for VCR, tuners, and audio equipment.

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol " " indicates socket for EPROM.
NC: No connection.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P1, P3, $P2_6$ and $P2_7$.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, a resistor is connected between the X_{IN} and X_{OUTS} or the X_{OUTF} pins. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUTS} and X_{OUTF} pins should be left open.
X_{OUTS}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
X_{OUTF}	Clock output	Output	This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X_{IN} pin.
ϕ	Timing output	Output	This is the timing output pin.
X_{CIN}	Clock I/O for timer X	Input	These are I/O pins of the clock oscillating circuit for the timer X. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN}pin and X_{COUT} pin.
X_{COUT}		Output	
$\overline{INT_1}$	Interrupt input	Input	This is the lowest order interrupt input pin.
INT_2	Time output or interrupt input	I/O	This is in common with an output for the time X and an interrupt input pin.
R_0~R_3	Input port R	Input	Port R is a 4-bit input port.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port. The output structure is P-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. For $P2_6$ and $P2_7$ pins, output structure is P-channel open drain, and a pull-down transistor is built in between the V_P pin.
$P3_0$~$P3_7$	Output port P3	Output	Port P3 is an 8-bit output port and has basically the same functions as port P1.
A_0~A_{12}	Output port A	Output	Port A outputs the address of the EPROM loaded on the top side of the package.
D_0~D_7	Input port D	Input	Port D takes the input data from the EPROM loaded on the top side of the package.

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50752-PGYS and the M50757-XXXSP/M50752-XXXSP are explained below. As all other points are the same, only the differences are explained.

MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is 0100_{16} to $1FFF_{16}$, having 7936 bytes. Other than this, the M50752-PGYS has the same functions as the M50752-XXXSP has. Actually, ROM area depends on EPROM capacity.

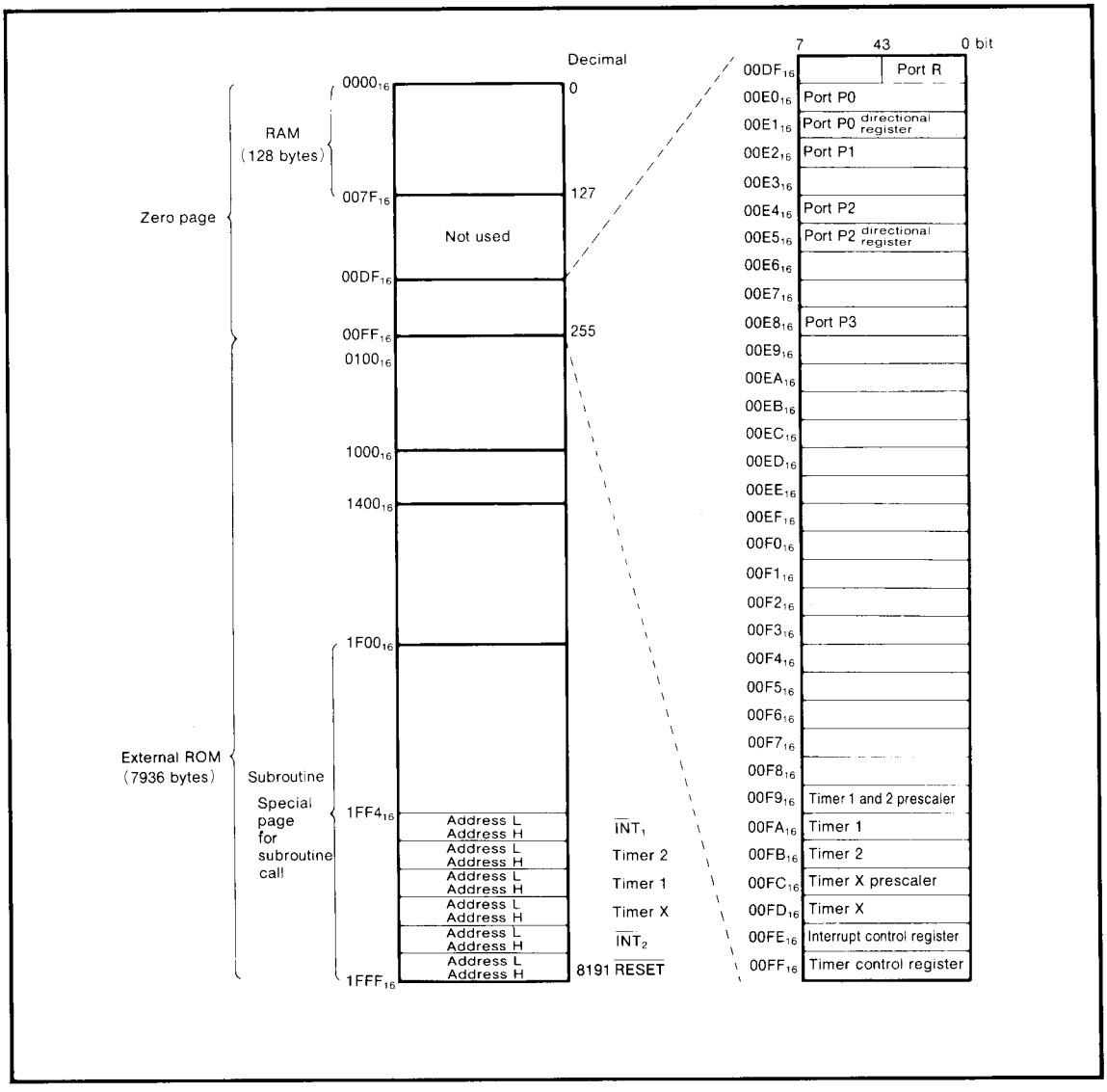


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50757-XXXSP/M50752-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50752-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50757-XXXSP/M50752-XXXSP.

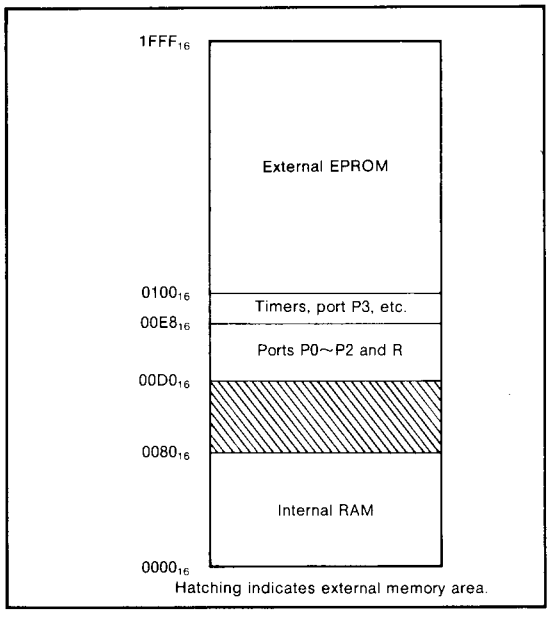


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) Because of the loading of the EPROM, the external dimensions differ from those of the M50757-XXXSP/M50752-XXXSP, being 19.0 × 50.8mm. Lower pin measurements are the same.

(2) When developing programs with the M50752-PGYS, carefully consider the ROM capacity of the M50757-XXXSP/M50752-XXXSP.
In the case of the M50757-XXXSP, use the ROM area from 1400_{16} to $1FFF_{16}$.
(In the case of the M5L2732K use the areas from 0400_{16} to $0FFF_{16}$.)
In the case of the M50752-XXXSP, use the ROM area from 1000_{16} to $1FFF_{16}$.
(In the case of the M5L2732K use the areas from 0000_{16} to $0FFF_{16}$.)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	Measured using V_{SS} as standaard. Output transistor is interrupted.	−0.3~7	V
V_P	Supply voltage		V_{CC}−35~V_{CC}+0.3	V
V_I	Input voltage R_0~R_3, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}, D_0~D_7		−0.3~7	V
V_I	Input voltage $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$~$P0_7$, $P2_0$~$P2_5$		−0.3~13	V
V_O	Output voltage X_{OUTF}, X_{OUTS}, X_{COUT}, ϕ, A_0~A_{12}		−0.3~V_{CC}+0.3	V
V_O	Output voltage $\overline{INT_2}$, $P0_0$~$P0_7$, $P2_0$~$P2_5$		−0.3~13	V
V_O	Output voltage $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$		V_{CC}−35~V_{CC}+0.3	V
P_d	Power consumption	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (T_a = −10~70℃ and V_{CC}=5V±5% unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Nom.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_P	Supply voltage	V_{CC}−33		V_{CC}	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" Input voltage R_0~R_3	0.4V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage CNV_{SS}, X_{IN}, X_{CIN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$~$P0_7$, $P2_0$~$P2_5$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage D_0~D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage R_0~R_3, X_{IN}, X_{CIN}	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage CNV_{SS}, $\overline{INT_1}$, $\overline{INT_2}$, $P0_0$~$P0_7$, $P2_0$~$P2_5$	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage D_0~D_7	0		0.15V_{CC}	V
$f_{(X_{IN})}$	Internal clock oscillating frequency			4	MHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, and $f_{(X_{IN})}$ = 4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	Output voltage $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$	V_{CC}=5V, T_a=25℃, I_{OH}=−12mA	3			V
V_{OH}	Output voltage, ϕ, A_0~A_{12}	V_{CC}=5V, T_a=25℃, I_{OH}=−2.5mA	3			V
V_{OL}	Output voltage $\overline{INT_2}$, $P0_0$~ $P0_7$, $P2_0$~$P2_5$	V_{CC}=5V, T_a=25℃, I_{OL}=10mA			2	V
V_{OL}	Output voltage ϕ, A_0~A_{12}	V_{CC}=5V, T_a=25℃, I_{OL} = 5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$, $\overline{INT_2}$	V_{CC}=5V, T_a=25℃	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis RESET	V_{CC}=5V, T_a=25℃		0.4	0.7	V
I_{IL}	Input leak current P0~P3, CNV_{SS}, $\overline{RESET}$, X_{IN}, X_{CIN}	V_{CC}=5V, T_a=25℃, 0≦V_I≦5V	−5		5	μA
I_{IL}	Input current $\overline{INT_1}$, $\overline{INT_2}$, D_0~D_7, $P0_0$~$P0_7$, $P2_0$~$P2_5$	V_{CC}=5V, T_a=25℃, 0≦V_I≦5V	−5		5	μA
I_{IL}	Input leak current $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P2_6$, $P2_7$	V_{CC}=5V, T_a=25℃, V_{CC}−33V≦V_I≦V_{CC}	−33		33	μA
I_{CC}	Supply current	V_{CC}=5V, T_a=25℃, $P2_6$ and $P2_7$ are V_{CC}, output pins are left open, Input and I/O pins except $P2_6$ and $P2_7$ are V_{SS}		3	6	mA