M50964-PGYS

PIGGYBACK for M50964-XXXSP,M50963-XXXSP

DESCRIPTION

The M50964-PGYS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputers the M50964-XXXSP/M50963-XXXSP. It is housed in a piggyback-type 64-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M50964-PGYS simplifies the development of programs for the M50964-XXXSP/M50963-XXXSP, and is excellent for making prototypes.

The differences between the M50964-XXXSP and the M50963-XXXSP are only ROM size.

Therefor the M50964-PGYS can be used for the development of programs for the M50964-XXXSP/M50963-XXXSP.

DISTINCTIVE FEATURES

- Differences with the M50964-XXXSP/M50963-XXXSP are:

(1) ROMless, EPROM is attached externally.

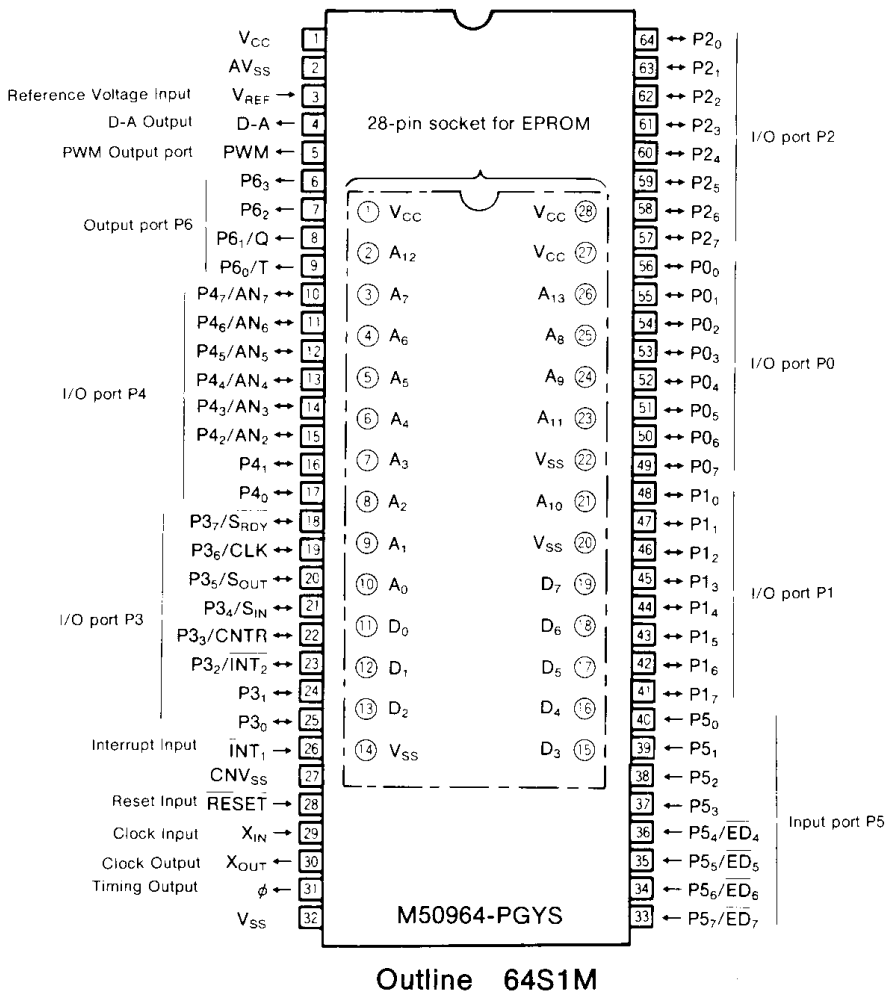
(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for the following systems;

- Office automation equipment
- VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol " " indicates sockets for EPROM.

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC} V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin.
AV_{SS}	Voltage input for A-D and D-A		This is GND input pin for the A-D and D-A converters.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters.
D-A	D-A output	Output	This is output pin from the D-A convereter.
PWM	PWM output	Output	This is output pin from the pulse width modulator. The output structure is N-channel open drain.
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is N-channel open drain.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_4$~$P4_7$ work as analog input port AN_4~AN_7.
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port. $P5_4$~$P5_7$ can be used as the edge sense inputs.
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is a 4-bit output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
A_0~A_{13}	Output port A	Output	These are for addresses to an EPROM mounted on the package.
D_0~D_7	Input port D	Input	These are for input data from an EPROM mounted on the package.

BASIC FUNCTION BLOCK

The differences between the M50964-PGYS and the M50964-XXXSP/M50963-XXXSP are noted below. The following explanations apply to the M50964-PGYS.
Specification variations for other chips are noted accordingly.

MEMORY

The memory map is shown in Figure 1. The M50964-PGYS is mounted an EPROM instead of an internal ROM.
The address of an EPROM is $C000_{16} \sim FFFF_{16}$, and this memory size is 16384 bytes. Other than these, the M50964-PGYS has the same functions as the M50964-XXXSP/M50963-XXXSP have.

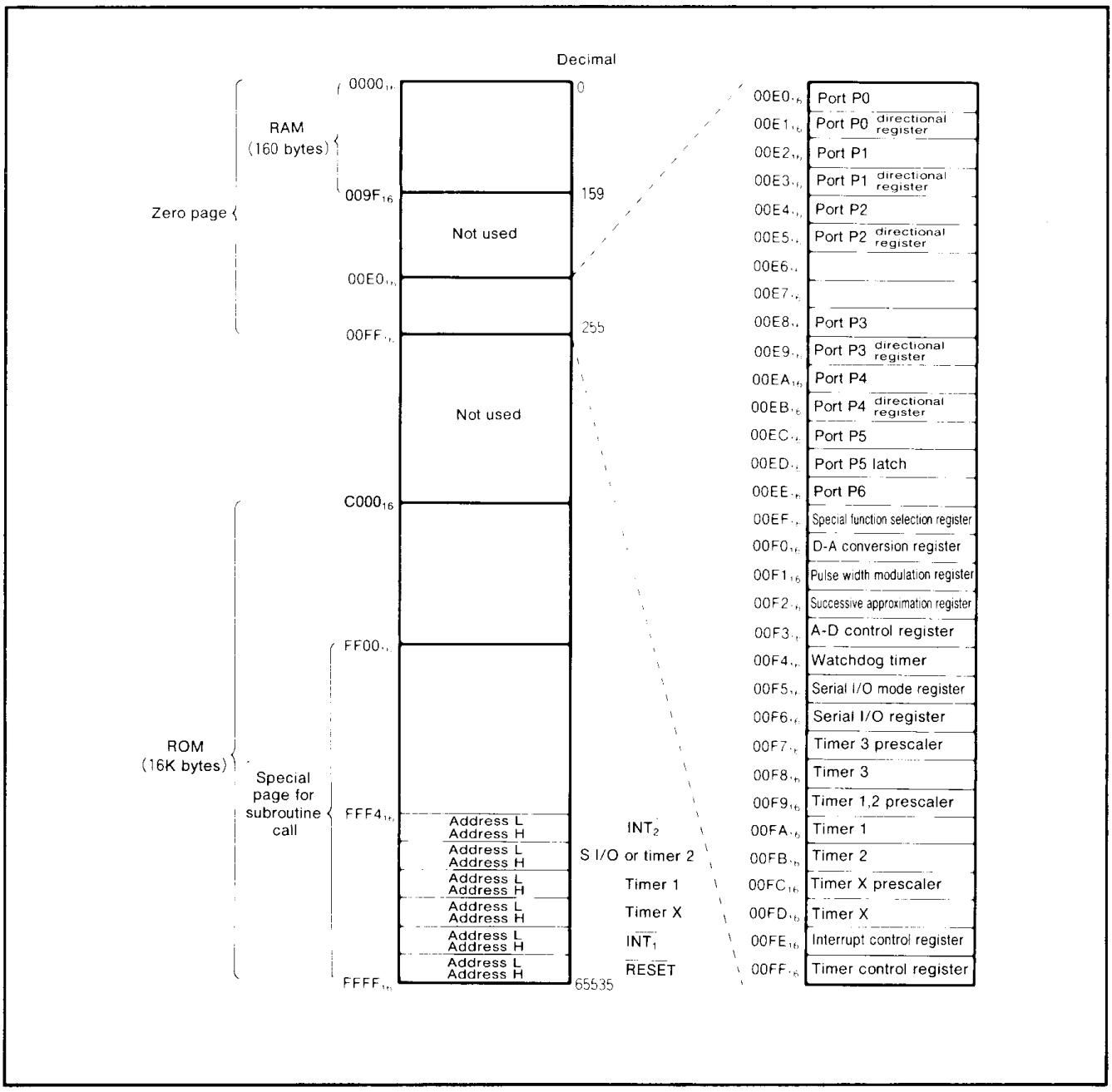


Fig.1 Memory map

PROCESSOR MODE

External memory area differs from the M50964-XXXSP/M50963-XXXSP in the memory expanding mode.
External memory map in the memory expanding mode is shown in Figure 2.

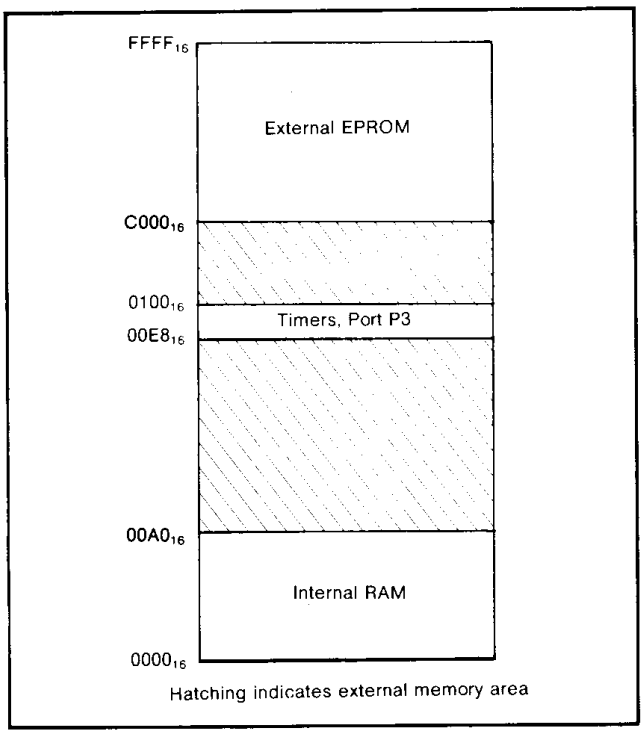


Fig.2 Memory map in memory expanding mode

PRECAUTION FOR USE

(1) In case of the M5L2764K or the M5L27128K EPROM use the following areas (refer to Figure 1):
- For the M50964-XXXSP, usable ROM area are $E800_{16}$~$FFFF_{16}$.

M5L2764K ..... addresses 0800_{16}~$1FFF_{16}$
M5L27128K ..... addresses 2800_{16}~$3FFF_{16}$
- For the M50963-XXXSP, usable ROM area are $D800_{16}$~$FFFF_{16}$.

M5L27128K ..... addresses 1800_{16}~$3FFF_{16}$

(2) The M50964-PGYS has no options as the M50964-XXXSP/M50963-XXXSP. But, the M50964-PGYS can use the STP instruction.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_2$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$, $P4_1$, $P5_0$∼$P5_7$, $\overline{INT_1}$	With respect to V_{SS} Output transistors cut-off	−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_2$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$, $P4_1$, $P6_0$∼$P6_3$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	1000(Note 1)	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Nom.	Limits Max.	Unit
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
V_{IL}	"L" output voltage $P0_0$∼$P0_7$	0		0.15V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$ (Note 2)		10		mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 2)		15		mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 2)		5		mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, (Note 1)		5		mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 1)		7		mA
$I_{OL(avg)}$	"L" average output current PWM (Note 1)		2.5		mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 2)		−10		mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 1)		−5		mA
$f_{(X_{IN})}$	Internal clock oscillating frequency		4		MHz

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
2 : Total of "L" output current I_{OL}, of ports P0, P1, P2, P3, P4, P6, and PWM is 80mA max.
Total of "H" output current I_{OH}, of port P2 is 50mA max.
3 : "H" input voltage of ports P0, P1, P3, $P4_0$∼$P4_3$, P5, and $\overline{INT_1}$ is available up to +12V.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25°C, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA	3			V
V_{OH}	"H" output voltage ϕ, A_0~A_{13}	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ, PWM, A_0~A_{13}	I_{OL}=5mA			2	V
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$		0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_6$	When used as CLK input	0.3	0.8		V
V_{T+}−V_{T-}	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
V_{T+}−V_{T-}	Hysteresis $P6_0$	When used as T input	0.5	1		V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, D_0~D_7	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=12V			12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$, D_0~D_7	V_I=5V			5	μA
V_{RAM}	RAM retention voltage	When clock stopped	2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition. — $f_{X_{IN}}$=4MHz Square wave		3	6	mA
		When clock stopped T_a=25°C			1	μA
		When clock stopped T_a=75°C			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25°C, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25°C, $f_{X_{IN}}$=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{su}	Set up time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V