M51271SP/FP

NTSC/PAL DECODER

DESCRIPTION

The M51271 is a semiconductor integrated circuit designed for 5V video system signal processing. It processes color signal and conduct color demodulation. With outputs of R-Y, B-Y color difference signals, it is applicable to both NTSC and PAL system.

M51271SP has R-Y axis demodulation carrier and ID pulse output in addition to M51271FP output. This carrier is applicable as a sub-carrier in M51272SP, when encoding color difference signal demodulated in M51271SP.

Regarding the package, M51271SP uses 30 pin plastic shrink DIP and M51271FP uses 28 pin plastic flat package.

FEATURES

- Low power dissipation (Supply voltage = 5V, circuit current = 50mA - standard)
- Utilizing 4fsc (17.73MHz, 14.32MHz) oscillation, carries out color demodulation by forming R-Y, B-Y sub-carrier at 1/4 dividing.
- Utilizing external constant, able to set the position and width of burst gate pulse discretionary.

APPLICATION

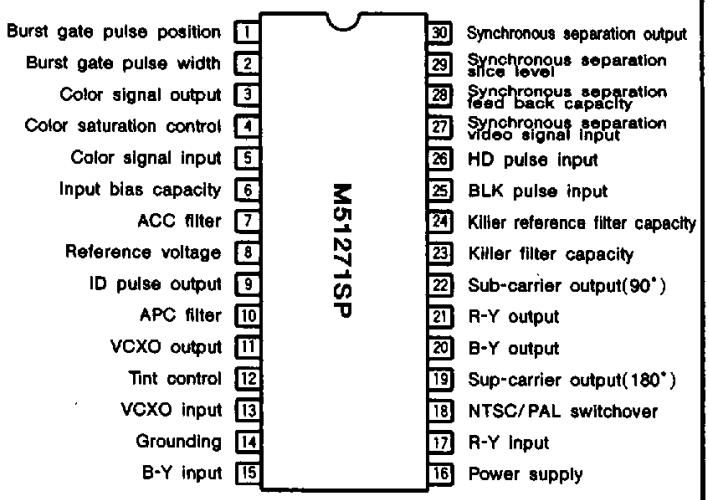
Color TV, VCR

RECOMMENDED OPERATING CONDITION

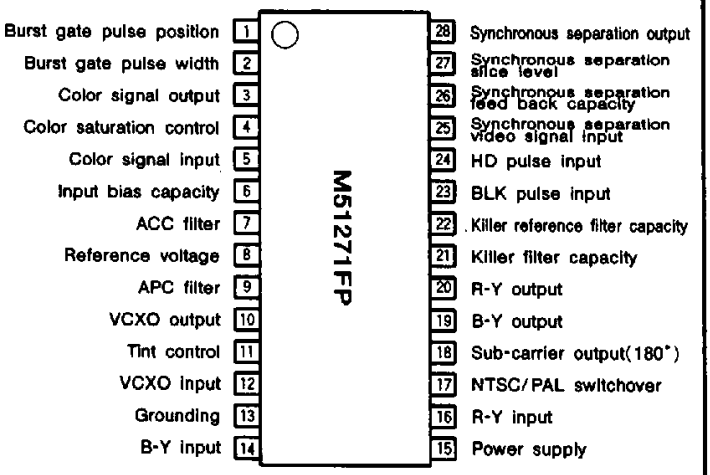
Supply voltage .....4.0 ~ 6.0V

Recommended supply voltage 5.0V

PIN CONFIGURATION (TOP VIEW)



Outline 30P4B

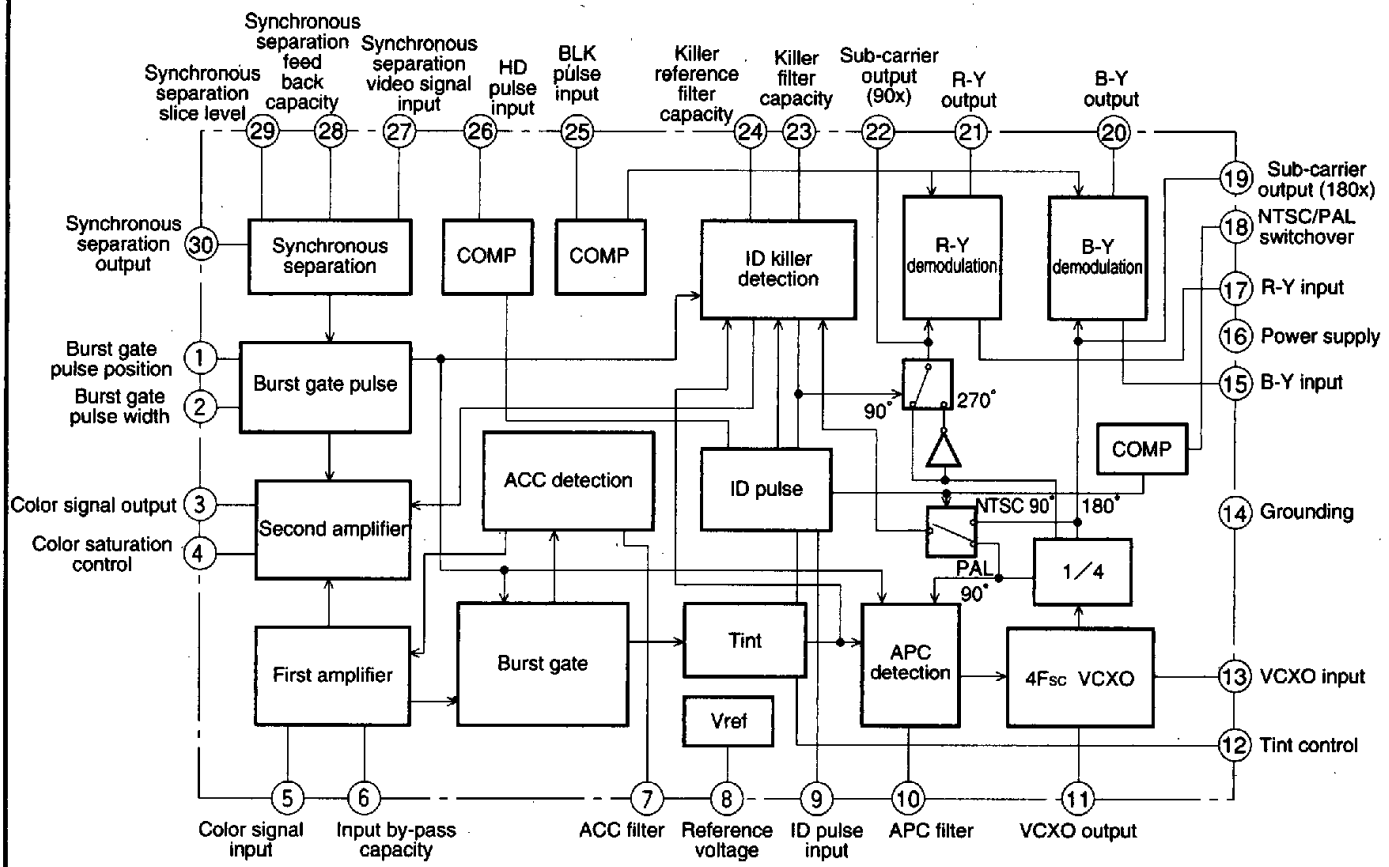


Outline 28P2W-A

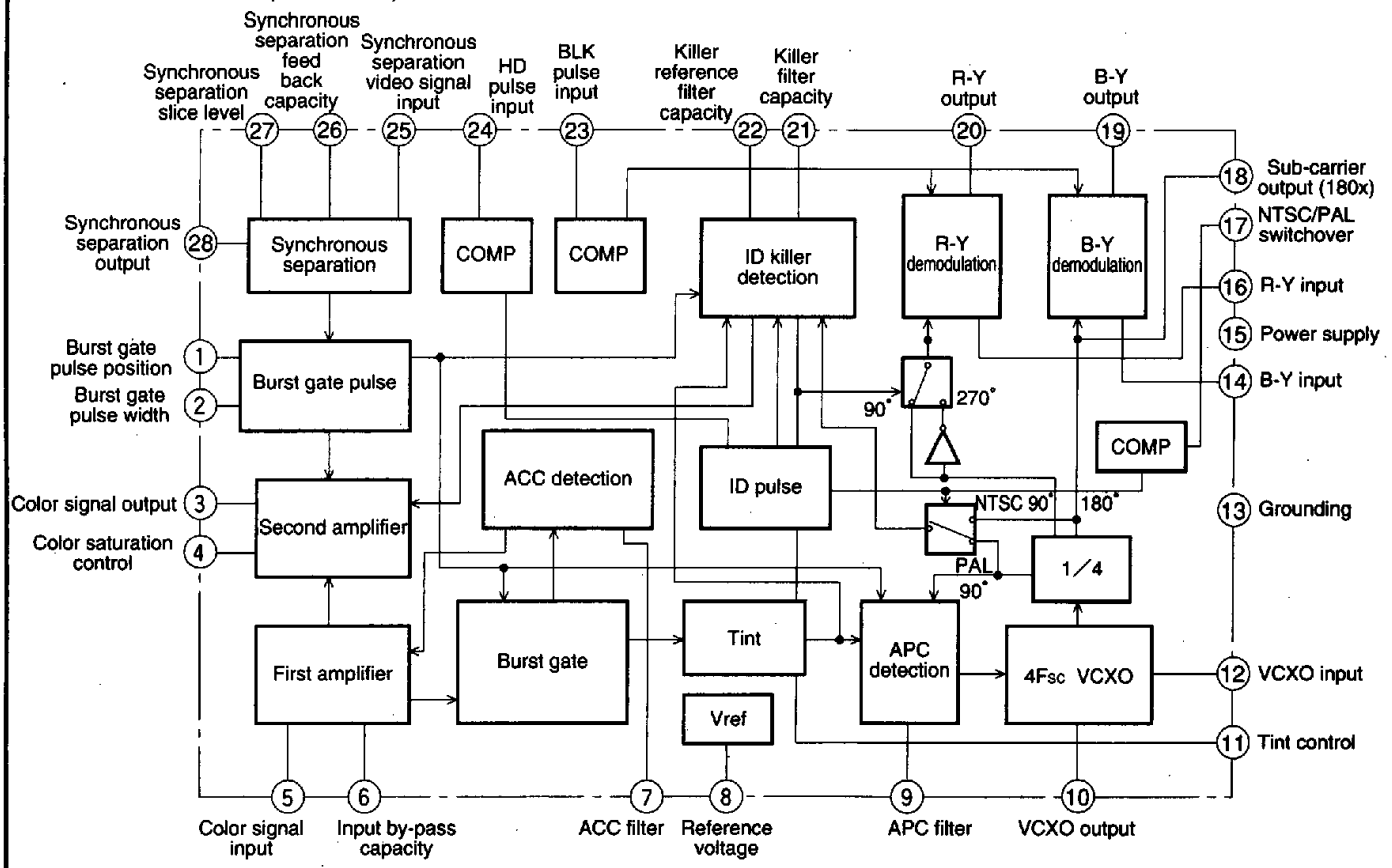
M51271SP/FP

NTSC/PAL DECODER

BLOCK DIAGRAM (M51271SP)



BLOCK DIAGRAM (M51271FP)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
Vcc	Supply voltage	6	V
Pd	Power consumption	1.25(0.5)	W
Topr	Operating temperature	−20~75	℃
Tstg	Storing ambient temperature	−40~125	℃
Kθ	Heat reduction rate	12.5(5)	mW/℃

Note : numeric values in ( ) are FP versions

ELECTRICAL CHARACTERISTICS (Ta=25℃, Vcc=5.0V, unless otherwise noted)

DC characteristics

Note : symbols in ( ) are FP versions

Symbol	Item Parameter	Test conditions	Test circuit	Limits			Unit
				Min.	Typ.	Max.	
Icc	Circuit current	DC bias alone	A	40	50	60	mA
V1 (V1)	Voltage at terminal 1 (1)	DC bias alone		2.6	2.9	3.2	V
V3 (V3)	Voltage at terminal 3 (3)	DC bias alone		1.9	2.2	2.5	V
V4 (V4)	Voltage at terminal 4 (4)	DC bias alone		2.3	2.5	2.7	V
V6 (V6)	Voltage at terminal 6 (6)	DC bias alone		2.8	3.0	3.2	V
V7 (V7)	Voltage at terminal 7 (7)	DC bias alone		4.4	4.7	5.0	V
V8 (V8)	Voltage at terminal 8 (8)	DC bias alone		2.8	3.0	3.2	V
V10 (V9)	Voltage at terminal 10 (9)	DC bias alone		2.6	2.9	3.2	V
V11 (V10)	Voltage at terminal 11 (10)	DC bias alone		2.4	2.7	3.0	V
V12 (V11)	Voltage at terminal 12 (11)	DC bias alone		2.3	2.5	2.7	V
V13 (V12)	Voltage at terminal 13 (12)	DC bias alone		3.1	3.4	3.7	V
V15 (V14)	Voltage at terminal 15 (14)	DC bias alone		2.6	2.9	3.2	V
V17 (V16)	Voltage at terminal 17 (16)	DC bias alone		2.6	2.9	3.2	V
V18 (V17)	Voltage at terminal 18 (17)	DC bias alone		0.6	0.8	1.0	V
V20 (V19)	Voltage at terminal 20 (19)	DC bias alone		1.9	2.1	2.3	V
V21 (V20)	Voltage at terminal 21 (20)	DC bias alone		1.9	2.1	2.3	V
V24 (V22)	Voltage at terminal 24 (22)	DC bias alone		2.5	2.8	3.1	V
V27 (V25)	Voltage at terminal 27 (25)	DC bias alone		2.6	2.9	3.2	V
V28 (V26)	Voltage at terminal 28 (26)	DC bias alone		2.2	2.5	2.8	V
V29 (V27)	Voltage at terminal 29 (27)	DC bias alone		2.2	2.5	2.8	V

INPUT TERMINAL CHARACTERISTICS

Pin No.	Input form	Internal bias voltage (standard)	Test conditions	Input resistance or current standard value			Unit
				Min.	Typ.	Max.	
② (2)	Open base (PNP)	Not specified	V_2=2.5V (V_2)	−2.0	−1.0	—	μA
④ (4)	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑤ (5)	Open base (NPN)	Not specified	V_5=3.0V (V5)	—	1.0	2.0	μA
⑥ (6)	Resistor	3.0V	—	9.0	12.0	15.0	kΩ
⑫ (11)	Resistor	2.5V	—	20.0	25.0	30.0	kΩ
⑬ (12)	Resistor	3.4V	—	4.0	5.0	6.0	kΩ
⑮ (14)	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
⑰ (16)	Resistor	2.9V	—	4.0	5.0	6.0	kΩ
㉓ (23)	Open base (NPN)	Not specified	V_{25}=5.0V (V23)	—	0.5	1.0	μA
㉔ (24)	Open base (NPN)	Not specified	V_{26}=5.0V (V24)	—	0.5	1.0	μA
㉕ (25)	Resistor	2.9V	—	16.0	20.0	24.0	kΩ

OUTPUT TERMINAL CHARACTERISTICS

Pin No.	Output form	Test conditions	Bias current			Unit
			Min.	Typ.	Max.	
③ (3)	Emitter follower (NPN)	Ammeter between ③ pin and Vcc (3)	0.6	0.8	1.0	mA
⑪ (10)	Emitter follower (NPN)	Ammeter between ⑪ pin and Vcc (10)	1.5	1.8	2.1	mA
⑲ (18)	Emitter follower (NPN)	Ammeter between ⑲ pin and Vcc (18)	230	280	330	μA
⑳ (19)	Emitter follower (NPN)	Ammeter between ⑳ pin and Vcc (19)	0.8	1.0	1.2	mA
㉑ (20)	Emitter follower (NPN)	Ammeter between ㉑ pin and Vcc (20)	0.8	1.0	1.2	mA
㉒ (—)	Emitter follower (NPN)	Ammeter between ㉒ pin and Vcc (—)	230	280	330	μA

AC CHARACTERISTICS

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min.	Typ.	Max.	
V_{CCR}	Operating supply voltage range		There should not be any abnormal operation in the standard application circuit		4.0	5.0	6.0	V
Acc I	ACC circuit	ACC characteristics I	SG1 : 200mV Reference value is determined by measuring output value when inputting 100mV signal from SG1.	B	0	1.0	3.0	dB
Acc II	ACC circuit	ACC characteristics II	SG1 : 10mV Reference value is determined by measuring output value when inputting 100mV signal from SG1.	B	−2.0	0	2.0	dB
G_{CA}	ACC circuit	Open-loop gain	SG1 5mV_{p-p} SW7 ON	B	21.0	24.0	27.0	dB
Vcmax	Color control	Chroma maximum output amplitude	④ pin 5V	B	160	200	240	mV_{P-P}
Vctyp	Color control	Chroma typical output amplitude	④ pin open	B	80	100	120	mV_{P-P}
Vcmin	Color control	Chroma maximum attenuation	④ pin GND	B	—	—	−35	dB
Sd_1	Synchronous separation	Synchronous output delay 1	SG2 APL 100% 500mV_{P-P}	B	—	—	500	ns
Sd_2	Synchronous separation	Synchronous output delay 2	SG2 APL 100% 500mV_{P-P}	B	—	—	500	ns
Sv	Synchronous separation	Synchronous output amplitude	SG2 APL 100% 500mV_{P-P}	B	4.0	4.2	4.4	V
Smin	Synchronous separation	Synchronous separation minimum input level	SG2 : APL 100% Signal attenuation	B	—	—	350	mV_{P-P}
NC	Synchronous separation	Synchronous separation noise cancel	SG3 input	B	—	—	1.2	V
BGP_P I	Burst gate pulse generator	Burst gate pulse position I	① pin 10kΩ, pull up=560kΩ ② pin 3.0V	B	2.0	2.5	3.0	μS
BGP_P II	Burst gate pulse generator	Burst gate pulse position II	① pin 39kΩ, pull up=2.2MΩ ② pin 3.0V	B	8.0	8.5	9.0	μS
BGP_W I	Burst gate pulse generator	Burst gate pulse width I	① pin 24kΩ, pull up=1.2MΩ ② pin 2.0V	B	3.5	4.0	4.5	μS
BGP_W II	Burst gate pulse generator	Burst gate pulse width II	① pin 24kΩ, pull up=1.2MΩ ② pin 4.0V	B	0.8	1.3	1.8	μS
Gdr-y	R-Y demodulator	Demodulation gain	SG5 100mV_{P-P} f(beat)=10kHz	C	10	12	14	dB
ΔEr-y	R-Y demodulator	Residual carrier wave	No input at ⑰ pin. (16)	C	—	—	30.0	mV_{P-P}
Vmr-y	R-Y demodulator	Demodulation maximum output	SG5 600mV_{P-P} f(beat)=10kHz	C	2.1	2.4	2.7	V_{P-P}
BWr-y	R-Y demodulator	Demodulation band width	Reference : f(beat) =10kHz Measuring point : f(beat) of−3dB	C	1.0	—	—	MHz
BLKΔvr	R-Y demodulator	Blanking DC offset	㉕(23) pin 0V, 5V ; ㉑(20) pin DC fluctuation	C	—	—	50.0	mV_{P-P}

AC CHARACTERISTICS (cont.)

Note : *) only SP version

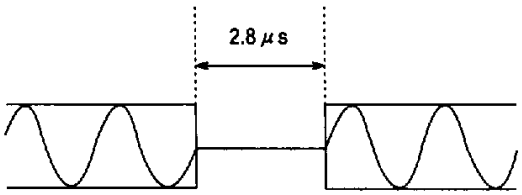
Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min.	Typ.	Max.	
Gdb-y	B-Y demodulator	Demodulation gain	SG5 100mVP-P f(beat)10kHz	C	10	12	14	dB
⊿Eb-y		Residual carrier wave	No input ⑮(14) pin.		—	—	30.0	mVP-P
Vmb-y		Demodulation maximum output	SG5 600mVP-P f(beat)10kHz		2.1	2.4	2.7	VP-P
BWb-y		Demodulation band width	Reference : f(beat) =10kHz f(beat) of −3dB		1.0	—	—	MHz
BLK⊿vb		Blanking DC offset	㉕(23)pin 0V, 5V ; ㉑(20)pin DC fluctuation		—	—	50.0	mV
R-Y / B-Y	Demodulator	R-Y, B-Y demodulation gain ratio	—		0.8	1.0	1.2	—
⊿V		R-Y, B-Y DC voltage offset	DC difference between output values at ⑳(19) pin and ㉑(20) pin.		—	—	50.0	mV
TCP	TINT PAL	Center	Measure value of V12 (V11) when output of ㉑(20) pin crosses 0.		2.30	2.35	2.40	V
TWP		Variable width	Measure amount of phase shift when voltage at ⑫(11) pin changes between 0V and 5V.		80	85	—	deg
TCN	NTSC	Center	—		2.40	2.45	2.50	V
TWN		Variable width	—		80	85	—	deg
Kthp		Killer operation input level	Burst voltage 100mVP-P is 0dB.		−33	−30	−27	dB
KthN		Killer operation input level	Burst voltage 100mVP-P is 0dB.		−36	−33	−30	dB
ID	ID operation		Observe R-Y output (21pin). ⑳		There shall be no abnormality in operation.			
IDP	ID pulse output	ID pulse*)	—		There shall be no abnormality in operation.			
IDv		ID vsat*)	SW18 : OFF Open collector Vsat DC 5mA		—	250	500	mV
BLKth	Blanking pulse input threshold		㉕(23) pin DC variable		3.3	3.5	3.7	V
HDth	HD pulse input threshold		㉖(24) pin DC variable		3.8	4.0	4.2	V
SCob	B-Y Sub-carrier output	Output level	⑲(18) pin output	D	500	550	600	mVP-P
SCdb		Duty	⑲(18) pin output		45	50	55	%
SCor	R-Y Sub-carrier output	Output level*)	㉒(21) pin output		500	550	600	mVP-P
SCdr		Duty*)	㉒(21) pin output		45	50	55	%
Or-y,b-y	Sub-carrier orthogonality*)		Phase difference between output carrier of ⑲ (18) pin and ㉒ (21) pin		85	90	95	deg
FCPP	PAL frequency-locking range		⑤ pin input frequency variable		1.0	—	—	kHz
FCPN	NTSC frequency-locking range		⑤ pin input frequency variable		1.0	—	—	kHz

ELECTRICAL CHARACTERISTICS TEST METHOD

Icc, V1~V29(V27)

Each value read by ammeter or voltmeter is the measured value at each measuring point.

ACCI and ACCII; Set SW 1,5 and 27 at 2; SW 4 at 3, and turn off SW 7. Input 3.579545MHz, 100mVp-p (0dB) from SG 1. Adjust VF 2 (3V approximately) so as to set burst gate pulse width in 2.8μs (burst, 10 cycle approximately) observing measuring point 3.



Output waveform at measuring point 3

In the following equations, V_A (mVp-p) represents output value at measuring point 3 under this condition. V_B (mVp-p) and VC (mVp-p) represent output values at measuring point 3 when output of SG1 is 6dB and —20dB respectively.

$$ACC\ I = 20 \log V_B / V_A\ (dB) \qquad ACC\ II = 20 \log V_C / V_A\ (dB)$$

G_{CA};Turn SW7 on. Set other SWs under the same conditions as specified in 1). Set output of SG1 at 3.579545MHz, 5mVp-p. In the following equation, V_D(mVp-p) represents output value at measuring point 3.

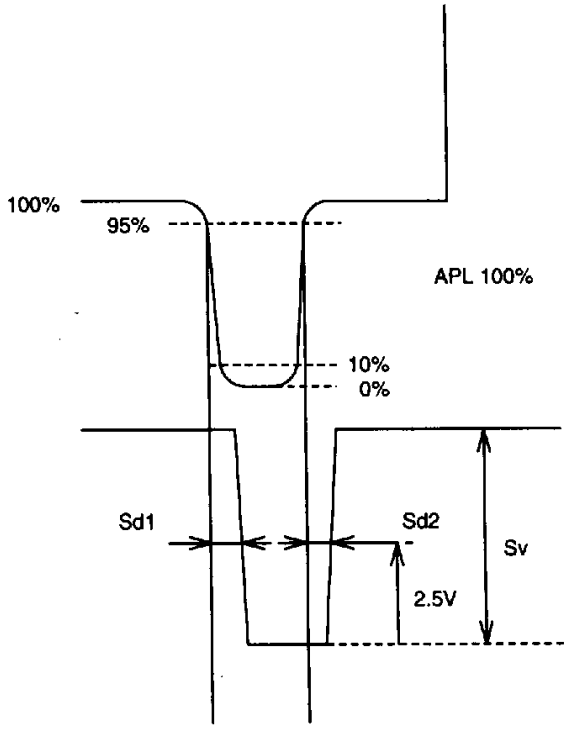
$$G_{CA} = 20 \log V_D / 5\ (dB)\ \text{(Burst gate pulse 2.8}\mu\text{ s)}$$

Vctyp and Vcmin; Set the SWs under the same conditions as specified in 1). Set output of SG1 at 3.579545MHz, 100mV_{P-P}. Vcmax, Vctyp and C (mV_{P-P}) represent output amplitude values at measuring point 3 when SW4 is set at 3, 2 or 1 respectively. Vcmin is obtained through the following equation.

$$Vcmin = 20 \log C / Vcmax\ (dB)\ \text{(Burst gate pulse 2.8}\mu\text{ s)}$$

Sd1, Sd2 and Sv; Set SW27 at 2. Other SWs can be set at any position.

Input an APL 100% standard signal from SG2 (500mVp-p). Determine Sd1, Sd2 and Sv as shown in the right-hand figure observing input signal and synchronizing pulse output from measuring point 30.

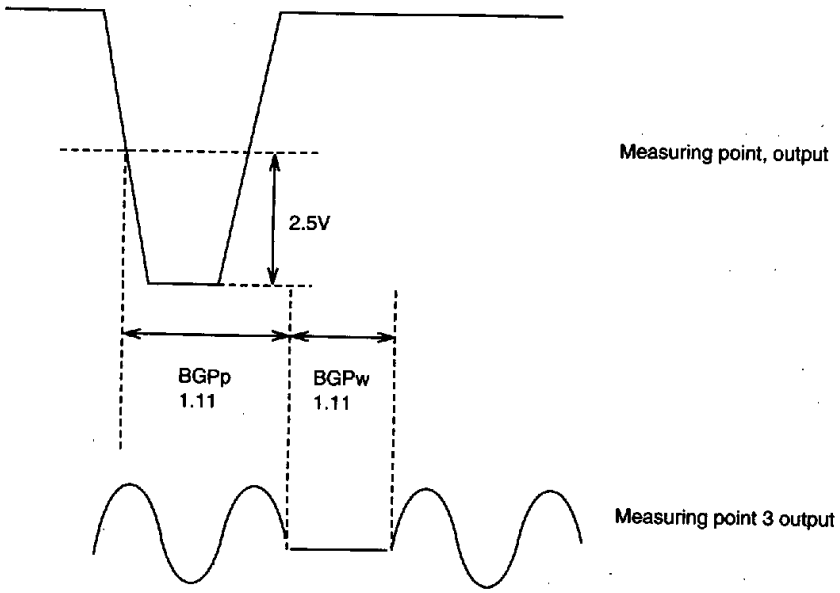


Smin; Under the same conditions as specified in 4), reduce output of SG2. Smin (mVp-p)represents output value of SG2 just before output values at measuring point 30 begin to be outside the standard value of Sd1, Sd2 and Sv.

NC; Set27 at 1. Set other SWs under the same conditions as specified in 4). Vary noise pulse level of SG3. NC (V) represents potential difference between input synchronizing. tip and noise pulse tip when noise pulse at measuring point 30 starts to expire.

BGPp I and BGPpII; Set SW4 at 3; SW5 and 27 at 2; turn off SW7. Input 3.579545MHz, 100mVp-p from SG1; input an APL100% standerd signal from SG2. Observe output at measuring point 3 and 30. Measure BGPpI and BGPpII setting SW1 at 1 then at 3. (V2 = 3V)

BGPwI and BGPwII; Set SW1 at 2; and other SWs under the same conditions as specified in 7).
Measure BGPwI and BGPwII at measuring point 3 setting V2 at 2.0V then at 4.0V.



Gdb-y and Gdr-y; Set SW5, 12, 13, 25 and 26 at 1; SW15 at 2, and turn off SW18. Input 3.579545MHz, 100mVp-p from SG1, an APL100% standard signal from SG2,and 3.589545MHz, 100mVp-p from SG3. In the following equation, DB (mVp-p) and DR (mVp-p) represent output (f(beat)=10kHz) at measuring points 20A, and 21A respectively.

Gdb - y = 20 log DB / 100 (db)
Gdr - y = 20 log DB / 100 (db)

Δ Eb - y and Δ Er - y; Set SW15 at 3, and other SWs and SG1, 2 under the same conditions as given in 1). Δ Eb-y (mVp-p) and Δ Er-y (mVp-p) represent carrier leakage output values (3.58MHz component) at measuring point 20B and 21B respectively.

Vmb-y and Vmr-y; Set each SW, and SG1 and 2 under the same conditions as given in 1). Measure output values (f(beat)=10kHz) at measuring points 20A and 21A setting output of SG3 at 600mVp-p. Values are represented by Vmb-y and Vmr-y (Vp-p) respectively.

BWb-y and BWr-y; Set each SW, and SG1 and 2 under the same conditions as given in 1). Vary output frequency of SG3 from 3.58 to 5MHz while setting voltage at 100mVp-p. BWb-y and BWr-y (MHz) represent output frequency at measuring points 20A and 21A when output value of measuring points 20A and 21A are -3dB (reference is DB or DR).

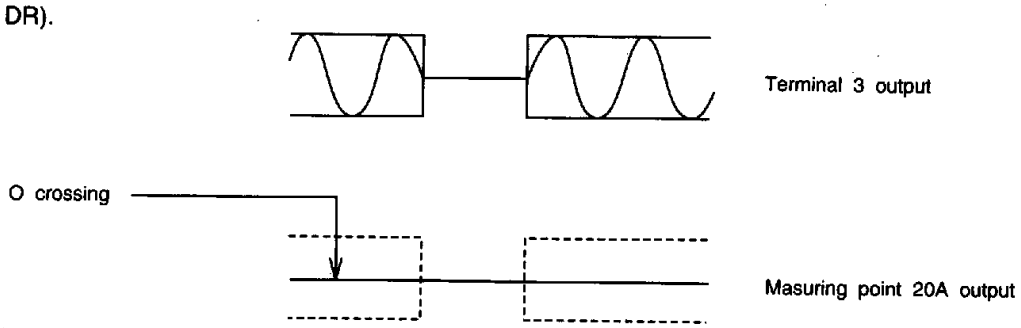
BLK Δ vd and BLK Δ vr; Set SW15 at 3, SW25 at 2,and 2,and other SWs and SG1 under the same conditions as given in 1). BLK Δ vb represents DC voltage fluctuation at measuring point 20B when VF25 is set at 5.0V or 0V. Similarly, measure BLK Δ vr at measuring point 21B.

650

$\frac{\text{R-Y}}{\text{B-Y}}$;From DB and DR obtained through measurement of Gdb-y and Gdr-y, the following equation (sobtained).
(R-Y) / (B-Y) = DR / DB

Δ V; Δ V represents the potential difference between measuring points 20A and 21A obtained through measurement of BLK Δ vb and BLK Δ vr when VF25 is at 5.0v.

T_{CP} and T_{CN}; Set SW5, 15, 25 and 26 at 1; SW12 and 13 at 2; and turn off SW18. Input 4.433618MHz, 100mV_{P-P} from SG1. Vary voltage of VF12. T_{CP} represents voltage of V12 (V) when output at measuring point 21A crosses 0.
Set SW13 at 1 and input 3.579545MHz, 100mV_{P-P} from SG1. Measure T_{CN} simiarly.



T_{WP} and T_{WN}; Set SW5, 15, 25 and 26 at 1; SW12 and 13 at 2, and turn off SW18. Input 4.433618MHz, 100mV_{P-P} from SG1. T_{WP} (deg) represents amount of phase shift output at measuring point 19 compared with measuring point 15 when VF12 is set at 5.0 or 0V.

Set SW13 at 1 and input 3.579545MHz, 100mV_{P-P} from SG1. Measure T_{WN} (deg) similarly.

Kthp and Kth_N; Set SW5, 13 and 26 at 2 ; sw12, 15 and 25 at 1, and turn SW18 on. Input PAL chroma standard signal from SG4. Start reducing output from SG4. In the following equation, Vkp (mV_{P-P}) represents the burst width of SG4 output when color difference signal output at measuring point 20A begins to be muted.

$$Kth_P = 20 \log Vk_D / 100 \text{ (dB)}$$

Set SW13 and 26 at 1 and turn off SW18. Input NTSC chroma standard signal from SG4. Determine Vk_N similarly, obtaining the following equation.

$$Kth_N = 20 \log Vk_N / 100 \text{ (dB)}$$

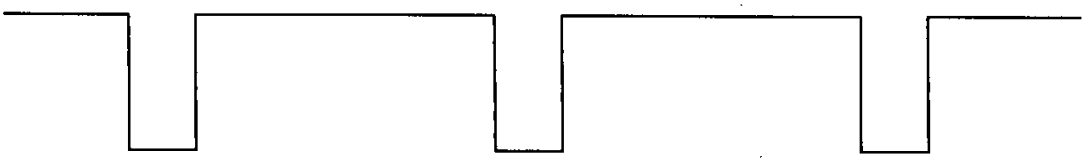
IDv; Under the same conditions as given in measurement of Kth_N, set SW9 at 2. IDvset (mV) represents DC voltage at measuring point 9 when 5mA is applied from IF9.

HDth; Set SW5 and 26 at 2; SW13 at 3, and turn SW17 on. Start reducing voltage at VF25 slowly from 5.0v. HDth (V) represents voltage of VF26 when DC voltage at measuring point 21 changes from High (4V approximately) to Low (0V approximately) or the other way round.

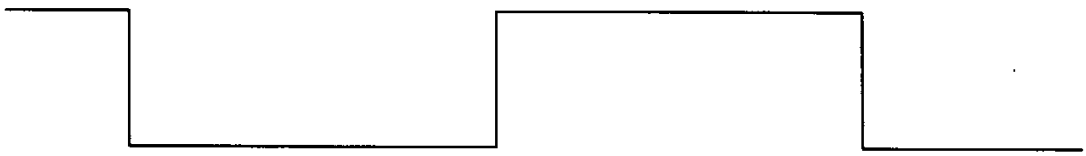
ID; Under the same conditions as given in measurement of Kth_P, input PAL chroma standard signal from SG4. Confirm color difference signal is not reversed by every 1H at measuring point 21A, R-Y output.

BLKth, Set SW25 at 2 and other SWs and SGs under the same conditions as given in the measurement of Kthp. Reduce voltage of VF25 slowly from 5.0v. BLKth represents the voltage of V25 (V) when color difference output at measuring point 20A and 21A begins to be muted.

IDP; Under the same conditions as given in measurement of Kthp, input PAL chroma standard signal from SG4. Set SW9 at 1. Observe pulse output from measuring point 9. Confirm that leading edge of HD pulse is reversed and has 1/2 dividing.



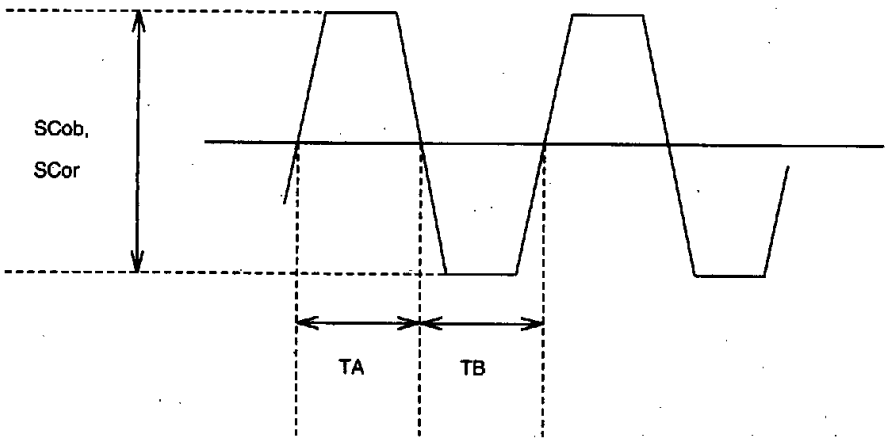
HD pulse



Measuring point 9,
ID pulse

SCob and SCor; Set SW5 and 26 at 1; SW13 at 2, and turn off SW17. Input 4.433618MHz, 100mVP-P from SG1. SCob (mVP-P) represents the output voltage at measuring point 19. SCor (mVP-P) represents output voltage at measuring point 22 under the same conditions.

SCdb and SCdr; Under the same conditions as given in 2), measure SCdb and SCdr at measuring point 19 and 22 respectively as follows.



$$SCdb, SCdr = \frac{TA}{TA+TB} \times 100\ (\%)$$

Or-y, b-y; Under the same conditions as given in 2), measure phase difference between output of measuring point 19 and that of 22. represented by Or-y · b-y .

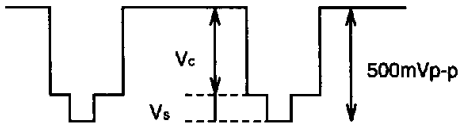
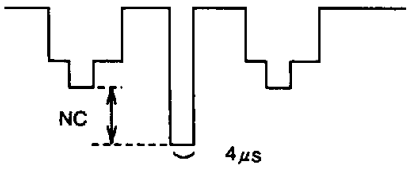
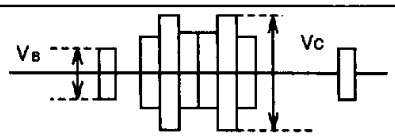
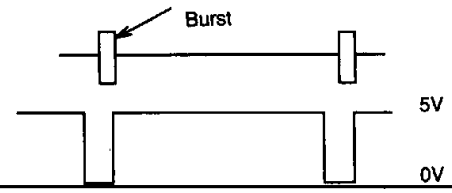
FCPP and FCPN; Under the same conditions as given in 2), approximate frequency output of SG1 starting from 4.435MHz (asynchronous) to center frequency (4.433618MHz) with output voltage 100mVP-P. Determine lock-in frequency f1. Also, approximate frequency starting from 4.432MHz (asynchronous state) to center frequency and determine lock-in frequency f2. Obtaining the following equation.

$$F_{CPP} = f1 - f2 \quad (Hz)$$

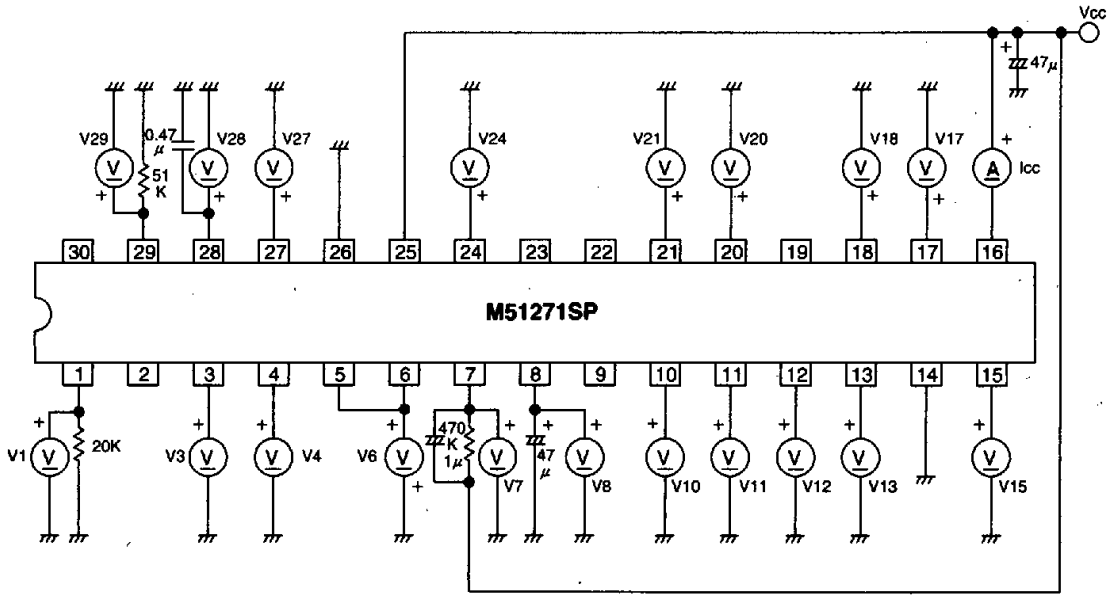
Set SW13 at 1. Approximate frequency of SG1 starting from 3.581MHz (asynchronous state) to center frequency (3.579545MHz). Determine lock-in frequency f3.
Also, approximate frequency starting from 3.578MHz (asynchronous state) to center frequency and determine lock-in frequency f4. Obtaining the following equation.

$$F_{CPN} = f3 - f4 \ (Hz)$$

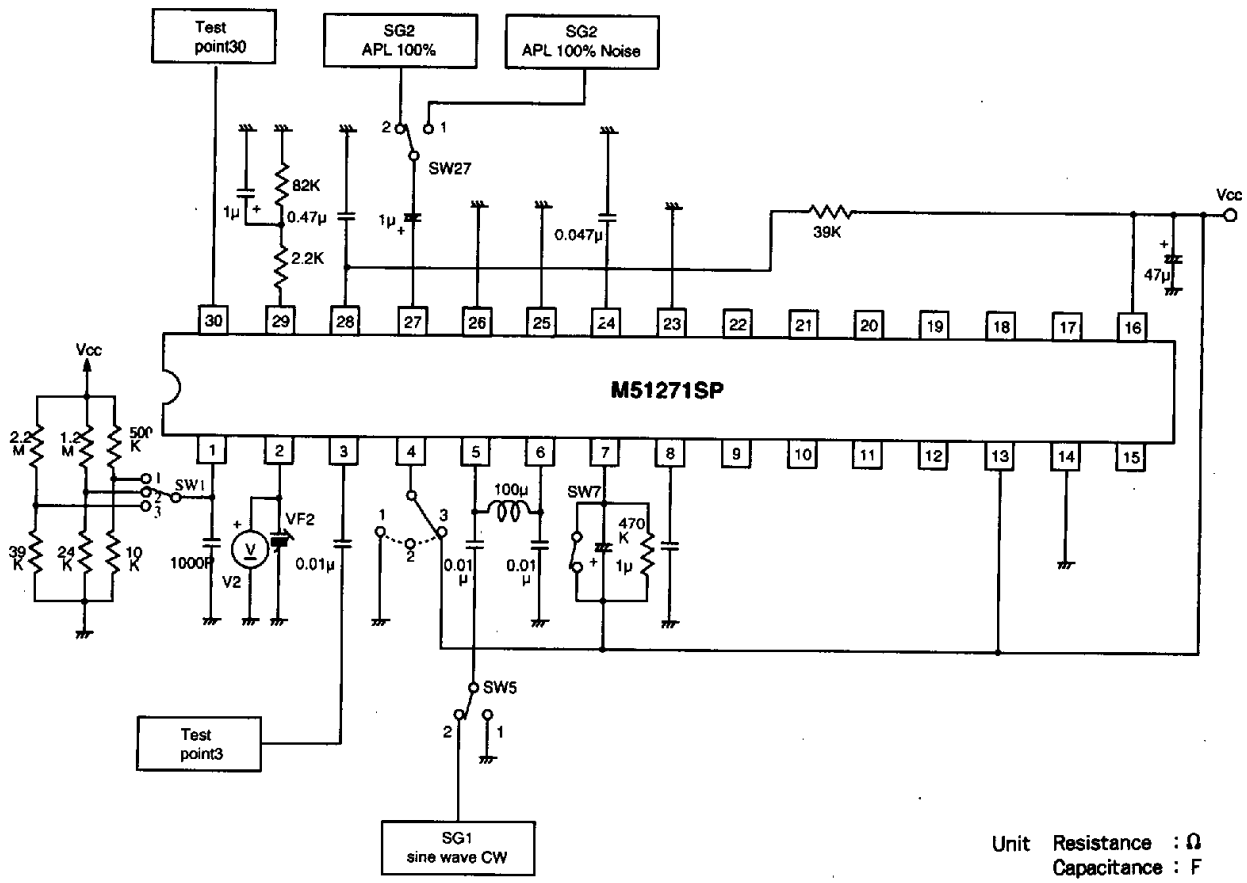
INPUT SIGNAL

SGNo.	Waveform	Standard	Remarks
SG1	 3.579545MHz 4.433619MHz	Sine wave CW, 100mVP-P (standard)	Frequency and output level SHOULD be variable.
SG2	 Vc Vs 500mVp-p	APL100 signal 500mVP-P (standard), Vc : Vs=10 : 4	Level SHOULD be variable.
SG3	 NC 4μs	Mix noise to SG2 standard signal (500mVP-P).	NC SHOULD be variable (noise level alone).
SG4	 VB Vc NTSC, PAL chroma standard signal	Vc : VB=2 : 1, VB=100mVP-P (standard)	Level SHOULD be variable.
SG5	 3~5MHz 0~1Vp-p	Sine wave CW	Frequency and output level SHOULD be variable.
HD pulse	 Burst 5V 0V	The pulse SHOULD have last transition preceding to burst in horizontal blanking interval.	The vertical blanking interval SHOULD also appear AT the same time.

TEST CIRCUIT A

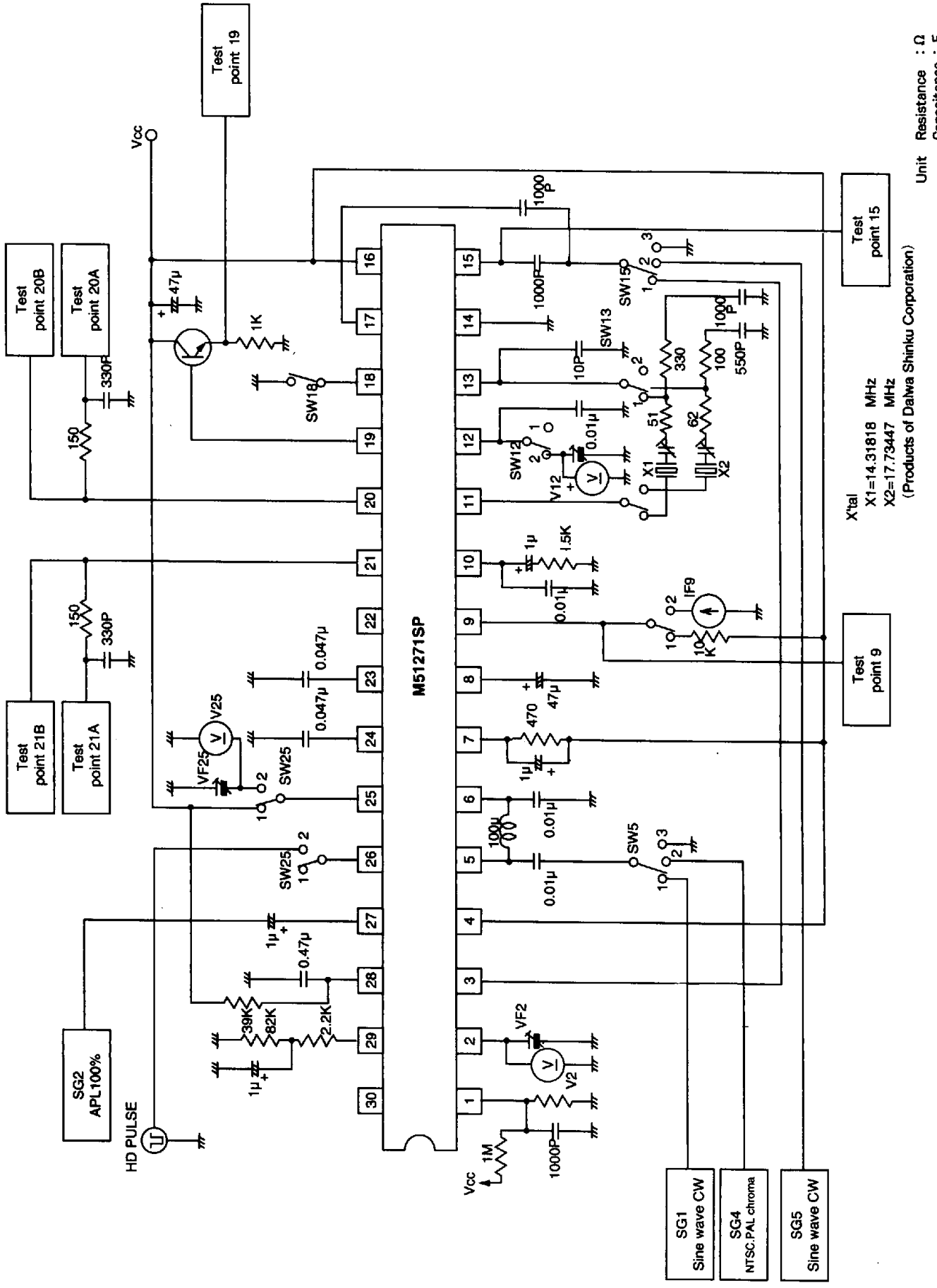


TEST CIRCUIT B



Unit Resistance : Ω
Capacitance : F

TEST CIRCUIT C



ADJUSTMENT OF BURST PULSE POSITION AND WIDTH

On inputing NTSC, PAL standard chroma signals, adjust resistance value at terminal 1 and voltage value at terminal 2 so as to locate burst gate pulse at burst position observing measuring point 3. (Chroma signal from which burst has been extracted is output at measuring point 3).

In other cases, set resistance value at terminal 1 at 24Ω

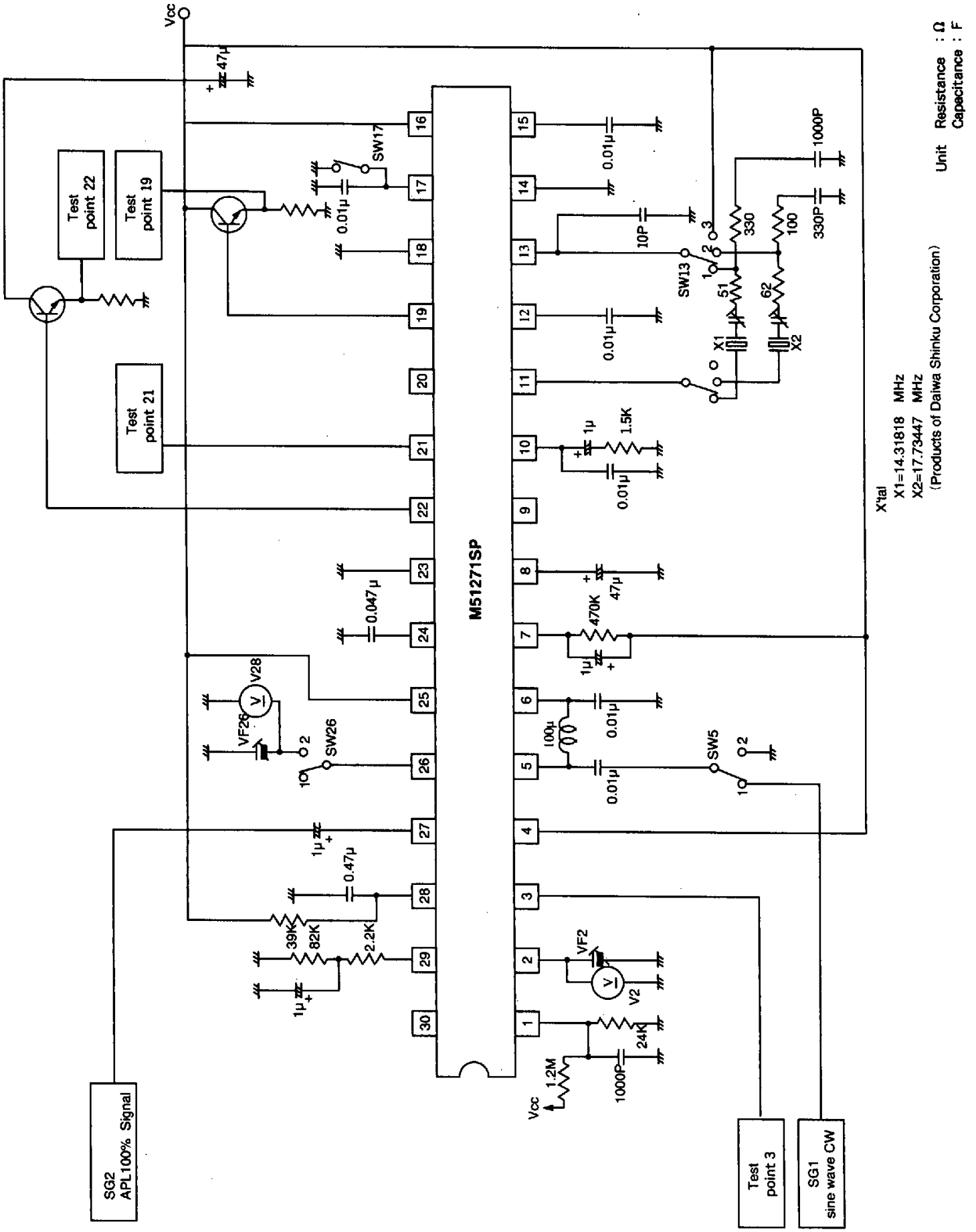
Vary burst gate width in 2.8μs when setting NTSC, and 2.3μs when setting PAL, adjusting voltage at terminal 2.

VCXO TO ADJUSTMENT

Set SW5 at 3, SW25 and 26 at 1, and turn SW18 on (in case of PAL). Apply an APL100% standard signal from SG2. Adjust VCXO external trimmer to set output frequency at measuring point 19 :

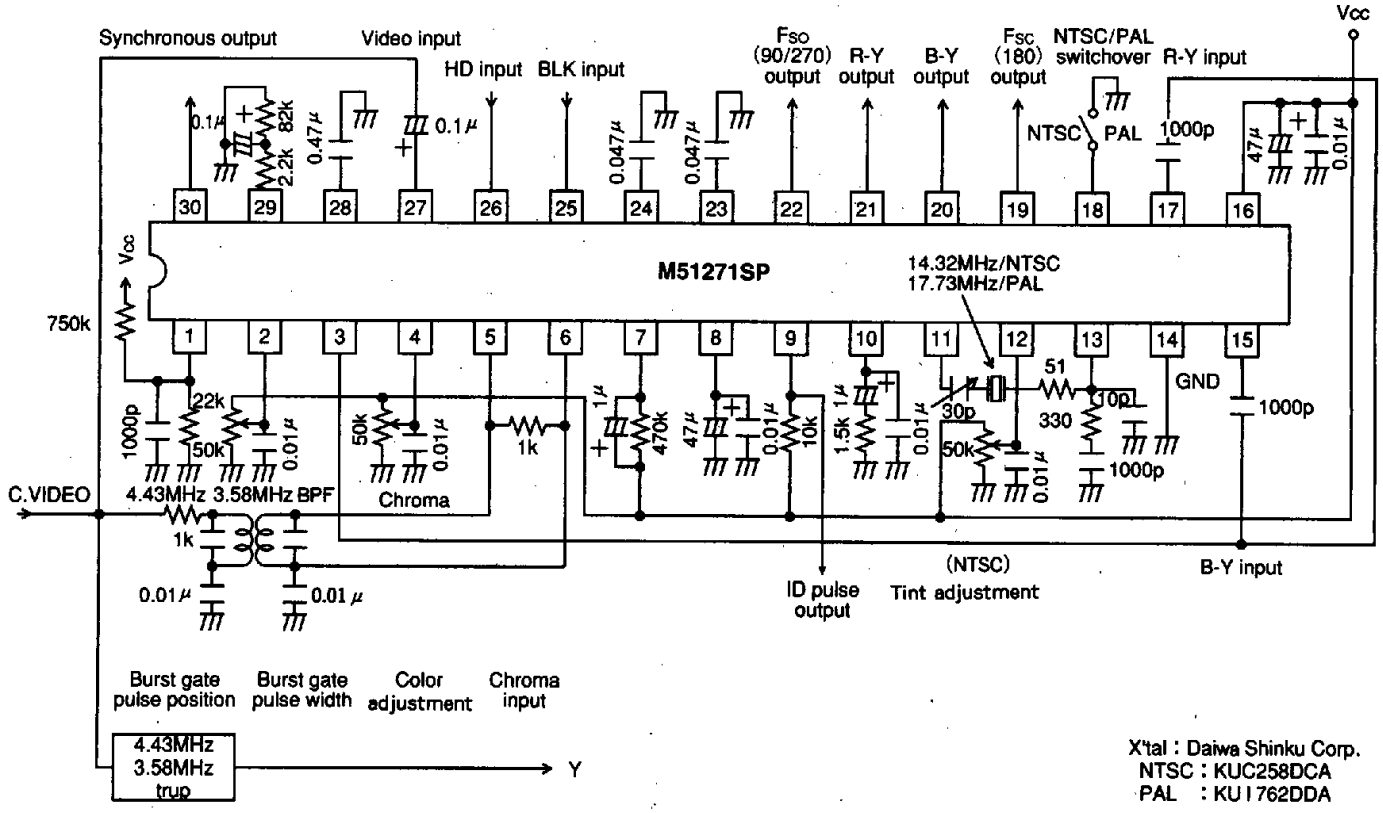
3.579545MHz (NTSC set SW13 at 1)
4.433618MHz (PAL set SW13 at 2).

TEST CIRCUIT D



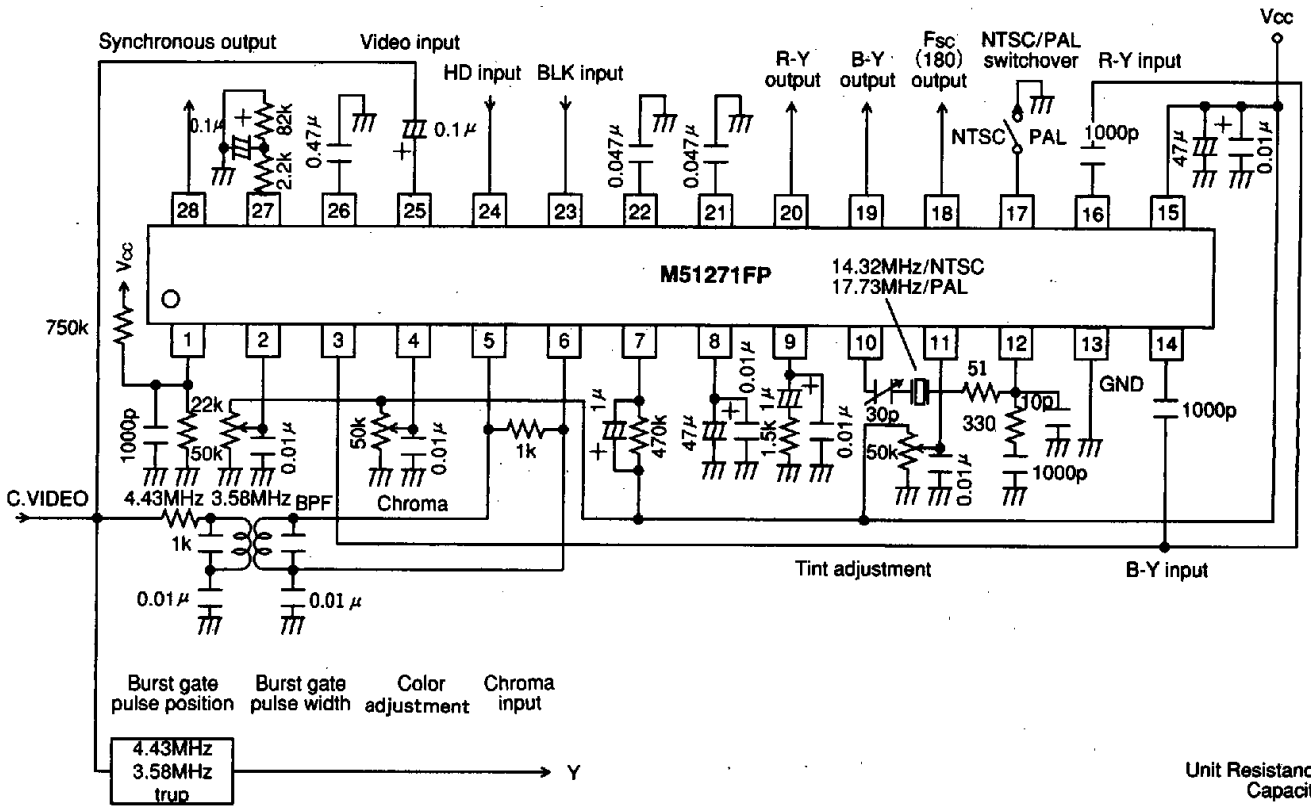
APPLICATION EXAMPLE

M51271SP



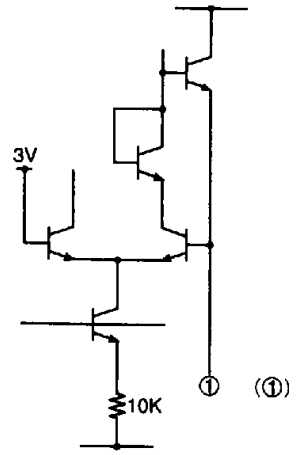
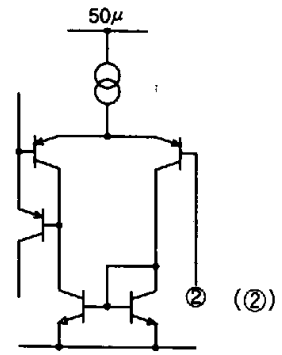
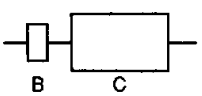
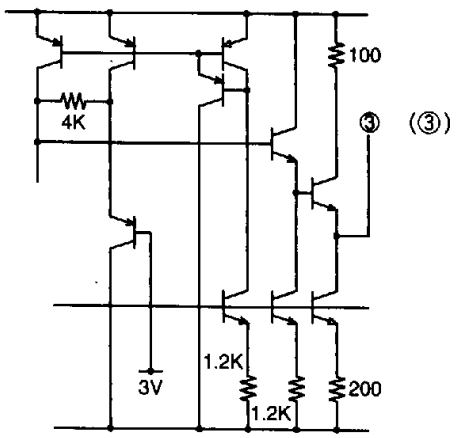
X'tal : Daiwa Shinku Corp.
NTSC : KUC258DCA
PAL : KU I 762DDA

M51271FP

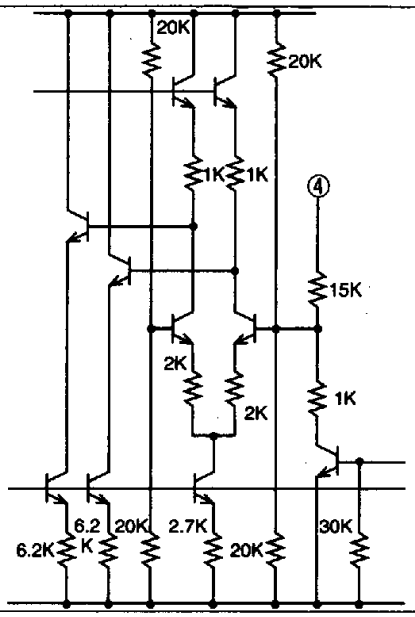
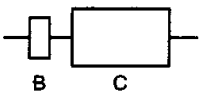
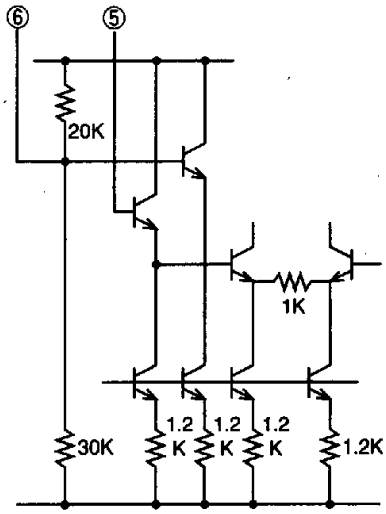
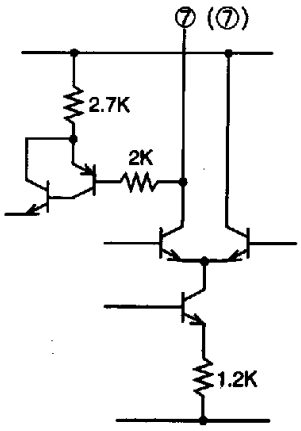


Unit Resistance : Ω
Capacity : F

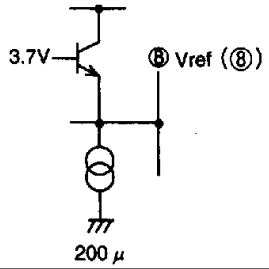
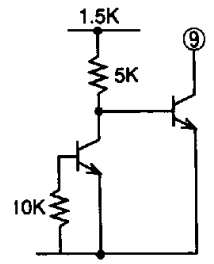
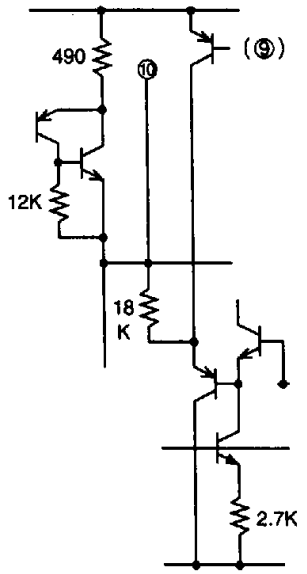
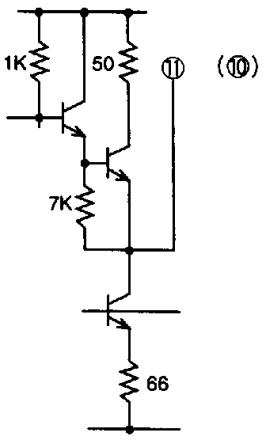
DESCRIPTION OF PIN

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
① ・ (1)	BURST GATE POSITION		
② ・ (2)	BGP WIDTH	Open base	
③ ・ (3)	CHROMA OUT	About 2.3VDC  B : About 250nVp-p C : About 500nVp-p	

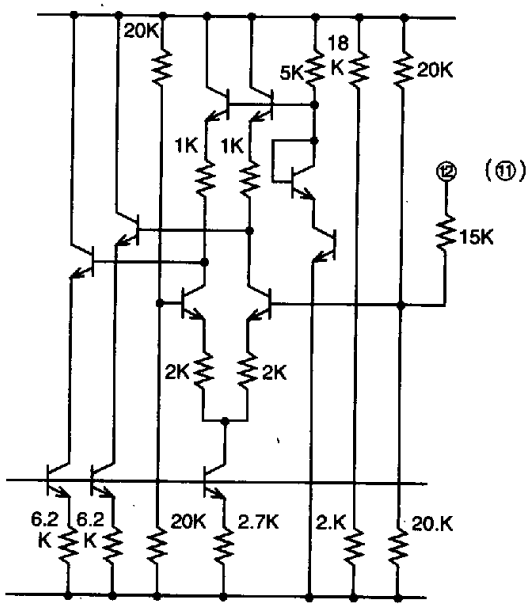
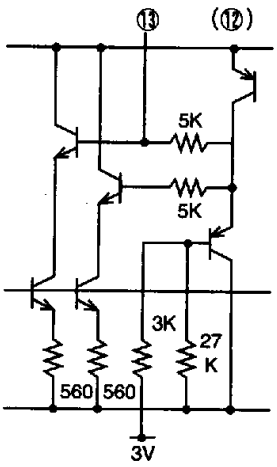
DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
④ • (4)	COLOR CONT	2.5VDC	
⑤ • (5)	CHROMA IN	Open base  B : About 100mVp-p C : About 200mVp-p	
⑥ • (6)	BIAS	3Vdc	
⑦ • (7)	Acc FILTER	About 4.2Vdc	

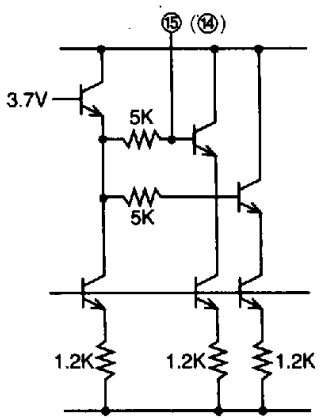
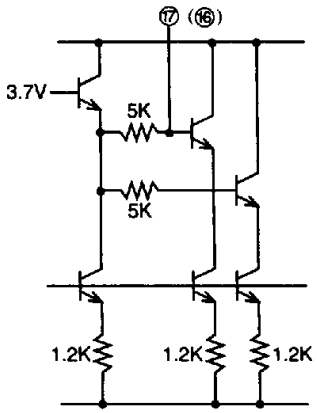
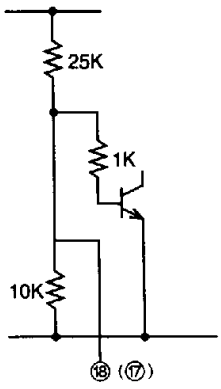
DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
⑧ • (8)	Vref	3Vdc	
⑨	ID PULSE OUT	Open collector	
⑩ • (9)	APC FILTER	About 2. 9V	
⑪ • (10)	VCXO OUT	About 1Vp-p 4fsc	

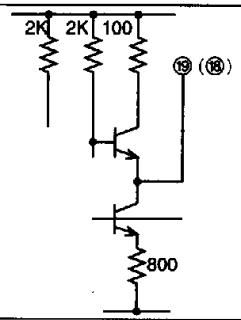
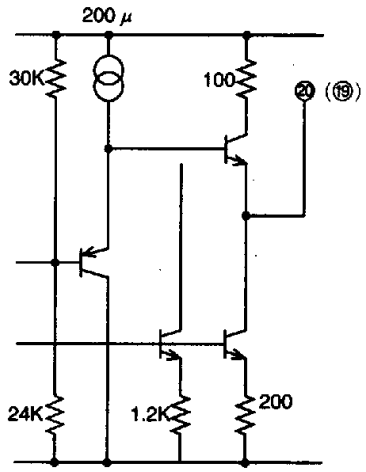
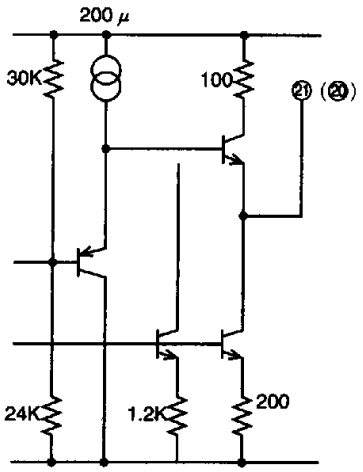
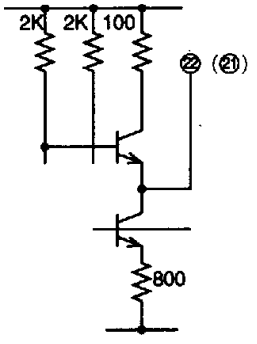
DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
⑫ • (11)	TINT CONT	2.5Vdc	
⑬ • (12)	VCXO IN	About 3.4Vdc	
⑭ • (13)	GND	0V	

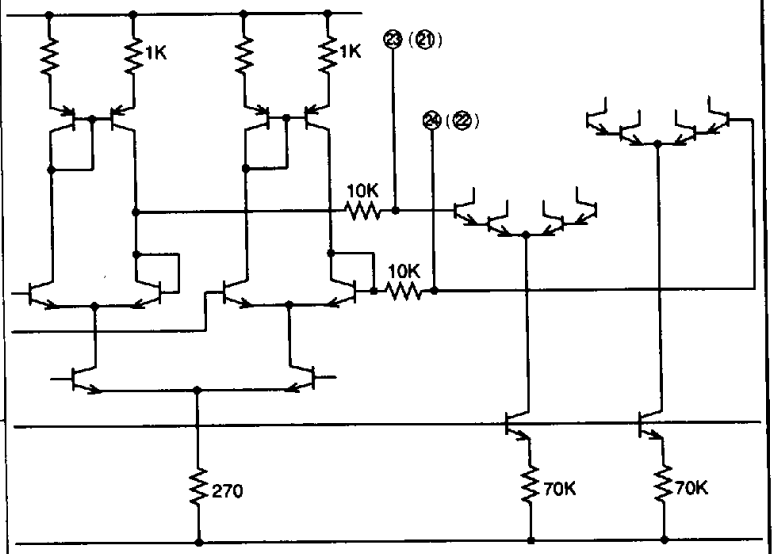
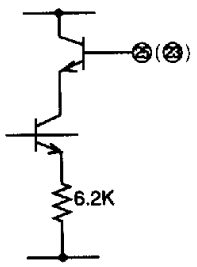
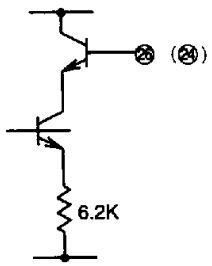
DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
⑮ • (14)	CHROMA IN B-Y	3Vdc	
⑯ • (15)	Vcc	5V	
⑰ • (16)	CHROMA IN R-Y	3Vdc	
⑱ • (17)	NTSC/PAL	1.4Vdc	

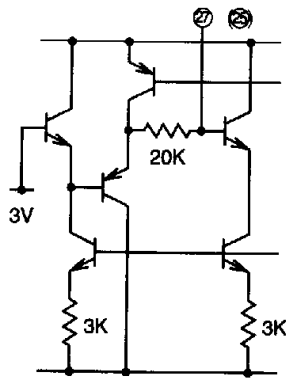
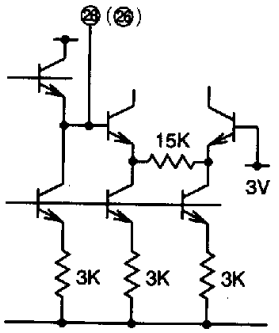
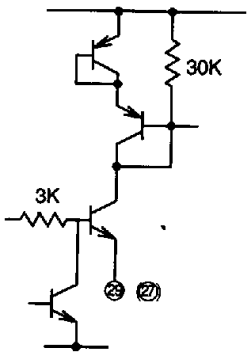
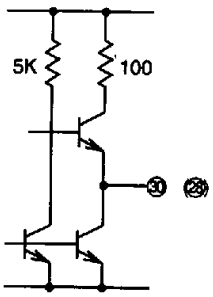
DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
⑲ • (18)	Fsc OUT (180deg)	4Vdc  About 500mVp-p	
⑳ • (19)	B-Y OUT	About 2. 3Vdc	
㉑ • (20)	R-Y OUT	About 2. 3Vdc	
㉒	Fsc OUT (90deg)		

DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
㉓ • (21)	ID KILLER FILTER	About 2V	
㉔ • (22)	ID KILLER Ref. FILTER	About 2. 7V	
㉕ • (23)	BLK IN	Open base	
㉖ • (24)	HD IN	Open base	

DESCRIPTION OF PIN (cont.)

Pin No. SP (FP)	Name	DC voltage (V)	Peripheral circuit of pins, shown in ( ) is FP
㉗ • (25)	VIDEO IN	3Vdc 0.5~1.5Vp-p	
㉘ • (26)	Sync Sepa FILTER	About 3V	
㉙ • (27)	Sync Sepa SLICE LEVEL		
㉚ • (28)	Sync OUT	4.3V 0.3V	

APPLICATION NOTE

PRECAUTIONS FOR APPLICATION

Burst gate pulse positioning time constant.
In the present document (provisional data, supply standard) CR time constant of ① pin which determines burst gate pulse starting point is specified by external constants as shown in figure 1.

However occasionucm, when RT has a smaller value (not exceeding 20K),the burst gate pulse may not be generated when power is switched on.

To prevent this it is necessary to apply approximate voltage 0.1V to ①pin, by connecting the pin to power supply through a resistor of high resistance value.

Detailed circuit and constants are given in figure 2.

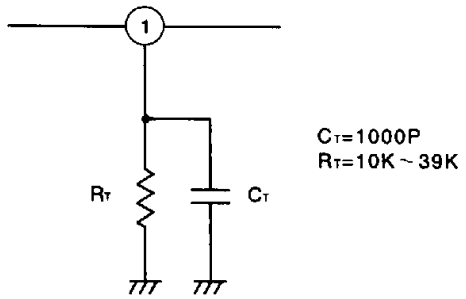


Figure 1. Present circuit

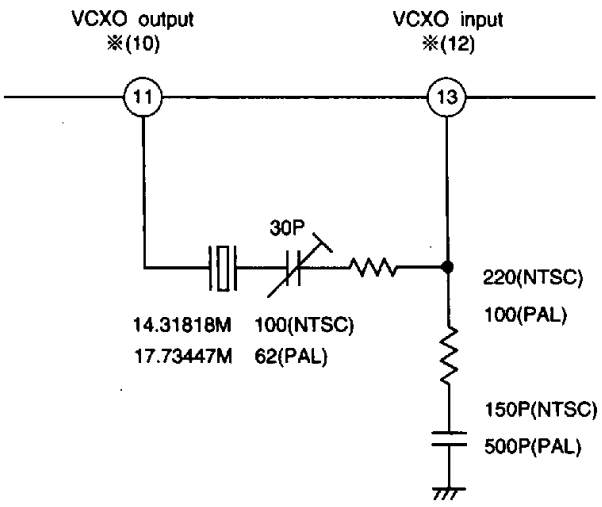


Figure 1. Present circuit

We recommend the following manufacturer s products for X'tal.
Manufacturer : Daishinku Corporation
Model and products number : HC-18 μ NTSC : KU Φ 258DCA
PAL : KU1762DDA

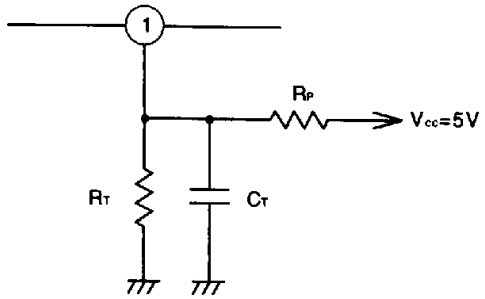


Figure 2. Reformed circuit

RT (Ω)	15K	22K	27K	33K
RP (Ω)	820K	1.2M	1.2M	1.5M

Examples for RT and RP pairs
(Determine CT so that BGP may come to the best position.)

•If using RT not given in the list above, determine RP by the fllowing equation.
$5.0 \times R_T / R_T + R_P = 0.1$
•When PR > RT, the time constant is apporoximately CT×RT. Therefore, the burst gate position is not affected by RP.

VCXO external constant
To prevent problems such as VCXO high frequency oscillation or oscillation stop at power-on, it is recommended to change the present external circuit (figure 1) into the following, given in figure 2.

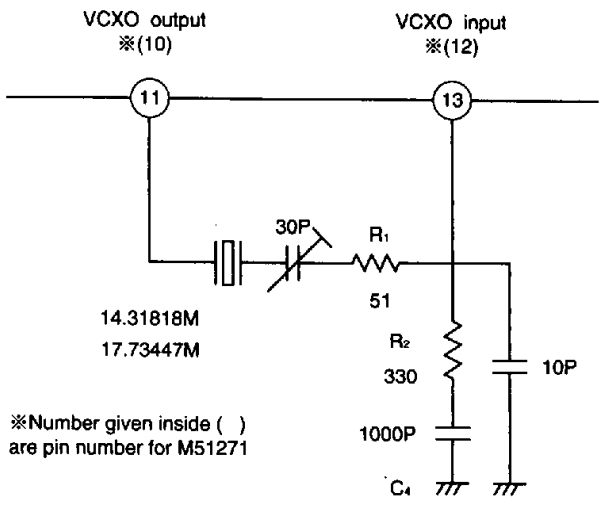


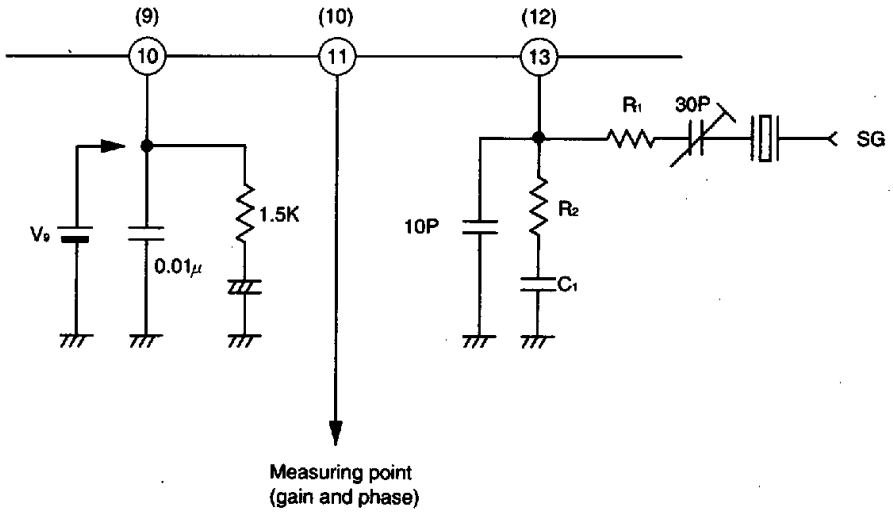
Figure 2. Reformed circuit

•When an X'tal different from the recommended product is used, suffcient consideration on values of external constants (R_1, R_2 and C_1) should be given. In that case, possibility of oscillation stop can be checked using the following method.

CHECKING METHOD

1.First, under a free running state, without applying V9, input SG=14.31818MHZ. Adjust ㉚ pin trimmer so that phase difference between input and output indicates 0°.

2.Next, apply V9=2.7V. Measure gain and phase of both input and output. To satisfy the required conditions, gain should be +3dB or more at the point where phase difference is 0°.



FREE RUNNING ADJUSTMENT METHOD (to set free running oscillation mode)

FREE RUNNING ADJUSTMENT

(I) Best method

Generate burst gate pulses and activate SYNC SEP by inputting normal video signals to SYNC SEP input (㉗ pin).

Adjust free running by inputting no signal to chroma input (⑤ pin). The important point here is to input absolutely no signal to the chroma input. It can be performed by terminating the chroma signal (turn it to monochrome signal) or by connecting the ⑤ pin to GND through a capacitor (with sufficient capacitance to absorb chroma signal).

Effectiveness can be evaluated consideaing conditions around the device (influence of noise etc.).

(II) Second - best method

If the chroma signal is not absolutely terminated, the following method is available. However, because output DC of APC DET is offset, free running frequency may shift(approximately ± 100Hz at the maximum).

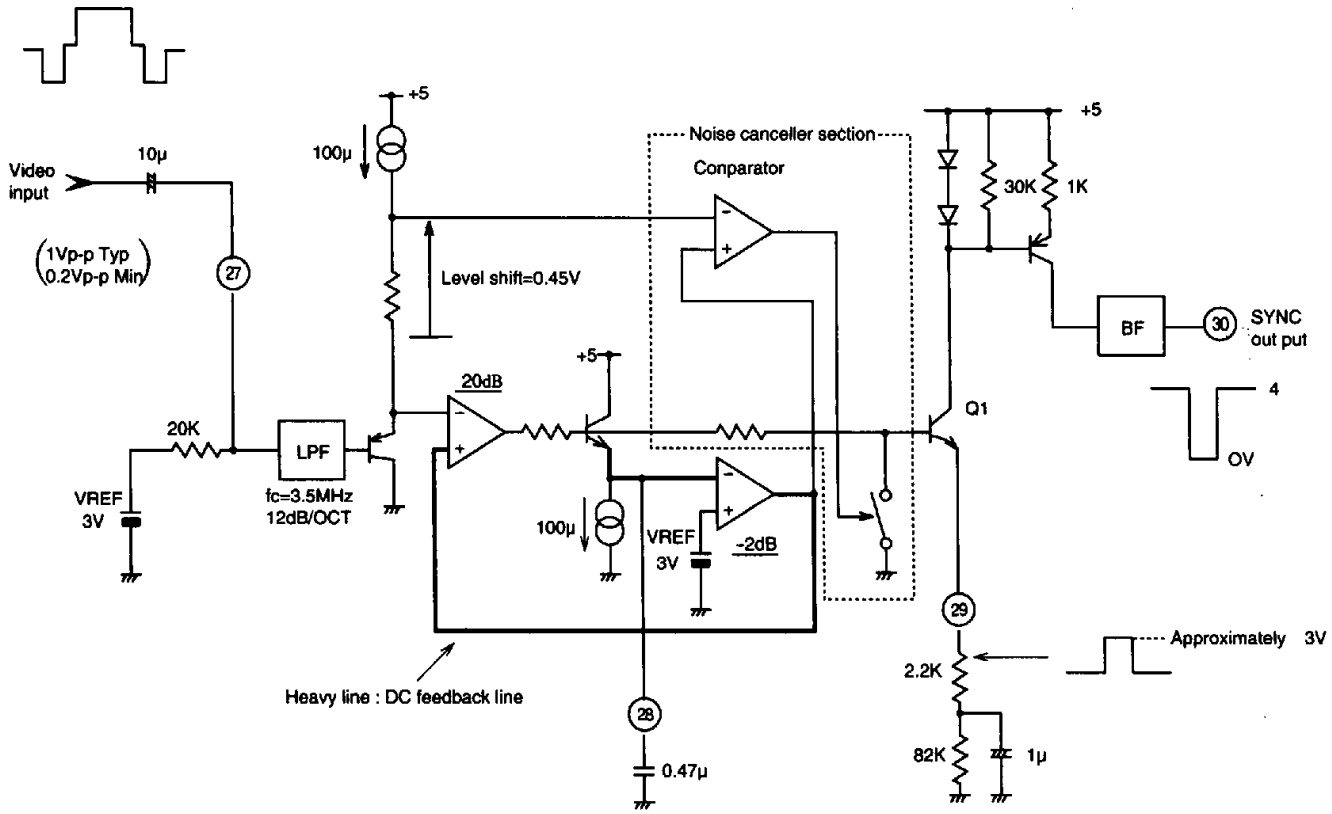
[Method]

Input no signal to SYNC SEP input(㉗pin). Set SYNC SEP output(㉚pin) to"H". (SYNC SEP may be set to"L"provided that the output is stable.)

Under this condition, the burst gate pulse and APC DET are at off state, that is, the condition of APC time constant is at hold state.

Therefore, free running adjustment is possible without being affected by chroma input even if chroma signal is inputted.

In addition, by measuring ㉓ pin DC voltage, it is possible to check whether burst gate pulse is off or not. If the pulse is off, potential of ㉓pin is 0V. (If it is on, potential is approximately 3.0V.)



DESCRIPTION

Video signal (1Vp-p Typ.) with SYNC of negative polarity is inputting to ㉗ pin. The LPF of Fc=3.5MHz removes high frequency noise contained in the video signal. Then, 20dB Amp.amplifies the signal. In order to suppress fluctuation in SYNC chip DC voltage caused by input APL fluctuation, this Amp. has a DC feedback circuit as shown by the heavy line in the block diagram. This means the circuit operates so that SYNC chip voltage held by the 0.47μF capacitor externally connected to ㉘ pin, is always kept equal to V_{REF}. THerefore, DC voltage at ㉘ pin indicates approximately 3.0V.

Thus,SYNC signals of positive polarity which SYNC chip DC voltage is matching, are inputted to the Amp. Q1. Then SYNC signals are separated. The Q1 emitter generates signals with SYNC chip DC voltage at approximately 3.0V.

Resistors of values 2.2kΩ and 82kΩ devided the potential which is held by 1μF capacitor. Electric current of value determined dividing difference between the holding voltage and the SYNC chip voltage by 2.2kΩ, flows into the Q1 collector.

SYNC output (negative polarity)is gained at ㉚pin.Therefore, it is possible to change slice level by changing ratio between the resistors which are 2.2kΩ and 82kΩ at present. If the 2.2kΩ resistor is replaced with a smaller one, slice level decreases (slice level comes closer to SYNC chip voltage). These resistors total value should not be changed too excessirely.

When pulse noise of voltage below SYNC chip voltage (input voltage not less than 0.4V) is inputted, the noise canceller prevents failure to separate correct SYNC signals.

DEMODULATION PERFORMANCE

1-1 DEMODULATION ANGLE SHIFT

90° and 180° fsc from 4fsc dividing output is used for demodulation carriers R-Y and B-Y.

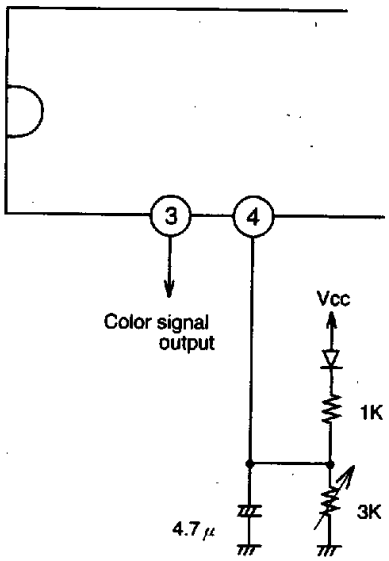
Measured value at 88° showed no dispersion. (N=10) assessing circuit type and allowing for ±2° dispersion may be sufficient.

1-2 DEMODULATION GAIN AND DEVIATION

Absolute values of each R-Y and B-Y outputs have approximate dispersion ±1dB (limit : ±2dB).

Demodulation gain ratio R-Y / B-Y within ±0.5dB is an actual value (limit : 0.8~1.2 times : ±2dB).

M51271SP/FP, M51279SP/FP IMPROVEMENT IN ACC OUTPUT TEMPERATURE CHARACTERISTICS



Principle; Existing temperature characteristic is canceled by adding counteractive temperature characteristic to the color saturation adjustment voltage.

Notes 1. The circuit shown above exhibits the largest temperature characteristics when color signal output amplitude (3 pin) is around 150 - 200 mV_{PP}.

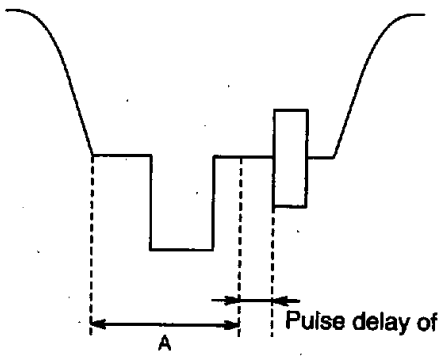
2. When it is over 200 mV_{PP}, this method can not be used because VCA works near the full gain.
3. When it is under 150 mV_{PP}, temperature characteristics are good even without compensating diode. In case of the circuit shown above, it becomes overcompensation.

INPUT PULSE

Blanking pulse ($\overline{BLKP}$) ····· BLKP is inputted through pin ㉕ in case of M51271SP and M51279SP and through pin ㉓ in M51271FP, with V_{th} of 3.5V. Switch off the demodulator at "L" (3.5 V - GND) and mute output.

Output pin DC voltage regulation is restrained within 50 mV. In case blanking is not conducted, set this pin at "H" (V_{CC} - 3.5 V).

HD pulse (HDP) ····· HDP is inputted through pin ㉖ in case of M51271FP and M51279SP, through pin ㉔ in M51271FP, and through pin ㉘ in M51279FP, with V_{th} of 4.0V. This pulse is divided by two in the IC to make an ID pulse which invert R-Y carrier every 1 H when PAL is demodulated. Since F.F inside the IC inverts by rising of input pulse, select input pulse which rises between the part A shown in the diagram below.
In this case selected pulse should constantly continue even in vertical blanking part. Therefore, this pulse is unnecessary when NTSC is demodulated, so set HDP input pin to V_{CC} or GND.



CONNECTION DIAGRAM OF M51271 AND M51272 (ENCODER)