M51361P/M5E565P

PLL

DESCRIPTION

The M51361P/M5E565P is semiconductor integrated circuit consisting of a phase locked loop (PLL)IC which includes a phase comparator, a voltage controlled oscillator and a DC amplifier.

The center frequency is determined by the oscillation frequency of the voltage controlled oscillator; the oscillation frequency can easily adjusted with a resistor and a capacitor, making this IC suitable for use in frequency modulators and tracking filters, etc.

FEATURES

- Variations in the supply voltage have little effect on the oscillation frequency ····· 200Hz/V typ (f_O = 30kHz)
- The total harmonic distortion of demodulated output is low ····· 0.35%
- Both square and triangular wave forms can be obtained as oscillator output
- Both lock range and capture range are externally controllable
- Wide oscillation frequency range ····· 0.5~500kHz
- The loop can be opened and a frequency divider inserted from outside

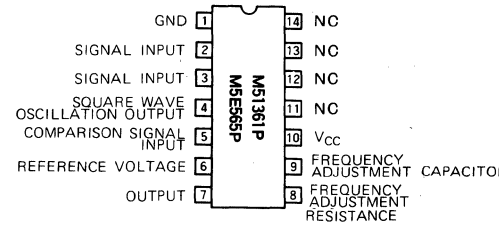
APPLICATION

Frequency modulators, frequency discriminators, tracking filters, frequency multipliers, FSK (Frequency shift keying) modulators.

RECOMMENDED OPERATING CONDITIONS

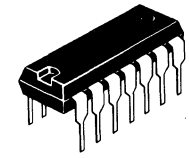
Supply voltage range ····· 12~15.6V
Rated supply voltage ····· 14V

PIN CONFIGURATION (TOP VIEW)



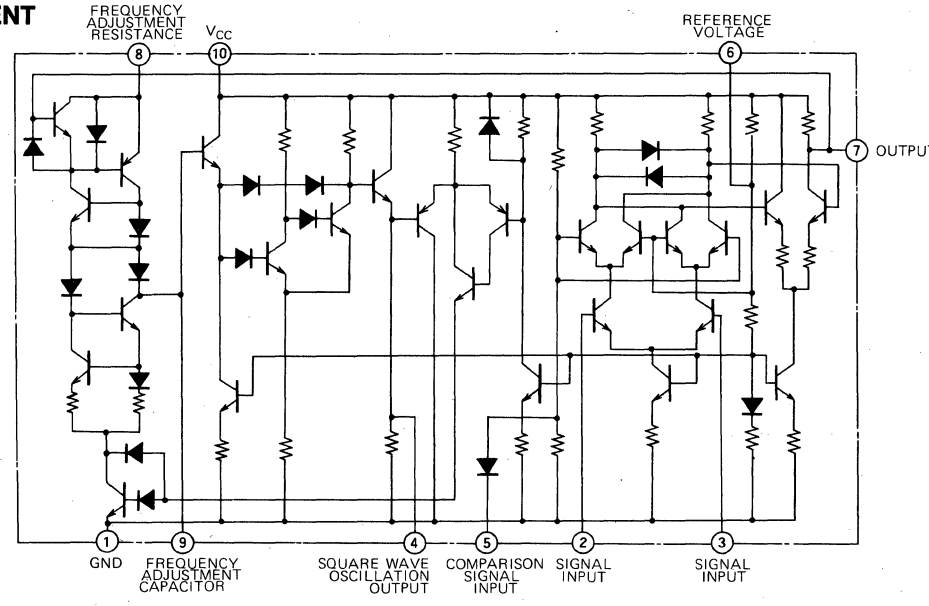
Outline 14P4

NC: NO CONNECTION



14-pin molded plastic DIL

EQUIVALENT CIRCUIT



MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS (T_a=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		16	V
Vin	Input voltage		1	V_{P-P}
I_{CC}	Circuit current		30	mA
Pd	Power dissipation		600	mW
K_θ	Thermal derating	Ta≧25℃	6	mW/℃
Topr	Operating temperature		0 ~ +75	℃
Tstg	Storage temperature		−40 ~ +125	℃

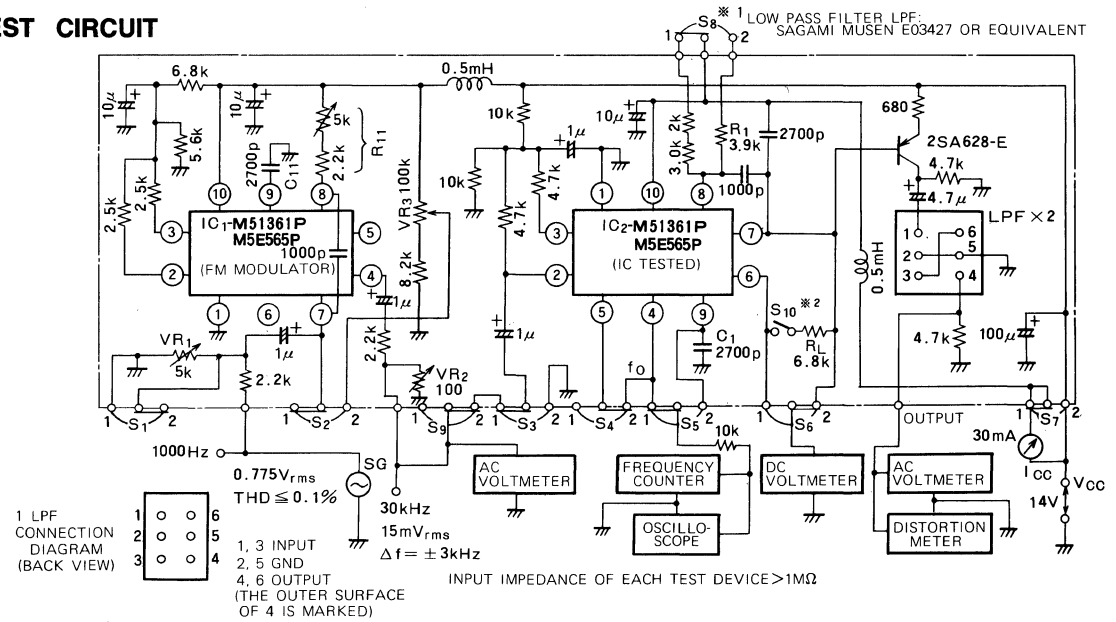
ELECTRICAL CHARACTERISTICS (T_a=25℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CCO}	Quiescent circuit current		No signal		11	17	mA
V⑦	Pin 7 voltage				12.5	13.5	V
V⑥−⑦	Offset voltage		Potential difference between pins 6 and 7		150	360	mV
Vo(af)	Demodulation circuit	Output voltage	Oscillation frequency 30kHz, Input frequency 30kHz, Input voltage 15mVrms, Modulation frequency 1kHz, Frequency deviation ±3kHz	200	300		mVrms
THD	Demodulation circuit	Total harmonic distortion			0.35	0.75	%
S/N	Demodulation circuit	Signal to noise ratio			※1 56		dB
V_{SQ}	Voltage controlled oscillator	Square wave output voltage			7.0		V_{P-P}
	Voltage controlled oscillator	Duty cycle	Oscillation frequency 30kHz	40	50	60	%
V_{TRI}	Voltage controlled oscillator	Triangular wave output voltage			2.4		V_{P-P}
fo(max)	Voltage controlled oscillator	Maximum free-running frequency	Frequency setting capacitor 100pF		※2 500		kHz
	Voltage controlled oscillator	Oscillation frequency drift vs V_{CC}	Oscillation frequency 30kHz		200		Hz/V
	Voltage controlled oscillator	Oscillation frequency drift vs temperature			850		ppm/℃
f_L	Voltage controlled oscillator	Lock range			25		kHz

※1: Unmodulated

※2: Free-running frequency adjustment resistor R_1 = 2k ~ 20kΩ (4kΩ standard)

TEST CIRCUIT



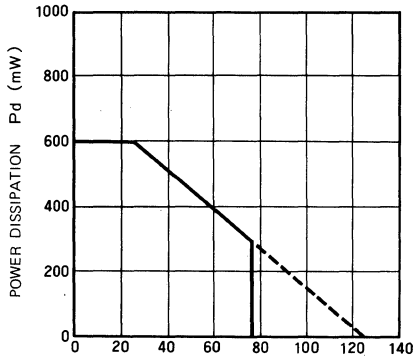
TEST METHODS

Parameter	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	Method
Oscillation frequency adjustment			2	2	1		2	1		Adjust f_O to 30±0.5kHz with R_1 to prepare for testing (testing with the frequency counter)
Quiescent circuit current			2	2			1	1		Ammeter
Demodulated output voltage	2	1	1	2			2	1	2	$V_{O(af)}$ (AC Voltmeter)
Total harmonic distortion	2	1	1	2			2	1	2	Distortion meter
Signal to noise ratio	1	1	1	2			2	1	2	Ratio to $V_{O(af)}$ (AC Voltmeter)
Pin⑦DC voltage			2	2		2	2	1		(DC Voltmeter)
Lock range	1	2	1	2		1	2	1	2	Measure the limits of the pin④output frequency which is synchronized with input frequency by variing VR_3.

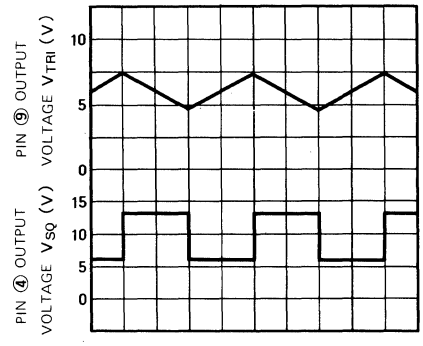
2: Connect pins⑥ and⑦ through a 6.8kΩ resistance only when measuring the lock range. (S_{10} ON)

TYPICAL CHARACTERISTICS (T_a=25°C, V_{CC}=12V, unless otherwise noted)

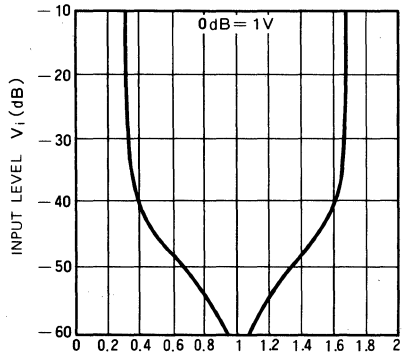
THERMAL DERATING (MAXIMUM RATING)



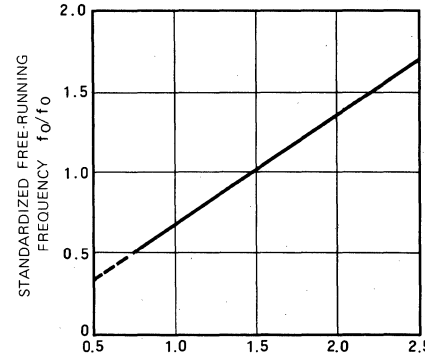
VOLTAGE CONTROLLED OSCILLATOR OUTPUT WAVE FORM



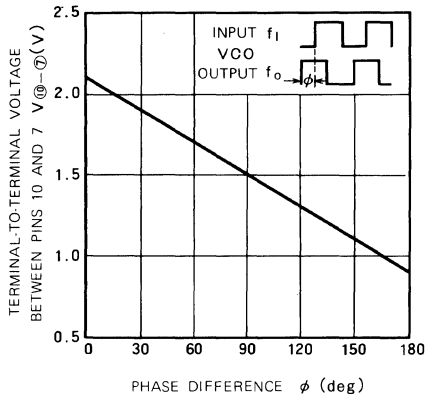
LOCK RANGE VS INPUT LEVEL



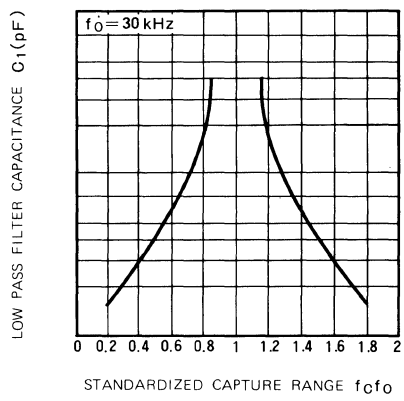
FREE-RUNNING FREQUENCY VS CONTROL VOLTAGE (VCO CONVERSION GAIN)



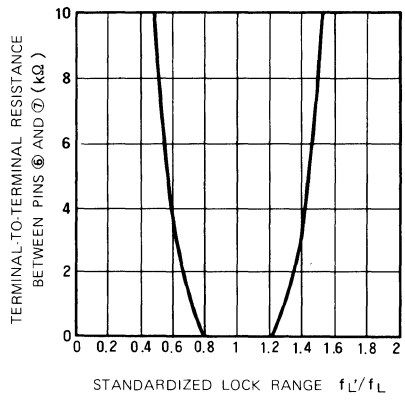
TERMINAL-TO-TERMINAL VOLTAGE BETWEEN PINS ⑩ AND ⑦ VS INPUT/OUTPUT PHASE DIFFERENCE



CAPTURE RANGE VS LOW PASS FILTER CAPACITANCE



LOCK RANGE VS TERMINAL-TO-TERMINAL RESISTANCE BETWEEN PINS ⑥ AND ⑦



EXPLANATION OF TERMINOLOGY AND THE BASIC COMPUTATIONAL DESIGN EXPRESSIONS

1. Terminology

Terms commonly employed in describing phase locked loop systems are explained below.

Free-running frequency f_O

This is the frequency produced by the voltage controlled oscillator (VCO) when no input signal is applied.

Lock state

When the loop can sequentially follow changes in the input signal phase or frequency it is said to be in the lock state.

Capture range

If the loop enters the lock state when a signal is input to it, then the frequency of the signal is within the capture range. Frequencies outside of the capture range cannot cause the loop to enter the lock state.

Lock range

A frequency is said to be within the lock range if the lock state is maintained after it is captured by a signal even though the frequency of the signal is changed. The loop will lose the lock state if the signal shifts to a frequency outside this range. In general, the lock range is wider than the capture range.

2. Computational expression

The computational expressions which are the basis for operation of the M51361P/M5E565P are as follows.

Free-running frequency f_O

$$f_O \fallingdotseq \frac{1}{4R_1C_1} \quad \text{(Hz)} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (1)$$

where R_1 is the resistance between pins ⑧ and ⑩ in ohms and C_1 is the capacitance between pin⑨and GND in Farads.

Lock range

$$f_L = \pm \frac{8f_o}{V_{CC}} \quad \text{(Hz)} \quad \text{..... (2)}$$

Capture range

$$f_C \fallingdotseq \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} \quad \text{(Hz)} \quad \text{..... (3)}$$

where $\tau = 3.6 \times 10^3) \times C_2$ and C_2 (F) is the capacitance between pins⑦and ⑩ in farads.

Lock range control

The lock range is determined by the supply voltage (V_{CC}) and the free-running frequency (f_O); this range can be reduced, however, by connecting pins ⑥ and ⑦ through a resistance. In such cases the lock range becomes

$$f_{L'} \fallingdotseq f_L \frac{(R_{⑥-⑦} + 1.6)}{(R_{⑥-⑦} + 5.2)} \quad \text{(Hz)} \quad \text{..... (4)}$$

where $R_{6\sim7}$ is, the resistance between pins⑥and⑦in kΩ and f_L is the lock range when pins ⑥ and ⑦ are not connected in Hz.

This method can be used to reduce the lock range about 30% from that when pins⑥and⑦are not connected.

APPLICATION EXAMPLE

FM Demodulation

FM signals can be demodulated with good linearity using the M51361P. When the loop is in the lock state, the amount of variation in the average direct current voltage level of the signal output by the phase comparator is proportional to variation in the frequency of the input signal. With the M51361P/M5E565P variations in the input frequency over a wide range (about ±60%) are followed with a linearity which is within about 0.5%.

A basic example of application of this IC as an FM demodulator is shown in the diagram at right. The VCO free-running frequency is $(f_O) = 1/4C_1R_1$ so that it is the same (at pin ④)as the center frequency of the input signal when the circuit is idle. A value for R_1 of about 4kΩ is appropriate, but any value from 2～20kΩ may be used. Sometimes it is desirable to insert a 300～1000pF capacitor between pins ⑦ and ⑧ to prevent parasitic oscillation. Capacitor C_2 between pin ⑦ and V_{CC} constitutes a low pass filter which, together with the internal output resistance (about 3.6kΩ), determines the cut-off frequency for the demodulated output.

FM demodulation circuit