

DESCRIPTION

The M51365SP is a semiconductor integrated circuit consisting of an IF signal processor suitable for color TV sets and VTRs with AV.

Circuits include VIF amplifiers, video detector, VCO, APC detector, AFT, video equalizer, plus IF/RF AGC and SIF detector functions.

FEATURES

- Employment of a full synchronous detector circuit using PLL as video detector provides excellent DG, DP, 920kHz beat and cross color characteristics.
- Usage of PLL-SPLIT method to obtain intercarrier by separating video IF and audio IF processing by VCO output provides good sound sensitivity and reduces buzz. In consumer sets, intercarrier is also available from the video detector output.
- Built-in video equalizer suitable for VTRs and color TV sets equipped with video output terminals.
- Employment of quadrature detector circuit for FM detection of audio IF requires no adjustment.

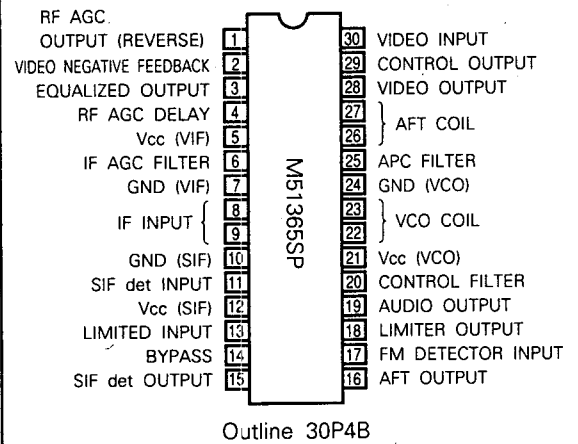
APPLICATIONS

TV sets, VTR tuners

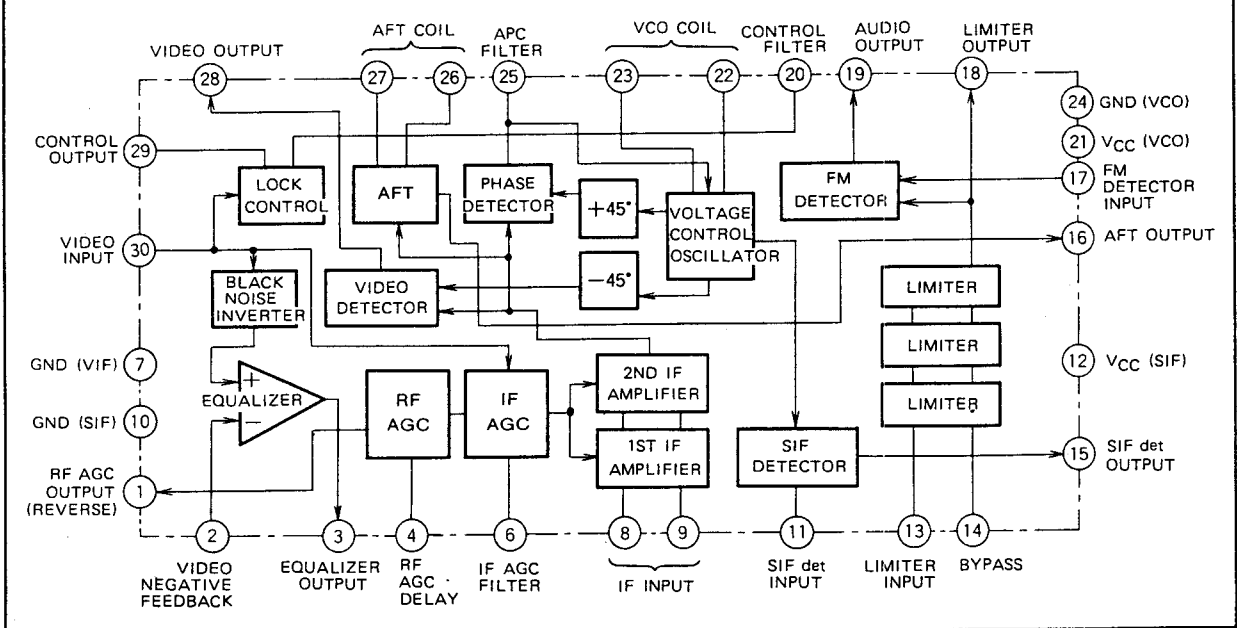
RECOMMENDED OPERATING CONDITIONS

Supply voltage range 8~10V
 Rated supply voltage 9V

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



M51365SP

PLL-SPLIT VIF/SIF

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rated	Unit
V _{CC}	Supply voltage	14	V
P _d	Power dissipation	1250	mW
T _{opr}	Operating temperature	-20~75	°C
T _{stg}	Storage temperature	-40~125	°C
Surge 8	Permissible surge (pin ⑧)	+200, -150	V
Surge 9	Permissible surge (pin ⑨)	+200, -150	V
	Permissible surge (other pins)	±200	V

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{CC}=9V, unless otherwise noted)

VIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions						Limits			Unit
				Input signal		External voltage(V)			* Switch is set at 1.	Min.	Typ.	Max.	
				VIF	SIF1	V ₁	V ₆	V ₂₀					
I _{CC(VIF)}	Circuit current (VIF)	1	A1	—	—	3	—	—	SW1=2, SW2=3	33	45	57	mA
V ₂₈	Video detector output DC voltage 1	1	TP9	—	—	3	0	—	SW2=3, SW3=2	3.4	3.75	4.1	V
V ₃	Video detector output DC voltage 2	1	TP2	—	—	3	0	—	SW2=3, SW3=2	4.4	4.8	5.2	V
V _{o det 1}	Video detector output 1	1	TP9	SG1	—	3	—	—	SW2=3	1.15	1.45	1.75	V _{P-P}
V _{o det 2}	Video detector output 2	1	TP2	SG1	—	3	—	—	SW2=3	1.6	1.95	2.3	V _{P-P}
P/N	Video S/N	1	TP10	SG2	—	3	—	—	SW2=3, SW6=2 Refer to note 1	50	58		dB
B _w	Video frequency characteristics	1	TP9	SG3	—	3	—	—	SW2=3 Refer to note 2	5.5	7		MHz
V _{in(min)}	Input sensitivity	1	TP9	SG4	—	3	—	—	SW2=3 Refer to note 3		46	51	dB _μ
V _{in(max)}	Maximum permissible input	1	TP9	SG5	—	3	—	—	SW2=3 Refer to note 4	107	110		dB _μ
GR	AGC control range	1	—	—	—	—	—	—	Refer to note 5	58	64		dB
V _{IH}	Maximum IF AGC voltage	1	TP3	—	—	3	—	—	SW2=3	6.5	8.6		V
V _{I(80dB_μ)}	IF AGC voltage (80dB _μ)	1	TP3	SG6	—	3	—	—	SW2=3	4.3	4.9	5.5	V
V _{IL}	Minimum IF AGC voltage	1	TP3	SG7	—	3	—	—	SW2=3	3.4	3.9	4.4	V
V _{O SIF-1}	SIF det 4.5MHz output (100dB _μ)	1	TP4	SG2	SG8	3	—	—	SW2=3	104	109	114	dB _μ
V _{O SIF-2}	SIF det 4.5MHz output (80dB _μ)	1	TP4	SG2	SG9	3	—	—	SW2=3	90	96	101	dB _μ
V ₁₆	AFT output voltage	1	TP5	—	—	3	0	—	SW2=3	3.2	4.3	5.4	V
μ	AFT detector sensitivity	1	TP5	SG10	—	3	—	—	SW2=3 Refer to note 6	48	70	92	mV/kHz
V _{16H}	Maximum AFT voltage	1	TP5	SG10	—	3	—	—	SW2=3 Refer to note 7	8	8.7		V
V _{16L}	Minimum RF AGC voltage	1	TP5	SG10	—	3	—	—	SW2=3 Refer to note 8		0.38	1.0	V
V _{1H}	Minimum RF AGC voltage	1	TP1	SG2	—	2	—	—	SW2=3	7	7.85		V
V _{1L}	Maximum RF AGC voltage	1	TP1	SG2	—	4	—	—	SW2=3		0	1.0	V
CL-U1	Capture range (U) 1	1	TP9	SG11	—	3	—	—	SW2=3 Refer to note 9	0.5	1.0		MHz
CL-L1	Capture range (L) 1	1	TP9	SG11	—	3	—	—	SW2=3 Refer to note 10	1.2	1.7		MHz
CL-T	Capture range (T)	1	—	—	—	—	—	—	Refer to note 11	2.0	2.7		MHz
CL-U2	Capture range (U) 2	1	TP9	SG11	—	3	—	—	SW2=3, SW5=2 Refer to note 9	0.45	0.9	1.45	MHz
CL-L2	Capture range (L) 2	1	TP9	SG11	—	3	—	—	SW2=3, SW5=2 Refer to note 10	0.7	1.0	1.35	MHz
V _{20TH}	Lock detection threshold voltage	1	TP8	—	—	3	5	Variable	SW2=3, SW3, 4, 5=2 Refer to note 12	3.6	4.0	4.4	V
V _{29L}	Minimum pin 29 voltage	1	TP8	—	—	3	5	Variable	SW2=3, SW3, 4, 5=2 Refer to note 13		0.15	0.5	V

VIF SECTION (cont.)

Symbol	Parameter	Test circuit	Test point	Test conditions					Limits			Unit	
				Input signal		External voltage(V)			* Switch is set at 1.	Min.	Typ.		Max.
				VIF	SIF1	V ₁	V ₆	V ₂₀					
FC1	EQ frequency characteristics 1	1	TP9 TP2	SG12	—	3	—	—	SW2=3 Refer to note 14	1.4	2.4	3.4	dB
FC2	EQ frequency characteristics 2	1	TP9 TP2	SG13	—	3	—	—	SW2=3 Refer to note 14	4.2	5.7	7.2	dB
FC3	EQ frequency characteristics 3	1	TP9 TP2	SG14	—	3	—	—	SW2=3 Refer to note 14	9.5	12.0	14.5	dB
IM	Intermodulation	1	TP9	SG15	—	3	Vari- able	—	SW2=3, SW3=2 Refer to note 15	30	35		dB
DG	DG	1	TP9	SG16	—	3	—	—	SW2=3 Refer to note 16		2	5	%
DP	DP	1	TP9	SG16	—	3	—	—	SW2=3 Refer to note 16		2	5	deg
V _{BTH}	Black spot inverter threshold level	1	TP2	SG1	—	3	Vari- able	—	SW2=3, SW3=2 Refer to note 17	1.3	1.7	2.1	V
V _{BCL}	Black spot inverter clamp level	1	TP2	SG1	—	3	Vari- able	—	SW2=3, SW3=2 Refer to note 17	3.7	4.2	4.7	V
V _{SYNC}	Pin ③ sync chip level	1	TP2	SG2	—	3	—	—	SW2=3	2.1	2.5	2.9	V
R _{in} (V)	VIF input resistance	2		90dB _μ	—	3	—	—			0.95		kΩ
C _{in} (V)	VIF input capacitance	2		90dB _μ	—	3	—	—			5		pF
R _{in} (S1)	SIF1 input resistance	2		—	90dB _μ	3	—	—			2.1		kΩ
C _{in} (S1)	SIF1 input capacitance	2		—	90dB _μ	3	—	—			2.5		pF

SIF SECTION

Symbol	Parameter	Test circuit	Test point	Test conditions					Limits			Unit	
				Input signal		External voltage(V)			* Switch is set at 1.	Min.	Typ.		Max.
				SIF2		V ₁	V ₆	V ₂₀					
I _{CC} (SIF)	Circuit current (SIF)	1	A2	—		0	—	—	SW1=3, SW2=2	5.0	7.2	9.4	mA
V ₁₉	AF output DC voltage	1	TP6	—		0	—	—	SW1=3	4.0	4.6	5.2	V
V _{OAFMAX}	Maximum AF output	1	TP6	SG17		0	—	—	SW1=3	530	680	830	mV _{rms}
THD _{AF}	AF output distortion	1	TP6	SG21		0	—	—	SW1=3		0.2	1.0	%
V _{in(lim)}	Input limiting sensitivity	1	TP6	SG18		0	—	—	SW1=3 Refer to note 18		38	46	dB _μ
AMR	AMR	1	TP6	SG19		0	—	—	SW1=3 Refer to note 19	50	60		dB
S/N	AF S/N	1	TP6	SG20		0	—	—	SW1=3 Refer to note 20	60	75		dB

ELECTRICAL CHARACTERISTICS TEST METHOD

Note 1. Video s/n "P/N"

- a. Input SG2 to VIF IN.
- b. Passing Pin 28 noise through a low pass filter (5MHz, at -3dB), measure the output voltage at TP10 in r.m.s.

c. $P/N=20 \log \frac{V_{odet1}(V_{p-p}) \times 0.7}{noise (V_{rms})}$

V_{odet 1} is video detector output 1.

Note 2. Video frequency characteristics "Bw"

- a. SG3 is set as follows.

$f_1=58.75\text{MHz}$ $f_2=57.75\text{MHz}$	$V_i=90\text{dB}\mu$ $V_i=70\text{dB}\mu$	}	mixed signal
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- b. Measure V₁, the component of 1MHz at TP9.
- c. Decrease frequency f₂ level until the component (f₁-f₂) at TP9 becomes 3dB smaller than V₁, and read the value at that level.
- d. Bw=58.75 - f₂ (MHz)

Note3. Input sensitivity "Vin(min)"

- a. Input SG4 to VIF IN.
- b. Decrease SG4 level until pin 28 detector output is 3dB smaller than V_{odet 1}. This is the input sensitivity level.

Note 4. Maximum permissible input "Vin(max)"

- a. Set SG5 at 90dBμ and input to VIF IN.
- b. V₂ is detector output at pin 28.
- c. Increase SG5 voltage until detector output becomes 3dB smaller than V₂. This is the maximum permissible voltage.

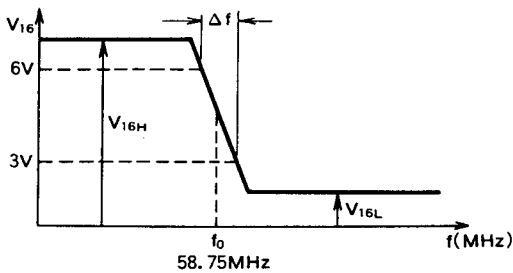
Note 5. AGC control range "GR"

- a. AGC control range is defined as follows:
GR=maximum permissible input-input sensitivity

Note 6. AFT detector sensitivity "μ"

- a. Input SG10 to VIF IN
- b. Measure frequency difference Δf when DC voltage at TP5 transits from 3.0V to 6.0V.
- c. AFT detector sensitivity is defined as follows:

$$\mu = \frac{3000\text{mV}}{\Delta f \text{ (kHz)}} \text{ (mV/kHz)}$$



Note 7. Maximum AFT voltage "V16H"

- a. Maximum AFT voltage is V_{16H} in the above figure.

Note 8. Minimum AFT voltage "V16L"

- a. Minimum AFT voltage is V_{16L} in the above figure.

Note 9. Capture range (U) "CL-U-1" "CL-U-2"

- a. Input SG11 to VIF IN and increase frequency until VCO lock is removed.
- b. Decrease SG11 frequency until VCO lock is enabled again. This frequency is f_v (MHz).
- c. Capture range (U) is f_v-58.75 (MHz).

Note 10. Capture range (L) "CL-L-1" "CL-L-2"

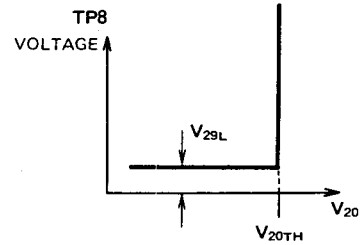
- a. Input SG11 to VIF IN and decrease frequency until VCO lock is removed.
- b. Increase SG11 frequency until VCO lock is enabled again. This frequency is f_L (MHz).
- c. Capture range (L) is between 58.75-f_L (MHz).

Note 11. Capture range (T) "CT-T"

- a. "CL-T" = "CL-U-1" + "CCL-L-1" (MHz)

Note 12. Lock detection threshold voltage "V20TH"

- a. Measure TP8 value with V₂₀ voltage at 3V.
- b. Increase V₂₀ voltage until TP8 voltage shows drastic change. This voltage is V_{20TH}. (threshold 1V).



Note 13. Minimum pin 29 voltage "V29L"

- a. V_{29L} is the minimum voltage mentioned in note 12.

Note 14. EQ frequency characteristics "FC1" "FC2" "FC3"

- a. Input SG12, SG13 or SG14 to VIF IN.
- b. Measure level of (f₁-f₂) component at TP9, this is V_{EQ IN} (dBμ).
- c. Measure level of (f₁-f₂) component at TP2, this is V_{EQ OUT} (dBμ).
- d. EQ frequency characteristics are defined as follows:
FC1~3=V_{EQ OUT}-V_{EQ IN} (dB)

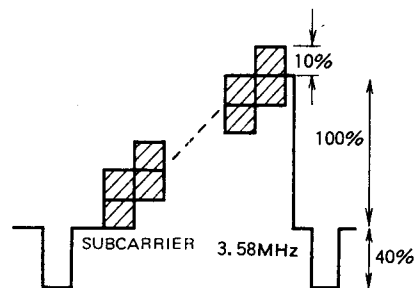
Note 15. Intermodulation "IM"

- a. Input SG15 to VIF IN
- b. Read values of TP9 on an oscilloscope and adjust V₆ voltage to set minimum level of detector output waveform at 2V.
- c. Observe TP9 value on a spectrum analyzer. The relation 920kHz level to 3.58MHz level is the intermodulation.



Note 16. DG,DP "DG,DP"

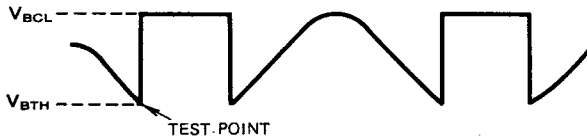
- a. As shown below, the modulated waveform of SG16 is a 10-step wave with 87.5% video modulation.
- b. Measure values of DG and DP at TP9 on a vectorscope.



Note 17. Black spot inverter threshold, clamp level

" $V_B TH$, $V_B CL$ "

- Input SG1 to VIF IN.
- Measure DC voltages from output waveform at TP2 as shown in the figure.

**Note 18. Input limiting sensitivity " $V_{in(lim)}$ "**

- Set SG18 value at 80dB μ and input to SIF2 IN.
- Decrease SG18 output until detector output at TP6 becomes 3dB smaller than $V_{OAF MAX}$.

That SG18 level is the input limiting sensitivity.

Note 19. AMR " AMR "

- Input SG19 to SIF2 IN.
- Measure V_{AM} , which is output voltage at TP6.
- AMR is defined as follows:

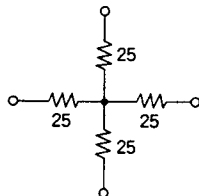
$$MR = 20 \log \frac{V_{OAF MAX} (mV_{rms})}{V_{AM} (mV_{rms})} \quad (dB)$$

Note 20. AF S/N " S/N "

- Input SG20 to SIF2 IN.
- The output voltage measured at TP6 is V_N .
- AF S/N is defined as follows :

$$S/N = 20 \log \frac{V_{OAF MAX} (mV_{rms})}{V_N (mV_{rms})} \quad (dB)$$

- The oscillation levels of all AM modulated waves are those at the peak level.
- The following circuit is used for the mixer.



- Set IF AGC voltage of V_{co} coil at 0V and adjust free run frequency at 58.75MHz in quiescent state.

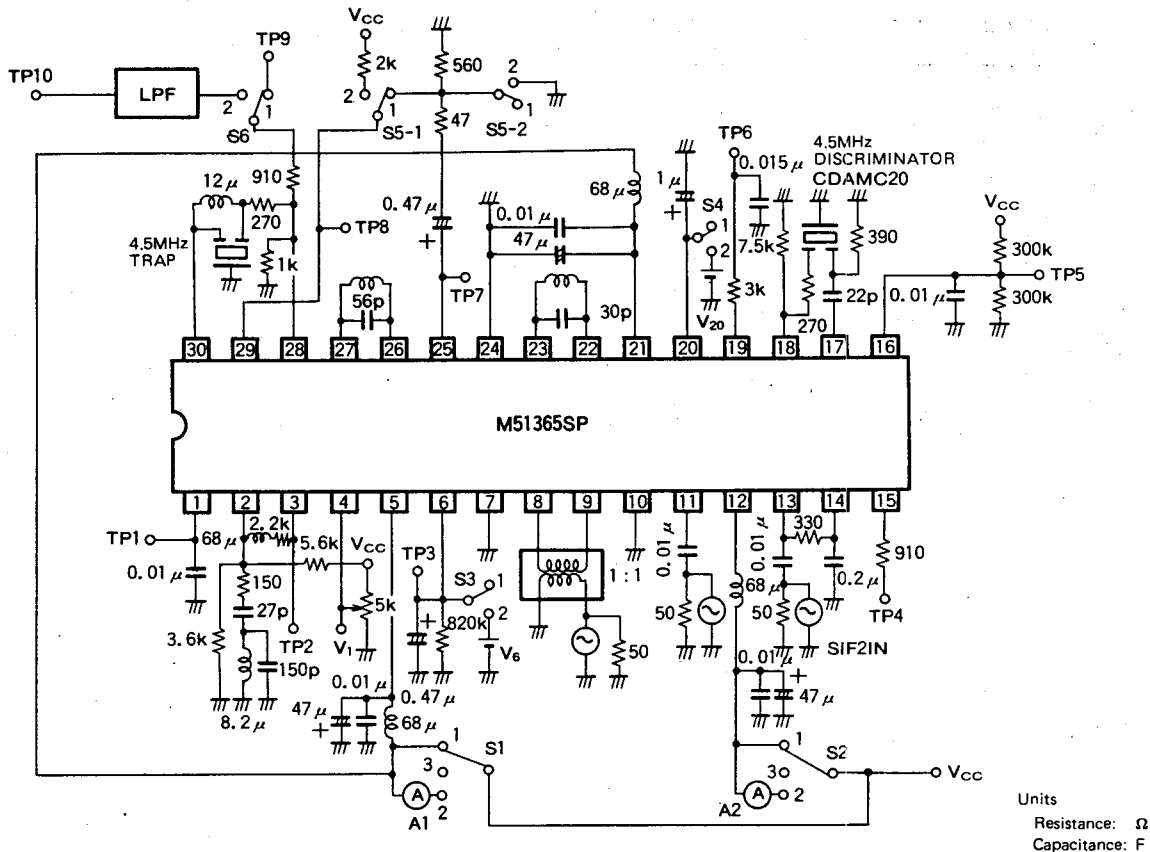
INPUT SIGNAL

SG	Input signal (Value at pin terminal, 50 Ω)
1	$f_0 = 58.75MHz$ $V_i = 90dB\mu$ 77.78%AM (Equivalent to 87.5% video modulation $f_m = 20kHz$)
2	$f_0 = 58.75MHz$ $V_i = 90dB\mu$
3	$f_1 = 58.75MHz$ $V_i = 90dB\mu$ $f_2 = 53 \pm 5MHz$ $V_i = 70dB\mu$ } mixed signal
4	$f_0 = 58.75MHz$ $V_i = V_{variable}$ $f_m = 20kHz$ 77.78%AM
5	$f_0 = 58.75MHz$ $V_i = V_{variable}$ $f_m = 20kHz$ 16%AM
6	$f_0 = 58.75MHz$ $V_i = 80dB\mu$
7	$f_0 = 58.75MHz$ $V_i = 110dB\mu$
8	$f_0 = 54.25MHz$ $V_i = 100dB\mu$
9	$f_0 = 54.25MHz$ $V_i = 80dB\mu$
10	$f_0 = 58.75MHz \pm 5MHz$ $V_i = 90dB\mu$
11	$f_0 = 58.75MHz \pm 5MHz$ $V_i = 90dB\mu$ $f_m = 20kHz$ 77.78%AM
12	$f_1 = 58.75MHz$ $V_i = 90dB\mu$ $f_2 = 58.25MHz$ $V_i = 60dB\mu$ } mixed signal
13	$f_1 = 58.75MHz$ $V_i = 90dB\mu$ $f_2 = 55.75MHz$ $V_i = 60dB\mu$ } mixed signal
14	$f_1 = 58.75MHz$ $V_i = 90dB\mu$ $f_2 = 54.75MHz$ $V_i = 60dB\mu$ } mixed signal
15	$f_1 = 58.75MHz$ $V_i = 90dB\mu$ $f_2 = 55.17MHz$ $V_i = 80dB\mu$ $f_3 = 54.25MHz$ $V_i = 80dB\mu$ } mixed signal
16	$f_0 = 58.75MHz$, standard 10-step modulation $m = 87.5\%$ video modulation sync chip level 90dB μ
17	$f_0 = 4.5MHz \pm 25kHz$ dev $V_i = 100dB\mu$ $f_m = 400Hz$
18	$f_0 = 4.5MHz \pm 25kHz$ dev $V_i = V_{variable}$ $f_m = 400Hz$
19	$f_0 = 4.5MHz$ $V_i = 100dB\mu$ 30%AM $f_m = 400Hz$
20	$f_0 = 4.5MHz$ $V_i = 100dB\mu$
21	$f_0 = 4.5MHz$ $V_i = 100dB\mu$ $f_m = 400Hz \pm 7.5kHz$ dev

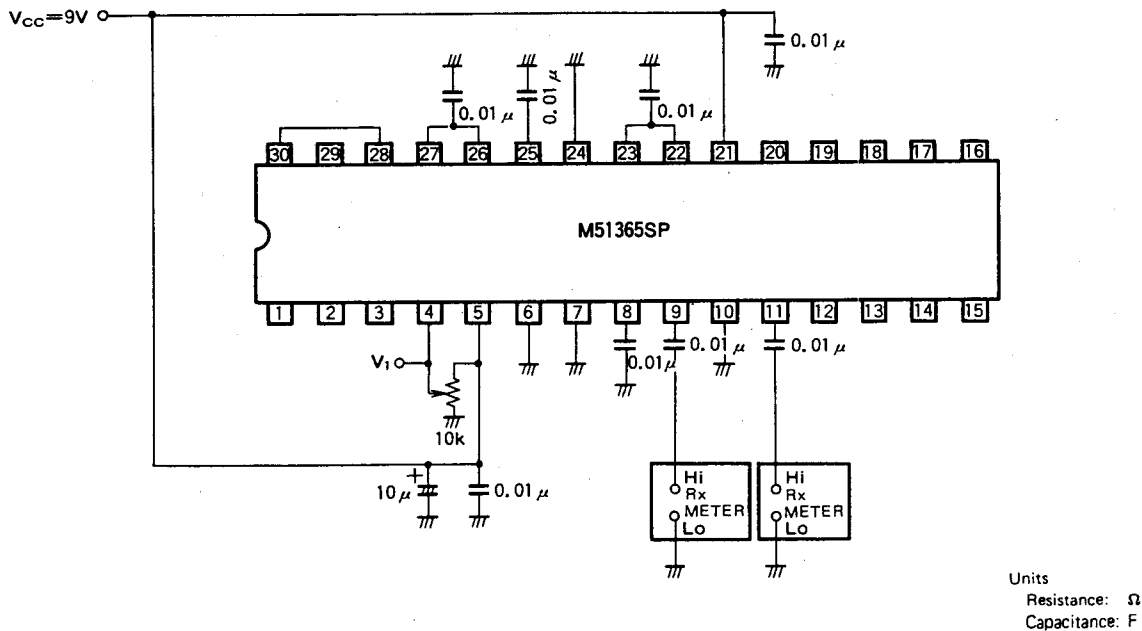
M51365SP

PLL-SPLIT VIF/SIF

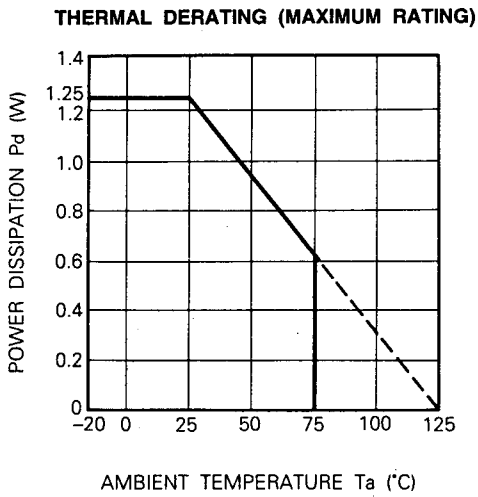
TEST CIRCUIT 1



TEST CIRCUIT 2



TYPICAL CHARACTERISTICS



APPLICATION EXAMPLE

