E2G0023-17-41

OKI Semiconductor

This version: Jan. 1998
Previous version: May 1997

MSM514400D/DL

1,048,576-Word × 4-Bit DYNAMIC RAM : FAST PAGE MODE TYPE

DESCRIPTION

The MSM514400D/DL is a 1,048,576-word × 4-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MSM514400D/DL achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/ single-layer metal CMOS process. The MSM514400D/DL is available in a 26/20-pin plastic SOJ, 20-pin plastic ZIP, or 26/20-pin plastic TSOP. The MSM514400DL (the low-power version) is specially designed for lower-power applications.

FEATURES

- 1,048,576-word × 4-bit configuration
- Single 5 V power supply, ±10% tolerance
- Input : TTL compatible, low input capacitance
- Output : TTL compatible, 3-state
- Refresh : 1024 cycles/16 ms, 1024 cycles/128 ms (L-version)
- Fast page mode, read modify write capability
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, hidden refresh, $\overline{\text{RAS}}$-only refresh capability
- Multi-bit test mode capability
- Package options:

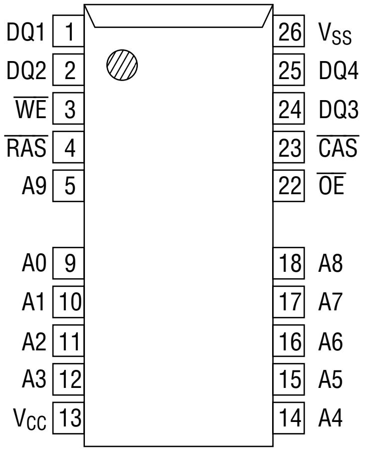
26/20-pin 300 mil plastic SOJ	(SOJ26/20-P-300-1.27)	(Product : MSM514400D/DL-xxSJ)
20-pin 400 mil plastic ZIP	(ZIP20-P-400-1.27)	(Product : MSM514400D/DL-xxZS)
26/20-pin 300 mil plastic TSOP	(TSOPII26/20-P-300-1.27-K)	(Product : MSM514400D/DL-xxTS-K)

xx indicates speed rank.

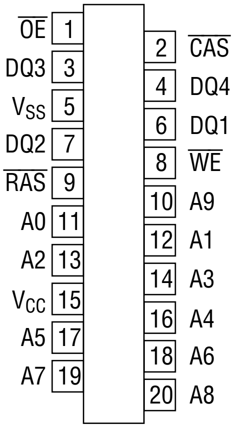
PRODUCT FAMILY

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max.)	Standby (Max.)
MSM514400D/DL-50	50 ns	25 ns	13 ns	13 ns	90 ns	550 mW	5.5 mW/ 1.1 mW (L-version)
MSM514400D/DL-60	60 ns	30 ns	15 ns	15 ns	110 ns	495 mW	
MSM514400D/DL-70	70 ns	35 ns	20 ns	20 ns	130 ns	440 mW	

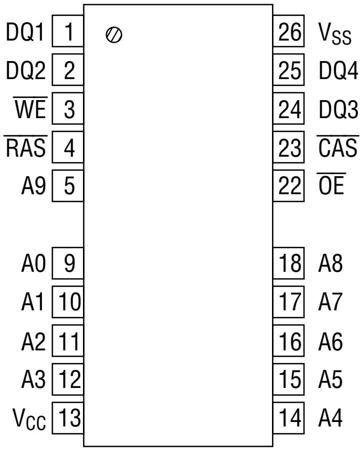
PIN CONFIGURATION (TOP VIEW)



26/20-Pin Plastic SOJ



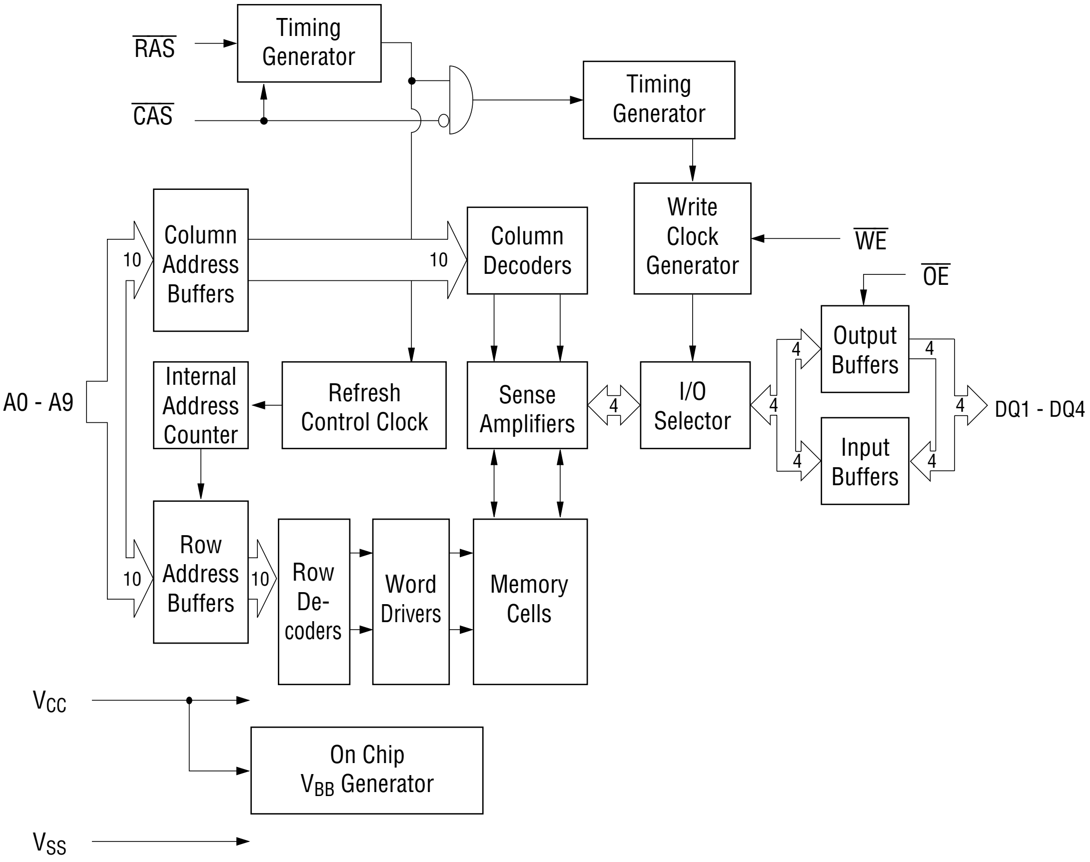
20-Pin Plastic ZIP



26/20-Pin Plastic TSOP
(K Type)

Pin Name	Function
A0 - A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 - DQ4	Data Input/Data Output
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (5 V)
V_{SS}	Ground (0 V)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	–1.0 to 7.0	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D*	1	W
Operating Temperature	T_{opr}	0 to 70	°C
Storage Temperature	T_{stg}	–55 to 150	°C

*: Ta = 25°C

Recommended Operating Conditions

(Ta = 0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.4	—	6.5	V
Input Low Voltage	V_{IL}	–1.0	—	0.8	V

Capacitance

(V_{CC} = 5 V ±10%, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9)	C_{IN1}	—	6	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	—	7	pF
Output Capacitance (DQ1 - DQ4)	$C_{I/O}$	—	7	pF

DC Characteristics

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Condition	MSM514400 D/DL-50		MSM514400 D/DL-60		MSM514400 D/DL-70		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
Output High Voltage	V_{OH}	I_{OH} = –5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0 V ≤ V_I ≤ 6.5 V; All other pins not under test = 0 V	–10	10	–10	10	–10	10	µA	
Output Leakage Current	I_{LO}	DQ disable 0 V ≤ V_O ≤ 5.5 V	–10	10	–10	10	–10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t_{RC} = Min.	—	100	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I_{CC2}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = V_{IH}	—	2	—	2	—	2	mA	1
		$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ ≥ V_{CC} –0.2 V	—	1	—	1	—	1		
			—	200	—	200	—	200	µA	1, 5
Average Power Supply Current ($\overline{\text{RAS}}$-only Refresh)	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ = V_{IH}, t_{RC} = Min.	—	100	—	90	—	80	mA	1, 2
Power Supply Current (Standby)	I_{CC5}	$\overline{\text{RAS}}$ = V_{IH}, $\overline{\text{CAS}}$ = V_{IL}, DQ = enable	—	5	—	5	—	5	mA	1
Average Power Supply Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	I_{CC6}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	100	—	90	—	80	mA	1, 2
Average Power Supply Current (Fast Page Mode)	I_{CC7}	$\overline{\text{RAS}}$ = V_{IL}, $\overline{\text{CAS}}$ cycling, t_{PC} = Min.	—	80	—	70	—	60	mA	1, 3
Average Power Supply Current (Battery Backup)	I_{CC10}	t_{RC} = 125 µs, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, t_{RAS} ≤ 1 µs	—	300	—	300	—	300	µA	1, 4, 5

Notes :
1. I_{CC} Max. is specified as I_{CC} for output open condition.
2. The address can be changed once or less while $\overline{\text{RAS}}$ = V_{IL}.
3. The address can be changed once or less while $\overline{\text{CAS}}$ = V_{IH}.
4. V_{CC} – 0.2 V ≤ V_{IH} ≤ 6.5 V, –1.0 V ≤ V_{IL} ≤ 0.2 V.
5. L-version.

AC Characteristics (1/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM514400 D/DL-50		MSM514400 D/DL-60		MSM514400 D/DL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	t_{RC}	90	—	110	—	130	—	ns	
Read Modify Write Cycle Time	t_{RWC}	131	—	150	—	180	—	ns	
Fast Page Mode Cycle Time	t_{PC}	35	—	40	—	45	—	ns	
Fast Page Mode Read Modify Write Cycle Time	t_{PRWC}	76	—	80	—	95	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	4, 5, 6
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	20	ns	4, 5
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	4, 6
Access Time from $\overline{\text{CAS}}$ Precharge	t_{CPA}	—	30	—	35	—	40	ns	4
Access Time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	20	ns	4
Output Low Impedance Time from $\overline{\text{CAS}}$	t_{CLZ}	0	—	0	—	0	—	ns	4
$\overline{\text{CAS}}$ to Data Output Buffer Turn-off Delay Time	t_{OFF}	0	13	0	15	0	20	ns	7
$\overline{\text{OE}}$ to Data Output Buffer Turn-off Delay Time	t_{OEZ}	0	13	0	15	0	20	ns	7
Transition Time	t_T	3	50	3	50	3	50	ns	3
Refresh Period	t_{REF}	—	16	—	16	—	16	ms	
Refresh Period (L-version)	t_{REF}	—	128	—	128	—	128	ms	
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RASP}	50	100,000	60	100,000	70	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	13	—	15	—	20	—	ns	
$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	t_{ROH}	10	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	t_{CP}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	13	10,000	15	10,000	20	10,000	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	20	37	20	45	20	50	ns	5
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	15	25	15	30	15	35	ns	6
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	10	—	15	—	15	—	ns	
Column Address Hold Time from $\overline{\text{RAS}}$	t_{AR}	45	—	50	—	55	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{RAL}	25	—	30	—	35	—	ns	

AC Characteristics (2/2)

(V_{CC} = 5 V ±10%, Ta = 0°C to 70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM514400 D/DL-50		MSM514400 D/DL-60		MSM514400 D/DL-70		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	8
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t_{RRH}	0	—	0	—	0	—	ns	8
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	9
Write Command Hold Time	t_{WCH}	10	—	10	—	10	—	ns	
Write Command Hold Time from $\overline{\text{RAS}}$	t_{WCR}	40	—	45	—	50	—	ns	
Write Command Pulse Width	t_{WP}	10	—	10	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t_{OEH}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	13	—	15	—	20	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	13	—	15	—	20	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	10
Data-in Hold Time	t_{DH}	10	—	15	—	15	—	ns	10
Data-in Hold Time from $\overline{\text{RAS}}$	t_{DHR}	45	—	50	—	55	—	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t_{OED}	13	—	15	—	20	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	36	—	35	—	45	—	ns	9
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	48	—	50	—	60	—	ns	9
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	73	—	80	—	95	—	ns	9
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t_{CPWD}	53	—	55	—	65	—	ns	9
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{WRP}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$)	t_{WRH}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Set-up Time (Test Mode)	t_{WTS}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Hold Time (Test Mode)	t_{WTH}	10	—	10	—	10	—	ns	

Notes:

1. A start-up delay of 200 µs is required after power-up, followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$-only refresh or $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh) before proper device operation is achieved.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring input timing signals. Transition times (t_T) are measured between V_{IH} and V_{IL}.

4. This parameter is measured with a load circuit equivalent to 2 TTL loads and 100 pF.

5. Operation within the t_{RCD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
   t_{RCD} (Max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then the access time is controlled by t_{CAC}.

6. Operation within the t_{RAD} (Max.) limit ensures that t_{RAC} (Max.) can be met.
   t_{RAD} (Max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (Max.) limit, then the access time is controlled by t_{AA}.

7. t_{OFF} (Max.) and t_{OEZ} (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

8. t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (Min.) , $t_{RWD} \geq t_{RWD}$ (Min.), $t_{AWD} \geq t_{AWD}$ (Min.) and $t_{CPWD} \geq t_{CPWD}$ (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.

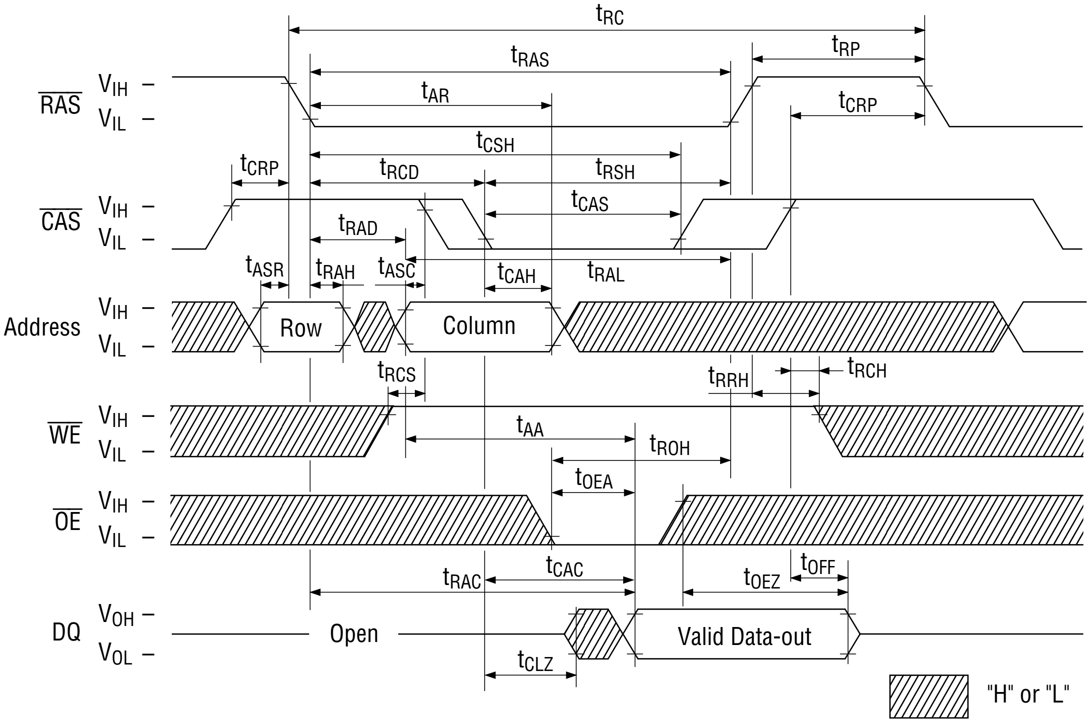
10. These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in an early write cycle, and to the $\overline{\text{WE}}$ leading edge in an $\overline{\text{OE}}$ control write cycle, or a read modify write cycle.

11. The test mode is initiated by performing a $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.
    This mode is latched and remains in effect until the exit cycle is generated.
    The test mode specified in this data sheet is a 2-bit parallel test function. CA0 is not used. In a read cycle, if all internal bits are equal, the DQ pin will indicate a high level. If any internal bits are not equal, the DQ pin will indicate a low level.
    The test mode is cleared and the memory device returned to its normal operating state by performing a $\overline{\text{RAS}}$-only refresh cycle or a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle.

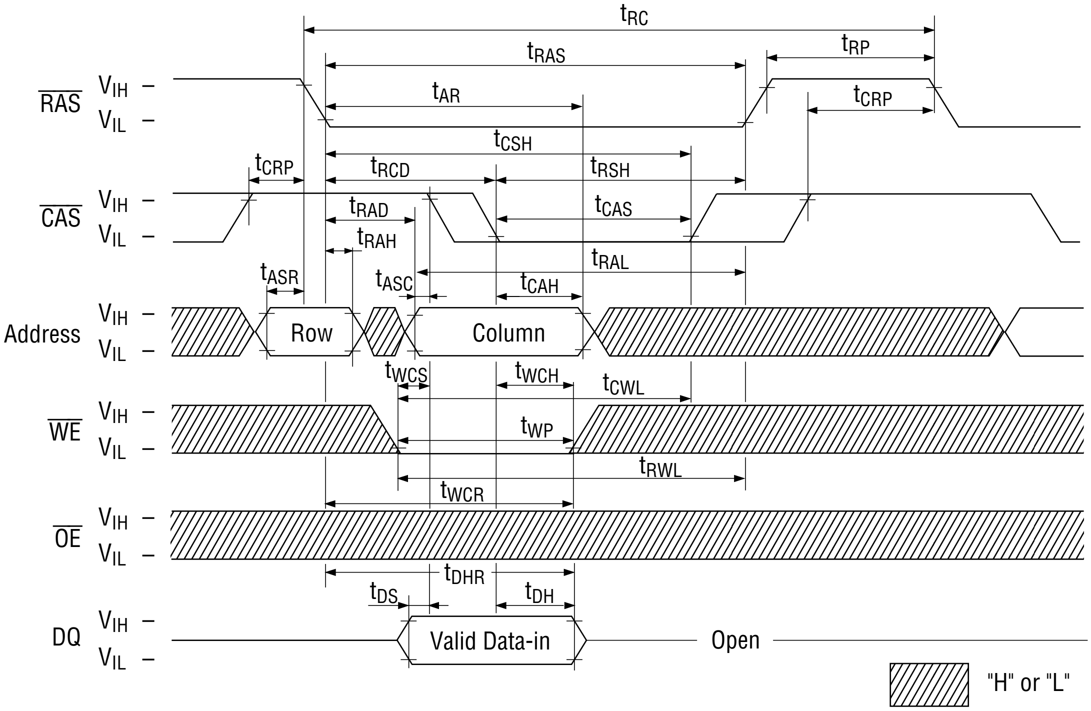
12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycle by adding the above value to the specified value in this data sheet.

TIMING WAVEFORM

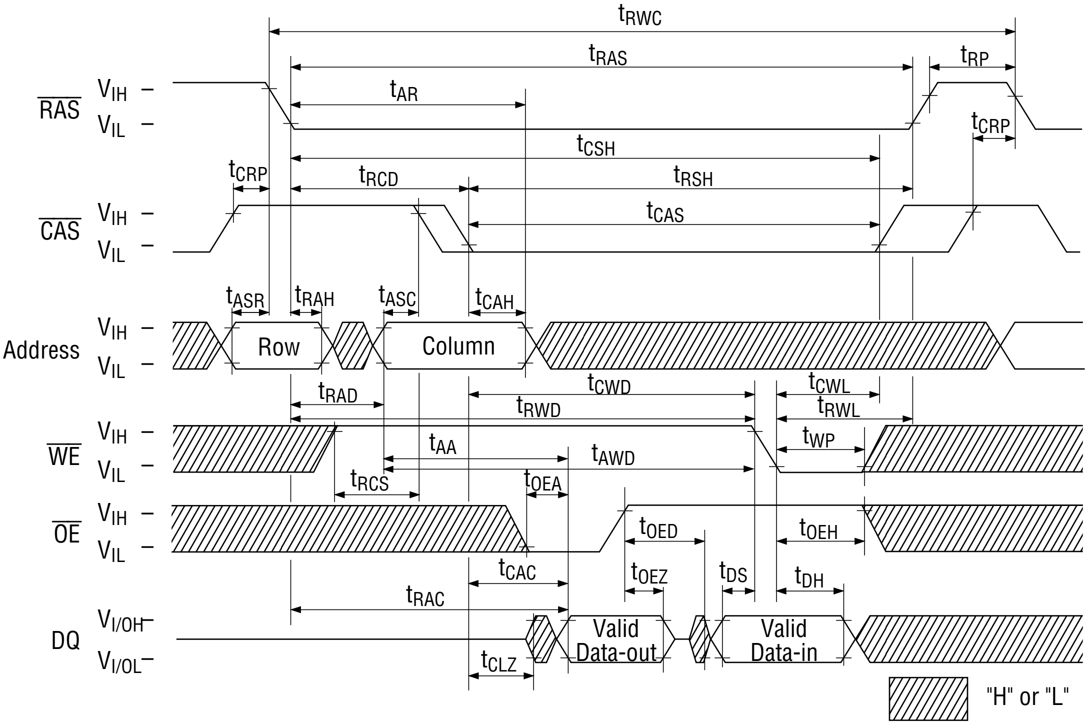
Read Cycle



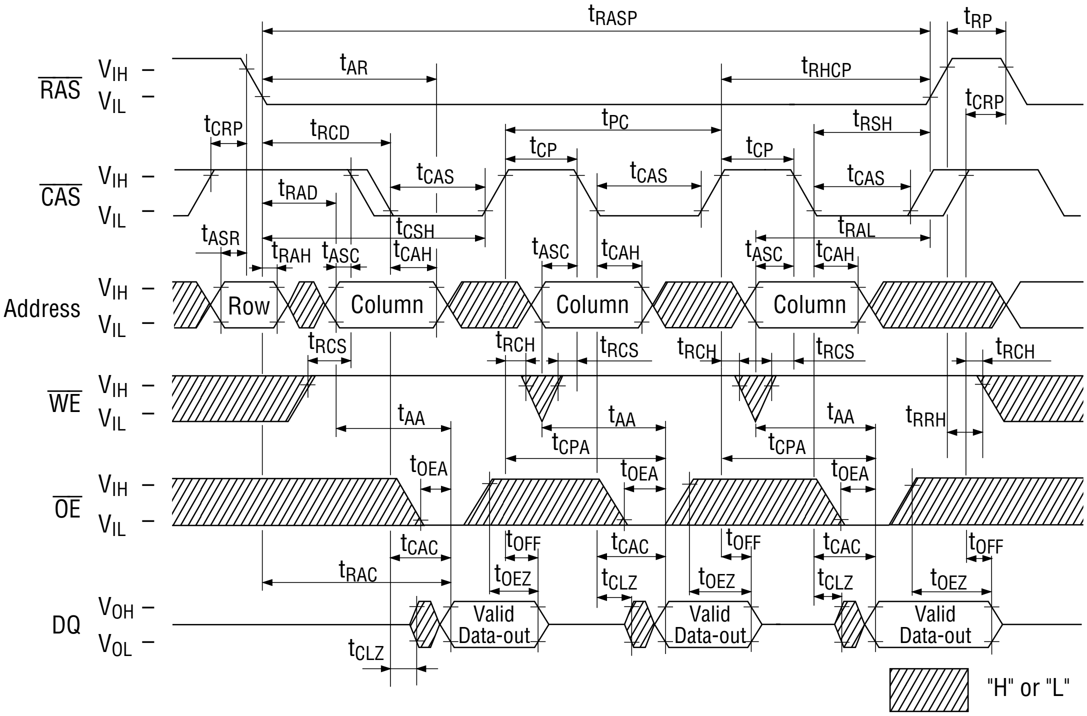
Write Cycle (Early Write)



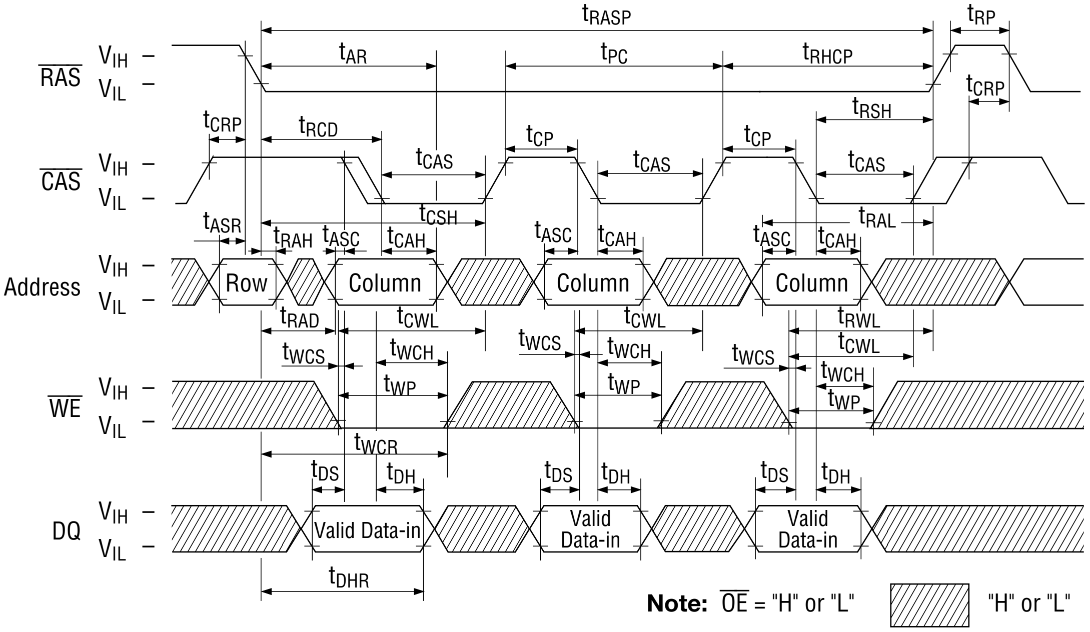
Read Modify Write Cycle



Fast Page Mode Read Cycle

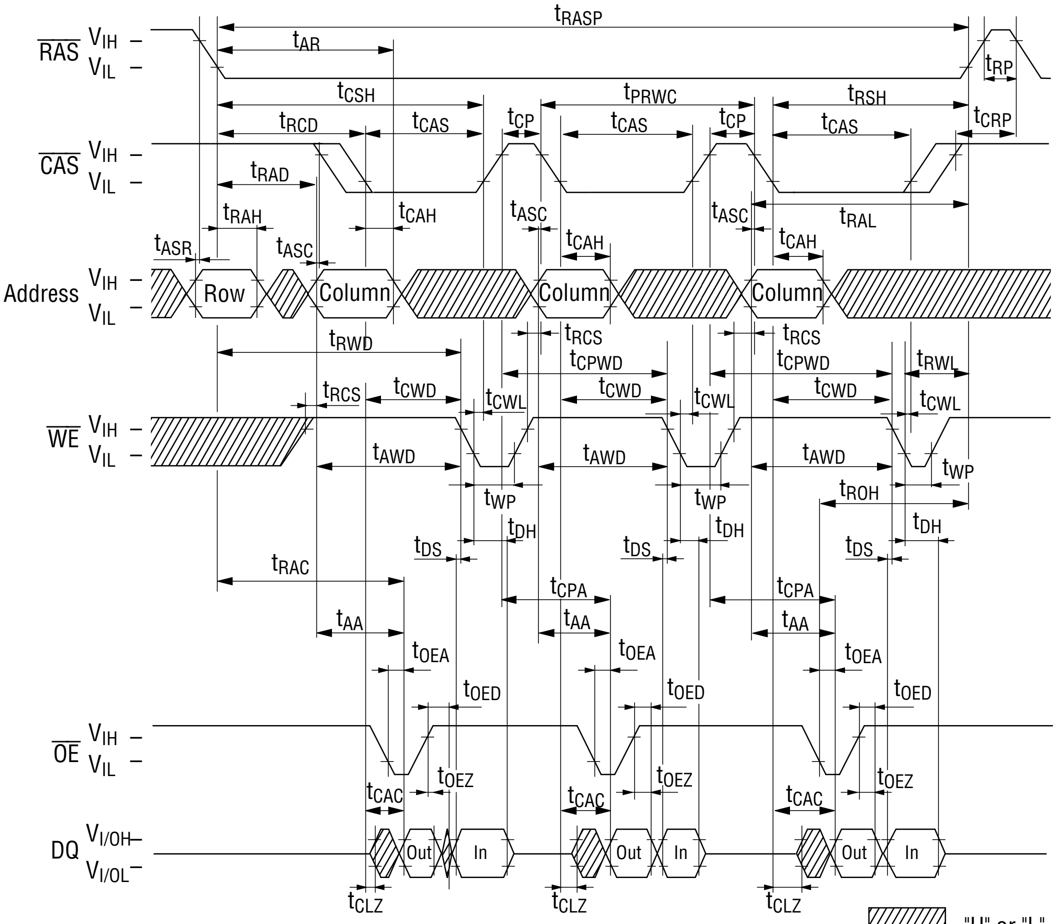


Fast Page Mode Write Cycle (Early Write)



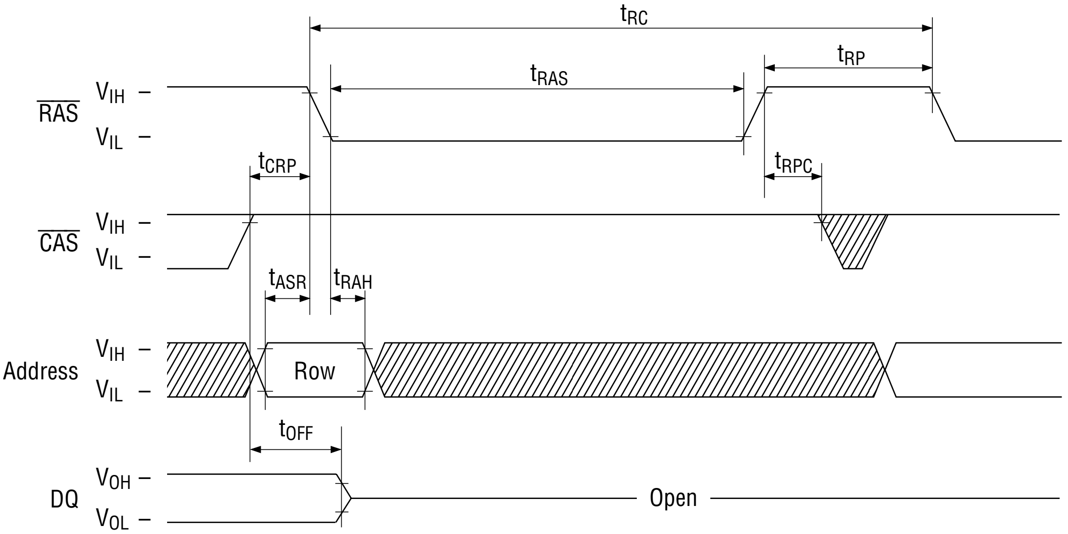
Note: $\overline{OE}$ = "H" or "L"

Fast Page Mode Read Modify Write Cycle



▨ "H" or "L"

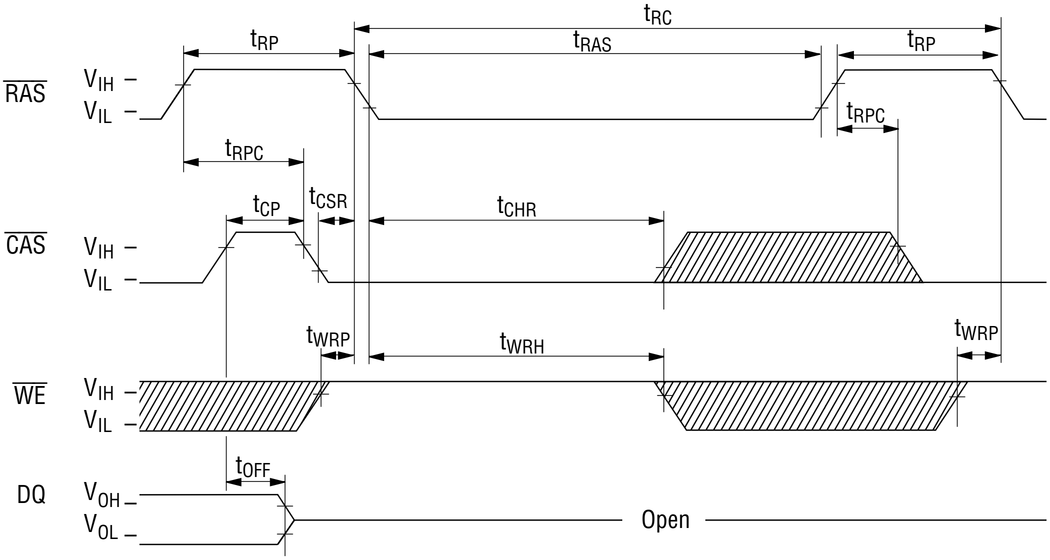
RAS-Only Refresh Cycle



Note: WE, OE = "H" or "L"

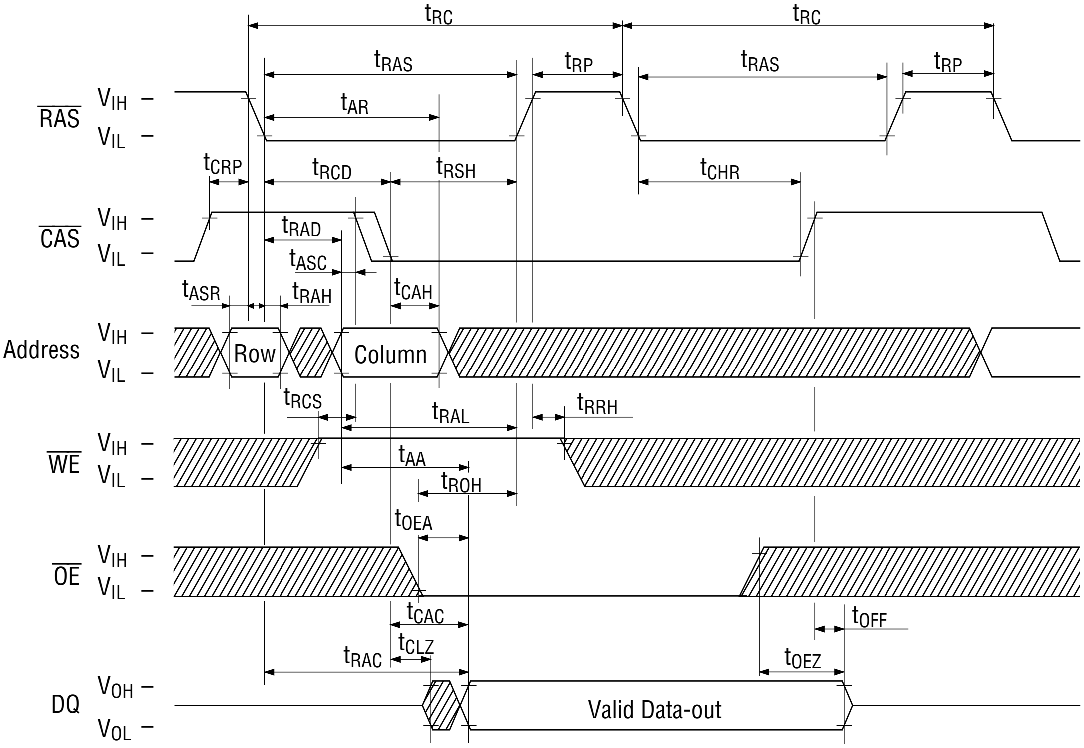
▨ "H" or "L"

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle



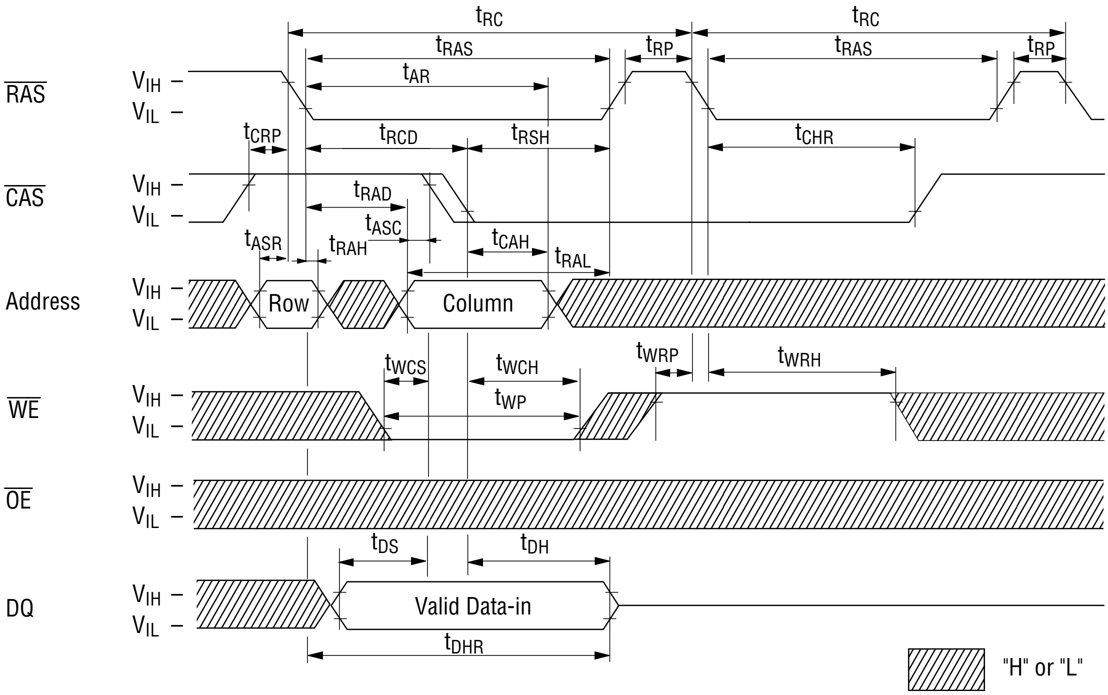
Note: $\overline{\text{OE}}$, Address = "H" or "L" ▨ "H" or "L"

Hidden Refresh Read Cycle

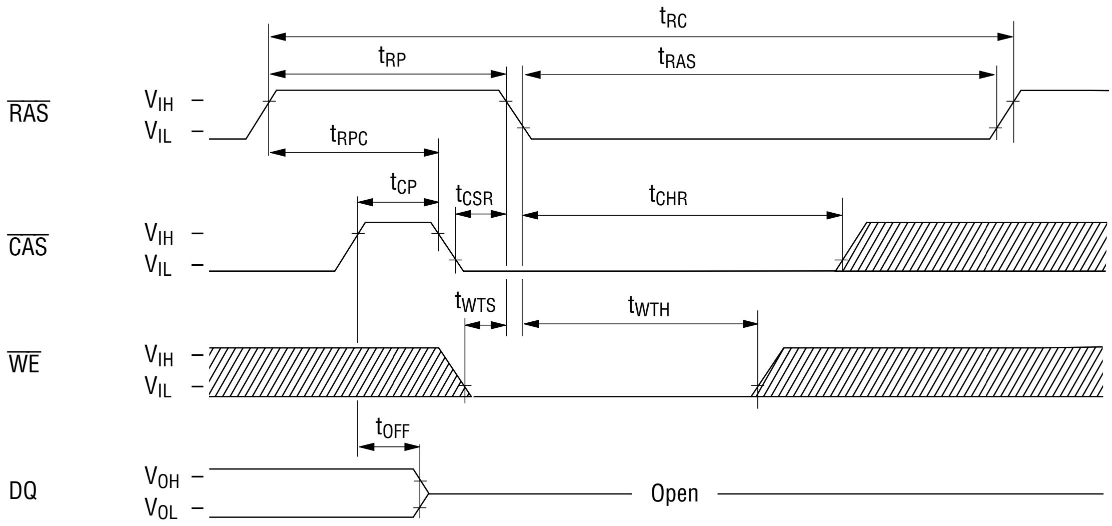


▨ "H" or "L"

Hidden Refresh Write Cycle



Test Mode Initiate Cycle

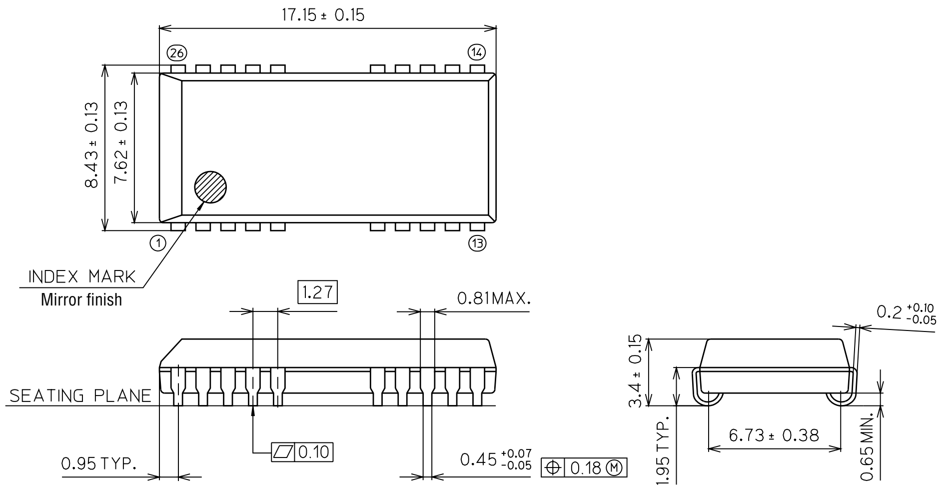


Note: $\overline{OE}$, Address = "H" or "L" ▨ "H" or "L"

PACKAGE DIMENSIONS

(Unit : mm)

SOJ26/20-P-300-1.27



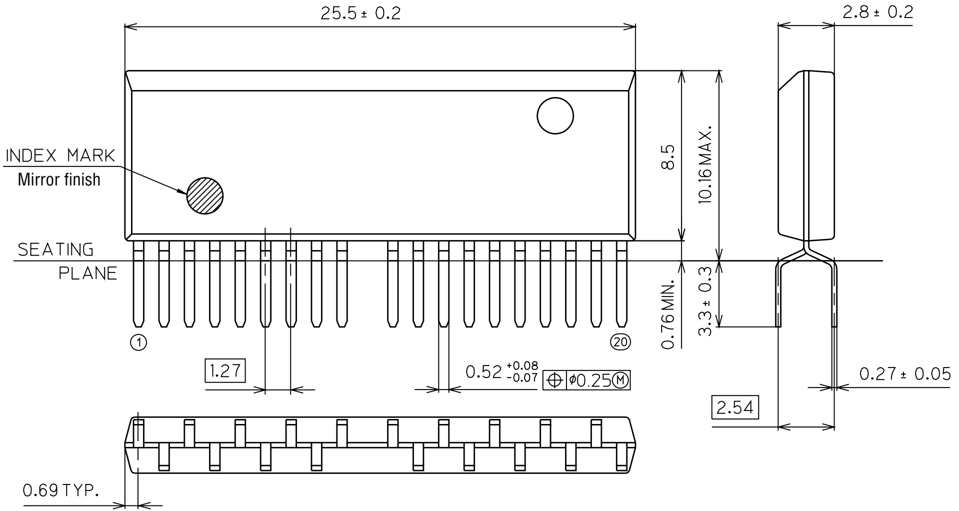
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.80 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

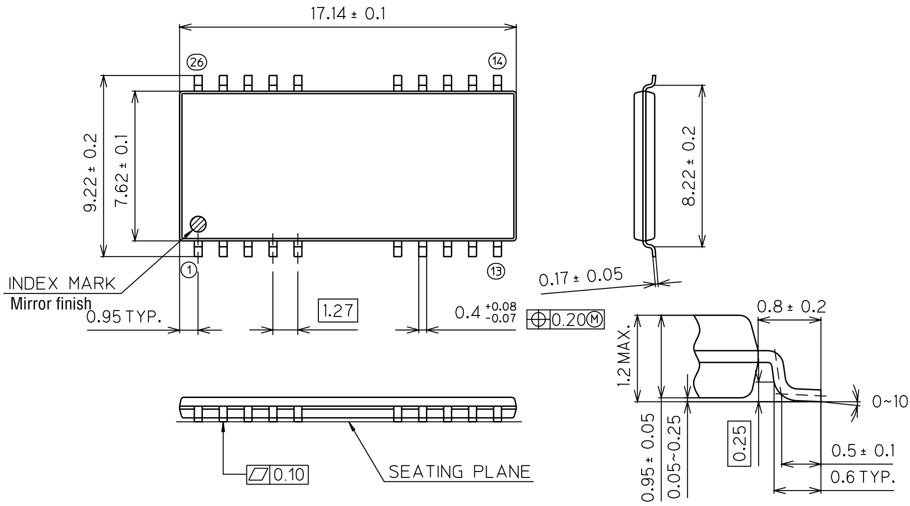
ZIP20-P-400-1.27



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.50 TYP.

(Unit : mm)

TSOPII26/20-P-300-1.27-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 µm or more
Package weight (g)	0.38 TYP.

Notes for Mounting the Surface Mount Type Package

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