



# M5156

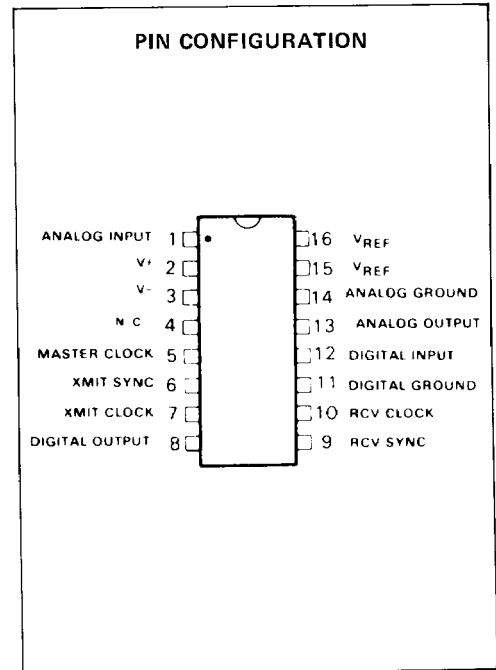
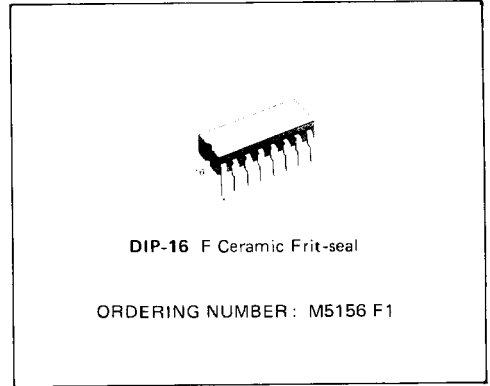
## A-LAW COMPANDING CODEC

- $\pm 5V$  POWER SUPPLY
- LOW POWER DISSIPATION -30mW (TYP.)
- FOLLOWS THE A-LAW COMPANDING CODE
- EXCEEDS CCITT SPECIFICATIONS, INCLUDES EVEN-ORDER-BIT INVERSION
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION
- ON-CHIP SAMPLE AND HOLD
- ON-CHIP OFFSET NULL CIRCUIT ELIMINATES LONG-TERM DRIFT ERRORS AND NEED FOR TRIMMING
- SINGLE 16-PIN PACKAGE
- MINIMAL EXTERNAL CIRCUITRY REQUIRED
- SERIAL DATA OUTPUT OF 64KB/s-2.1 Mb/s AT 8KHz SAMPLING RATE
- SEPARATE ANALOG AND DIGITAL GROUNDING PINS REDUCE SYSTEM NOISE PROBLEMS

### DESCRIPTION

The M5156 is a monolithic CMOS companding CODEC which contains two sections: (1) An analog-to-digital converter which has a transfer characteristics conforming to the A-law companding code and (2) a digital-to-analog converter which also conforms to the A-law code. These two sections form a coder-decoder which is designed to meet the needs of the telecommunications industry for per-channel voice-frequency codecs used in PCM systems. Digital input and output are in serial format. Actual transmission and reception of 8-bit data words containing the analog information is done at a 64Kb/s-2.1Mb/s rate with analog signal sampling occurring at an 8KHz rate.

A sync pulse input is provided for synchronizing transmission and reception of multichannel information being multiplexed over a single transmission line.



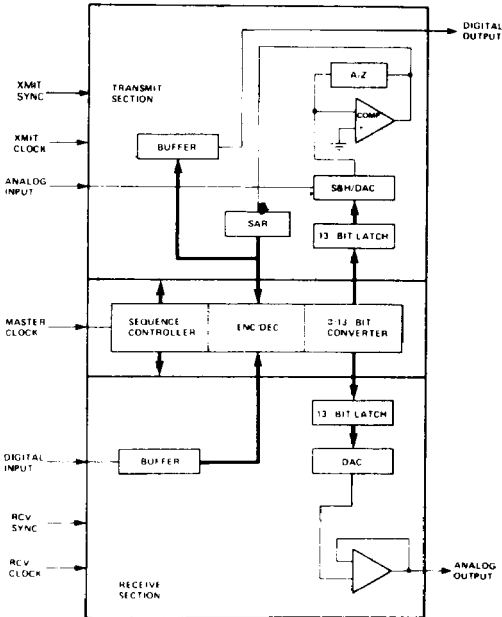
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## ABSOLUTE MAXIMUM RATINGS

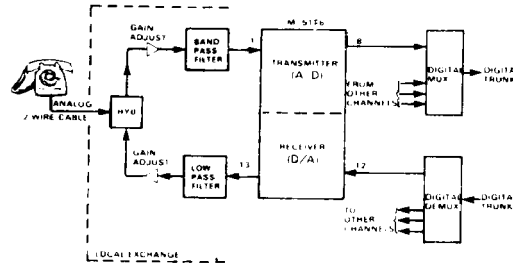
Parameter	Value	Unit
DC Supply Voltage, V+	+ 6	V
DC Supply Voltage, V-	- 6	V
Operating Temperature range	0 to 70	°C
Storage Temperature range	-55 to +125	°C
Package Dissipation at 25°C (Derated 9mW/°C when soldered into PCB)	500	mW
Digital Input	$-0.5 \leq V_{IN} \leq V+$	V
Analog Input	$V- \leq V_{IN} \leq V+$	V
+V <sub>REF</sub>	$-0.5 \leq +V_{REF} \leq V+$	V
-V <sub>REF</sub>	$V- \leq -V_{REF} \leq +0.5$	V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## BLOCK DIAGRAM



## PCM SYSTEM



## POWER SUPPLY REQUIREMENTS

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
V+	Positive Supply Voltage	4.75	5.0	5.25	V	
V-	Negative Supply Voltage	-5.25	-5.0	-4.75	V	
+V <sub>REF</sub>	Positive Reference Voltage	2.375	2.5	2.625	V	1
-V <sub>REF</sub>	Negative Reference Voltage	-2.625	-2.5	-2.375	V	1

DC CHARACTERISTICS (Test conditions: V+ = 5.0V, V- = -5.0V, +V<sub>REF</sub> = 2.5V, -V<sub>REF</sub> = -2.5V)

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
R <sub>INAS</sub>	Analog Input Resistance During Sampling		2		kΩ	2
R <sub>INANS</sub>	Analog Input Resistance Non-Sampling		100		MΩ	
C <sub>INA</sub>	Analog Input Capacitance		150	250	pF	
V <sub>OFFSET/I</sub>	Analog Input Offset Voltage		± 1	± 8	mV	
R <sub>OUTA</sub>	Analog Output Resistance		20	50	Ω	
I <sub>OUTA</sub>	Analog Output Current	0.25	0.5		mA	
(V <sub>OFFSET/O</sub> )	Analog Output Offset Voltage		-200	±850	mV	
I <sub>INLOW</sub>	Logic Input Low Current (V <sub>IN</sub> = 0.8V) Digital Input, Clock Input, Sync Input		± 0.1	± 10	μA	3
I <sub>INHIGH</sub>	Logic Input High Current (V <sub>IN</sub> = 2.4V) Digital Input, Clock Input, Sync Input		-0.25	-0.8	mA	3
C <sub>DO</sub>	Digital Output Capacitance		8	12	pF	
I <sub>DOL</sub>	Digital Output Leakage Current		± 0.1	± 10	μA	
V <sub>OUTLOW</sub>	Digital Output Low Voltage			0.4	V	4
V <sub>OUTHIGH</sub>	Digital Output High Voltage	3.9			V	4
I+	Positive Supply Current		4	10	mA	
I-	Negative Supply Current		2	6	mA	
I <sub>REF+</sub>	Positive Reference Current		4	20	μA	
I <sub>REF-</sub>	Negative Reference Current		4	20	μA	

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## AC CHARACTERISTICS (Refer to Figure 3 and Figure 4)

Parameter		Values			Unit	Note
		Min.	Typ.	Max.		
$F_M$	Master Clock Frequency	1.5	2.048	2.1	MHz	
$F_R, F_X$	XMIT, RCV. Clock Frequency	0.064	2.048	2.1	MHz	
$PW_{CLK}$	Clock Pulse Width (MASTER, XMIT, RCV.)	200			ns	
$t_{RC}, t_{FC}$	Clock Rise, Fall Time (MASTER, XMIT, RCV)			25% of $PW_{CLK}$	ns	
$t_{RS}, t_{FS}$	Sync Rise, Fall Time (XMIT, RCV.)			25% of $PW_{CLK}$	ns	
$t_{DIR}, t_{DIF}$	Data Input Rise, Fall Time			25% of $PW_{CLK}$	ns	
$t_{WSX}, t_{WSR}$	Sync Pulse Width (XMIT, RCV.)		$\frac{8}{F_X(F_R)}$		$\mu s$	
$t_{PS}$	Sync Pulse Period (XMIT, RCV.)		125		$\mu s$	
$t_{XCS}$	XMIT Clock-to-XMIT Sync Delay	50% of $t_{FC}(t_{RS})$			ns	6
$t_{XCSN}$	XMIT Clock-to-XMIT Sync (Negative Edge) Delay		200		ns	
$t_{XSS}$	XMIT Sync Set-Up Time	200			ns	
$t_{XDD}$	XMIT Data Delay	0		200	ns	4
$t_{XDP}$	XMIT Data Present	0		200	ns	4
$t_{XDT}$	XMIT Data Three State			150	ns	4
$t_{DOF}$	Digital Output Fall Time		50		ns	4
$t_{DOR}$	Digital Output Rise Time		50		ns	4
$t_{SRC}$	RCV. Sync-to-RCV. Clock Delay	50% of $t_{RC}(t_{FS})$			ns	6
$t_{RDS}$	RCV. Data Set-Up Time	50			ns	5
$t_{RDH}$	RCV. Data Hold Time	200			ns	5
$t_{RCS}$	RCV. Clock-to-RCV. Sync Delay	200			ns	
$t_{RSS}$	RCV. Sync Set-Up Time	200			ns	5
$t_{SAO}$	RCV. Sync-to-Analog Output Delay		7		$\mu s$	
SLEW+	Analog Output Positive Slew Rate		1		V/ $\mu s$	
SLEW-	Analog Output Negative Slew Rate		1		V/ $\mu s$	
DROOP	Analog Output Droop Rate		25		$\mu V/\mu s$	

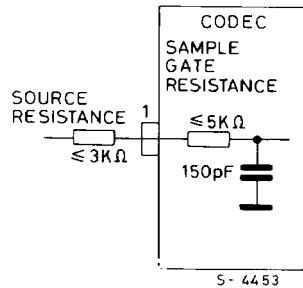
## SYSTEM CHARACTERISTICS (Refer to Figures 10 and 11)

Parameter	Test conditions	Values			Unit	
		Min.	Typ.	Max.		
S/D	Signal-to-Distortion Ratio	Analog Input = 0 to -30 dBmO Analog Input = -40 dBmO Analog Input = -45 dBmO	35 29 24	39 34 29		dB dB dB
GT	Gain Tracking	Analog Input = +3 to -37 dBmO Analog Input = -37 to -50 dBmO Analog Input = -50 to -55 dBmO	-0.4 -0.8 -2.5	± 0.1 ± 0.1 ± 0.2	+0.4 +0.8 +2.5	dB dB dB
N <sub>IC</sub>	Idle Channel Noise	Analog Input = 0 Volts		-80	-72	dBmOp
TLP	Transmission Level Point	600 Ω		+4		dB

### Notes:

1.  $+V_{REF}$  and  $-V_{REF}$  must be matched with in  $\pm 1\%$  in order to meet system requirements.
2. Sampling is accomplished by changing the internal capacitor to within  $\frac{1}{2}$  LSB ( $\leq 300 \mu V$ ) in 20  $\mu s$ . Therefore, the external source resistance must be 3k or less. The equivalent circuit during sampling is shown on the right.
3. The M5156 will source current through an internal 6 k $\Omega$  resistor to help pull up the TTL output. When a transition from a "1" to a "0" takes place, the user must sink the "1" current until reaching the "0" level.
4. Driving one 74L or 74LS TTL load plus 30 pF with  $I_{OH} = -100 \mu A$ ,  $I_{OL} = 500 \mu A$ .
5. The first bit of data is loaded when Sync. and Clock are both "1" during bit time 1 as shown on RCV, timing diagram.
6. This delay is necessary to avoid overlapping Clock and Sync.

## EQUIVALENT INPUT RESISTANCE CIRCUIT DURING SAMPLING



## FUNCTIONAL DESCRIPTION

### Pin 1 – Analog Input

Voice-frequency analog signals which are bandwidth-limited to 4 kHz are input at this pin. Typically, they are then sampled at an 8 kHz rate (Refer to Figure 1). The analog input must remain between  $+V_{REF}$  and  $-V_{REF}$  for accurate conversion.

### Pin 5 – Master Clock

This signal provides the basic timing and control signals required for all internal conversions. It does not have to be synchronized with RCV, SYNC, RCV, CLOCK, XMIT SYNC or XMIT CLOCK and is not internally related to them.

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## FUNCTIONAL DESCRIPTION (continued)

Fig. 1 - A/D, D/A conversion timing

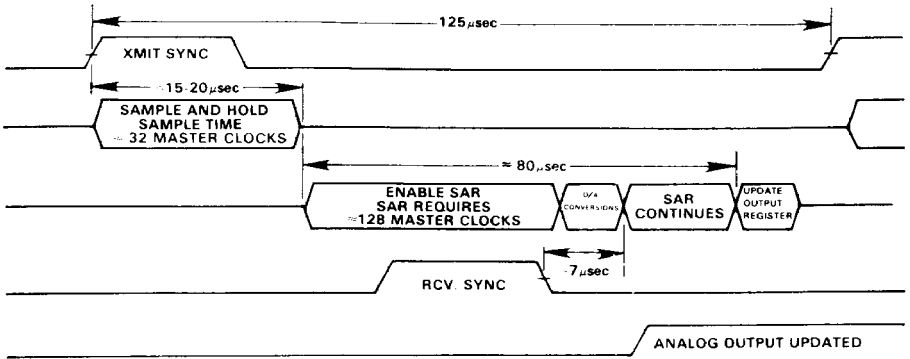
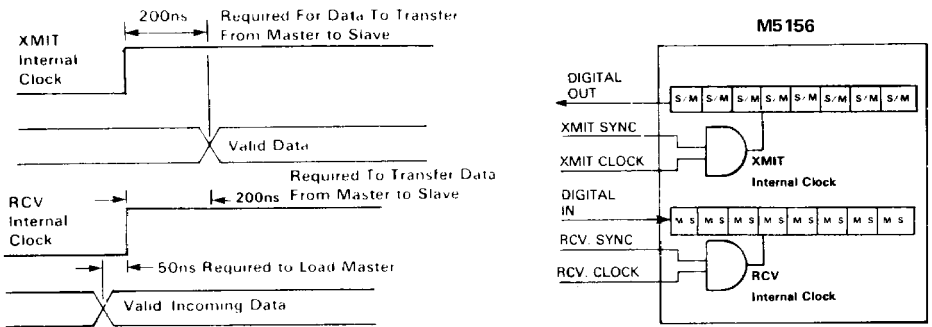


Fig. 2 - Data input/output timing



### Pin 6 - XMIT SYNC (Refer to Figure 3 for the Timing Diagram)

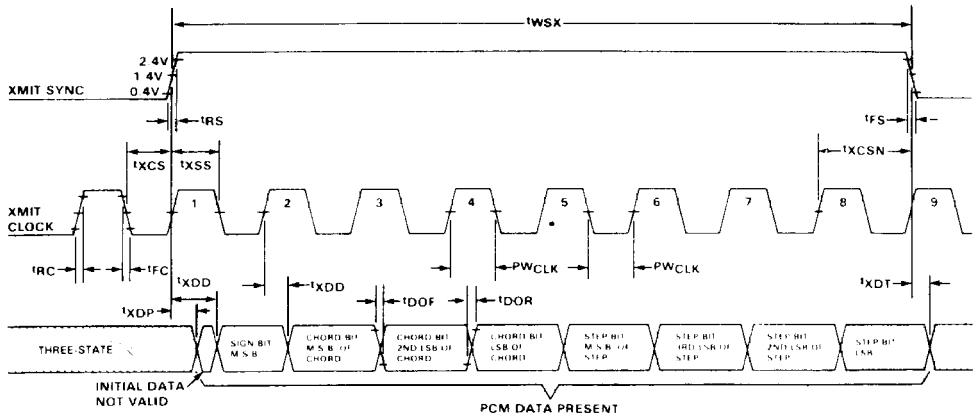
This input is synchronized with XMIT CLOCK. When XMIT SYNC goes high, the digital output is activated and the A/D conversion begins on the next positive edge of MASTER CLOCK. The conversion by MASTER CLOCK can be asynchronous with XMIT CLOCK. The serial output data is clocked out by the positive edges of XMIT CLOCK. The negative edge of XMIT SYNC causes the digital output to become three-state. XMIT SYNC must go low for at least 1 master clock prior to the transmission of the next digital word (Refer to Figure 7).

### Pin 7 - XMIT CLOCK (Refer to Figure 3 for the Timing Diagram)

The on-chip 8-bit output shift register of the M5156 is unloaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for XMIT CLOCK. The positive edge of the INTERNAL CLOCK transfers the data from the master to the slave of a master-slave flip-flop (Refer to Figure 2). If the positive edge of XMIT SYNC occurs after the positive edge of XMIT CLOCK, XMIT SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the hold time for the first clock pulse is measured from the positive edge of XMIT SYNC.

## FUNCTIONAL DESCRIPTION (continued)

Fig. 3 - Transmitter section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

### Pin 9 - RCV. SYNC (Refer to Figure 4 for the Timing Diagram)

This input is synchronized with RCV. CLOCK and serial data is clocked in by RCV. CLOCK. Duration of the RCV. SYNC pulse is approximately 8 RCV. CLOCK periods. The conversion from digital-to-analog starts after the negative edge of the RCV. SYNC pulse (Refer to Figure 1). The negative edge of RCV. SYNC should occur before the 9th positive clock edge to insure that only eight bits are clocked in. RCV. SYNC must stay low for 17 MASTER CLOCKS (min.) before the next digital word is to be received (Refer to Figure 8).

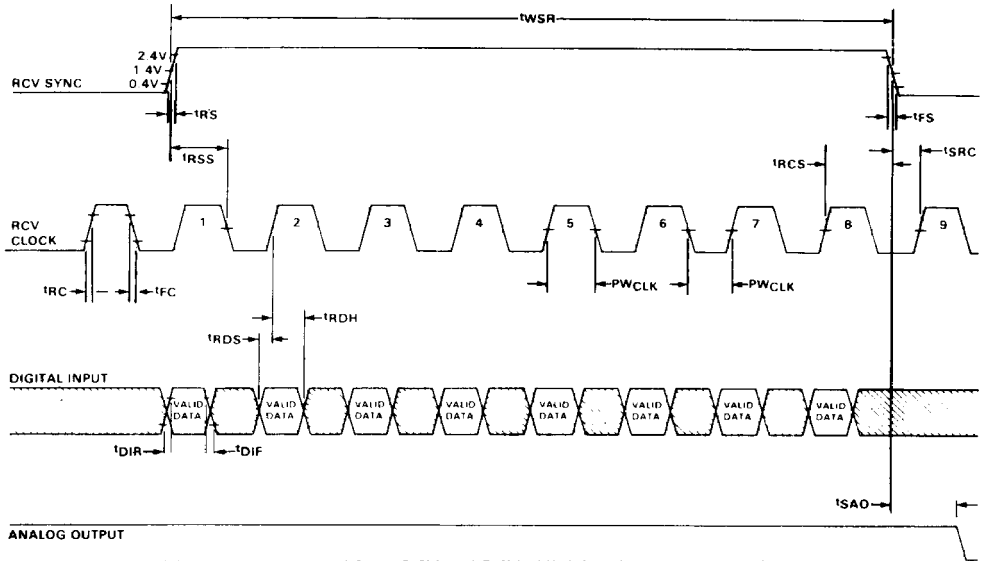
### Pin 10 - RCV. CLOCK (Refer to Figure 4 for the Timing Diagram)

The on-chip 8-bit shift register for the M5156 is loaded at the clock rate present on this pin. Clock rates of 64 kHz - 2.1 MHz can be used for RCV. CLOCK. Valid data should be applied to the digital input before the positive edge of the internal clock (Refer to Figure 2). This set up time,  $t_{RDS}$ , allows the data to be transferred into the MASTER of a master-slave flip-flop. The positive edge of the INTERNAL CLOCK transfers the data to the SLAVE of the master-slave flip-flop. A hold time,  $t_{RDH}$ , is required to complete this transfer. If the rising edge of RCV. SYNC occurs after the first rising edge of RCV. CLOCK, RCV. SYNC will determine when the first positive edge of INTERNAL CLOCK will occur. In this event, the set-up and hold times for the first clock pulse should be measured from the positive edge of RCV. SYNC.

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## FUNCTIONAL DESCRIPTION (continued)

Fig. 4 - Receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 5 - A/D converter (A-Law Encoder) transfer characteristic

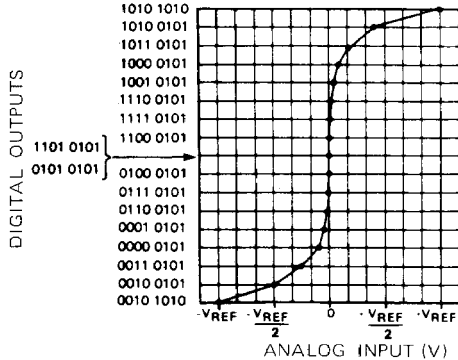
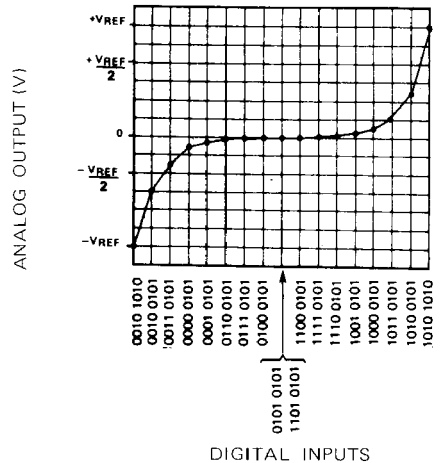


Fig. 6 - D/A converter (A-Law Decoder) transfer characteristic





## FUNCTIONAL DESCRIPTION (continued)

**Table 1 – Digital output code: A Law**

Chord Code	Chord Value	Step Value
1. 101	0.0 mV	1.221 mV
2. 100	20.1 mV	1.221 mV
3. 111	40.3 mV	2.44 mV
4. 110	80.6 mV	4.88 mV
5. 001	161.1 mV	9.77 mV
6. 000	332 mV	19.53 mV
7. 011	645 mV	39.1 mV
8. 010	1.289 V	78.1 mV

**EXAMPLE:**

1            110    0111 = +80.6mV + (2x4.88mV)  
 Sign Bit   Chord   Step Bits

If the sign bit were a zero, then both plus signs would be changed to minus signs.

### Pin 8 – Digital Output

The M5156 output register stores the 8-bit encoded sample of the analog input. This 8-bit word is shifted out under control of XMIT SYNC and XMIT CLOCK. When XMIT SYNC is low, the DIGITAL OUTPUT is an open circuit. When XMIT SYNC is high, the state of the DIGITAL OUTPUT is determined by the value of the output bit in the serial shift register. The output is composed of a Sign Bit, 3 Chord Bits, and 4 Step Bits. The Sign Bit indicates the polarity of the analog input while the Chord and Step Bits indicate the magnitude. In the first two Chords, the Step Bit has a value of 1.2 mV. In the third Chord, the Step Bit has a value of 2.4 mV. This doubling of the step value continues for each of the five successive Chords. Each Chord has a specific value and the Step Bits, 16 in each Chord, specify the displacement from that value (Refer to Table 1). Thus the output, which follows the A-law, has resolution that is proportional to the input level rather than to full scale. This provides the resolution of a 12-bit A/D converter at low input levels and that of a 6-bit converter as the input approaches full scale. The transfer characteristic of the A/D converter (A-law Encoder) is shown in Figure 5.

### Pin 12 – Digital Input

The M5156 input register accepts the 8-bit sample of an analog value and loads it under control of RCV. SYNC and RCV. CLOCK. The timing diagram is shown in Figure 4. When RCV. SYNC goes high, the M5156 uses RCV. CLOCK to clock the serial data into its input register. RCV. SYNC goes low to indicate the end of serial input data. The 8 bits of the input data have the same functions described for the DIGITAL OUTPUT. The transfer characteristic of the D/A converter (A-law Decoder) is shown in Figure 6.

### Pin 13 – Analog Output

The analog output is in the form of voltage steps (100% duty cycle) having amplitude equal to the analog sample which was encoded. This waveform is then filtered with an external low-pass filter with  $\sin x/x$  correction to recreate the sampled voice signal.

### Pins 16 and 15 – Positive and negative reference voltages (+V<sub>REF</sub> and -V<sub>REF</sub>)

These inputs provide the conversion references for the digital-to-analog converters in the M5156. +V<sub>REF</sub> and -V<sub>REF</sub> must maintain 100 ppm/°C regulation over the operating temperature range. Variation of the reference directly affects system gain.

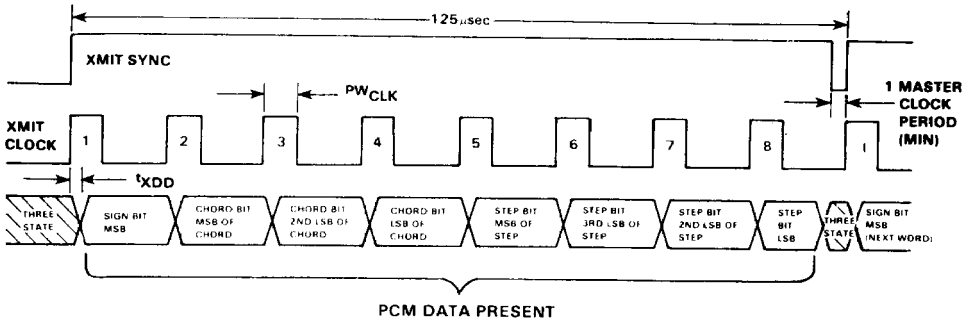
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## OPERATION OF DECODEC WITH 64 kHz XMIT/RCV.

### Clock Frequencies

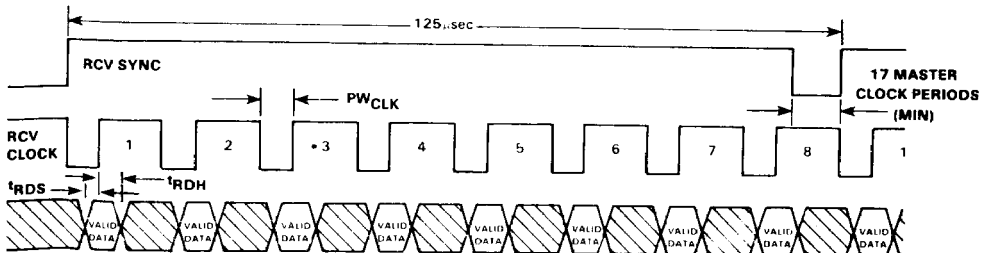
XMIT/RCV. SYNC must not be allowed to remain at a logic "1" state. XMIT SYNC is required to be at a logic "0" state for 1 master clock period (min.) before the next digital word is transmitted. RCV. SYNC is required to be at a logic "0" state for 17 master clock periods (min.) before the next digital word is received (Refer to Figs. 7 and 8).

Fig. 7 - 64 kHz operation, transmitter section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

Fig. 8 - 64 kHz operation, receiver section timing



Note: All rise and fall times are measured from 0.4V and 2.4V. All delay times are measured from 1.4V.

## Offset Null

The offset null feature of the M5156 eliminates long-term drift errors and conversion errors due to temperature changes by going through an offset adjustment cycle before every conversion, thus guaranteeing accurate A/D conversion for inputs near ground. There is no offset adjust of the output amplifier because, since the output is intended to be AC - coupled to the external filter, the resultant DC error ( $V_{\text{OFFSET/O}}$ ) will have no effect. The sign bit is not used to null the analog input. Therefore, for an analog input of 0 volts, the sign bit will be stable.

## Performance Evaluation

The equipment connections shown in Figure 9 can be used to evaluate the performance of the M5156. An analog signal provided by the HP3552A Transmission Test Set is connected to the Analog Input (Pin 1) of the M5156. The Digital Output of the CODEC is tied back to the Digital Input and the Analog Output is fed through a low-pass filter to the HP3552A. Remaining pins of the M5156 are connected as follows:

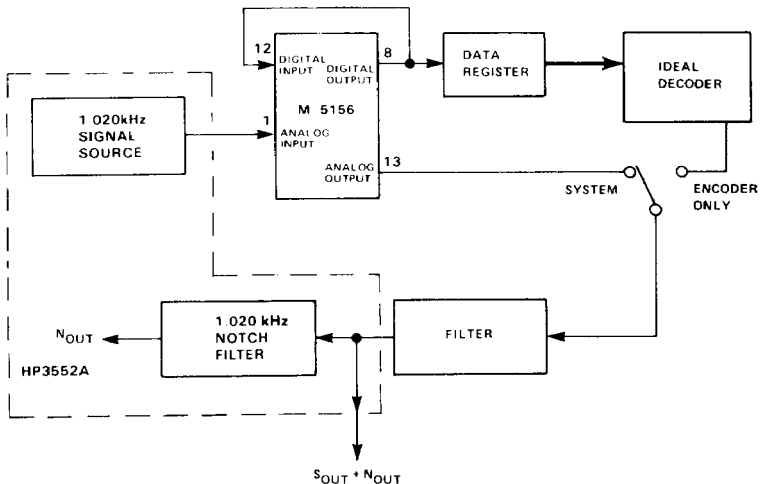
- (1) RCV. SYNC is tied to XMIT SYNC.
  - (2) XMIT CLOCK is tied to MASTER CLOCK. The signal is inverted and tied to RCV. CLOCK.
- The following timing signals are required:

- (1) MASTER CLOCK = 2.048 MHz.
- (2) XMIT SYNC repetition rate = 8 kHz
- (3) XMIT SYNC width = 8 XMIT CLOCK periods.

When all the above requirements are met, the setup of Figure 9 permits the measurement of synchronous system performance over a wide range of analog inputs.

The data register and ideal decoder provide a means of checking the encoder portion of the M5156 independently of the decoder section. To test the system in the asynchronous mode, MASTER CLOCK should be separated from XMIT CLOCK and MASTER CLOCK should be separated from RCV. CLOCK. XMIT CLOCK and RCV. CLOCK are separated also. Some experimental results obtained with the M5156 are shown in Figs. 10 and 11.

Fig. 9 - System characteristics test configuration



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Figure 10

Fig. 10 - S/D ratio vs. input level

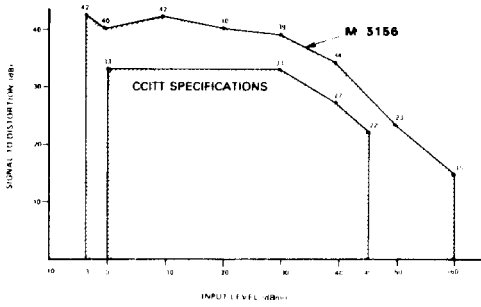


Fig. 11 - Gain tracking performance

