M52025SP

PAL/NTSC VIDEO CHROMA DEFLECTION

DESCRIPTION

The M52025SP is a semiconductor integrated circuit for video, chroma, and deflection signal processing. Combined with IC component M51496P for VIF/SIF, it realizes practical color television using only two IC components.

Circuit configuration includes built-in sync separation, horizontal AFC, horizontal oscillator, horizontal count-down, vertical count-down, contrast control, luminance control, picture quality control, ACC/killer detector, ident detector, APC detector, chroma oscillator, NTSC tint control, and chroma demodulator functions.

FEATURES

- PAL / NTSC / SECAM multi-system processing can be realized by adding IC component M52026SP for processing SECAM chroma signals.
- Large-scale, single-chip construction enhances practicality and reliability of the television set itself while contributing to lower power consumption.
- Places of adjustment and number of external components are minimized.
- NTSC system switch enables construction of a PAL/NTSC system with a minimal amount of peripheral components. (Switches demodulator axis, demodulation ratio, PAL matrix, and tint control.)
- Employs a sync detector system for ACC/killer detector; realizes superior weak electric field killer level.
- Double AFC in the horizontal circuit effectively reduces weak electric field horizontal "jitter," and "bending" on the screen is minimized thanks to luminance alteration. Sync sensor circuit can be used as a sensor signal for sound muting, automatic channel selection, etc.
- Contains built-in service switch. (Contrast minimum killer ON, vertical output OFF)
- No vertical blanking for –Y output

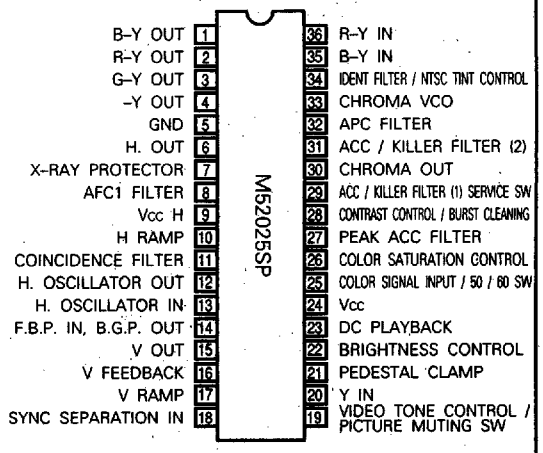
APPLICATION

PAL/SECAM Dual, PAL/NTSC System Color Television Receiver

RECOMMENDED OPERATING CONDITION

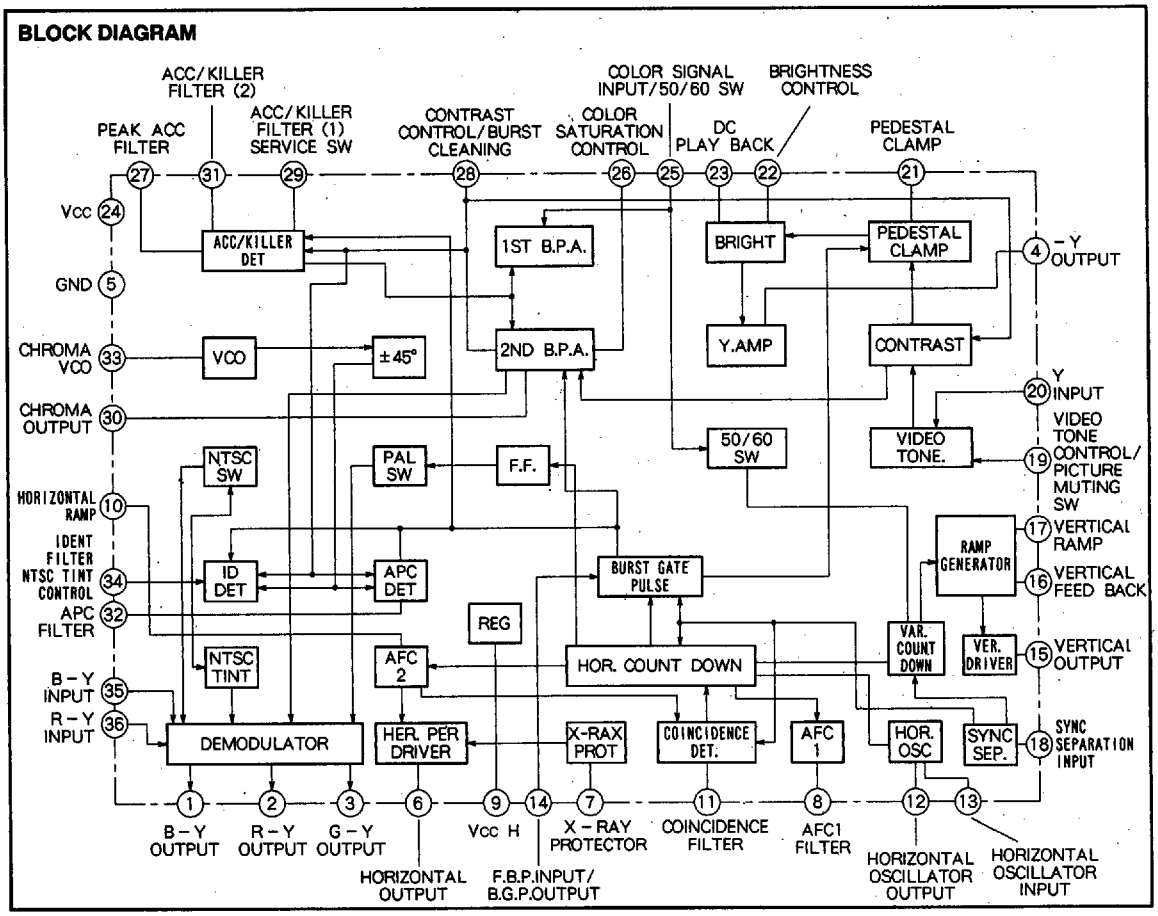
Supply voltage range ..... 10.0~12.5V (Pin ㉔)
Rated supply voltage ..... 11V (Pin ㉔)
Rated supply Current ..... 33mA (Pin ⑨)

PIN CONFIGURATION (TOP VIEW)



Outline 36P4E

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	13.5	V
P_d	Power dissipation	1.25	W
Surge	Surge voltage resistance	± 200	V
V_{16}	Pin ⑯ voltage	0.28Vcc + 6	V
I_{17}	Pin ⑰ input current	+ 6	mA
I_{14}	Pin ⑭ input current	− 1.0	mA
T_{opr}	Operating temperature	− 20~65	℃
T_{stg}	Storage temperature	− 40~125	℃

ELECTRICAL CHARACTERISTICS (Ta = 25°C, unless otherwise noted)

VIDEO SECTION

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Icc – YC	Circuit current		46	60	74	mA
Ymax	Maximum output		6.9	8.0		V_{P-P}
GY	Video amplifier gain		18	21	24	dB
GYmid	Contrast control characteristics – 1		0.65	0.95	1.35	V_{P-P}
GYmin	Contrast control characteristics – 2			– 39	– 29	dB
GYmax	Contrast control characteristics – 3		4.3	7.3	10.3	dB
YTmid	Video tone control characteristics-1		0.95	1.35	1.85	V_{P-P}
YTmin	Video tone control characteristics-2		– 11	– 8	– 5	dB
YTmax	Video tone control characteristics-3		1.6	4.6	7.6	dB
Y_{BRTmid}	Brightness control characteristics-1		3.4	4.0	4.6	V
Y_{BRTmin}	Brightness control characteristics-2		7.4	8.0	8.6	V
Y_{BRTmax}	Brightness control characteristics-3			0.8	1.4	V
Yf	Frequency characteristics		– 2	2	6	dB
H.BLKTH	Horizontal blanking threshold voltage		8.9	9.5	10.1	V

CHROMA SECTION

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Cmax	Maximum output		1.6	2.2	2.8	V_{P-P}
GC	Chroma maximum gain		35	40	45	dB
Acc1	ACC characteristics – 1		– 8	– 2.5	0	dB
Acc2	ACC characteristics – 2		– 2	0.4	3	dB
KIL	Killer operation input		– 34	– 28	– 22	dB
D.KIL	Killer color residual				200	mV_{P-P}
CCmid	Color control characteristics – 1		0.65	0.95	1.35	V_{P-P}
CCmin	Color control characteristics – 2			– 40	– 36	dB
CCmax	Color control characteristics – 3		5	9	13	dB
UCmid	Color tracking characteristics – 1		0.45	1.1	1.75	V_{P-P}
UCmin	Color tracking characteristics – 2			– 40	– 36	dB
UCmax	Color tracking characteristics – 3		1	5	8	dB
APC1	APC pull – in range – 1		500	900		Hz
APC2	APC pull – in range – 2		870	1500		Hz
Doc	Demodulated output DC voltage		5.9	6.4	6.9	V
Doffset	Demodulated output DC offset				0.3	V
Dmax	Demodulated output maximum amplitude		5.5	6.5	7.5	V_{P-P}
D_{B-Y}	B – Y demodulated sensitivity		2.5	3.0	3.5	V_{P-P}
R/B	Demodulation ratio – 1		0.53	0.60	0.67	–
G/B	Demodulation ratio – 2		0.30	0.36	0.42	–
V_{23}	Pin ㉓ voltage (killer ON)			0.13	1.00	V
NTSC B	Demodulated output (NTSC)		2.25	3.25	4.55	V_{P-P}
NTSC R/B	Demodulation ratio – 1 (NTSC)		0.60	0.70	0.80	–
NTSC G/B	Demodulation ratio – 2 (NTSC)		0.20	0.31	0.36	–
DBW	Demodulated output bandwidth		0.8	1.0		MHz
CD	Chroma input dynamic range		1.0	1.4		V_{P-P}
∠R-Y-P	PAL demodulated phase angle			90		deg.
∠R-Y-N	NTSC demodulated phase angle			100		deg.
Tmin	NTSC TINT		27	– 47	67	deg.
Tmax			20	+ 40	60	deg.

DEFLECTION SECTION

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC-D}	Circuit current		26	35	44	mA
V_{smin}	Horizontal oscillator starting voltage			6	7.2	V
f_H	Horizontal free run frequency		15.45	15.625	15.8	kHz
f_{PH1L}	Horizontal pull – in range – 1			– 970	– 600	Hz
f_{PH1H}			+ 550	+ 900		Hz
V_{9H}	Coincidence detection maximum voltage		8.5	9.1		V
V_{9L}	Coincidence detection minimum voltage				0.5	V
τ_H	Horizontal output pulse amplitude		22	25	28	μ sec
VHmin	Horizontal output voltage			0.04	0.16	V
VHmax			3.1	3.9	4.8	V
t_{GP}	Burst gate pulse position		4.1	5.0	5.9	μ sec
f_{V50}	Vertical free run frequency 50 (Hz)		45.6	47	48.6	Hz
f_{V60}	Vertical free run frequency 60 (Hz)		52.7	55	57.2	Hz
f_{PV50}	Vertical pull – in range 50 (Hz)		54	55.7	58	Hz
f_{PV60}	Vertical pull – in range 60 (Hz)		65	66.3	69	Hz
τ_{V50}	Vertical output pulse amplitude 50 (Hz)		474	544	614	μ sec
τ_{V60}	Vertical output pulse amplitude 60 (Hz)		474	544	614	μ sec
Vvmax	Vertical output maximum voltage		3.2	4.2		V_{O-P}
Vvmin	Vertical output minimum voltage				0.3	V
PRamp	Ramp peak voltage		5.6	6.05	6.5	V
VRamp	Ramp amplitude		1.5	1.8	2.1	V_{P-P}
G_{VV}	Vertical open loop gain		16	20	24	dB
I_{SS}	Sync separation input sensitivity current		0.07	0.1	0.15	mA
T_{BGP1}	Burst gate pulse timing – 1		0.35	0.5	0.7	μ sec
T_{BGP2}	Burst gate pulse timing – 2		3.2	3.6	4.1	μ sec
V_{FBP}	Flyback pulse clamp voltage		4.3	4.8	5.3	V
V_{BGP}	Burst gate pulse voltage		9.5	10.0	10.5	V

ELECTRICAL CHARACTERISTICS TEST METHOD

GY Video Amplifier Gain

1. Test –Y output amplitude and make VC0 the testing value.
2. $GY = 20 \times \log \frac{V_{C0}\ (mV_{PP})}{200\ (mV_{PP})}$ (dB)

GYmid Contrast Control Characteristics–1

1. GYmid = Y_{C0} (V_{PP})

GYmin Contrast Control Characteristics–2

1. Test –Y output amplitude and make V_{C1} the testing value.
2. $GYmin = 20 \times \log \frac{V_{C1}}{V_{C0}}$ (dB)

GYmax Contrast Control Characteristics–3

1. Test –Y output amplitude and make V_{C2} the testing value.
2. $GYmax = 20 \times \log \frac{V_{C2}}{V_{C0}}$ (dB)

YTmid Video Tone Control Characteristics-1

1. Test –Y output amplitude and make V_{T0} the testing value.
2. YTmid = V_{T0} (V_{PP})

YTmid Video Tone Control Characteristics-2

1. Test –Y output amplitude and make V_{T1} the testing value.
2. $YTmin = 20 \times \log \frac{V_{T1}}{V_{T0}}$ (dB)

YTmax Video Tone Control Characteristics-3

1. Test –Y output amplitude and make V_{T2} the testing value.
2. $YTmax = 20 \times \log \frac{V_{T2}}{V_{T0}}$ (dB)

Y_{BRT}mid Brightness Control Characteristics–1

1. Test –Y output DC voltage.

Y_{BRT}min Brightness Control Characteristics–2

1. Same as Y9.

Y_{BRT}max Brightness Control Characteristics–3

1. Same as Y9.

Y_f Frequency Characteristics

1. Test –Y output amplitude.
2. Make V_{f1} the amplitude when SG2 is input.
3. Make V_{f2} the amplitude when SG4 is input.
4. $Y_f = 20 \times \log \frac{V_{f2}}{V_{f1}}$ (dB)

DG Differential Gain

1. Test –Y output DC voltage.
2. Make VG1 the amplitude when ㉑ is set to 2.4V.
3. Make VG2 the amplitude when ㉑ is set to 1.8V.
4. $DG = \frac{|V_{G1} - V_{G2}|}{V_{G2}} \times 100$ (%)

H. BLK TH Horizontal Blanking Threshold Voltage

1. Apply voltage to pin ④ and increase from 8V.
2. Test the voltage of pin ④ when signal ceases to be output by ⑯.

GC Chroma Maximum Gain

1. Test output amplitude (P–P) and make V_{GC} the testing value.
2. $GC = 20 \times \log \frac{V_{GC}\ (mV_{PP})}{\text{Input Amplitude } (\fallingdotseq 7.94mV_{PP})}$ (dB)

ACC 1 ACC Characteristics–1

1. Test output amplitude (P-P).
2. Make V_{A0} the testing value when SG5 0dB is input.
3. Make V_{A1} the testing value when SG5 –22dB is input.
4. $ACC\ 1 = 20 \times \log \frac{V_{A1}}{V_{A0}}$ (dB)

ACC 2 ACC Characteristics–2

1. In the same manner as in C3, make V_{A2} the testing value when SG5 +6dB is input.
2. $ACC\ 2 = 20 \times \log \frac{V_{A2}}{V_{A0}}$ (dB)

KIL Killer Operation Input

1. Gradually attenuate the level of SG5.
2. While monitoring DC voltage of pin ⑱, input level of SG5 when voltage becomes less than 1V.

D. KIL Killer Color Residual

1. Test output amplitude within 1H interval.

CCmid Color Control Characteristics–1

1. Test output amplitude (P–P) and make V_{C10} the testing value.
2. CCmid = V_{C10} (V_{PP})

CCmin Color Control Characteristics–2

1. Test output amplitude (P–P) and make V_{C11} the testing value.
2. $CCmin = 20 \times \log \frac{V_{C11}}{V_{C10}}$ (dB)

CCmax Color Control Characteristics–3

1. Test output amplitude (P–P) and make V_{C12} the testing value.
2. $CCmax = 20 \times \log \frac{V_{C12}}{V_{C10}}$ (dB)

UCmid Color Tracking Characteristics–1

1. Test output amplitude (P–P) and make V_{U0} the testing value.
2. UCmid = V_{U0} (V_{PP})

UCmin Color Tracking Characteristics–2

1. Test output amplitude (P–P) and make V_{U1} the testing value.
2. $UCmin = 20 \times \log \frac{V_{U1}}{V_{U0}}$ (dB)

UCmax Color Tracking Characteristics–3

1. Test output amplitude (P–P) and make V_{U2} the testing value.
2. $UCmax = 20 \times \log \frac{V_{U2}}{V_{U0}}$ (dB)

APC 1 APC Pull-In Range–1

1. Set so that the frequency of SG6 is less than 4.433MHz and pin ㉖ is Lo.
2. Gradually increase the frequency of SG6.
3. Test the frequency when the voltage of pin ㉖ changes from Lo to Hi and make F_{AU} the testing value.
4. APC 1 = 4433619 (Hz) – F_{AU} (Hz)

APC 2 APC Pull-In Range–2

1. Set so that the frequency of SG6 is more than 4.434MHz and pin ㉖ is Lo.
2. Gradually decrease the frequency of SG6.
3. Test the frequency when the voltage of pin ㉖ changes from Lo to Hi and make F_{Ad} the testing value.
4. APC 2 = F_{Ad} (Hz) – 4433619 (Hz)

D_{DC} Demodulated Output DC Voltage

1. Test DC voltage at ①Ⓐ, ②Ⓐ and ③Ⓐ.

Dffset Demodulated Output DC Offset

1. Calculate each voltage difference of, ①Ⓐ②Ⓐ, ②Ⓐ③Ⓐ and ③Ⓐ①Ⓐ from the testing value of C15.

R/B Demodulation Ratio–1

1. Test output amplitude and make $D_{R\text{-}Y}$ the testing value.
2. $R/B = \frac{D_{R\text{-}Y}}{D_{B\text{-}Y}\text{ (Testing Value at C18)}}$

G/B Demodulation Ratio–2

1. Test output amplitude and make $D_{G\text{-}Y}$ the testing value.
2. $G/B = \frac{D_{G\text{-}Y}}{D_{B\text{-}Y}\text{ (Testing Value at C18)}}$

ΔD/H Demodulated Output 1H Level Difference

1. Test both AC, DC for each 1H level difference.

C leak Demodulated Output Carrier Leak

1. Test output carrier element for 1A, 2A, and 3A.

V_{NTSC} NTSC Operation Control Voltage

1. Gradually decrease voltage of 34A from the area of 8V.
2. Test the 34A voltage when signal ceases to be output by 1A.

NTSC R/B Demodulation Ratio (NTSC)–1

1. Test output amplitude and make $NTSC_R$ the testing value.
2. NTSC $R/B = \frac{NTSC_R}{NTSC_B\text{ (Testing Value at C25)}}$

NTSC G/B Demodulation Ratio (NTSC)–2

1. Test output amplitude and make $NTSC_G$ the testing value.
2. NTSC $G/B = \frac{NTSC_G}{NTSC_B\text{ (Testing Value at C25)}}$

V P/N PAL/NTSC Demodulated Output DC Voltage Difference

1. Test the difference in DC voltage when S34 is ON and when it is OFF.

SS Service Switch Operation

1. No output signal from ④
2. No vertical sync pulse from ⑮
3. Voltage of ㉖ drops below 1V.
4. Check 1, 2 and 3.

D_{BW} Demodulated Output Bandwidth

1. Set frequency of SG8 to 4.5MHz, and test output amplitude of ①, ② and ③.
2. Gradually increase the frequency of SG8.
3. Test output frequency of ①, ② and ③ when output amplitude is 3dB less than when 4.5MHz is input.

CD Chroma Input Dynamic Range

1. Increase the level of SG5 and test the input amplitude when output becomes distorted.

∠R–Y–P, ∠G–Y–P PAL Demodulated Phase Angle

1. Make ∠R–Y–P the phase difference of ①Ⓐ ②Ⓐ.
2. Make ∠G–Y–P the phase difference of ①Ⓐ ③Ⓐ.

∠R–Y–N, ∠G–Y–N NTSC Demodulated Phase Angle

1. Make ∠R–Y–N the phase difference of ①Ⓐ ②Ⓐ.
2. Make ∠G–Y–N the phase difference of ①Ⓐ ③Ⓐ.

Tmin, Tmax NTSC Tint

1. Set oscilloscope to X–Y. Connect ①Ⓐ to X and ②Ⓐ to Y.
2. Open ㉞ and set SG6 frequency to 4.433619MHz.
3. At this time the oscilloscope waveform is shown as 180°.
4. Make Tmin the remainder of subtracting 180° from the angle when ㉞ was set to 4V.
5. Make Tmax the remainder of subtracting 180° from the angle when ㉞ was set to 1V.

Horizontal Oscillator Starting Voltage

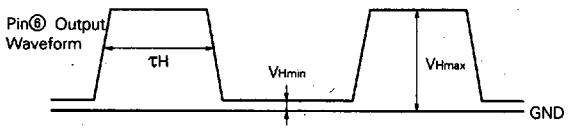
1. Increase ㉜ from 0V.
2. Test ㉜ voltage where the output waveform cycle of ⑥ is approx. 64μs.

f_{PH1L}, f_{PH1H} Horizontal Pull-In Range–1

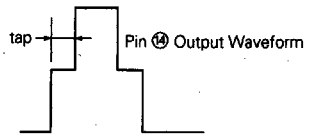
1. Decrease the frequency of input signal so that the SGb input signal and pin ⑥ output waveform are not synchronized.
2. Increase the frequency of SGb.
3. Test the SGb frequency when SGb and pin ⑥ output waveform become synchronized and make f_{L1} the testing value.

4. $f_{PH1L} = f_{L1} - f_H$ (Testing Value at J3)
5. Test the upper side pull-in in the same manner and make f_{H1} the SGb frequency when the two become synchronized.
6. $f_{PH1H} = f_{H1} - f_H$ (Testing Value at J3)

τ_H Horizontal Output Pulse Amplitude
V_{Hmin}, V_{Hmax} Horizontal Output Voltage



t_{GP} Burst Gate Pulse Position



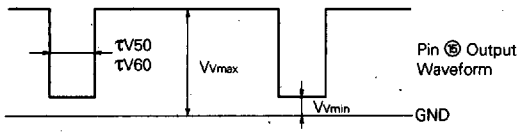
f_{PV} 50 Vertical Pull-In Range 50 (Hz)

1. Increase the frequency of input signal so that the SGc input signal and pin ⑮ output waveform are not synchronized.
2. Decrease the frequency of SGc and test the SGc frequency when SGc and the output waveform of pin ⑮ become synchronized.

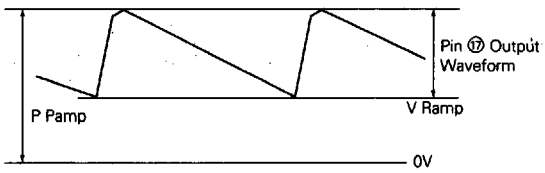
f_{PV} 60 Vertical Pull-In Range 60 (Hz)

1. Same as J12.

τ_{V50} Vertical Output Pulse Amplitude 50 (Hz)
τ_{V60} Vertical Output Pulse Amplitude 60 (Hz)
Vvmax Vertical Output Maximum Voltage
Vvmin Vertical Output Minimum Voltage



P Ramp Ramp Peak Voltage
V Ramp Ramp Amplitude



Gvv Vertical Open Loop Gain

1. Test the output amplitude of pin ⑮ and make Vvo the testing value.
2. $Gvv = 20 \times \log \frac{Vvo\ (mV_{PP})}{\text{Input Amplitude } (=50mV_{PP})}$ (dB)

Iss Sync Separation Input Sensitivity Current

1. Increase Is from 0 mA.
2. Test Is when burst gate pulse ceases to be output by ⑭.

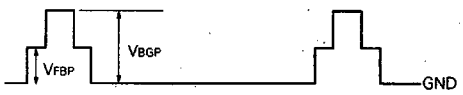
T_{BGP} 1 Burst Gate Pulse Timing–1

1. Test the time from SGa rise to burst gate pulse rise.

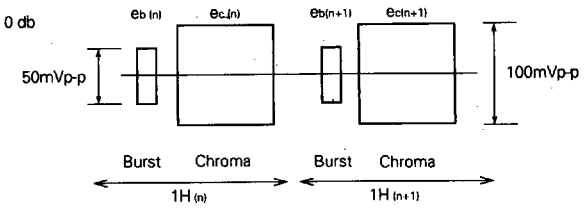
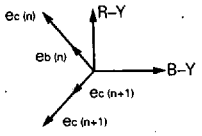
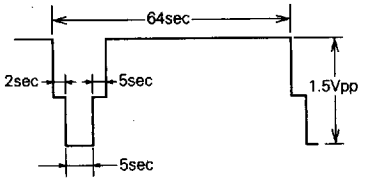
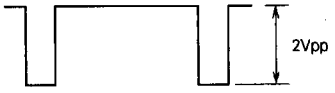
T_{BGP} 2 Burst Gate Pulse Timing–2

1. Test burst gate pulse amplitude.

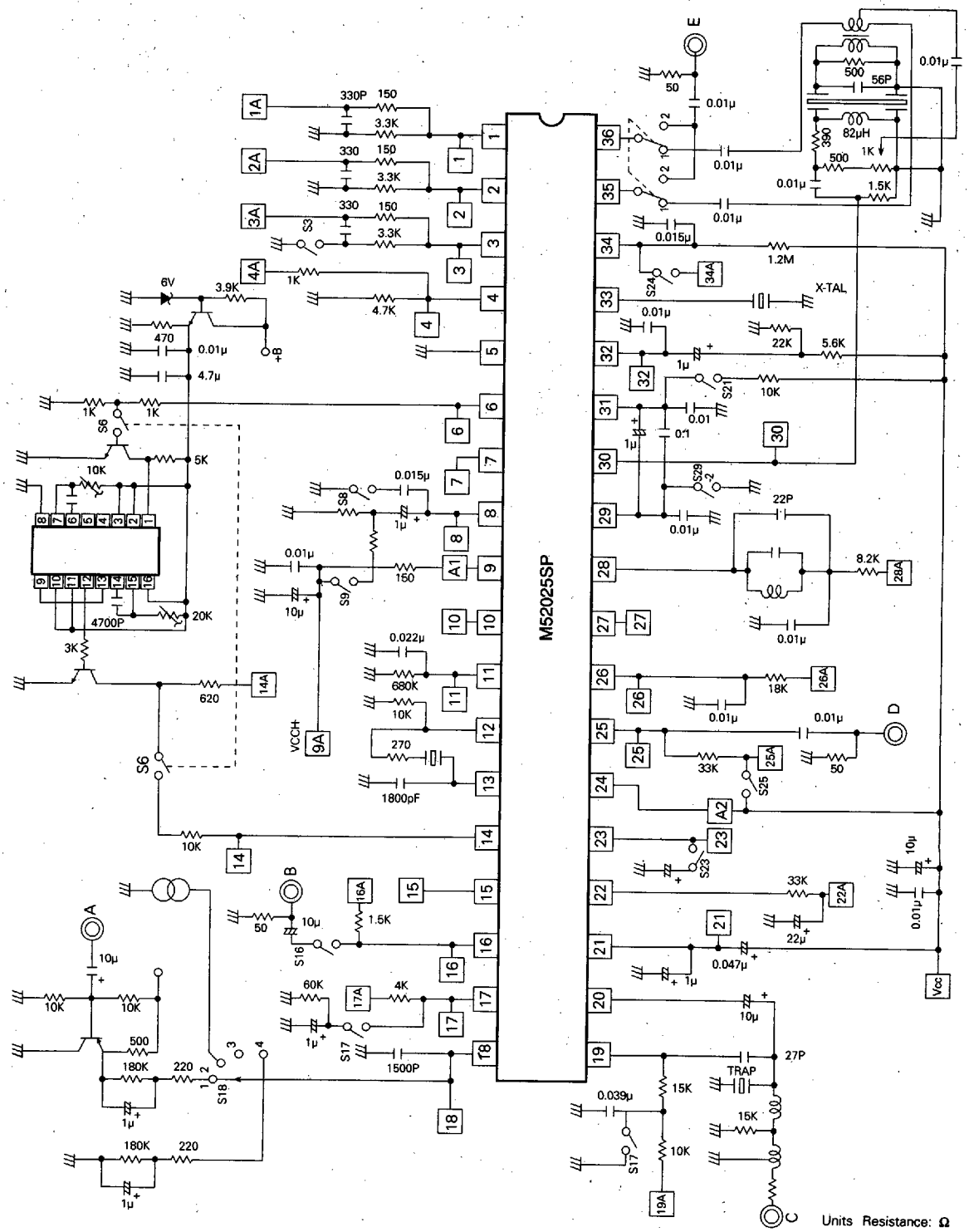
V_{FBR} Flyback Pulse Clamp Voltage
V_{BGP} Burst Gate Pulse Voltage



INPUT SIGNAL

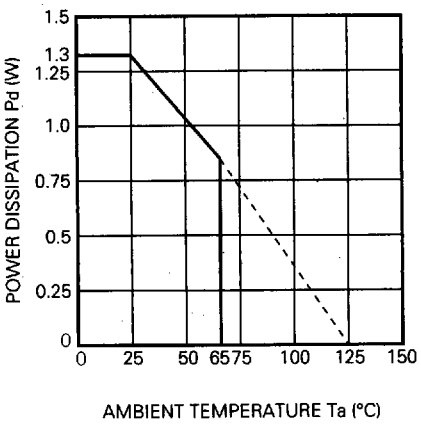
SG No.	Signals
SG 1	100 kHz CW 3 V_{P-P}
SG 2	100 kHz CW 200 mV_{P-P}
SG 3	2 MHz CW 200 mV_{P-P}
SG 4	5 MHz CW 200 mV_{P-P}
SG 5	PAL Simple Chroma Signal  $f_{ab(m)}=f_{ac(m)}$=4.433619MHz (Same Phase) The phase correlation between the about signals is outlined in the figure on the right. The phase correlation with burst of e_c (n) and e_c (n + 1) does not always have to be as shown in the figure on the right, and in particular must be adjustable according to conditions when testing phase correlation. 
SG 6	With PAL simple chroma signals for SG5, the phase of burst and chroma signals should be the same and the frequency should be ajustable.
SG 7	4.42 MHz CW 0.2~0.5 V_{P-P}
SG 8	4~6 MHz CW
SG 9	f_{sb} (Burst) = 4.433619 MHz, f_{sc} (Chroma) = 4.53 MHz at SG5.
SG a	Input for sync separation should be APL 100% standard combined image signal 1.5 V_{PP} for PAL system such as illustrated by the figure on the right. 
SG b	 Duty 90%
SG c	 Duty 95%
SG d	2 kHz, CW; 500 mV_{PP} = 0 dB

TEST CIRCUIT

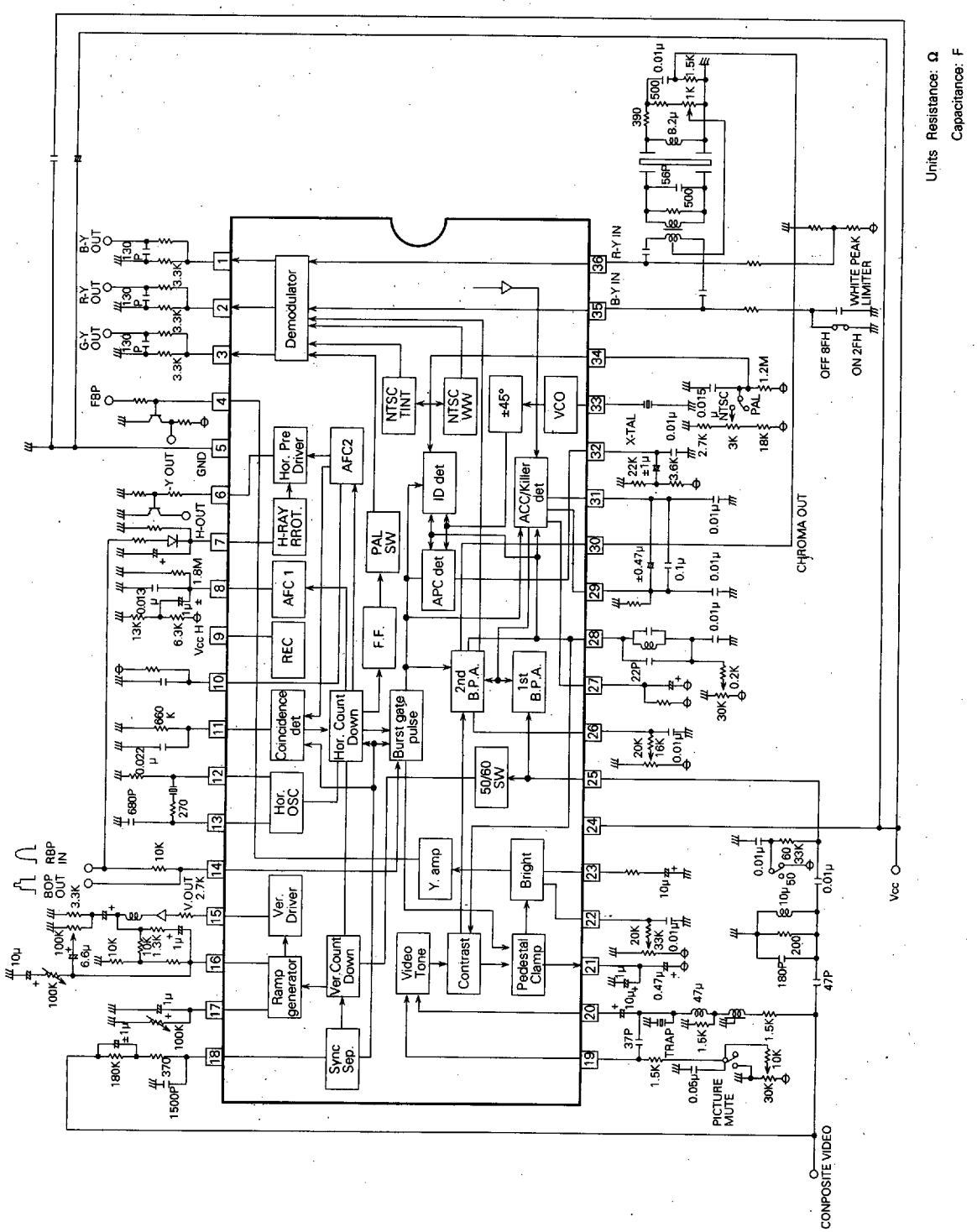


TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)

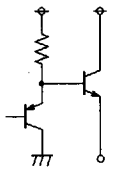
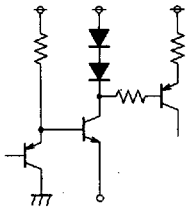
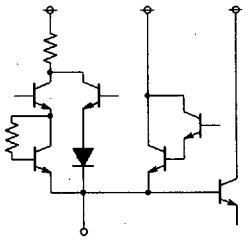
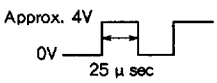
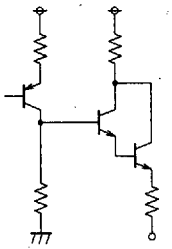
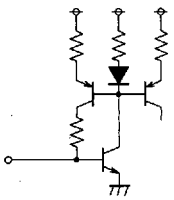


APPLICATION EXAMPLE

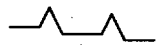
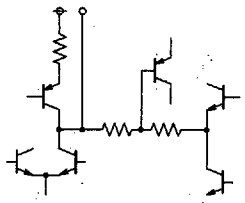
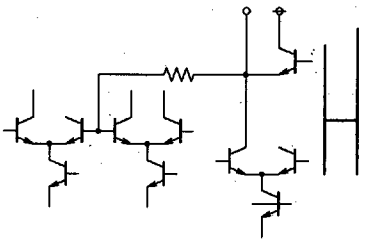
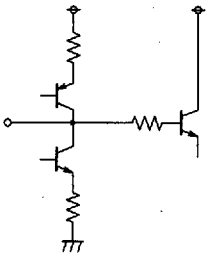
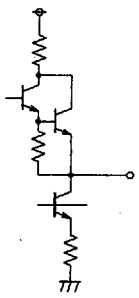


MITSUBISHI ELECTRIC

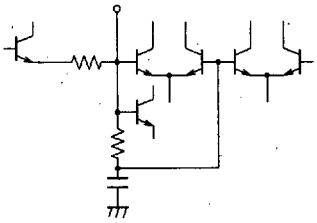
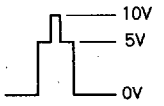
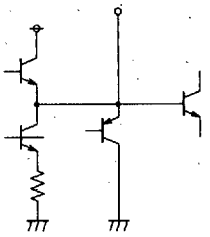
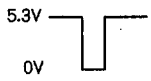
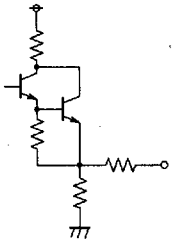
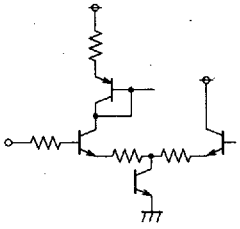
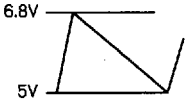
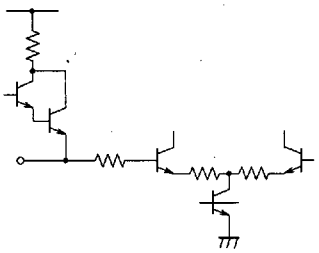
DESCRIPTION OF PIN

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
① ②	B-Y output R-Y output	• Chroma output B – Y R – Y		6.4
③	G-Y output	• Chroma output G – Y • If color tracking switch external resistor (emitter resistor) is removed, color tracking is ineffectual.		6.4
④	– Y output	• – Y output • Horizontal blanking input		——
⑤	GND	——	——	0
⑥	Horizontal output	 Horizontal pre – driver output		——
⑦	X – RAY protector	X – RAY protector is actuated when pin voltage exceeds approx. 0.75V.		——

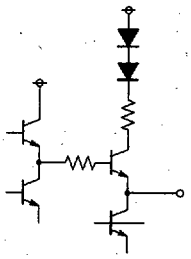
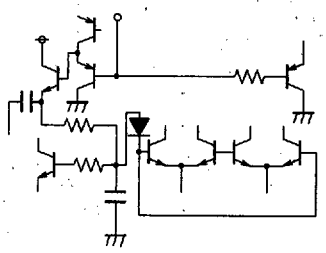
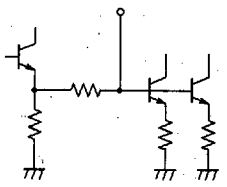
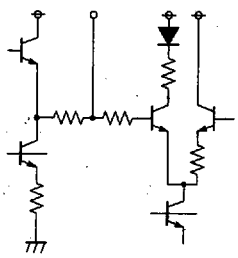
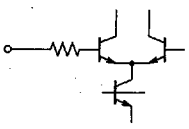
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage (V)
⑧	AFC1 filter	 When VCO frequency becomes high  filter voltage decreases causing VCO frequency to drop. Operates oppositely when frequency becomes high.		6.6
⑨	Vcc H	Built – in regulator	—	10
⑩	Horizontal ramp	 Generates horizontal ramp. Horizontal output pulse is created according to this ramp.		—
⑪	Coincidence detection filter	High when horizontal SYNC and horizontal output are synchronized, low when not synchronized.		Low 0.2 High 9.1
⑫	Horizontal oscillator output	 f = approx. 500kHz Output to external phase shifter.		9.5

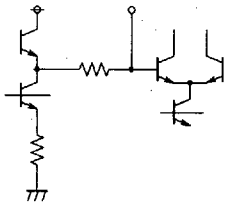
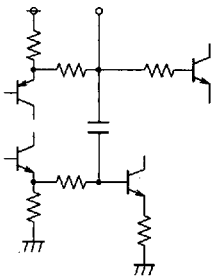
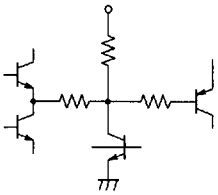
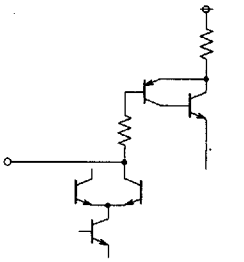
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
⑬	Horizontal oscillator input	 f = approx. 500kHz Output to external phase shifter.		5.2
⑭	F.B.P. input/ B.G.P. output	 B.G.P. and F.B.P. output as sand castle.		—
⑮	Vertical output			—
⑯	Vertical return	AC/DC return input pin		—
⑰	Vertical ramp	 Vertical ramp generation		—

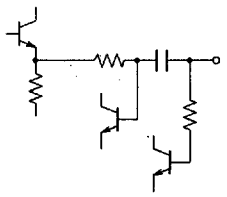
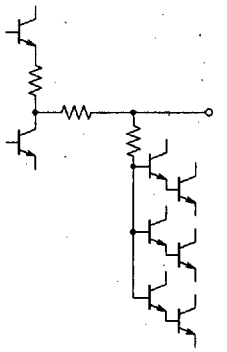
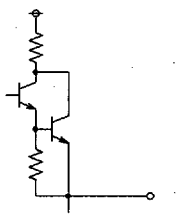
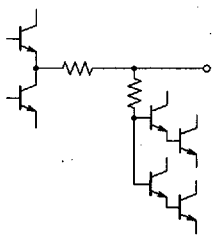
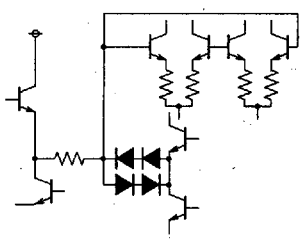
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage (V)
⑱	Sync separation input	Sync separation of emitter input		8.4
⑲	Picture quality control/ picture muting switch	• Picture quality control High – pass increases as pin voltage is decreased. • Picture muting If voltage is less than 2V, picture muting is actuated and – Y output becomes BLK level. • Built – in buffer		—
⑳	Y input	Y signal input		1.3
㉑	Pedestal clamp	Pedestal DC voltage of – Y output is determined by this clamp voltage.		2
㉒	Luminance control	Luminance control Becomes brighter as voltage is increased.		—

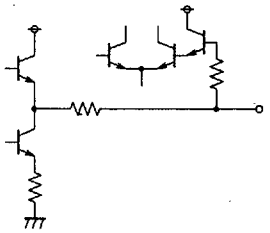
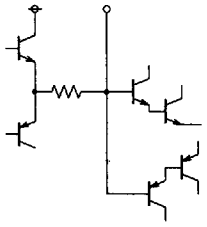
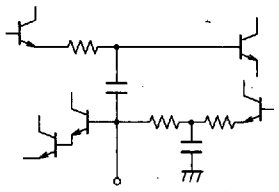
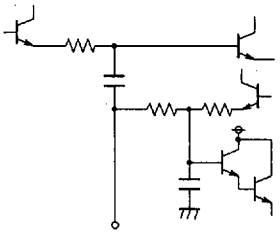
DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage (V)
㉓	DC playback	DC playback ratio can be changed by external CR. 100% when open.		——
㉔	Vcc	——	——	11
㉕	Color signal input 50/60 SW	• Chroma input • 50/60 switching Vertical countdown toggles between 50Hz and 60Hz. When voltage exceeds 5.6V, toggles to 60Hz.		2.7 ——
㉖	Color saturation control	Changes amplitude of chroma output.		——
㉗	Peak ACC filter	Gain of chroma amp is controlled by this filter in order to maintain a constant chroma amplitude.		——

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage(V)
㉙	Contrast control/ burst cleaning	Burst cleaning Coil connection contrast control Changes amplitude of −Y output. Amplitude increases as voltage is increased.		——
㉘	ACC/ killerfilter (1) / service switch	Sync ACC/killer filter ACC and killer are operated according to voltage differential between this pin and pin ㉛. When this pin is connected to GND, the service switch is ON. (Vertical stop and contrast MIN. killer ON.)		7.3
㉚	Chroma output	PAL system ACC chroma signals are output. NTSC system Low DC chroma signals are output.		7.1 4.2
㉛	ACC/killer filter (2)	Sync acc/killer filter ACC and killer are operated according to voltage differential between this pin and pin ㉘.		7.3
㉜	APC filter	Chroma VCO phase is controlled by this voltage in order to check burst.		9.1

DESCRIPTION OF PIN (cont.)

Pin No.	Name	Description	Peripheral circuit of pins	DC voltage (V)
㉝	Chroma VCO	Generates carrier for chroma.		8
㉞	Ident filter NTSC tint control	PAL system Functions as ident filter. When voltage drops below reference voltage, F.F. is stopped. NTSC system (less than 5V) Tint control is carried out at 2~4V. If NTSC switch is less than 5V, switches to NTSC mode.		8
㉟	B – Y input	PAL system Synthesized B – Y chroma signal input		6
㊱	R – Y input	PAL system Synthesized R – Y chroma signal input		2