

REJ03F0164-0201 Rev.2.01 Jan 25, 2008

Description

The M52334FP is IF signal-processing IC for VCRs and TVs. It enables the PLL detection system despite size as small as that of conventional quasi-synchronous VIF/SIF detector, IF/RF AGC, SIF limiter and FM detector.

Features

- Video detection output is $2 V_{P-P}$. It has built-in EQ AMP.
- The package is a 20-pin flat package, suitable for space saving.
- The video detector uses PLL for full synchronous detection circuit. It produces excellent characteristics of DG, DP, 920 kHz beat, and cross color.
- Dynamic AGC realizes high-speed response with only single filter.
- Video IF and sound IF signal processing are separated from each other. VCO output is used to obtain intercarrier.
- As AFT output voltage uses the APC output voltage, VCO coil is not used.
- Audio FM demodulation uses PLL system, so it has wide frequency range with no external parts and no adjustment.
- This IC corresponds to only inter of NTSC system.

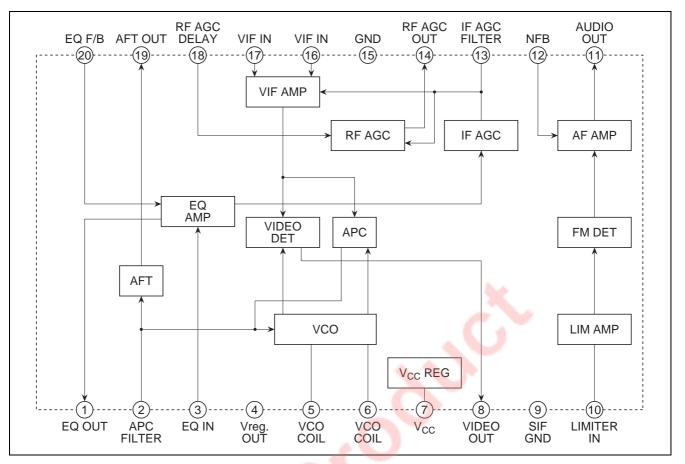
Application

TV sets, VCR tuners

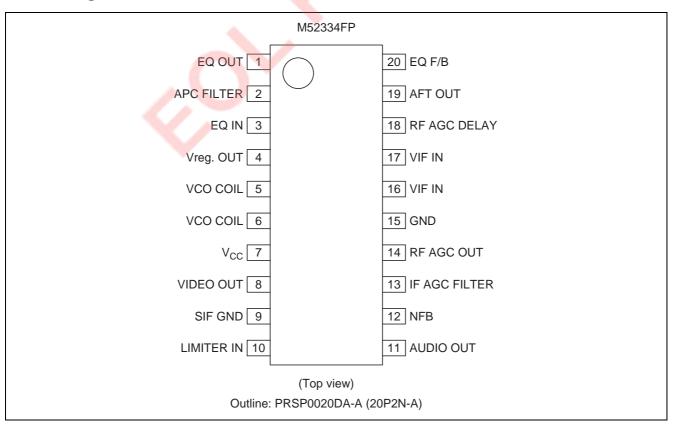
Recommended Operating Condition

- In case of V_{CC} and Vreg. OUT short
 - Supply voltage range: 4.75 to 5.25 V
 - Recommended supply voltage: 5.0 V
- Incase of Vreg. OUT open
 - Supply voltage range: 8.5 to 12.5 V

Block Diagram



Pin Arrangement



Absolute Maximum Ratings

				$(Ta = 25^{\circ}C, unless otherwise noted)$
Item	Symbol	Ratings	Unit	Condition
Supply voltage1	V _{cc}	13.2	V	V _{CC} and Vreg. out is not connected to each other.
Supply voltage Vreg. OUT	Vreg. OUT	6.0	V	V_{CC} and Vreg. out is not connected to each other.
Power dissipation	Pd	1225	mW	
Operating temperature	Topr	-20 to +85	°C	
Storage temperature	Tstg	-40 to +150	°C	
Surge voltage resistance	Surge	200	V	Surge protection capacitance 200 pF resistance 0

Electrical Characteristics

						(V _{CC}	= 9 V, 7	$Ta = 25^{\circ}$	C, unless c	otherwise noted.)
							Limits	*		Test Conditions
ltem	Symbol	Test Circuit	Test Point	Input Point	Input SG	Min	Тур	Max	Unit	Switches set to position 1 unless otherwise indicated
VIF section	-									
Circuit current1 $V_{CC} = 5V$	I _{CC1}	1	A	-	.Ū	33	40.5	47	mA	$V_{CC} = 5 V$ SW4 = 2, SW7 = 2
Circuit current2 $V_{CC} = 12V$	I _{CC2}	1	A	í		31	40.5	49	mA	$\begin{array}{l} V_{CC} = 12 \ V \\ SW7 = 2 \end{array}$
Vreg voltage2	V _{CC2}	1	TP4		•	4.7	5.00	5.3	V	$V_{CC} = 12 \text{ V}$
Video output DC voltage1	V1	1	TP1A	-	—	3.45	3.9	4.35	V	SW13 = 2 V13 = 0 V
Video output voltage8	Vo det8	1	TP8	VIF IN	SG1	0.85	1.1	1.35	V_{P-P}	
Video output voltage1	Vo det	1	TP1A	VIF IN	SG1	1.85	2.2	2.55	V_{P-P}	
Video S/N	Video S/N	1	TP1B	VIF IN	SG2	51	56	—	dB	SW1 = 2
Video band width	BW	1	TP1A	VIF IN	SG3	5.0	7.0	—	MHz	SW13 = 2 V13 = variable
Input sensitivity	VIN MIN	1	TP1A	VIF IN	SG4	_	48	52	dBμ	
Maximum allowable input	VIN MAX	1	TP1A	VIF IN	SG5	101	105	—	dBμ	
AGC control range input	GR	—	—	—		50	57	—	dB	
IF AGD voltage	V13	1	TP13	VIF IN	SG6	2.85	3.15	3.45	V	
Maximum IF AGC voltage	V13H	1	TP13	—		4.0	4.4	_	V	
Minimum IF AGC voltage	V13L	1	TP13	VIF IN	SG7	2.2	2.4	2.6	V	
Maximum RF AGC voltage	V14H	1	TP14	VIF IN	SG2	8.0	8.7	_	V	SW13 = 2 V13 = 4 V
Minimum RF AGC voltage	V14L	1	TP14	VIF IN	SG2	—	0.1	0.5	V	SW13 = 2 V13 = 1 V

 $(V_{CC} = 9 V, Ta = 25^{\circ}C, unless otherwise noted.)$

						Limits				Test Conditions
Item	Symbol	Test Circuit	Test Point	Input Point	Input SG	Min	Тур	Max	Unit	Switches set to position 1 unless otherwise indicated
RF AGC operation	V14	1	TP14	VIF IN	SG8	86	89	92	dBμ	
voltage										
Capture range U	CL-U	1	TP1A	VIF IN	SG9	0.8	1.3		MHz	
Capture range L	CL-L	1	TP1A	VIF IN	SG9	1.4	2.0		MHz	
Capture range T	CL-T	1	_	_		2.5	3.3		MHz	
AFT sensitivity		1	TP19	VIF IN	SG10	20	30	70	mV/kHz	
AFT maximum voltage	V19H	1	TP19	VIF IN	SG10	7.7	8.2	—	V	
AFT minimum voltage	V19L	1	TP19	VIF IN	SG10		0.7	1.2	V	
AFT defeat 1	AFT def1	1	TP19	VIF IN	—	4.2	4.5	4.8	V	
Inter modulation	IM	1	ТРЗА	VIF IN	SG11	35	42	5	dB	SW13 = 2 V13 = variable
Differential gain	DG	1	TP3A	VIF IN	SG12	_	2	5	%	
Differential phase	DP	1	TP3A	VIF IN	SG12	1	2	5	deg	
Sync. tip level	V3 SYNC	1	ТРЗА	VIF IN	SG2	1.0	1.4	1.8	V	
VIF input resister	RINV	2	TP17	_	6	-	1.2	—	kΩ	
VIF input capacitance	CINV	2	TP17	Ī		—	5	—	pF	
SIF section			4							
AF output DC voltage	V1	1	TP11	Y	—	3.5	4.4	5.3	V	
AF output	VoAF	1	TP11	SIF IN	SG16	565	790	1125	mVrms	
AF output distortion	THD AF	1	TP11	SIF IN	SG16	—	0.4	0.9	%	
Limiting sensitivity	LIM	1	TP11	SIF IN	SG17	_	42	55	dBμ	
AM rejection	AMR	1	TP11	SIF IN	SG18	55	65	—	dB	
AF S/N	AF S/N	1	TP11	SIF IN	SG19	55	65		dB	

Electrical Characteristics Test Method

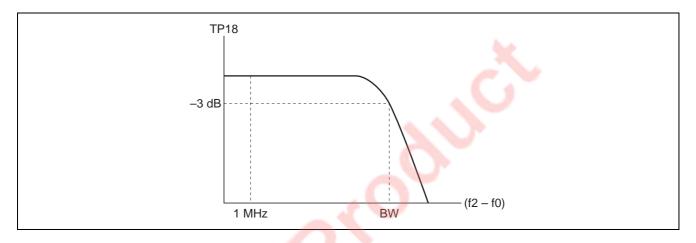
Video S/N

Input SG2 into VIF IN and measure the video out (Pin 3) noise in r.m.s at TP3-B through a 5 MHz (-3 dB) L.P.F.

$$S/N = 20 \log \left(\frac{0.7 \bullet Vo \ det}{NOISE} \right) (dB)$$

BW Video Band Width

- 1. Measure the 1 MHz component level of EQ output TP3A with a spectrum analyzer when SG3 (f2 = 44.75 MHz) is input into VIF IN. At that time, measure the voltage at TP13 with SW13, set to position 2, and then fix V13 at that voltage.
- 2. Reduce f2 and measure the value of (f2 f0) when the (f2 f0) component level reaches -3 dB from the 1 MHz component level as shown below.



VIN MIN Input Sensitivity

Input SG4 (Vi = 90 dB μ) into VIF IN, and then gradually reduce Vi and measure the input level when the 20 kHz component of EQ output TP3A reaches –3 dB from Vo det level.

VIN MAX Maximum Allowable Input

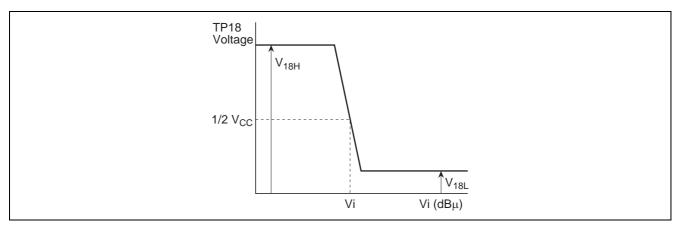
- 1. Input SG5 (Vi = 90 dB μ) into VIF IN, and measure the level of the 20 kHz components of EQ output.
- 2. Gradually increase the Vi of SG and measure the input level when the output reaches -3 dB.

GR AGC Control Range

GR = VIN MAX - VIN MIN (dB)

V18 RF AGC Operating Voltage

Input SG8 into VIF IN, and gradually reduce Vi and then measure the input level when RF AGC output TP14 reaches $1/2 V_{CC}$, as shown below.



CL-U Capture Range

- 1. Increase the frequency of SG9 until the VCO is out of locked-oscillation.
- 2. Decrease the frequency of SG9 and measure the frequency fU when the VCO locks. CL-U = fU - 45.75 (MHz)

CL-L Capture Range

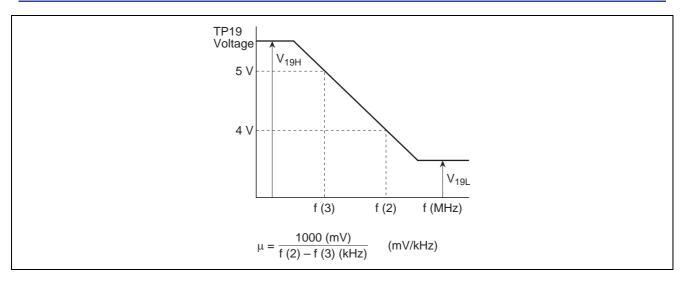
- 1. Decrease the frequency of SG9 until the VCO is out of locked-oscillation.
- 2. Increase the frequency of SG9 and measure the frequency fL when the VCO locks. CL-L = 45.75 - fL (MHz)

CL-T Capture Range

CL-T = CL-U + CL-L (MHz)

µAFT Sensitivity, V_{19H} AFT Maximum Voltage, V_{19L} AFT Minimum Voltage

- 1. Input SG10 into VIF IN, and set the frequency of SG 10 so that the voltage of AFT output TP19 is 5 V. This frequency is named f (3).
- 2. Set the frequency of SG10 so that the AFT output voltage is 4 V. This frequency is named f (2).
- 3. In the graph, maximum and minimum DC voltage are V_{19H} and V_{19L} , respectively.



IM Intermodulation

- 1. Input SG11 into VIF IN, and measure EQ output TP3A with an oscilloscope.
- 2. Adjust AGC filter voltage V13 so that the minimum DC level of the output waveform is 1.0 V.
- 3. At this time, measure, TP3A with a spectrum analyzer. The intermodulation is defined as a difference between 0.92 MHz and 3.58 MHz frequency components.

LIM Limiting Sensitivity

- 1. Input SG17 (Vi = 90 dB μ) into SIF input, and measure the 400 Hz component level of AF output TP11.
- 2. Lower the input level of SG17, and measure the level of SG17 when the VoAF level reaches -3 dB.

AMR AM Rejection

- 1. Input SG18 into SIF input, and measure the output level of AF output TP11. This level is named VAM.
- 2. AMR is;

 $AMR = 20 \log \left(\frac{VoAF (mVrms)}{VAM (mVrms)} \right) (dB)$

AF S/N

- 1. Input SG19 into SIF input, and measure the output noise level of AF output TP11. This level is named VN.
- 2. S/N is;

$$S/N = 20 \log \left(\frac{VoAF (mVrms)}{VN (mVrms)} \right) (dB)$$

The Note in the System Setup

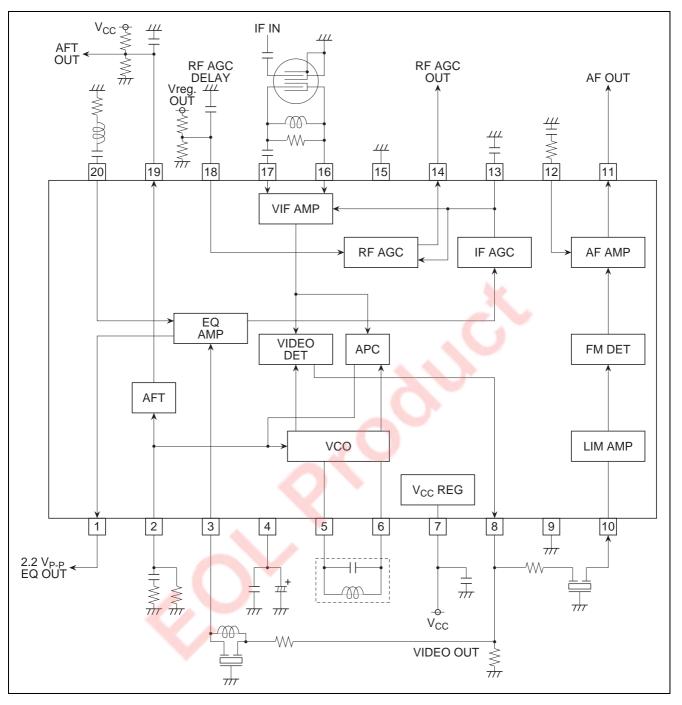
M52334FP has 2 power supply pins of V_{CC} (pin 7) and Vreg. OUT (pin 4). Pin 7 is for AFT output, RF AGC output circuits and 5 V regulated power supply circuit and pin 4 is for the other circuit blocks. In case M52334FP is used together with other ICs like VIF operating at more than 5 V, the same supply voltage as that of connected ICs is applied to V_{CC} and Vreg. OUT is opened. The other circuit blocks, connected to Vreg. OUT are powered by internal 5 V regulated power supply.

In case the connecting ICs are operated at 5 V, 5 V is supplied to both V_{CC} and Vreg. OUT.

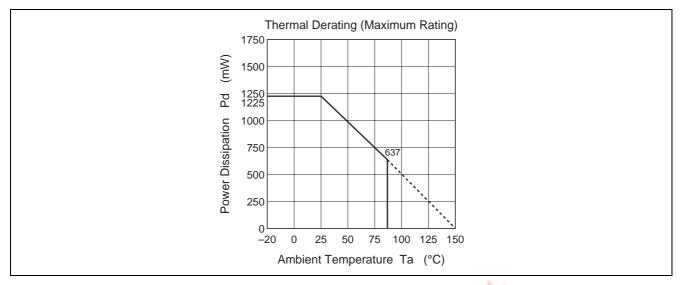
SG No.	Signals (50 Ω Termination)						
1	$f_0 = 45.75 \text{ MHz}$ AM 20 kHz 77.8% 90 dB μ						
2	$f_0 = 45.75 \text{ MHz} 90 \text{ dB}\mu \text{ CW}$						
3	$f_1 = 45.75 \text{ MHz} 90 \text{ dB}_{\mu} \text{ CW}$ (Mixed signal)						
	$f_2 =$ Frequency variable 70 dB μ CW (Mixed signal)						
4	f ₀ = 45.75 MHz AM 20 kHz 77.8% level variable						
5	f ₀ = 45.75 MHz AM 20 kHz 14.0% level variable						
6	f ₀ = 45.75 MHz 80 dBμ CW						
7	f ₀ = 45.75 MHz 110 dBμ CW						
8	f ₀ = 45.75 MHz CW level variable						
9	f ₀ = Variable AM 20 kHz 77.8% 90dBμ						
10	$f_0 = Variable 90 dB\mu CW$						
11	f ₁ = 45.75 MHz 90 dBμ CW (Mixed signal)						
	f ₂ = 42.17 MHz 80 dBμ CW (Mixed signal)						
	$f_3 = 41.25 \text{ MHz} 80 \text{ dB}\mu \text{ CW}$ (Mixed signal)						
12	f ₀ = 45.75 MHz 87.5%						
	TV modulation ten-step waveform						
	Sync tip level 90 dBμ						
13	$f_1 = 41.25 \text{ MHz} \ 103 \text{ dB}\mu \text{ CW}$						
14	$f_1 = 41.25 \text{ MHz} 70 \text{ dB}_{\mu} \text{ CW}$						
15	$f_1 = 45.75 \text{ MHz} 90 \text{ dB}_{\mu} \text{ CW}$ (Mixed signal)						
	$f_2 = 41.25 \text{ MHz} 70 dB_{\mu} CW \text{ (Mixed signal)}$						
16	$f_0 = 4.5 \text{ MHz} \ 90 \text{ dB}\mu \ FM \ 400 \text{ Hz} \pm 25 \text{ kHz} \text{ dev}$						
17	$f_0 = 4.5 \text{ MHz} \text{ FM } 400 \text{ Hz} \pm 25 \text{ kHz}$ dev level variable						
18	$f_0 = 4.5 \text{ MHz} 90 \text{ dB}\mu \text{ AM} 400 \text{ Hz} 30\%$						
19	$f_0 = 4.5 \text{ MHz} 90 \text{ dB}\mu \text{ CW}$						

Input Signal

Test Circuit

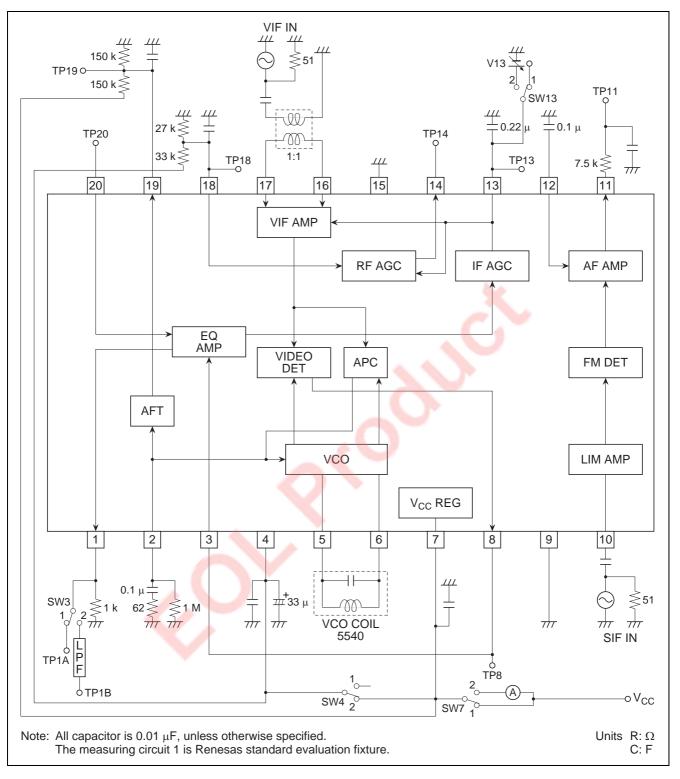


Typical Characteristics

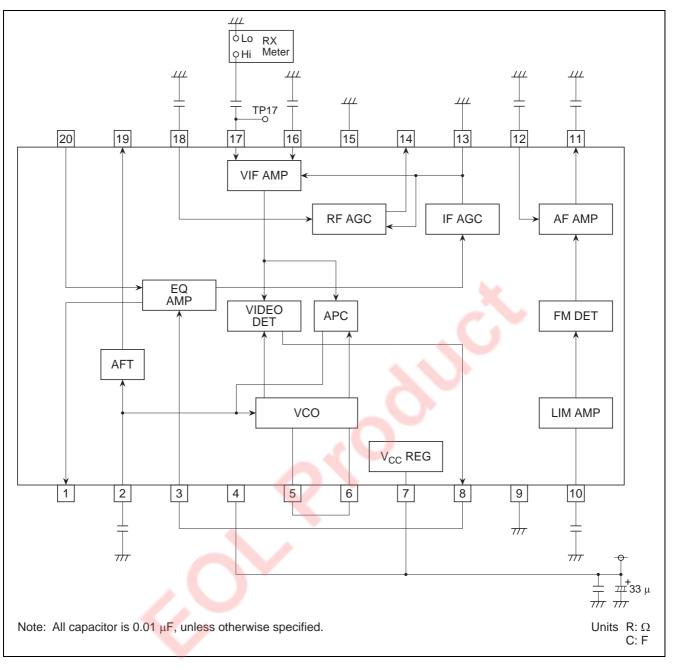


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Application Example 1

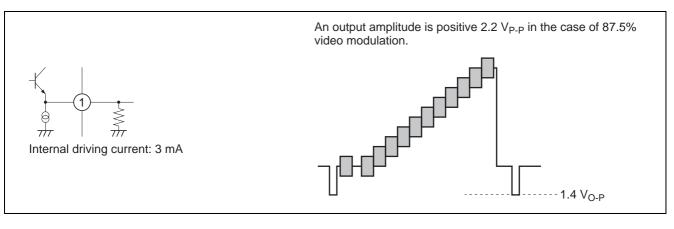


Application Example 2

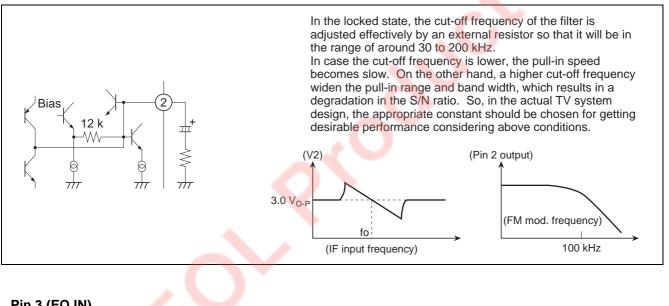


Pin Description

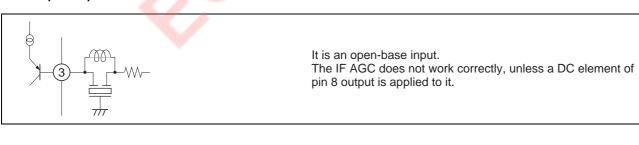
Pin 1 (EQ OUT)



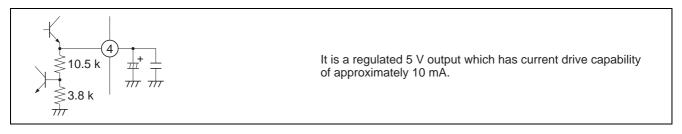
Pin 2 (APC FILTER)



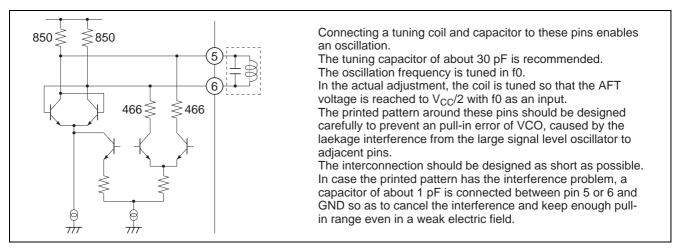
Pin 3 (EQ IN)



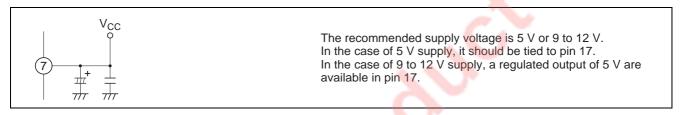
Pin 4 (Vreg. OUT)



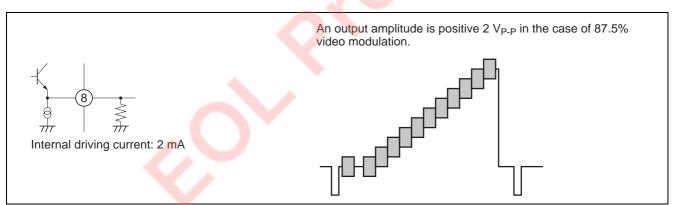
Pin 5, Pin 6 (VCO COIL)



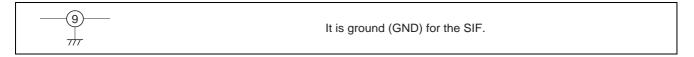
Pin 7 (V_{cc})



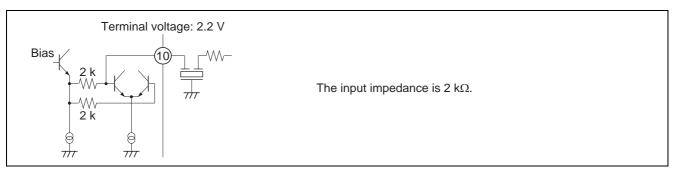
Pin 8 (VIDEO OUT)



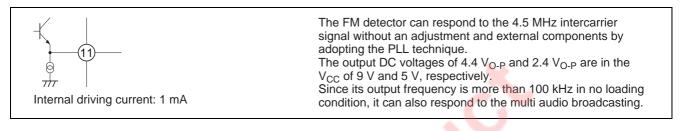
Pin 9 (SIF GND)



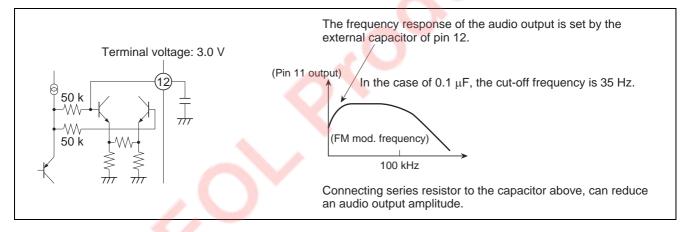
Pin 10 (LIMITER IN)



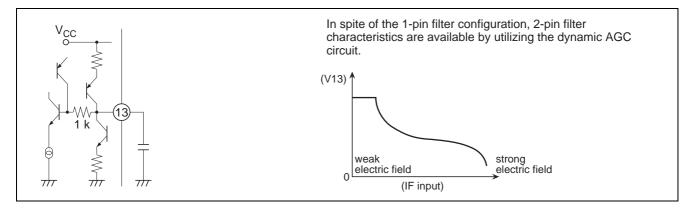
Pin 11 (AUDIO OUT)



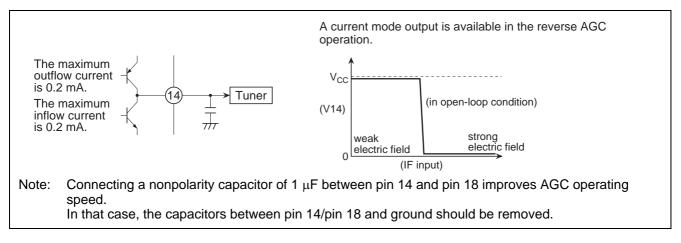
Pin 12 (NFB)



Pin 13 (IF AGC FILTER)



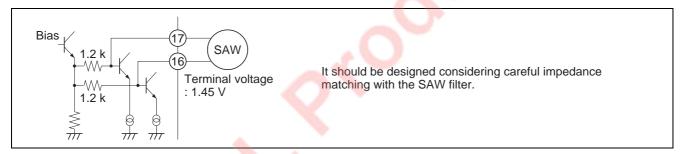
Pin 14 (RF AGC OUT)



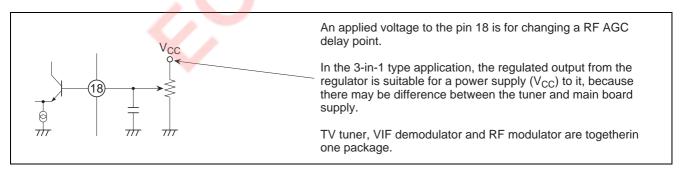
Pin 15 (GND)



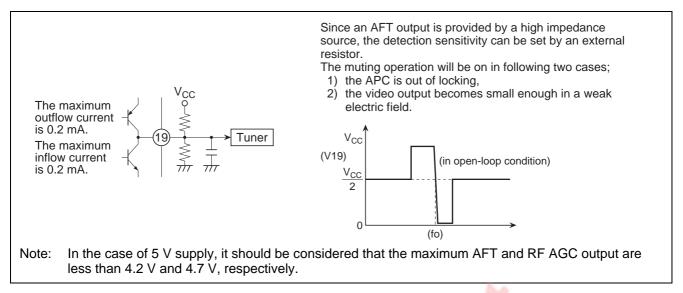
Pin 16, Pin 17 (VIF IN)



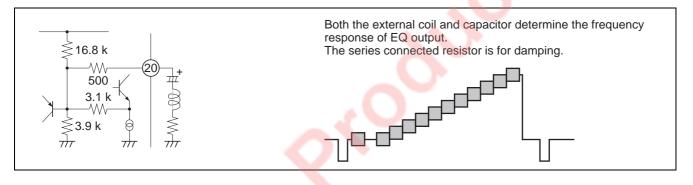
Pin 18 (RF AGC DELAY)



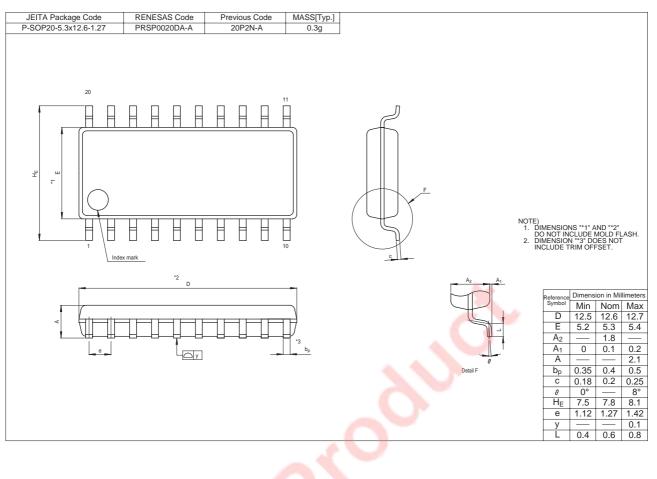
Pin 19 (AFT OUT)



Pin 20 (EQ F/B)



Package Dimensions



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