Revision History :

Revision 1.0 (Oct. 31, 2006)
- Original

Revision 1.1 (Dec. 29, 2006)
- Add -6 spec

Revision 1.2 (Mar. 02, 2007)
- Modify VOH and VOL
- Delete BGA ball name of packing dimensions

Revision 1.3 (May. 14,2007)
- Modify tSS (1.5ns => 2ns) and tSH(1ns => 1.5ns)

Revision 1.4 (Jul. 10,2007)
- Modify type error

SDRAM 512K x 32Bit x 2Banks

Synchronous DRAM

FEATURES

- 2.5V power supply
- LVCMOS compatible with multiplexed address
- Dual banks operation
- MRS cycle with address key programs
  - CAS Latency (1, 2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- EMRS cycle with address key programs.
- All inputs are sampled at the positive going edge of the system clock
- Burst Read Single-bit Write operation
- Special Function Support.
  - PASR (Partial Array Self Refresh)
  - TCSR (Temperature compensated Self Refresh)
  - DS (Driver Strength)
- DQM for masking
- Auto & self refresh
- 64ms refresh period (4K cycle)

GENERAL DESCRIPTION

The M52S32321A is 33,554,432 bits synchronous high data rate Dynamic RAM organized as 2 x 524,288 words by 32 bits, fabricated with high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

ORDERING INFORMATION

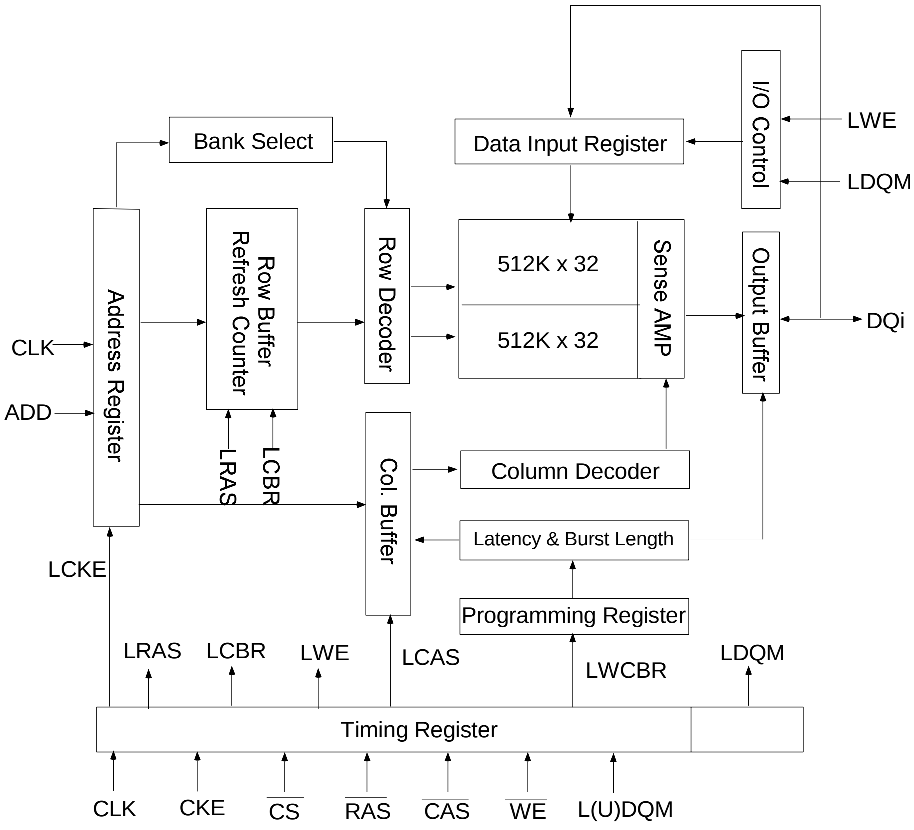
Part NO.	MAX Freq.	Package	Comments
M52S32321A -10BG	100MHz	90 Ball VFBGA	Pb-free
M52S32321A -7.5BG	133MHz	90 Ball VFBGA	Pb-free
M52S32321A -6BG	166MHz	90 Ball VFBGA	Pb-free

PIN CONFIGURATION (TOP VIEW)

90 Ball FBGA

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	NC				NC	NC	NC
J	CLK	CKE	A9				BA	$\overline{\text{CS}}$	$\overline{\text{RAS}}$
K	DQM1	NC	NC				**$\overline{\text{CAS}}$**	$\overline{\text{WE}}$	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System Clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip Select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	*Clock Enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A10	*Address*	Row / column addresses are multiplexed on the same pins. Row address : RA0 ~ RA10, column address : CA0 ~ CA7
BA	*Bank Select Address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row Address Strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column Address Strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write Enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	*Data Input / Output Mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.

DQ0 ~ 31	*Data Input / Output*	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	*Power Supply/Ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data Output Power/Ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No Connection/ Reserved for Future Use*	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD},V_{DDQ}	-1.0 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ + 150	°C
Power dissipation	P_D	0.7	W
Short circuit current	I_{OS}	50	MA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A= 0 °C ~ 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	2.3	2.5	2.7	V	
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	2.5	V_{DDQ}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	V_{DDQ} -0.2	-	-	V	I_{OH} =-0.1mA
Output logic low voltage	V_{OL}	-	-	0.2	V	I_{OL} = 0.1mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1.V_{IH} (max) = 3.0V AC for pulse width $\leq$ 3ns acceptable.

2.V_{IL} (min) = -1.0V AC for pulse width $\leq$ 3ns acceptable.
3.Any input 0V $\leq$ V_{IN} $\leq$ V_{DDQ}+0.3V, all other pins are not under test = 0V.
4.Dout is disabled, 0V $\leq$ V_{OUT} $\leq$ V_{DDQ}.

CAPACITANCE (V_{DD} = 2.5V, T_A = 25 °C , f = 1MHz)

Pin	Symbol	Min	Max	Unit
CLOCK	C_{CLK}	-	4.0	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, LDQM, UDQM	C_{IN}	-	4.0	pF
ADDRESS	C_{ADD}	-	4.0	pF
DQ0 ~DQ31	C_{OUT}	-	6.0	pF

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted, T_A = 0 °C ~ 70 °C)

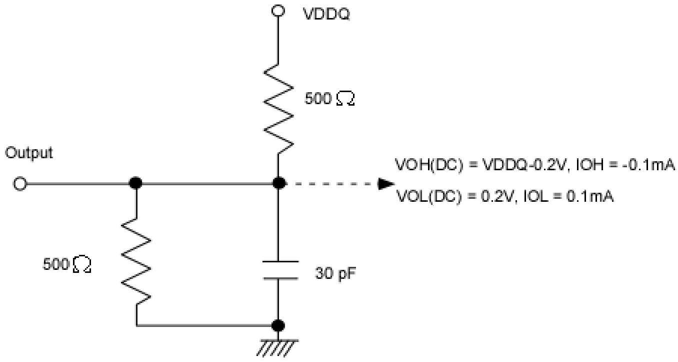
Parameter	Symbol	Test Condition	CAS Latency	Version			Unit	Note
				-6	-7.5	-10		
Operating Current (One Bank Active)	I_{CC1}	Burst Length = 1 $t_{RC} \geq t_{RC}$ (min), $t_{CC} \geq t_{CC}$ (min), I_{OL}= 0mA		100	80	60	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), t_{CC} =15ns		0.3			mA	
	I_{CC2PS}	CKE $\leq V_{IL}$(max), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		0.2			mA	
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} =15ns Input signals are changed one time during 30ns		9			mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		8			mA	
Active Standby Current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), t_{CC} =15ns		2			mA	
	I_{CC3PS}	CKE $\leq V_{IL}$(max), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$		1.5				
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC}=15ns Input signals are changed one time during 30ns		15			mA	
	I_{CC3NS}	CKE $\geq V_{IH}$ (min), CLK $\leq V_{IL}$(max), $t_{CC} = \infty$ Input signals are stable		8			mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}= 0Ma, Page Burst All Band Activated, tCCD = tCCD (min)		100	80	60	mA	1
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		40	40	40	mA	2
Self Refresh Current	I_{CC6}	CKE $\leq$ 0.2V	TCSR range	45	70		°C	
			2 Banks	180	200		uA	
			1 Bank	160	180			
Deep Power Down Current	I_{CC7}	CKE $\leq$ 0.2V		15			uA	

Note: 1.Measured with outputs open. Addresses are changed only one time during t_{CC}(min).

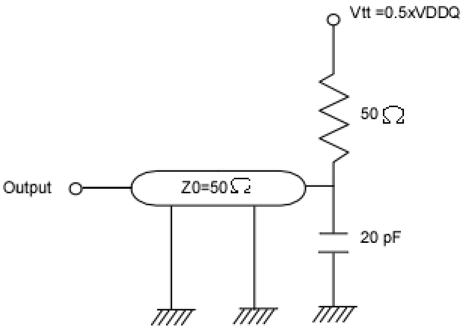
2.Refresh period is 64ms. Addresses are changed only one time during t_{CC}(min).

AC OPERATING TEST CONDITIONS (V_{DD}=2.5V ± 0.2V,T_A= 0 °C ~ 70 °C)

Parameter	Value	Unit
Input levels (Vih/Vil)	0.9 x V_{DDQ} / 0.2	V
Input timing measurement reference level	0.5 x V_{DDQ}	V
Input rise and fall time	tr / tf = 1 / 1	ns
Output timing measurement reference level	0.5 x V_{DDQ}	V
Output load condition	See Fig.2	



(Fig.1) DC Output Load circuit



(Fig.2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version			Unit	Note
		-6	-7.5	-10		
Row active to row active delay	t_{RRD}(min)	12	15	20	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay	t_{RCD}(min)	18	22.5	30	ns	1
Row precharge time	t_{RP}(min)	18	22.5	30	ns	1
Row active time	t_{RAS}(min)	36	45	50	ns	1
	t_{RAS}(max)	100			us	
Row cycle time	t_{RC}(min)	54	67.5	90	ns	1
Last data in to new col. Address delay	t_{CDL}(min)	1			CLK	2
Last data in to row precharge	t_{RDL}(min)	2			CLK	2
Last data in to burst stop	t_{BDL}(min)	1			CLK	2
Col. Address to col. Address delay	t_{CCD}(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	1				

Note: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
The earliest a precharge command can be issued after a Read command without the loss of data is CL+BL-2 clocks.

AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-7.5		-10		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS Latency =3	t_{CC}	6	1000	7.5	1000	9	1000	ns	1
	CAS Latency =2		10		12		15			
CLK to valid output delay	CAS Latency =3	t_{SAC}	-	5.5	-	7	-	8	ns	1
	CAS Latency =2		-	10	-	10	-	10		
Output data hold time		t_{OH}	2.0	-	2.0	-	2.0	-	ns	2
CLK high pulse width		t_{CH}	2.0	-	2.5	-	2.5	-	ns	3
CLK low pulse width		t_{CL}	2.0	-	2.5	-	2.5	-	ns	3
Input setup time		t_{SS}	2.0	-	2.0	-	2.0	-	ns	3
Input hold time		t_{SH}	1.5	-	1.5	-	1.5	-	ns	3
CLK to output in Low-Z		t_{SLZ}	1	-	1	-	1	-	ns	2
CLK to output in Hi-Z	CAS Latency =3	t_{SHZ}	-	5	-	6	-	7	ns	-
	CAS Latency =2		-	8	-	9	-	10		

*All AC parameters are measured from half to half.

Note: 1.Parameters depend on programmed CAS latency.

2.If clock rising time is longer than 1ns,(tr/2-0.5)ns should be added to the parameter.

3.Assumed input rise and fall time (tr & tf)=1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr+ tf)/2-1]ns should be added to the parameter.

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA	A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	0	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode			**CAS Latency**				**Burst Type**		**Burst Length**				
A8	**A7**	**Type**	**A6**	**A5**	**A4**	**Latency**	**A3**	**Type**	**A2**	**A1**	**A0**	**BT = 0**	**BT = 1**
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
			1	0	0	Reserved			1	0	0	Reserved	Reserved
			1	0	1	Reserved			1	0	1	Reserved	Reserved
			1	1	0	Reserved			1	1	0	Reserved	Reserved
			1	1	1	Reserved			1	1	1	Full Page	Reserved

Full Page Length : 256

Extended Mode Register

BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address bus
1	0	ATCSR	0	0	DS		TCSR		PASR			Extended Mode Register

	A2-0	Self Refresh Coverage
PASR	000	Full Array
	001	1/2 of Full Array
	010	1/4 of Full Array
	011	RFU
	100	RFU
	101	RFU
	110	RFU
	111	RFU

	A4-A3	Maximum Case Temperature
TCSR	11	85oC
	00	70oC
	01	45oC
	10	15oC

	A6-A5	Driver Strength
DS	00	Full Strength
	01	1/2 Strength
	10	1/4 Strength
	11	RFU

	A9	ATCSR
ATCSR	0	Enable
	1	R

TRUTH TABLE (Deep Power Down Mode)

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA	A10/AP	A9~A0
Deep Power Down Mode	Entry	H	L	L	H	H	L	X	X		
	Exit	L	H	X	X	X	X	X			

(V= Valid, X= Don’t Care, H= Logic High , L = Logic Low)

Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0 binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

Starting Address (column address A1-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence (decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of Sequential Addressing, with the length being 256 for 1Mx32 device.

POWER UP SEQUENCE

1.Apply power and start clock, attempt to maintain CKE= “H”, L(U)DQM = “H” and the other pin are NOP condition at the inputs.

2.Maintain stable power, stable clock and NOP input condition for a minimum of 200us.

3.Issue precharge commands for all banks of the devices.

4.Issue 2 or more auto-refresh commands.

5.Issue mode register set command to initialize the mode register.

Cf.)Sequence of 4 & 5 is regardless of the order.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	DQM	BA	A10/AP	A9~A0	Note
Register	Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
	Extended Mode Register Set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	4
	Both Banks									X	H		4
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operation Command			H	X	H	X	X	X	X	X			
			H		L	H	H	H					
Deep Power Down Mode		Entry	H	L	L	H	H	L	X	X			
		Exit	L	H	X	X	X	X	X				

(V= Valid, X= Don't Care, H= Logic High , L = Logic Low)

Note:

1. OP Code: Operation Code

   A0~A10, BA: Program keys.(@MRS). BA=0 for MRS and BA=1 for EMRS.
2. MRS/EMRS can be issued only at both banks precharge state.

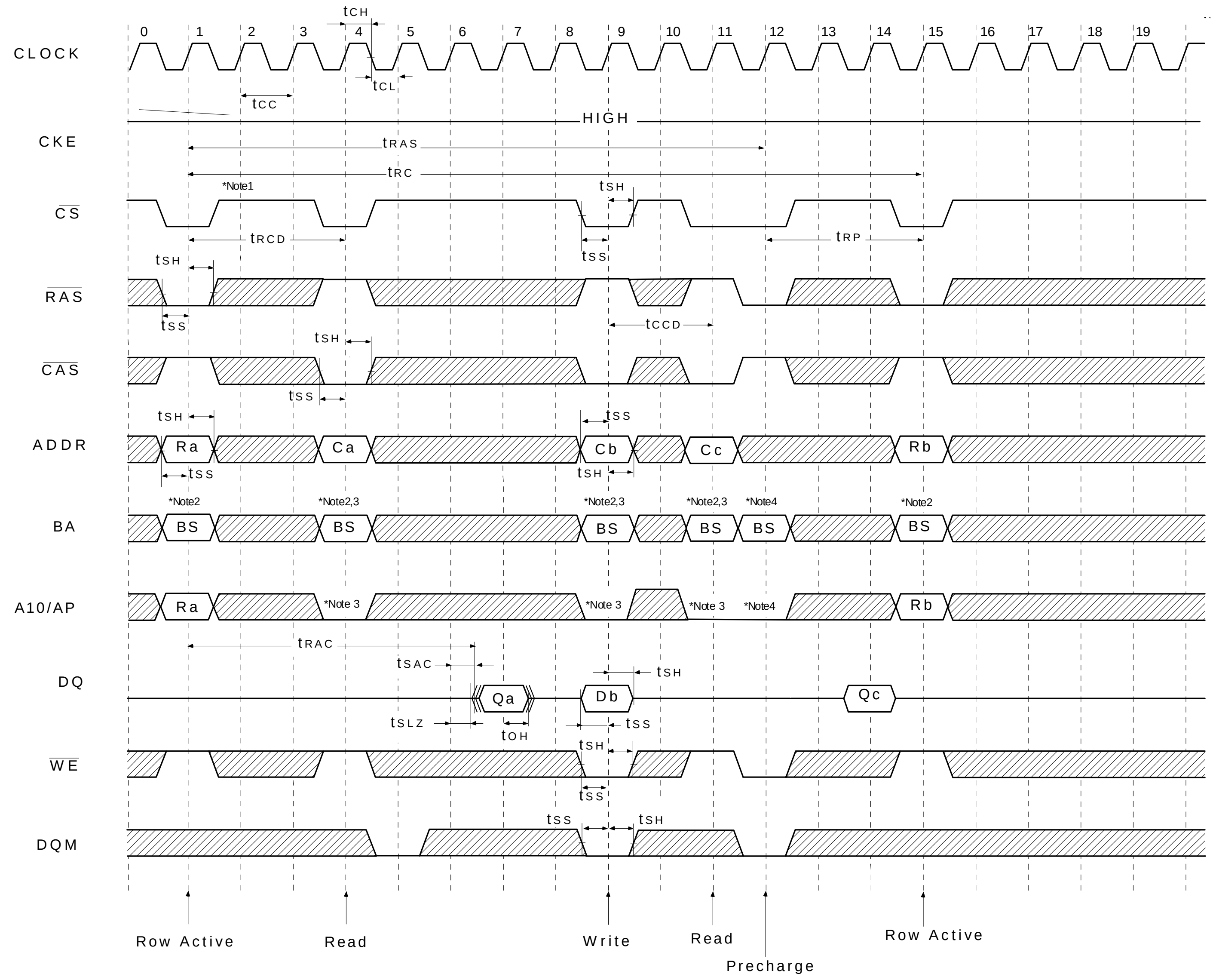
   A new command can be issued after 2 clock cycle of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.

   The automatical precharge without row precharge command is meant by "Auto".
   Auto / self refresh can be issued only at both banks precharge state.
4. BA: Bank select address.

   If "Low": at read, write, row active and precharge, bank A is selected.
   If "High": at read, write, row active and precharge, bank B is selected.
   If A10/AP is "High" at row precharge, BA ignored and both banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.

   Another bank read /write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK masks the data-in at the very CLK (Write DQM latency is 0), but makes
   Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

Single Bit Read-Write-Read Cycle (Same Page) @CAS Latency=3, Burst Length=1



▨ :Don't Care

***Note:** 1. All inputs expect CKE & DQM can be don’t care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active & read/write are controlled by BA.

BA	Active & Read/Write
0	Bank A
1	Bank B

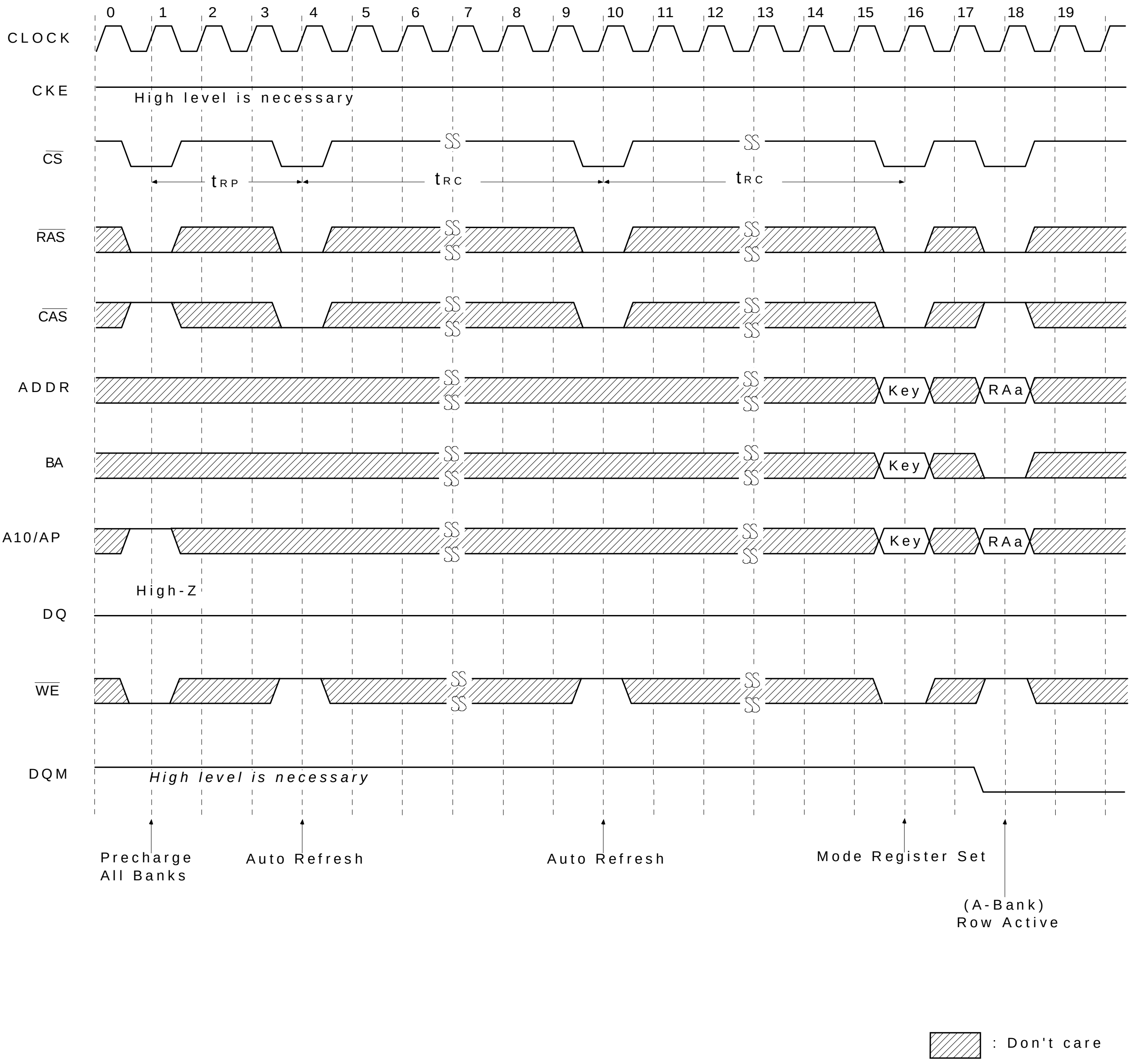
3.Enable and disable auto precharge function are controlled by A10/AP in read/write command.

A10/AP	BA	Operation
0	0	Disable auto precharge, leave bank A active at end of burst.
	1	Disable auto precharge, leave bank B active at end of burst.
1	0	Enable auto precharge, precharge bank A at end of burst.
	1	Enable auto precharge, precharge bank B at end of burst.

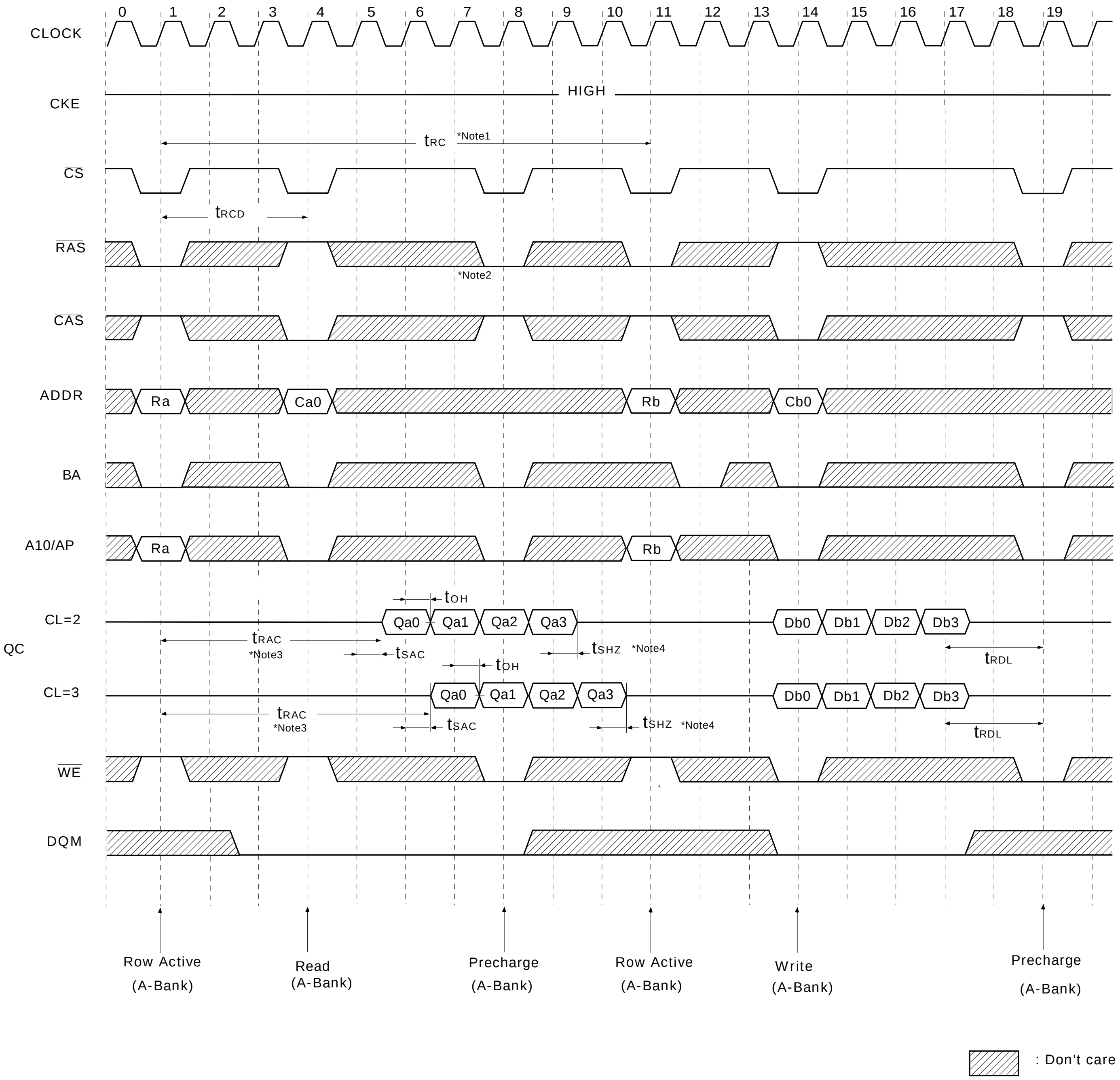
4.A10/AP and BA control bank precharge when precharge command is asserted.

A10/AP	BA	precharge
0	0	Bank A
0	1	Bank B
1	X	Both Banks

Power Up Sequence



Read & Write Cycle at Same Bank @Burst Length = 4



***Note:** 1.Minimum row cycle times is required to complete internal DRAM operation.

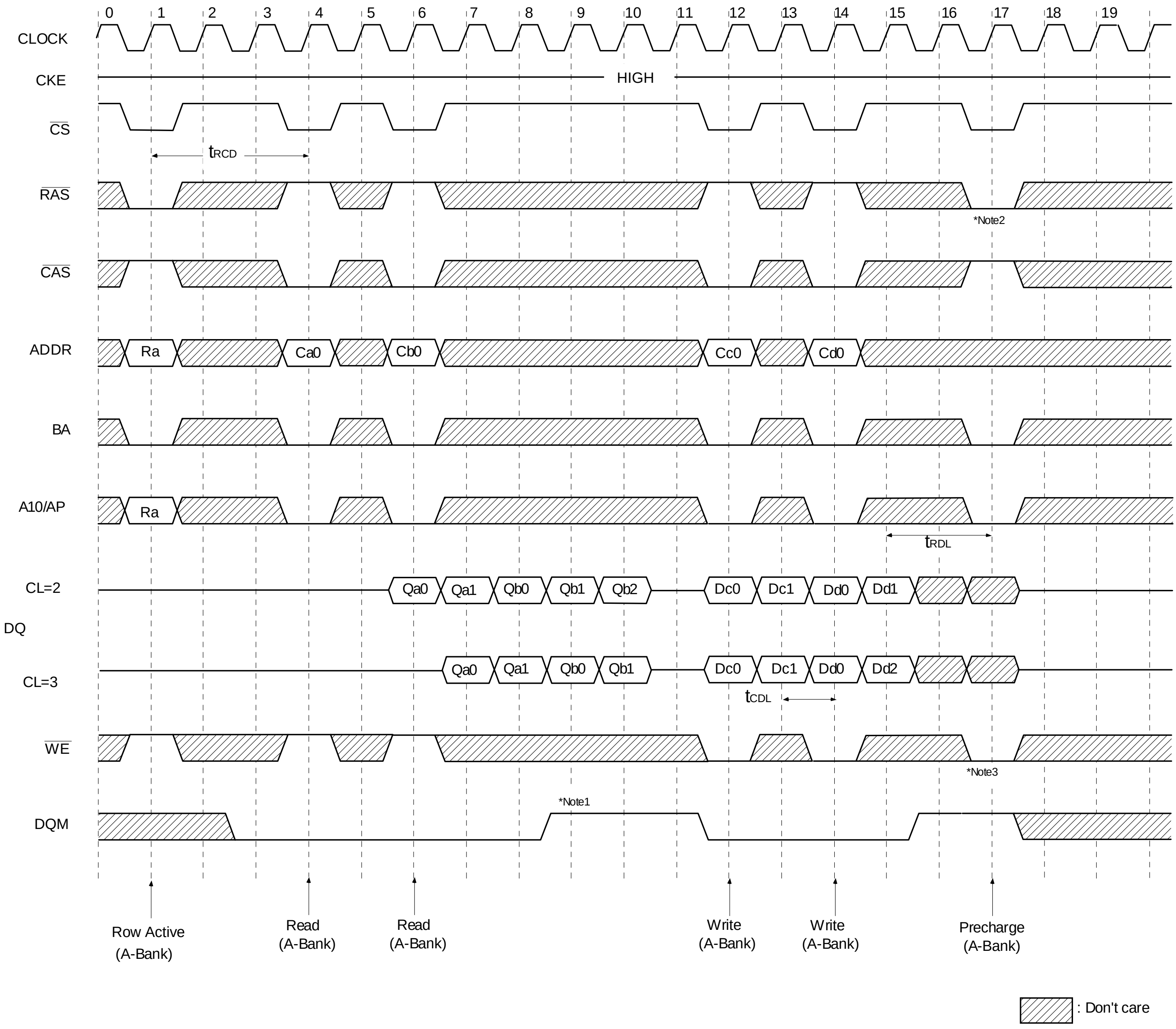
2.Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.

3.Access time from Row active command. tcc*(t_{RCD} +CAS latency-1)+t_{SAC}

4.Ouput will be Hi-Z after the end of burst.(1,2,4,8 bit burst)

Burst can't end in Full Page Mode.

Page Read & Write Cycle at Same Bank @ Burst Length=4

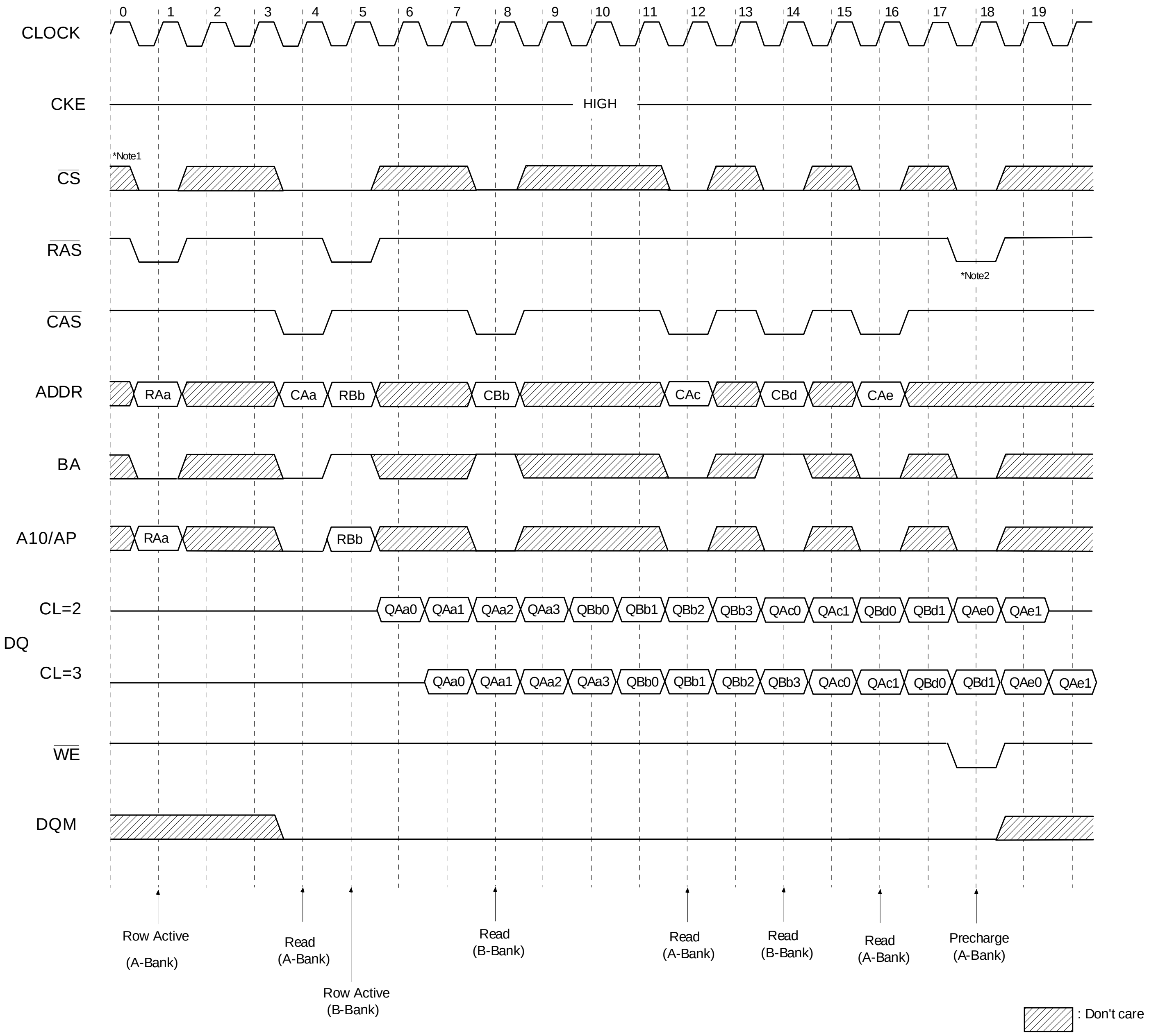


***Note :**1.To write data before burst read ends, DQM should be asserted three cycle prior to write command to avoid bus contention.

2.Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge, will be written.

3.DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

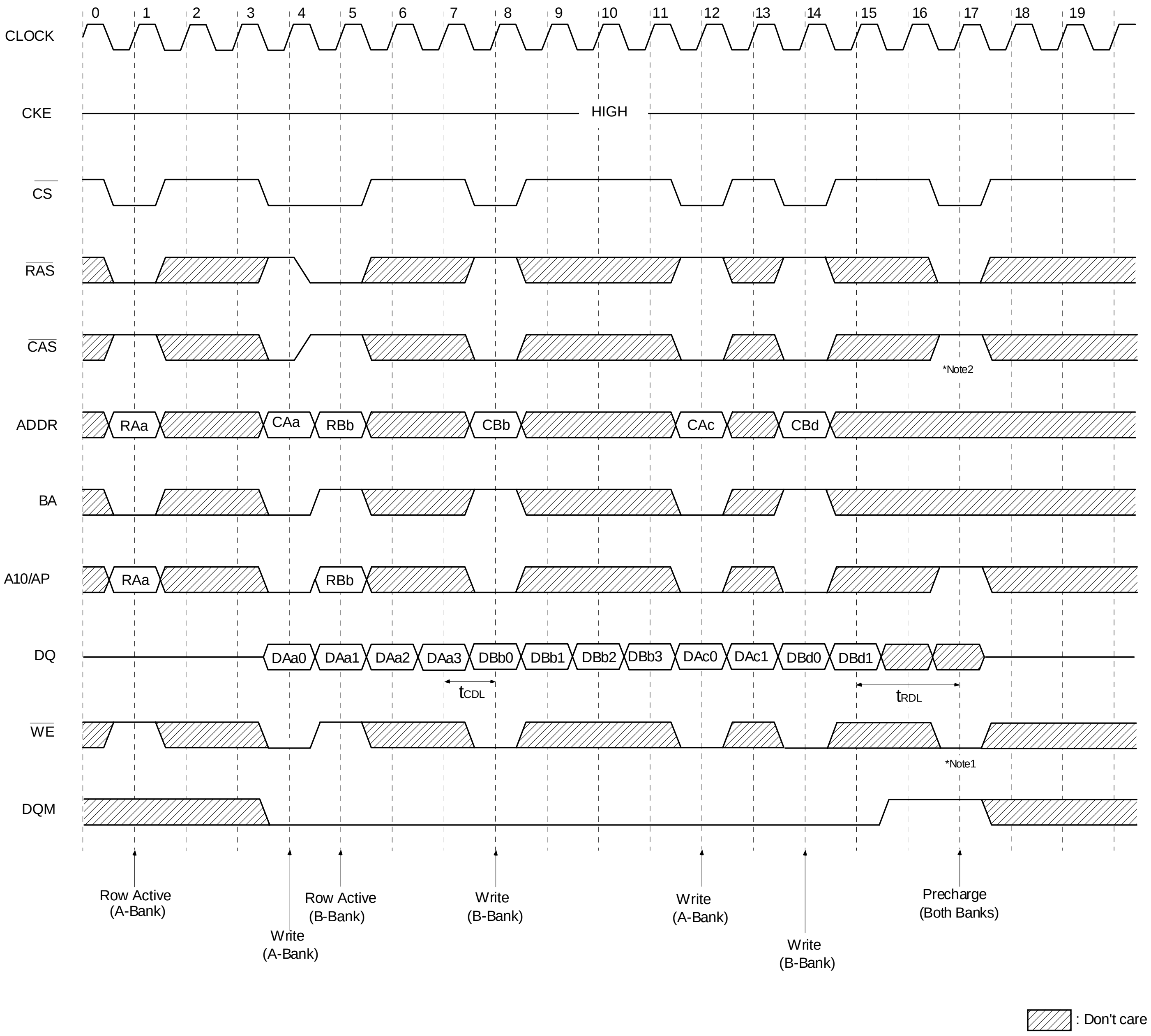
Page Read Cycle at Different Bank @ Burst Length=4



*Note: 1. $\overline{\text{CS}}$ can be don't cared when $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are high at the clock high going dege.

2.To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

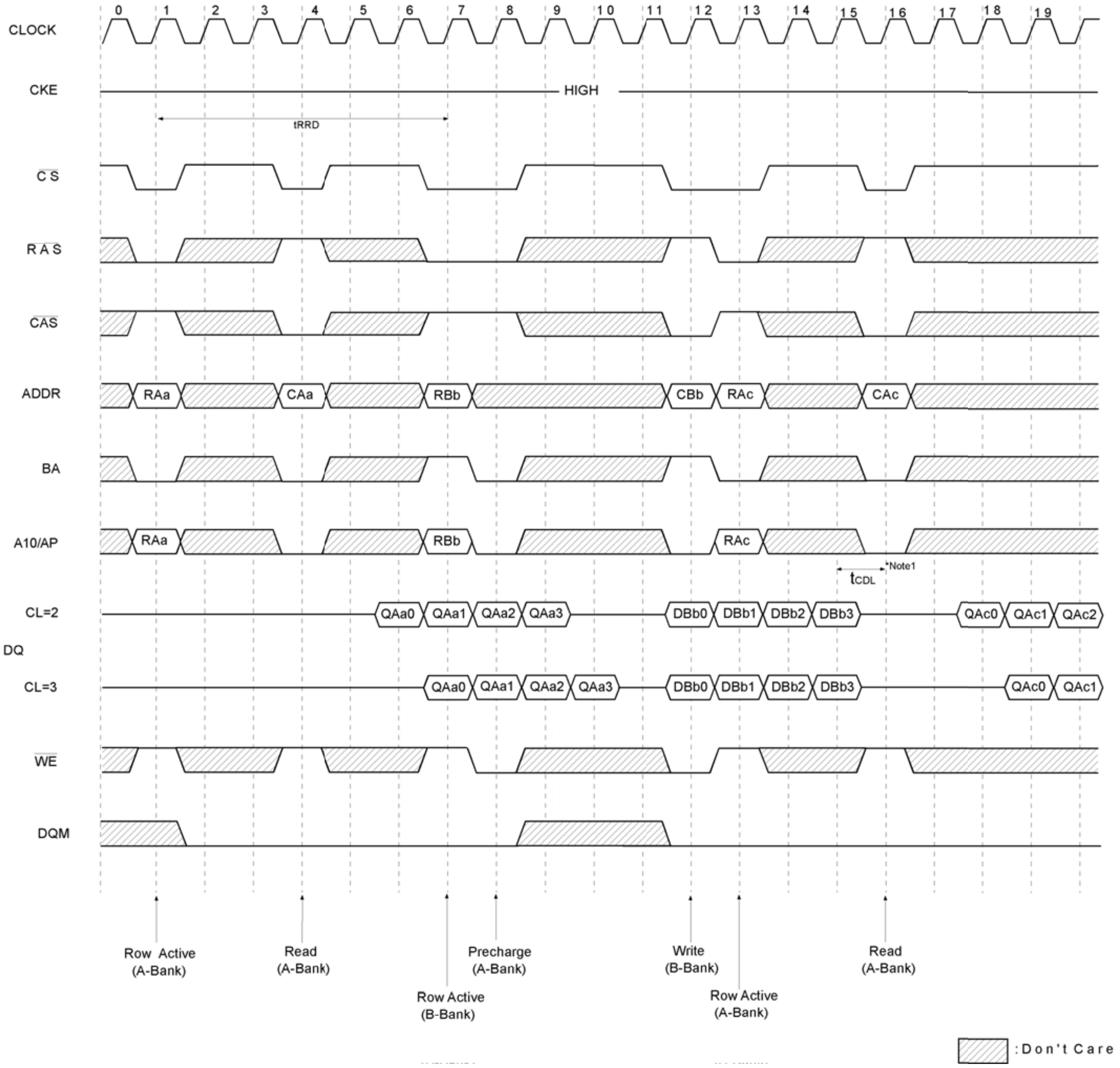
Page Write Cycle at Different Bank @Burst Length = 4



*Note: 1.To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.

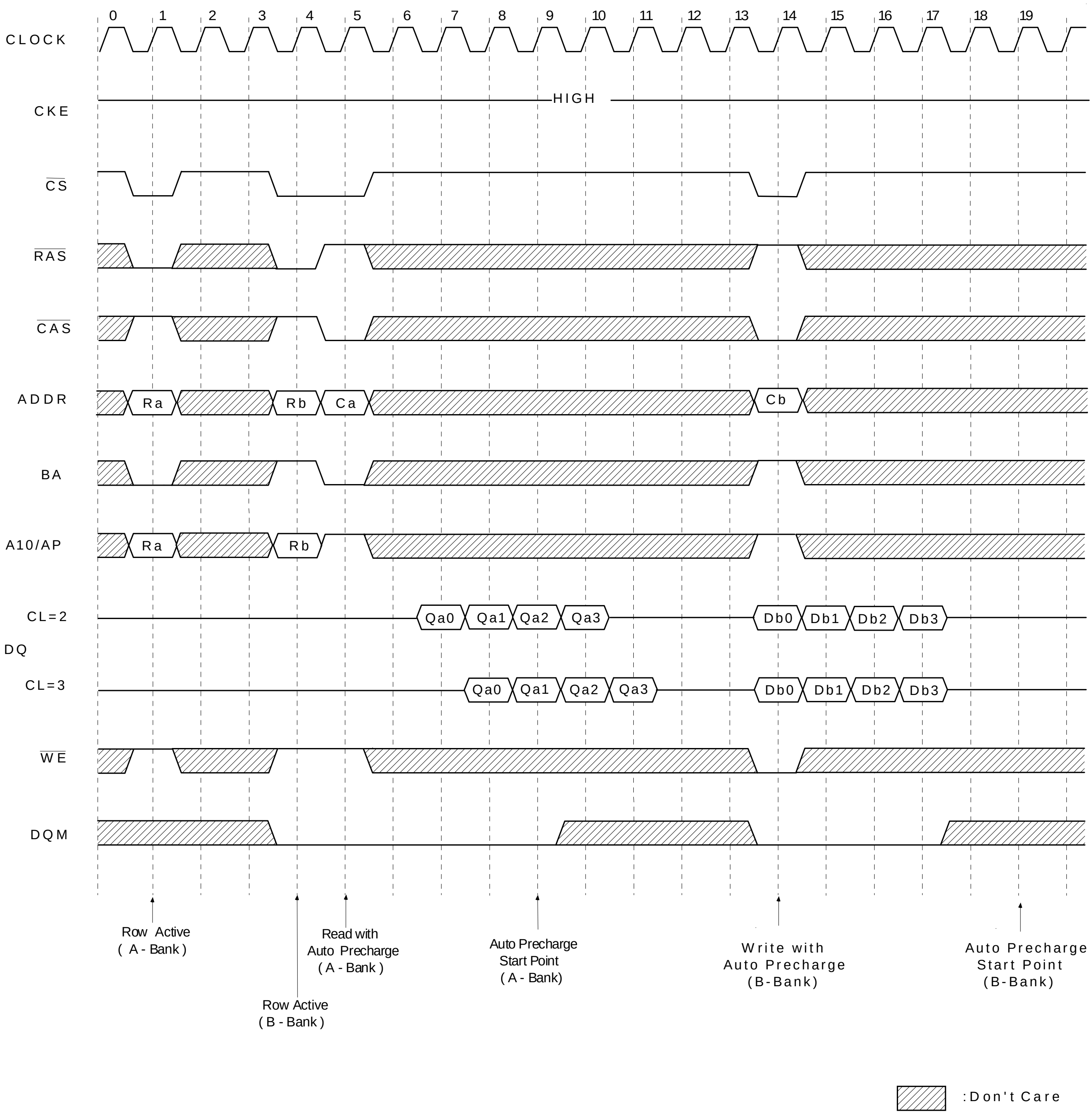
2.To interrupt burst write by row precharge, both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



*Note: 1.tCDL should be met to complete write.

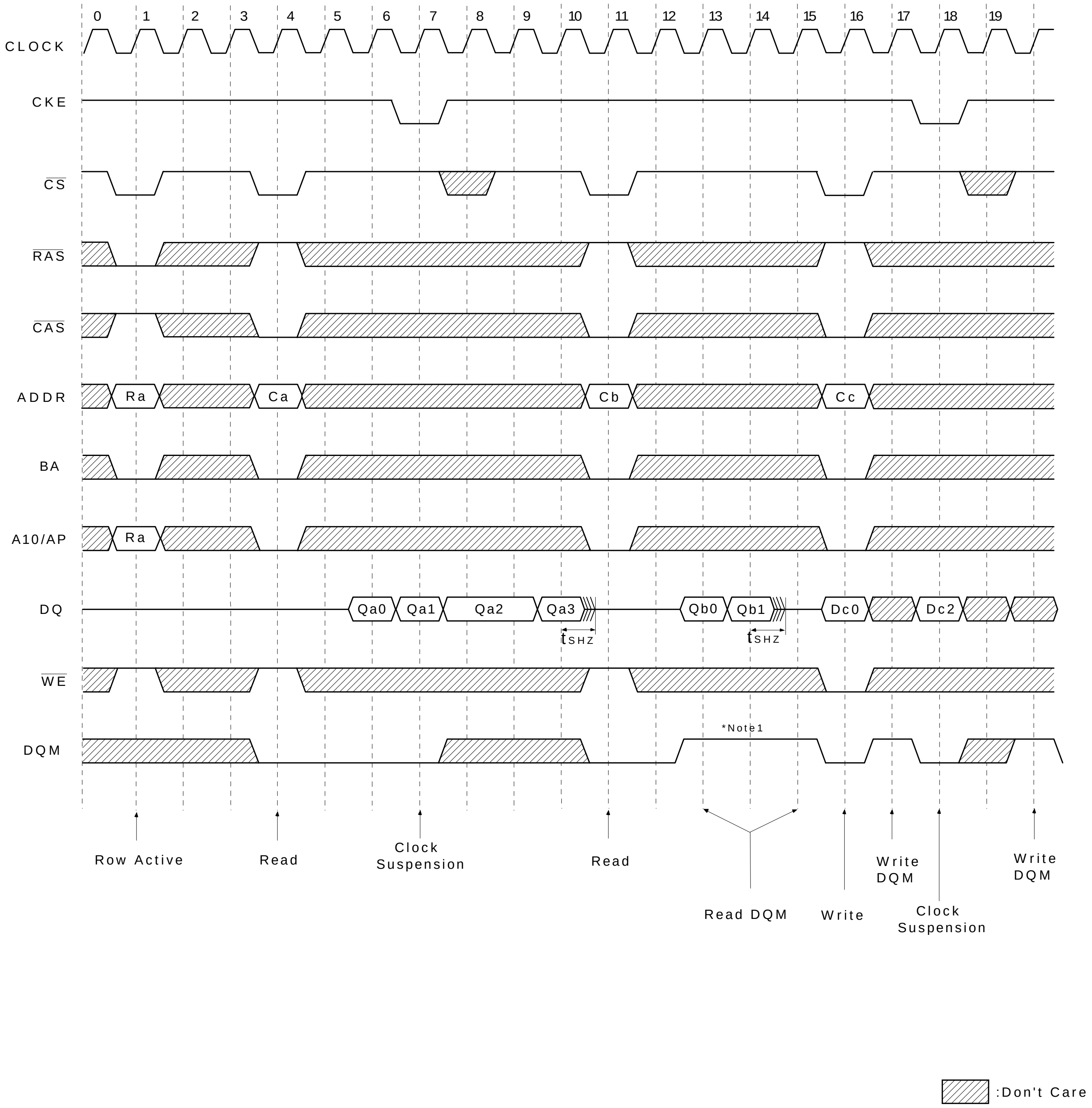
Read & Write Cycle with auto Precharge @ Burst Length =4



*Note: 1.t_{CDL} Should be controlled to meet minimum t_{RAS} before internal precharge start

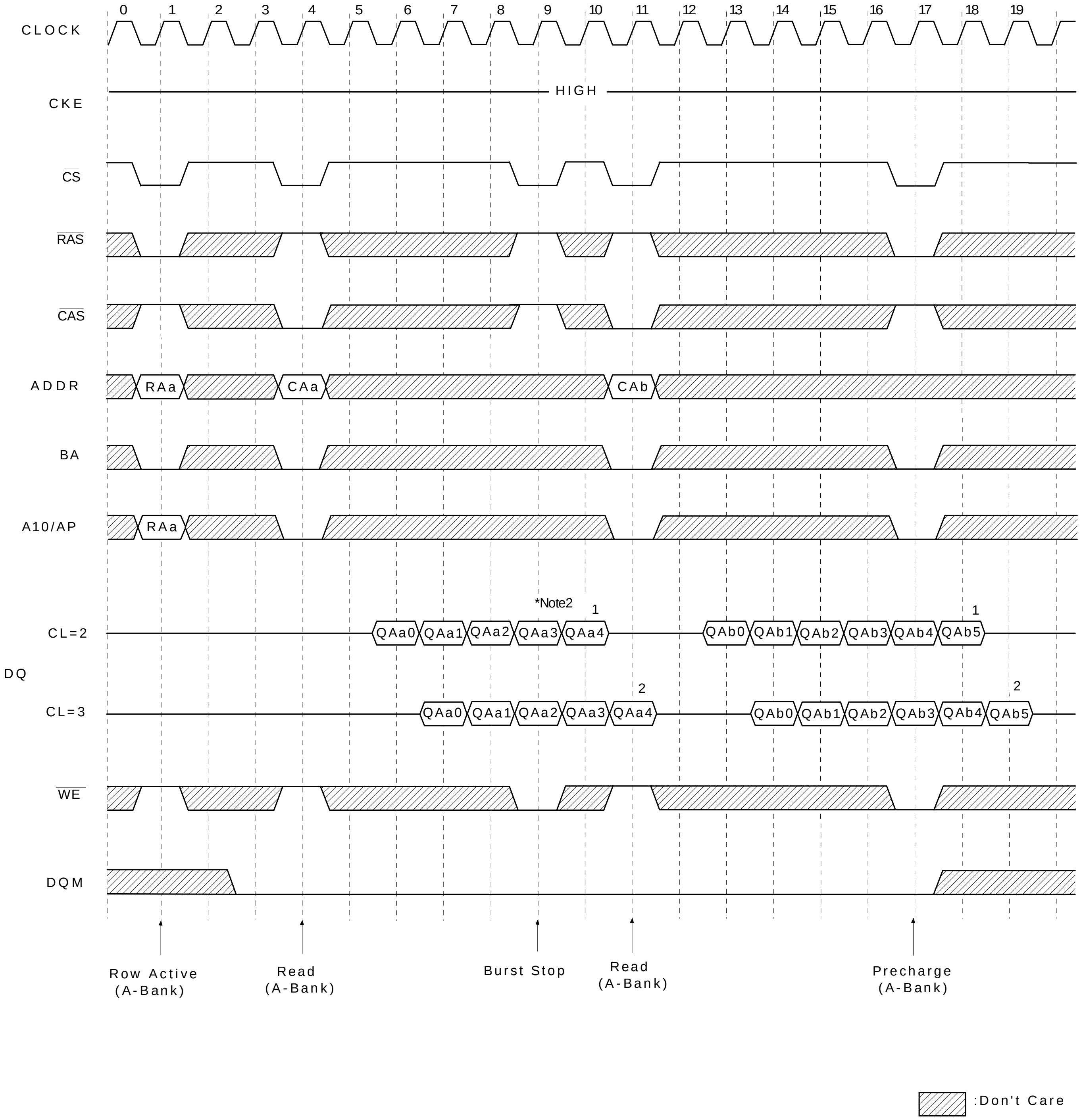
(In the case of Burst Length=1 & 2 and BRSW mode)

Clock Suspension & DQM Operation Cycle @CAS Latency=2, Burst Length=4



*Note:1.DQM is needed to prevent bus contention.

Read Interrupted by Precharge Command & Read Burst Stop Cycle @Burst Length =Full page



***Note:** 1.Burst can't end in full page mode, so auto precharge can't issue.

2.About the valid DQs after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt.

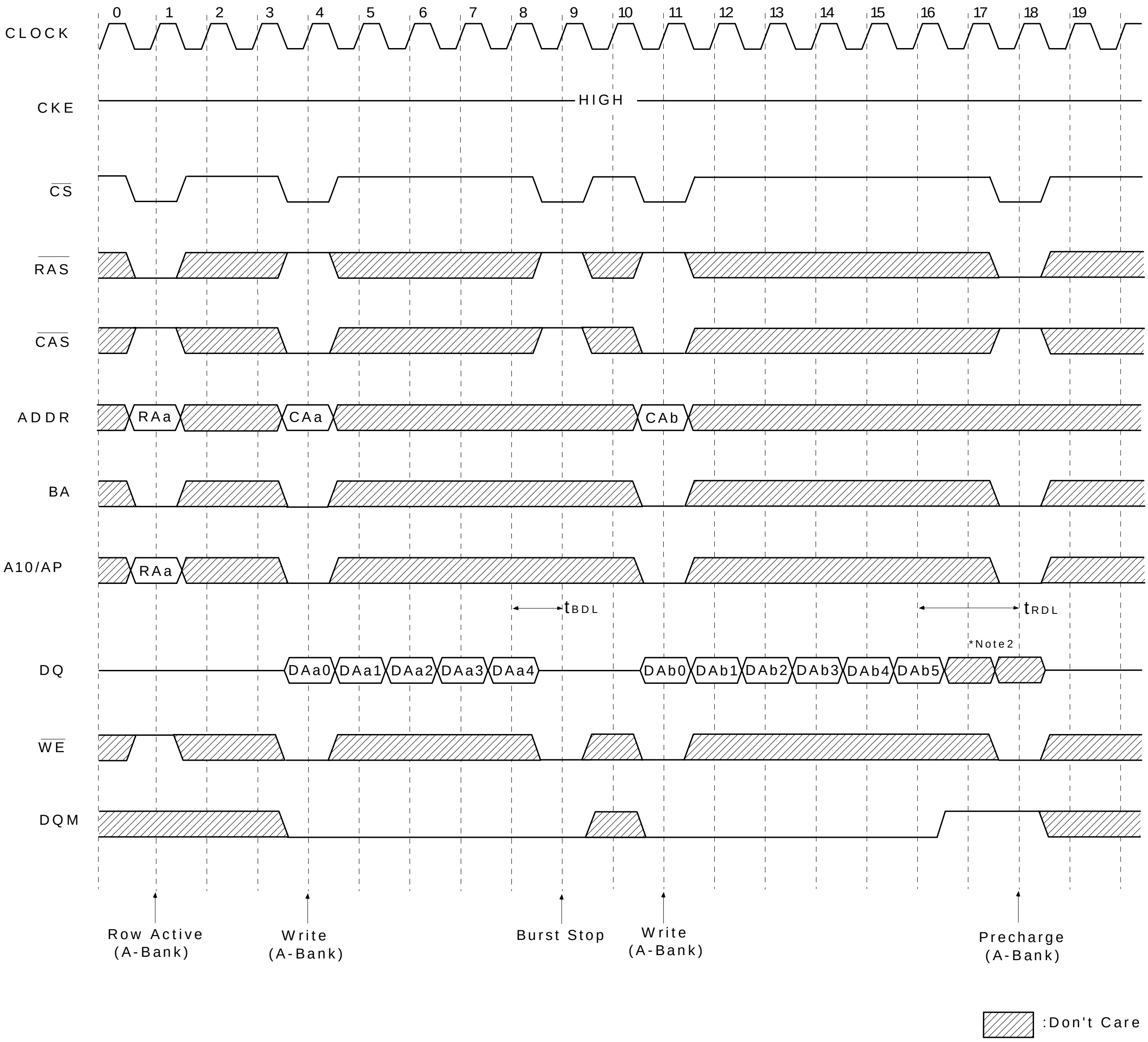
Both cases are illustrated above timing diagram. See the label 1,2 on them.

But at burst write, burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully.

Refer the timing diagram of "Full page write burst stop cycle".

3.Burst stop is valid at every burst length.

Write Interrupted by Precharge Command & Write Burst stop Cycle @ Burst Length =Full page



***Note:** 1. Burst can’t end in full page mode, so auto precharge can’t issue.

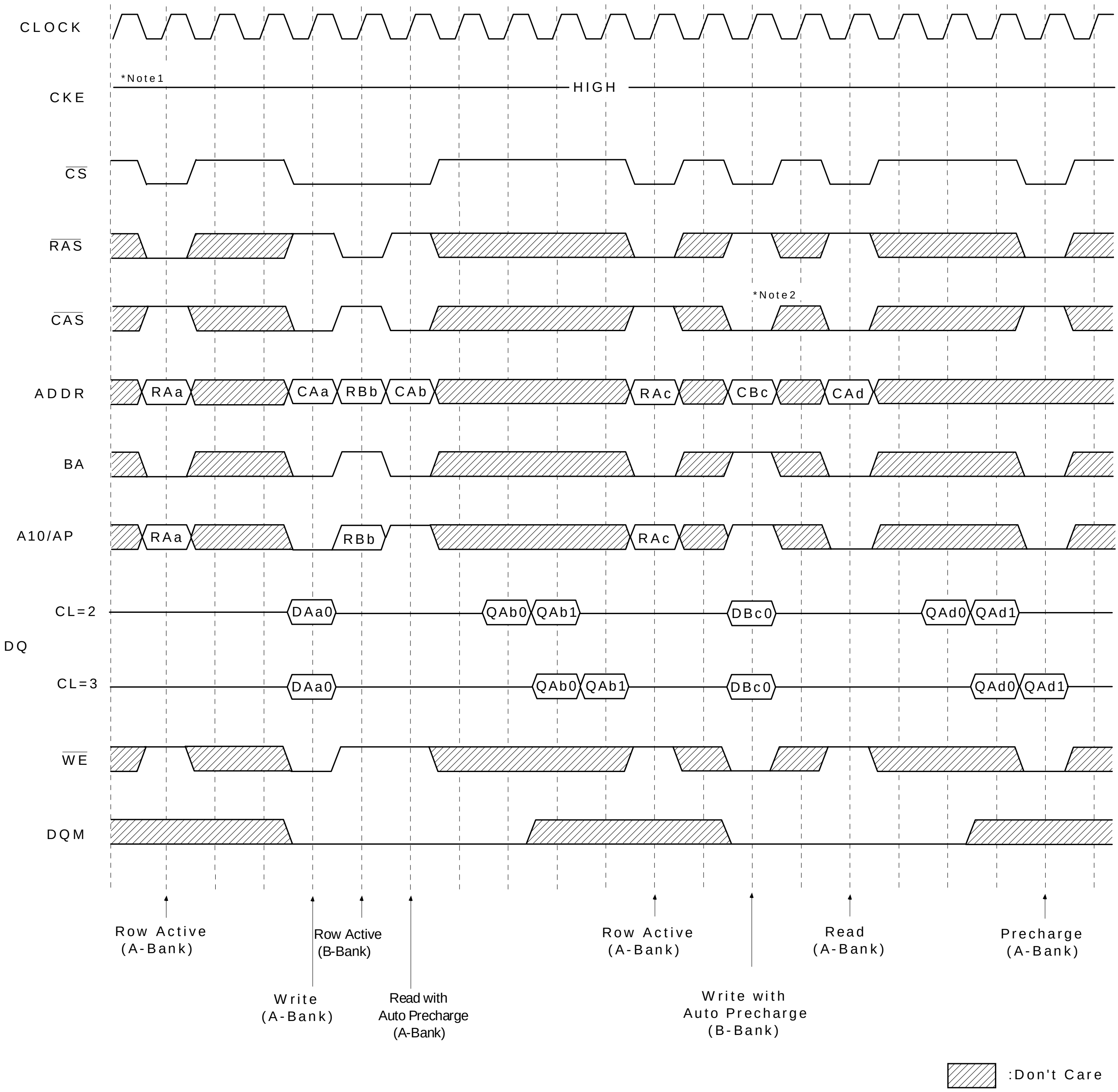
2.Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.

DQM at write interrupted by precharge command is needed to prevent invalid write.

Input data after Row precharge cycle will be masked internally.

3.Burst stop is valid at every burst length.

Burst Read Single bit Write Cycle @Burst Length=2



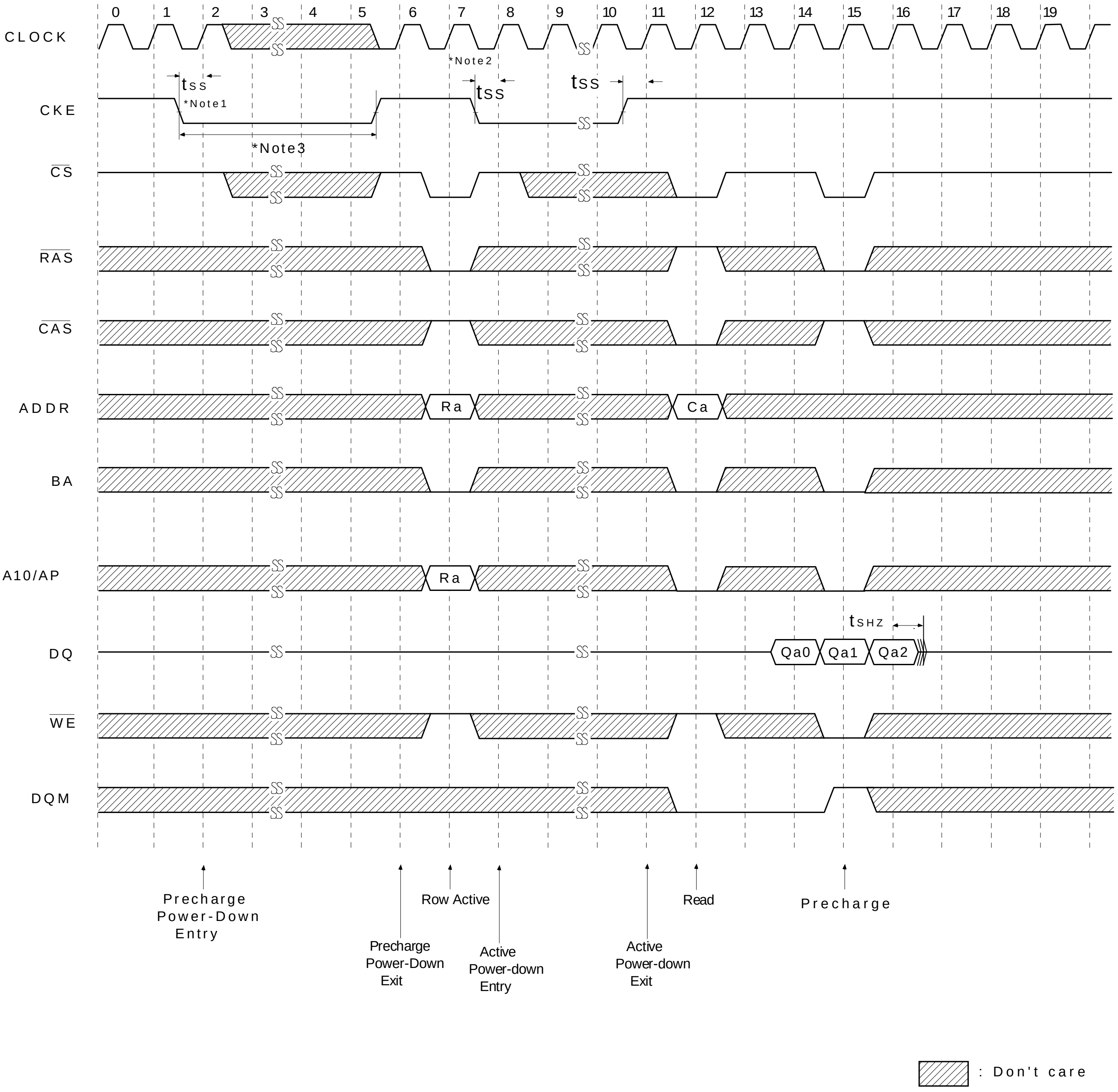
*Note:1.BRSW modes is enabled by setting A9 “High” at MRS(Mode Register Set).

At the BRSW Mode, the burst length at write is fixed to “1” regardless of programmed burst length.

2.When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.

Auto precharge is executed at the next cycle of burst-end, so in the case of BRSW write command, the precharge command will be issued after two clock cycles.

Active/Precharge Power Down Mode @CAS Latency=2, Burst Length=4

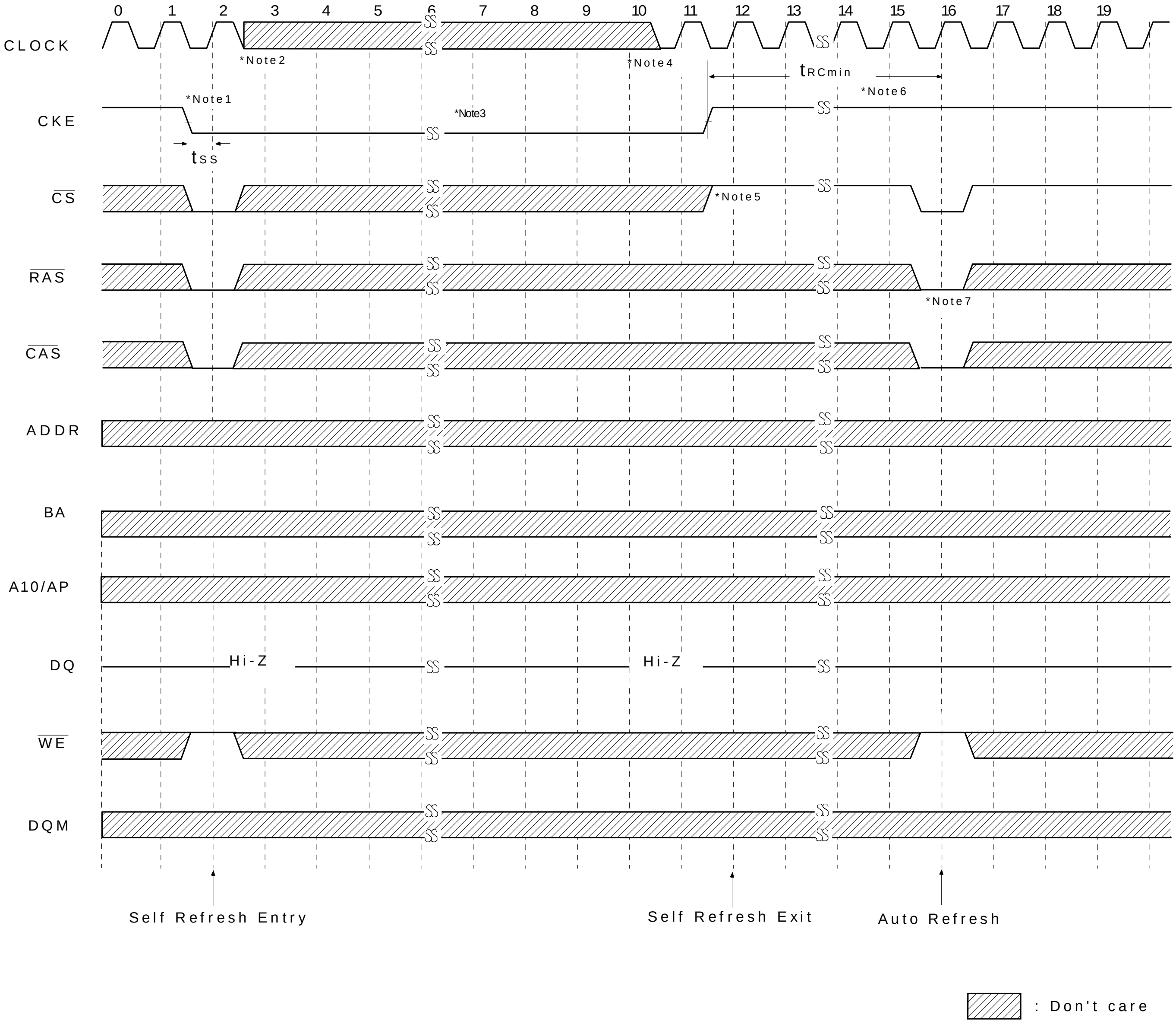


***Note :**1.Both banks should be in idle state prior to entering precharge power down mode.

2.CKE should be set high at least 1CLK+tss prior to Row active command.

3.Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



***Note: TO ENTER SELF REFRESH MODE**

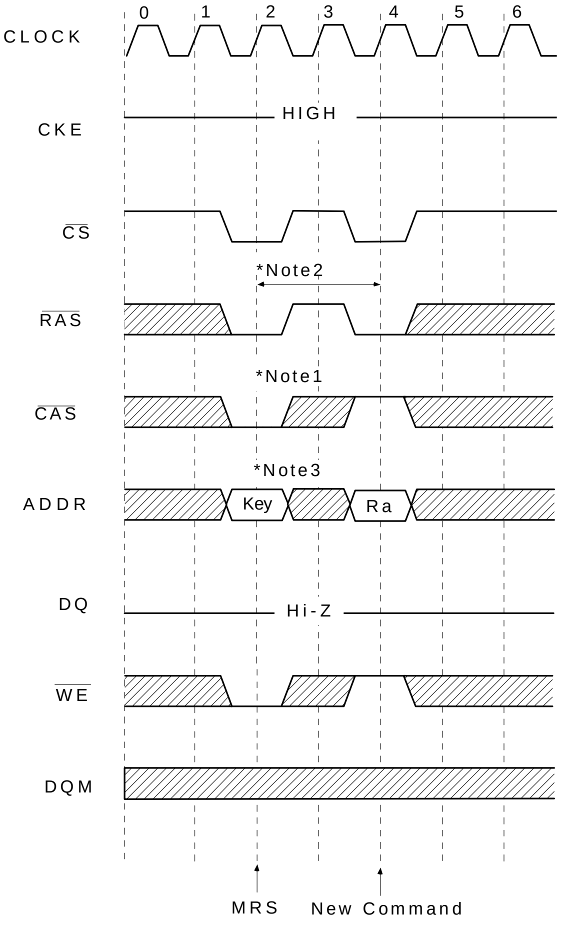
1. $\overline{CS}$, $\overline{RAS}$ & $\overline{CAS}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don’t care except for CKE.
3. The device remains in self refresh mode as long as CKE stays “Low”.

cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

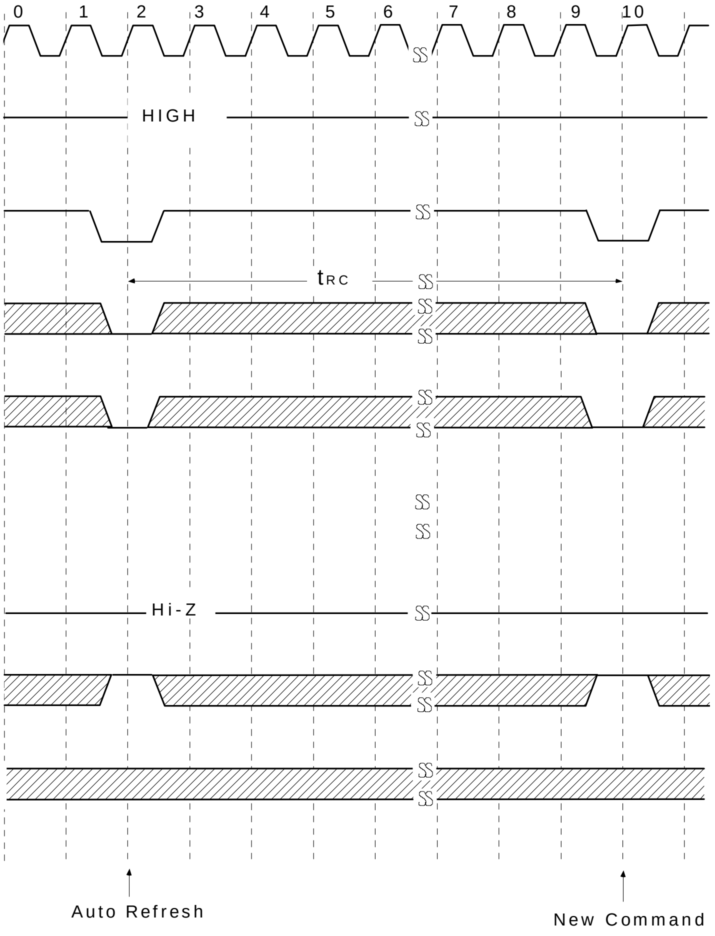
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ Starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



▨ :Don't Care

*Both banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

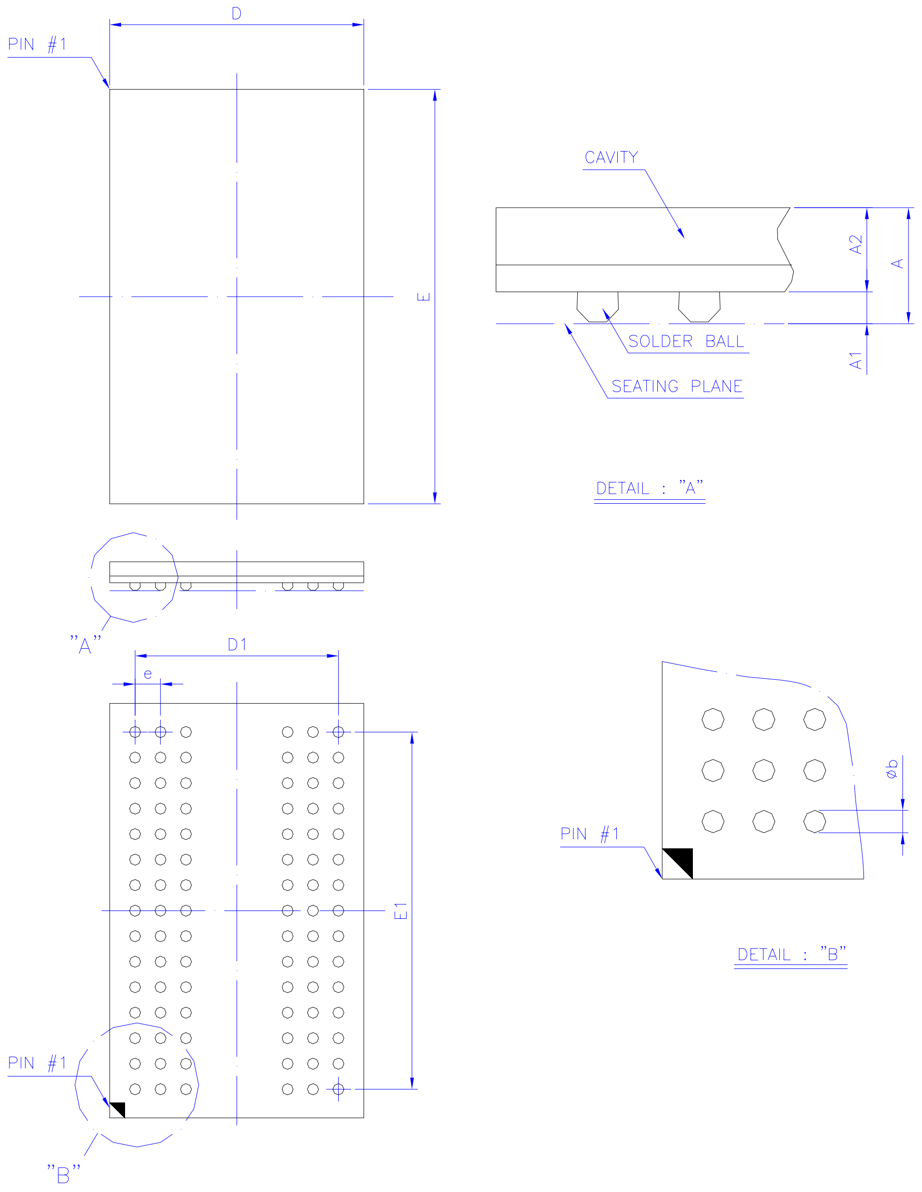
MODE REGISTER SET CYCLE

*Note: 1. $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ & $\overline{\text{WE}}$ activation at the same clock cycle with address key will set internal mode register.

2.Minimum 2 clock cycles should be met before new $\overline{\text{RAS}}$ activation.

3.Please refer to Mode Register Set table.

PACKING DIMENSIONS
90-BALL SDRAM (8x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.40	——	——	0.055
A_1	0.30	——	0.40	0.012	——	0.016
A_2	0.84	0.89	0.94	0.033	0.035	0.037
$Ø_b$	0.40	——	0.50	0.016	——	0.020
D	7.90	8.00	8.10	0.311	0.315	0.319
E	12.90	13.00	13.10	0.508	0.512	0.516
D_1	——	6.40	——	——	0.252	——
E_1	——	11.20	——	——	0.441	——
e	——	0.80	——	——	0.031	——

Controlling dimension : Millimeter.

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