

## DRAM MODULE

### M53230400DW0/DB0 & M53230410DW0/DB0 EDO Mode

4M x 32 DRAM SIMM using 4Mx4, 4K/2K Refresh, 5V

#### GENERAL DESCRIPTION

The Samsung M5323040(1)0D is a 4Mx32bits Dynamic RAM high density memory module. The Samsung M5323040(1)0D consists of eight CMOS 4Mx4bits DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M5323040(1)0D is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

#### PERFORMANCE RANGE

Speed	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>HPC</sub>
-50	50ns	13ns	90ns	25ns
-60	60ns	15ns	110ns	30ns

#### FEATURES

- Part Identification
  - M53230400DW0-C(4096 cycles/64ms Ref, SOJ, Solder)
  - M53230400DB0-C(4096 cycles/64ms Ref, SOJ, Gold)
  - M53230410DW0-C(2048 cycles/32ms Ref, SOJ, Solder)
  - M53230410DB0-C(2048 cycles/32ms Ref, SOJ, Gold)
- Extended Data Out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 1st Gen. JEDEC standard PDPin & pinout
- PCB : Height(1000mil), single sided component

#### PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	$\overline{\text{Vss}}$
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ17	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ18	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ19	45	Res( $\overline{\text{RAS1}}$ )
10	Vcc	46	NC
11	NC	47	$\overline{\text{W}}$
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	Res( $\overline{\text{RAS1}}$ )	69	PD3
34	$\overline{\text{RAS0}}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

#### PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}$	Row Address Strobe
$\overline{\text{CAS0}}$ - $\overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

#### PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	Vss	Vss
PD2	NC	NC
PD3	Vss	NC
PD4	Vss	NC

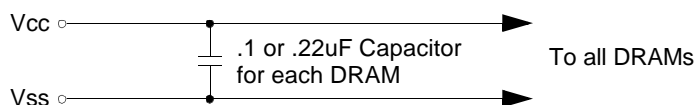
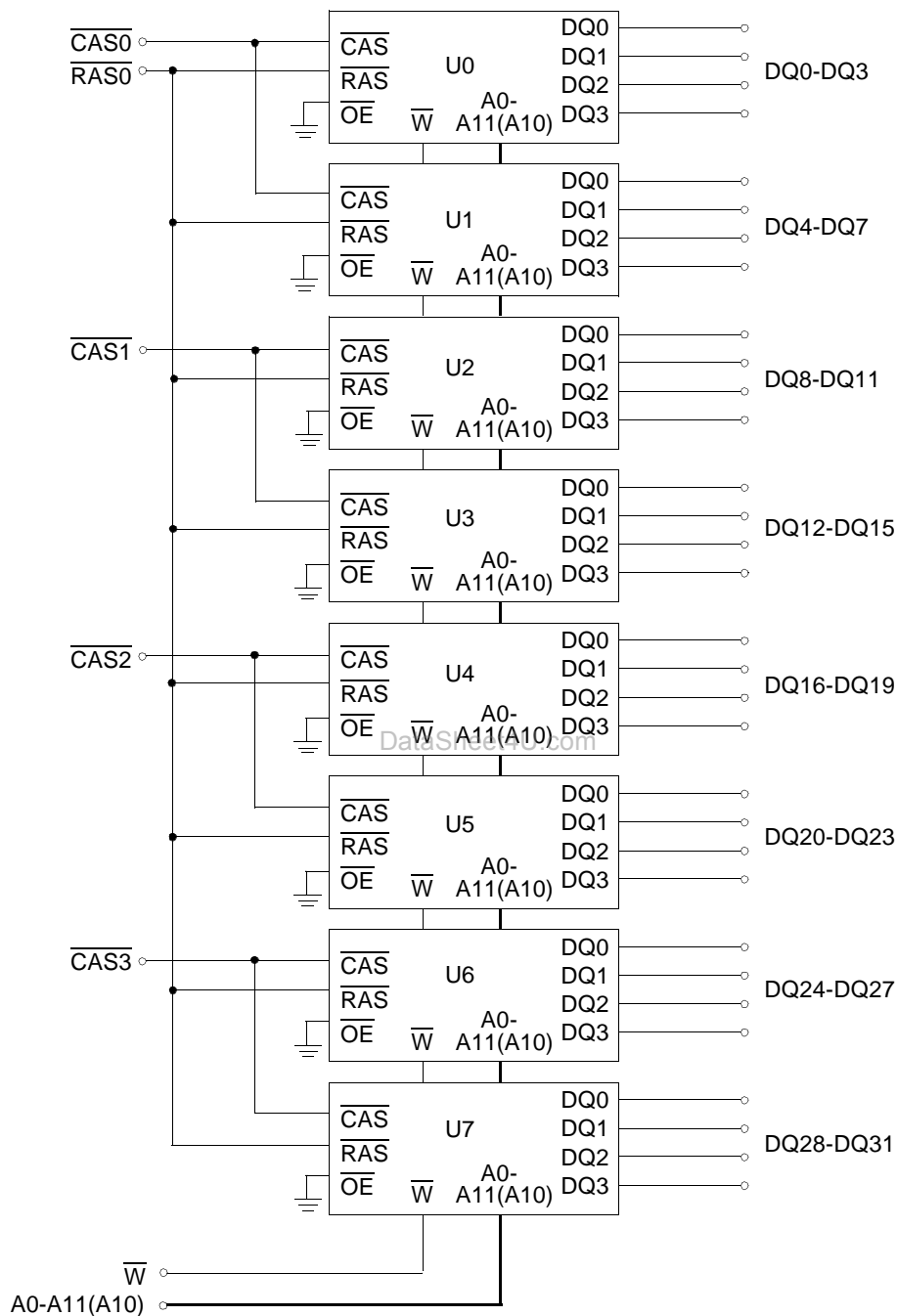
\* Pin connection changing available

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\* NOTE : A11 is used for only M53230400DW0/DB0 (4K ref.)

## DRAM MODULE

## FUNCTIONAL BLOCK DIAGRAM



# DRAM MODULE

## ABSOLUTE MAXIMUM RATINGS \*

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V <sub>CC</sub>	-1 to +7.0	V
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Power Dissipation	P <sub>d</sub>	8	W
Short Circuit Output Current	I <sub>OS</sub>	50	mA

\* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +1 <sup>*1</sup>	V
Input Low Voltage	V <sub>IL</sub>	-1.0 <sup>*2</sup>	-	0.8	V

\*1 : V<sub>CC</sub>+2.0V/20ns, Pulse width is measured at V<sub>CC</sub>.

\*2 : -2.0V/20ns, Pulse width is measured at V<sub>SS</sub>.

## DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230400DW0/DB0		M53230410DW0/DB0		Unit
		Min	Max	Min	Max	
I <sub>CC1</sub>	-50	-	720	-	880	mA
	-60	-	640	-	800	mA
I <sub>CC2</sub>	Don't care	-	16	-	16	mA
I <sub>CC3</sub>	-50	-	720	-	880	mA
	-60	-	640	-	800	mA
I <sub>CC4</sub>	-50	-	640	-	720	mA
	-60	-	560	-	640	mA
I <sub>CC5</sub>	Don't care	-	8	-	8	mA
I <sub>CC6</sub>	-50	-	720	-	880	mA
	-60	-	640	-	800	mA
I <sub>I(L)</sub> I <sub>O(L)</sub>	Don't care	-40	40	-40	40	uA
		-5	5	-5	5	uA
V <sub>OH</sub> V <sub>OL</sub>	Don't care	2.4	-	2.4	-	V
		-	0.4	-	0.4	V

I<sub>CC1</sub> : Operating Current \* ( $\overline{RAS}$ ,  $\overline{CAS}$ , Address cycling @trc=min)

I<sub>CC2</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$ )

I<sub>CC3</sub> :  $\overline{RAS}$  Only Refresh Current \* ( $\overline{CAS}=V_{IH}$ ,  $\overline{RAS}$  cycling @trc=min)

I<sub>CC4</sub> : EDO Mode Current \* ( $\overline{RAS}=V_{IL}$ ,  $\overline{CAS}$  Address cycling : t<sub>HPC</sub>=min)

I<sub>CC5</sub> : Standby Current ( $\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$ )

I<sub>CC6</sub> :  $\overline{CAS}$ -Before- $\overline{RAS}$  Refresh Current \* ( $\overline{RAS}$  and  $\overline{CAS}$  cycling @trc=min)

I<sub>I(L)</sub> : Input Leakage Current (Any input 0≤V<sub>IN</sub>≤V<sub>CC</sub>+0.5V, all other pins not under test=0 V)

I<sub>O(L)</sub> : Output Leakage Current(Data Out is disabled, 0V≤V<sub>OUT</sub>≤V<sub>CC</sub>)

V<sub>OH</sub> : Output High Voltage Level (I<sub>OH</sub> = -5mA)

V<sub>OL</sub> : Output Low Voltage Level (I<sub>OL</sub> = 4.2mA)

\* **NOTE** : I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC6</sub> are dependent on output loading and cycle rates. Specified values are obtained with the output open. I<sub>CC</sub> is specified as an average current. In I<sub>CC1</sub> and I<sub>CC3</sub>, address can be changed maximum once while  $\overline{RAS}=V_{IL}$ . In I<sub>CC4</sub>, address can be changed maximum once within one EDO mode cycle, t<sub>HPC</sub>.

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## CAPACITANCE (TA = 25°C, VCC=5V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	55	pF
Input capacitance[W]	CIN2	-	70	pF
Input capacitance[RAS0]	CIN3	-	70	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	30	pF
Input/Output capacitance[DQ0-31]	CDQ1	-	20	pF

## AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=5.0V±10%. See notes 1,2.)

Test condition : Vih/Vii=2.4/0.8V, Voh/Vol=2.0/0.8V, output loading CL=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	90		110		ns	
Access time from $\overline{\text{RAS}}$	tRAC		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	tCAC		13		15	ns	3,4,5
Access time from column address	tAA		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	tCLZ	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	tCEZ	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	tt	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	tRP	30		40		ns	
$\overline{\text{RAS}}$ pulse width	tRAS	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	tRSH	13		15		ns	
$\overline{\text{CAS}}$ hold time	tCSH	38		45		ns	
$\overline{\text{CAS}}$ pulse width	tCAS	8	10K	10	10K	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	tRCD	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	tRAD	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	tCRP	5		5		ns	
Row address set-up time	tASR	0		0		ns	
Row address hold time	tRAH	10		10		ns	
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	tRAL	25		30		ns	
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	tRCH	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	tRRH	0		0		ns	8
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	tRWL	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	tCWL	8		10		ns	
Data-in set-up time	tDS	0		0		ns	9
Data-in hold time	tDH	8		10		ns	9
Refresh period (4K Ref)	tREF		64		64	ms	
Refresh period (2K Ref)	tREF		32		32	ms	
Write command set-up time	tWCS	0		0		ns	7
$\overline{\text{CAS}}$ setup time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCSR	5		5		ns	
$\overline{\text{CAS}}$ hold time( $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	tCHR	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	tRPC	5		5		ns	

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AC CHARACTERISTICS (0°C≤T<sub>A</sub>≤70°C, V<sub>CC</sub>=5.0V±10%. See notes 1,2.)Test condition : V<sub>IH</sub>/V<sub>IL</sub>=2.4/0.8V, V<sub>OH</sub>/V<sub>OL</sub>=2.0/0.8V, output loading CL=100pF

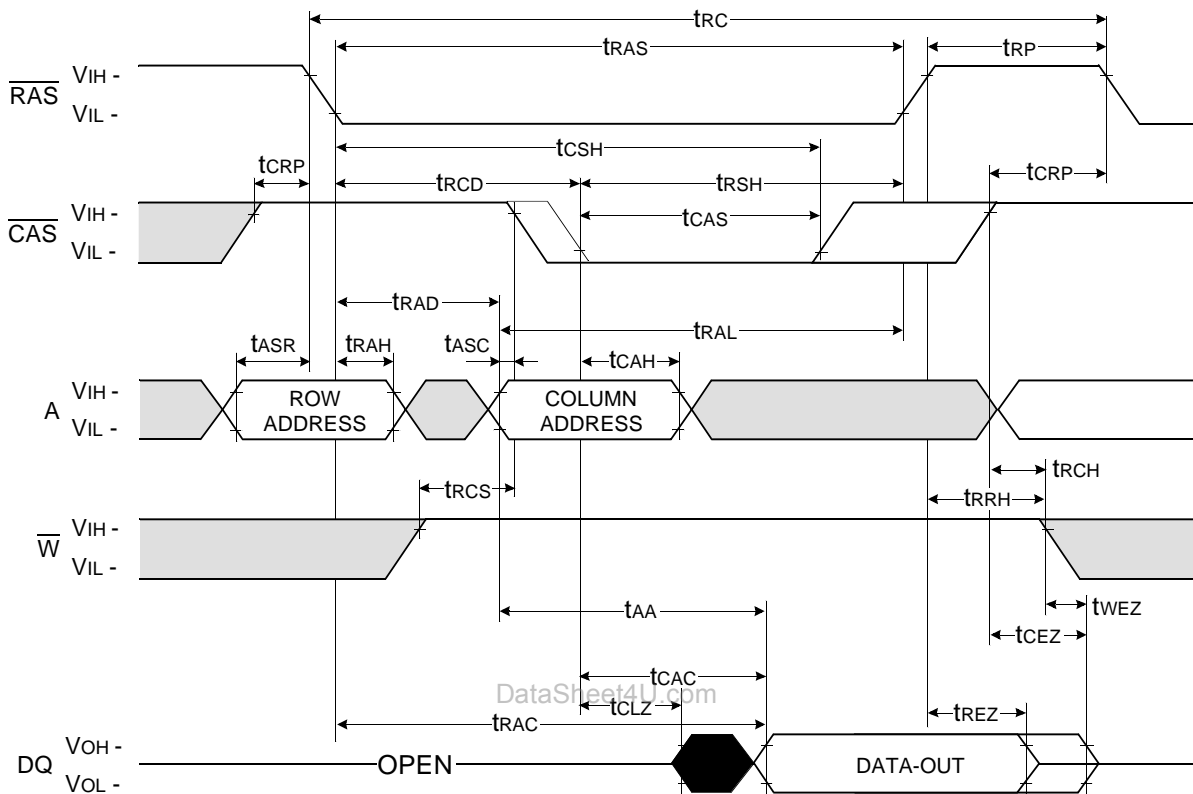
Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
CAS precharge time (C-B-R counter test)	tCPT	20		20		ns	
Access time from CAS precharge	tCPA		30		35	ns	3
Hyper page mode cycle time	tHPC	25		30		ns	13
CAS precharge time(Hyper page cycle)	tCP	8		10		ns	
RAS pulse width(Hyper page cycle)	tRASP	50	200K	60	200K	ns	
RAS hold time from CAS precharge	tRHCP	30		35		ns	
W to RAS precharge time(C-B-R refresh)	tWRP	10		10		ns	
W to RAS hold time(C-B-R refresh)	tWRH	10		10		ns	
Output data hold time	tDOH	5		5		ns	
Output buffer turn off delay from RAS	tREZ	3	13	3	15	ns	7,11,12
Output buffer turn off delay from W	tWEZ	3	13	3	15	ns	7,11
W to data delay	tWED	15		15		ns	
W pulse width (Hyper Page Cycle)	tWPE	5		5		ns	

## NOTES

- An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
- V<sub>IH</sub>(min) and V<sub>IL</sub>(max) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub>(min) and V<sub>IL</sub>(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t<sub>RC</sub>D(max) limit insures that t<sub>RC</sub>A(max) can be met. t<sub>RC</sub>D(max) is specified as a reference point only. If t<sub>RC</sub>D is greater than the specified t<sub>RC</sub>D(max) limit, then access time is controlled exclusively by t<sub>C</sub>A<sub>C</sub>.
- Assumes that t<sub>RC</sub>D≥t<sub>RC</sub>D(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
- t<sub>W</sub>C<sub>S</sub> is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t<sub>W</sub>C<sub>S</sub>≥t<sub>W</sub>C<sub>S</sub>(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t<sub>TR</sub>CH or t<sub>TR</sub>RH must be satisfied for a read cycle.
- These parameter are referenced to the CAS leading edge in early write cycles and to the W leading edge in read-write cycles.
- Operation within the t<sub>TR</sub>A<sub>D</sub>(max) limit insures that t<sub>TR</sub>A<sub>C</sub>(max) can be met. t<sub>TR</sub>A<sub>D</sub>(max) is specified as reference point only. If t<sub>TR</sub>A<sub>D</sub> is greater than the specified t<sub>TR</sub>A<sub>D</sub>(max) limit, then access time is controlled by t<sub>A</sub>A.
- t<sub>C</sub>E<sub>Z</sub>(max), t<sub>R</sub>E<sub>Z</sub>(max), t<sub>W</sub>E<sub>Z</sub>(max) and t<sub>O</sub>E<sub>Z</sub>(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.
- t<sub>A</sub>S<sub>C</sub>≥t<sub>C</sub>P min

# DRAM MODULE

## READ CYCLE



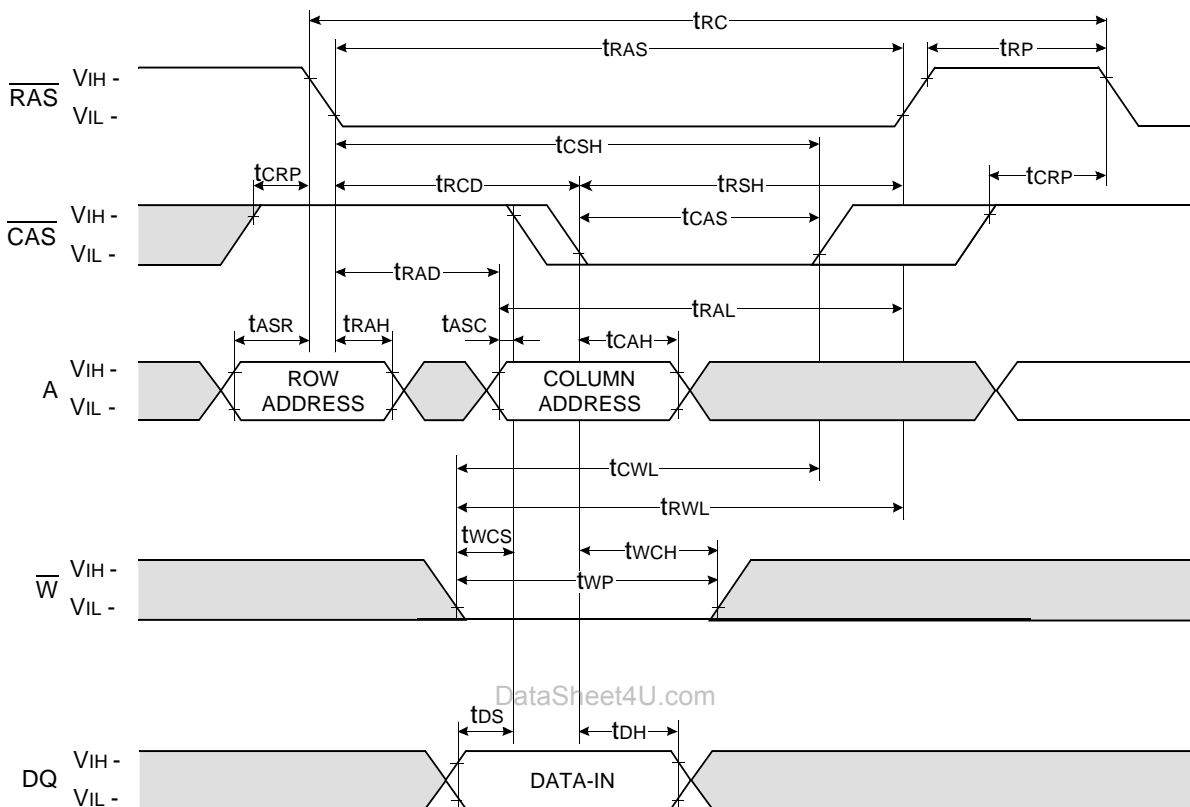
Don't care  
 Undefined



## DRAM MODULE

## WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



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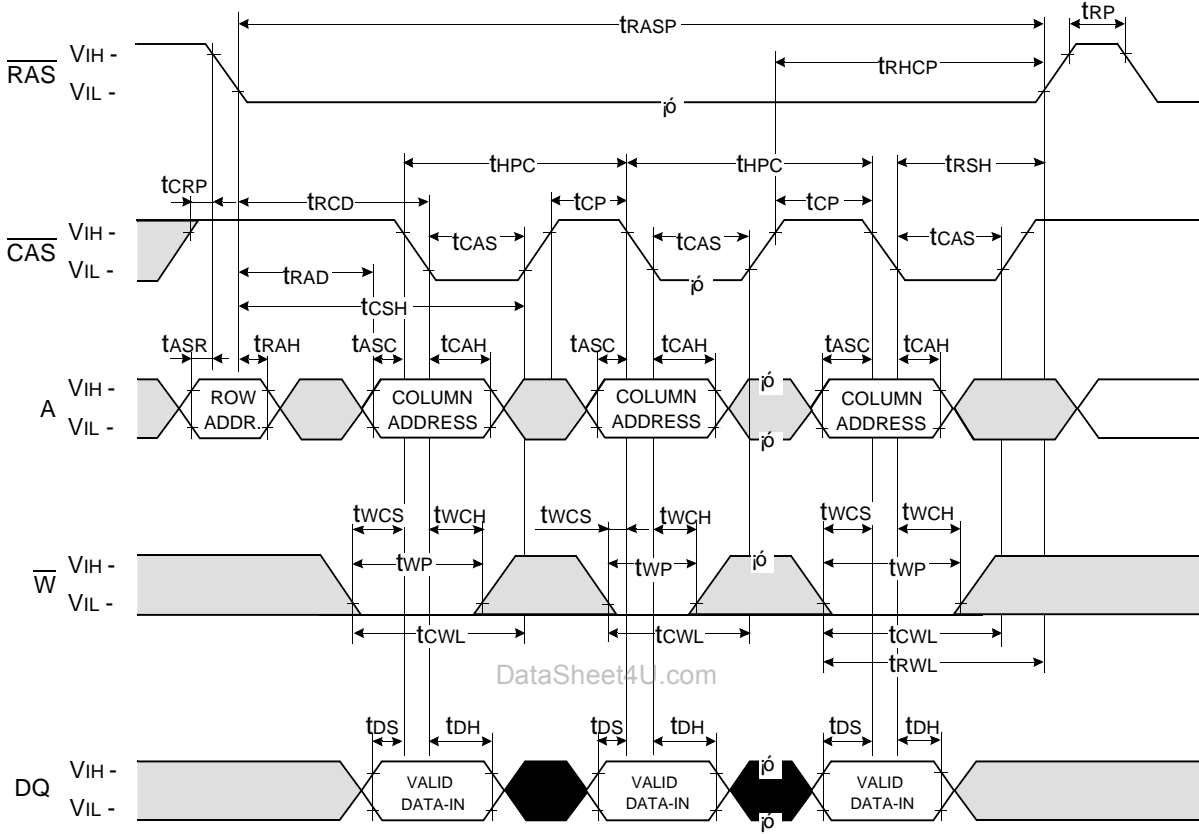




DRAM MODULE

HYPER PAGE WRITE CYCLE ( EARLY WRITE )

NOTE : DOUT = OPEN



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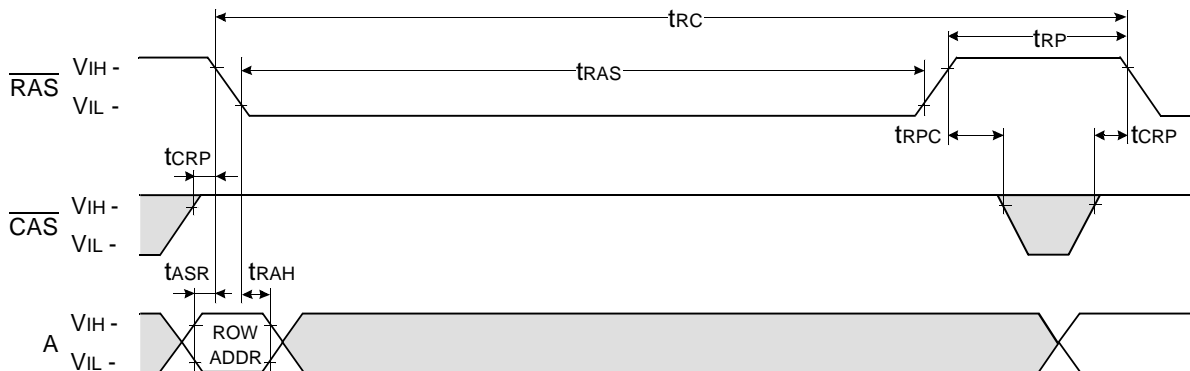
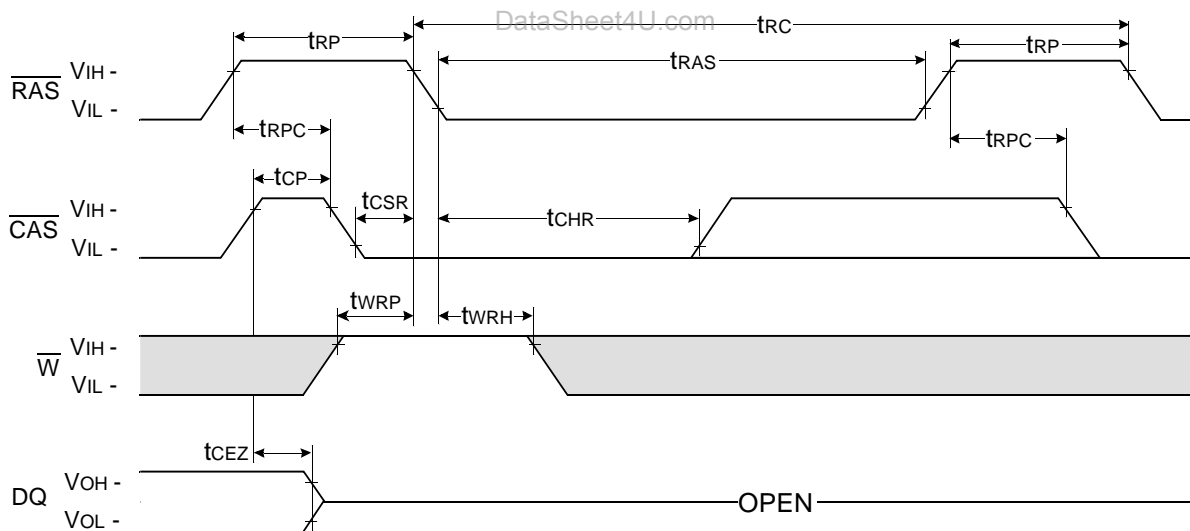
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## DRAM MODULE

 **$\overline{\text{RAS}}$  - ONLY REFRESH CYCLE\***NOTE :  $\overline{\text{W}}$ ,  $\overline{\text{OE}}$ , DIN = Don't care

DOUT = OPEN

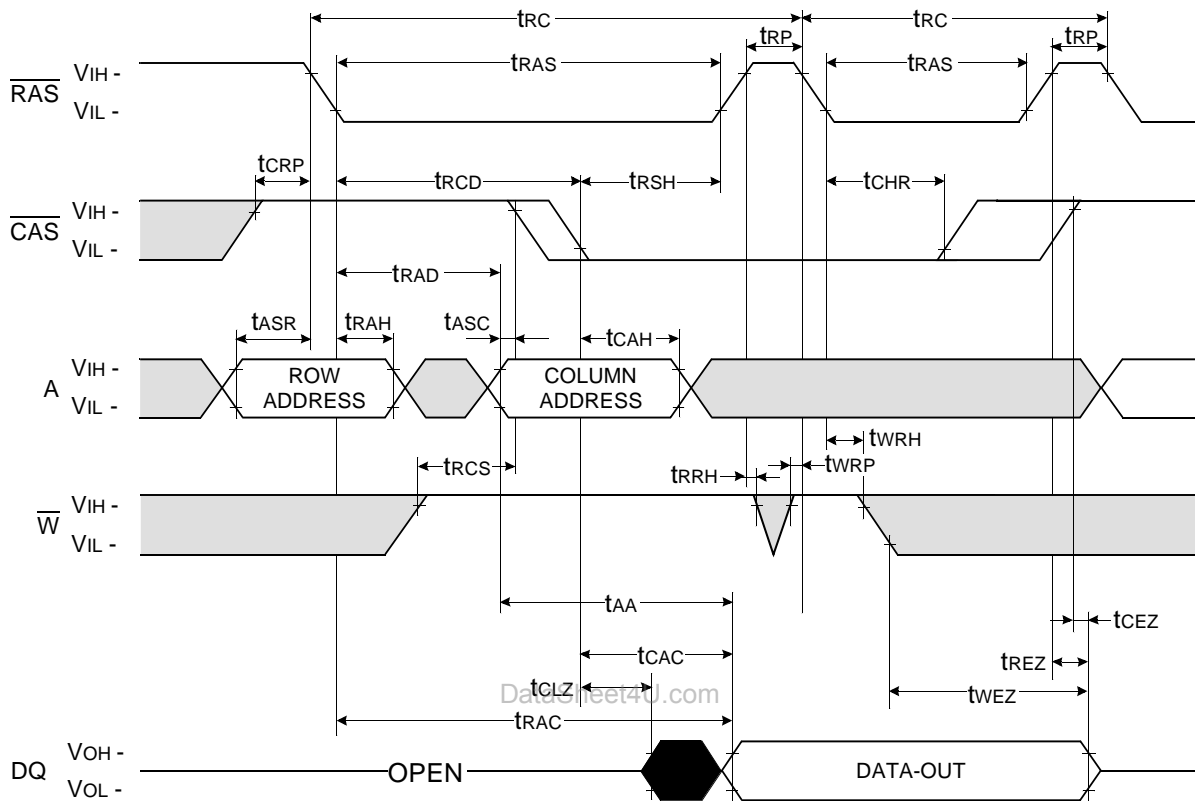
 **$\overline{\text{CAS}}$  - BEFORE -  $\overline{\text{RAS}}$  REFRESH CYCLE**NOTE :  $\overline{\text{OE}}$ , A = Don't care

□ Don't care  
■ Undefined

\* In  $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when  $\overline{\text{CAS}}$  signal transits from Low to High, the valid data may be cut off.

# DRAM MODULE

## HIDDEN REFRESH CYCLE ( READ )



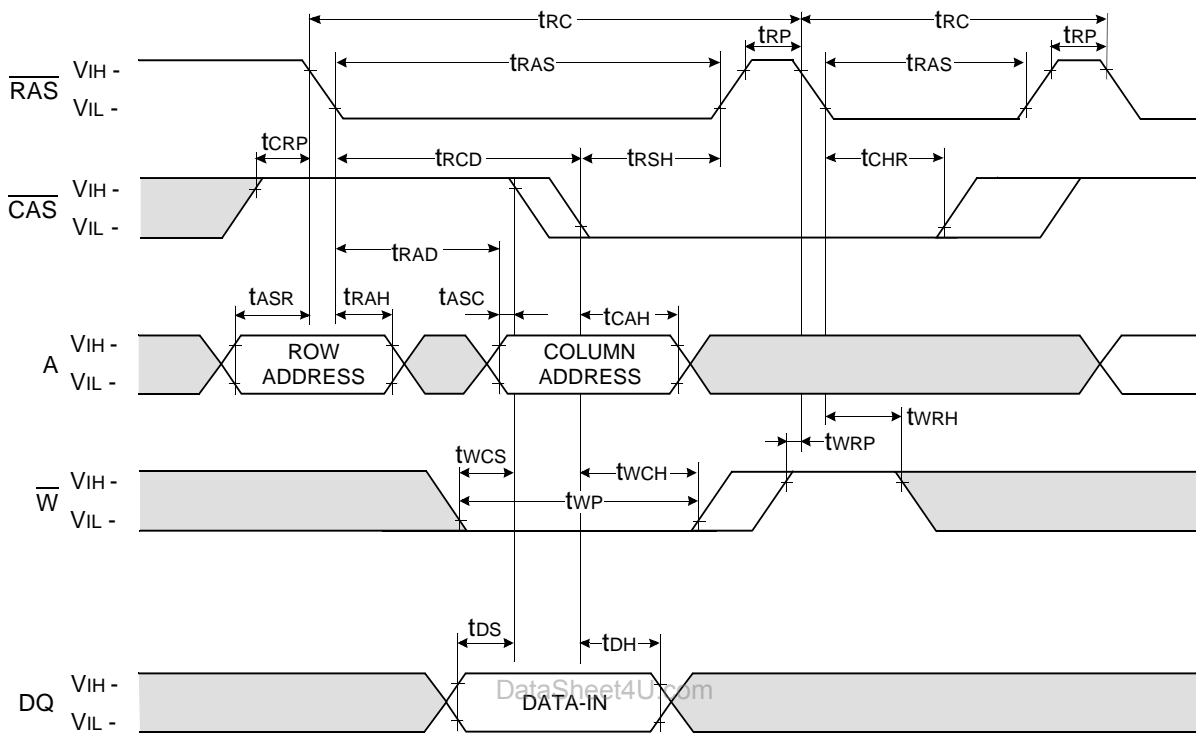
Don't care  
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# DRAM MODULE

## HIDDEN REFRESH CYCLE ( WRITE )

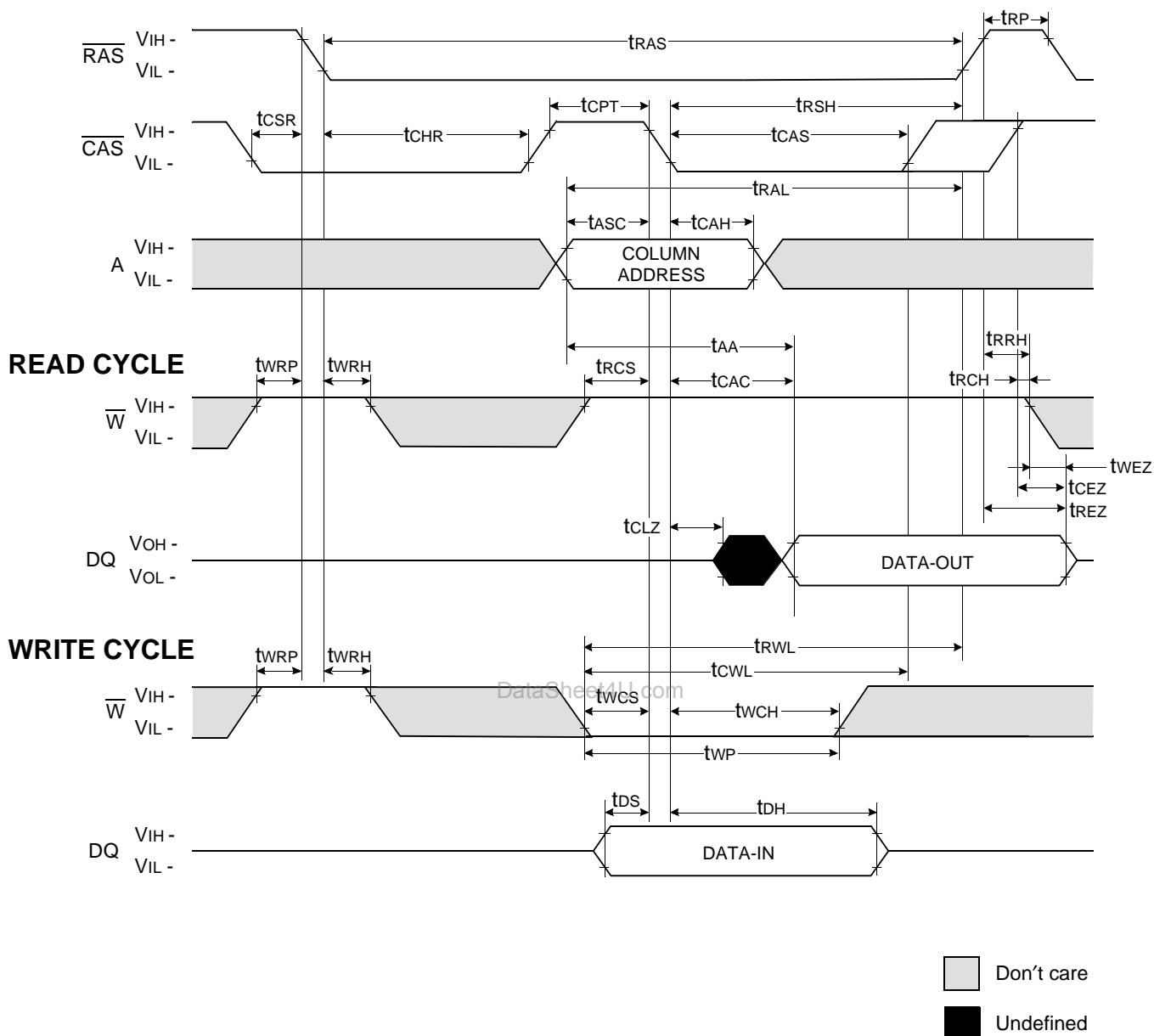
NOTE : DOUT = OPEN



Don't care  
 Undefined



## DRAM MODULE

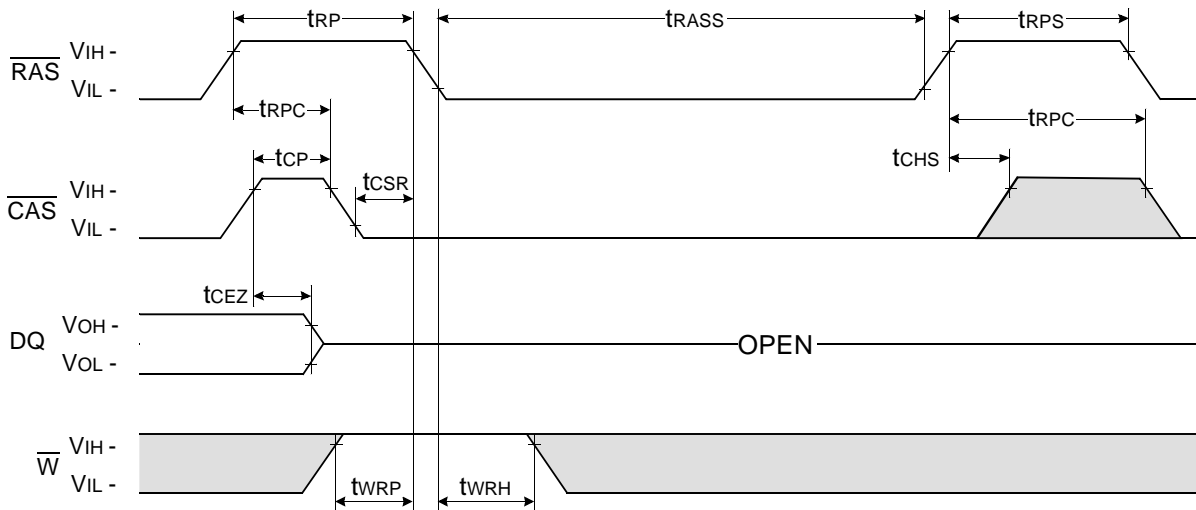
**CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE**

NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

# DRAM MODULE

## $\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE :  $\overline{\text{OE}}$ , A = Don't care



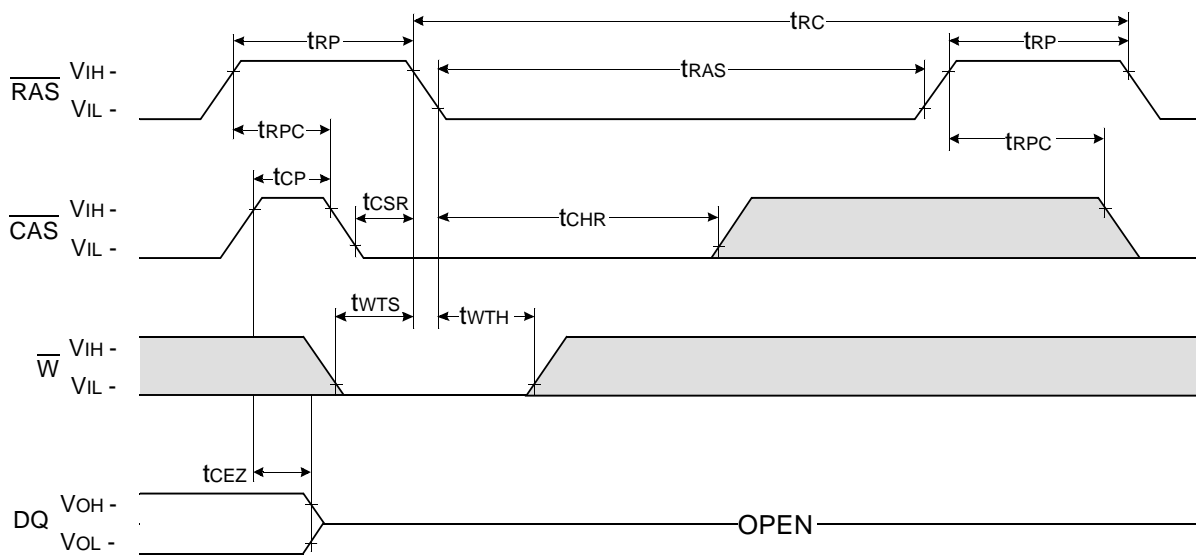
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## TEST MODE IN CYCLE

NOTE :  $\overline{\text{OE}}$ , A = Don't care

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□ Don't care  
■ Undefined



