

M53230800CW0/CB0 M53230810CW0/CB0

DRAM MODULE

M53230800CW0/CB0 & M53230810CW0/CB0 EDO Mode

8M x 32 DRAM SIMM using 4Mx4, 4K/2K Refresh, 5V

GENERAL DESCRIPTION

The Samsung M5323080(1)0C is a 8Mx32bits Dynamic RAM high density memory module. The Samsung M5323080(1)0C consists of sixteen CMOS 4Mx4bits DRAMs in 24-pin SOJ package mounted on a 72-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M5323080(1)0C is a Single In-line Memory Module with edge connections and is intended for mounting into 72 pin edge connector sockets.

PERFORMANCE RANGE

Speed	tRAC	tCAC	tRC	tHPC
-50	50ns	13ns	90ns	25ns
-60	60ns	15ns	110ns	30ns

FEATURES

- Part Identification
 - M53230800CW0-C(4096 cycles/64ms Ref, SOJ, Solder)
 - M53230800CB0-C(4096 cycles/64ms Ref, SOJ, Gold)
 - M53230810CW0-C(2048 cycles/32ms Ref, SOJ, Solder)
 - M53230810CB0-C(2048 cycles/32ms Ref, SOJ, Gold)
- Extended Data Out
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- RAS-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V±10% power supply
- 1st Gen. JEDEC standard PDPin & pinout
- PCB : Height(1000mil), double sided component

PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol
1	Vss	37	NC
2	DQ0	38	NC
3	DQ16	39	$\overline{\text{Vss}}$
4	DQ1	40	$\overline{\text{CAS0}}$
5	DQ17	41	$\overline{\text{CAS2}}$
6	DQ2	42	$\overline{\text{CAS3}}$
7	DQ18	43	$\overline{\text{CAS1}}$
8	DQ3	44	$\overline{\text{RAS0}}$
9	DQ19	45	RAS1
10	Vcc	46	NC
11	NC	47	W
12	A0	48	NC
13	A1	49	DQ8
14	A2	50	DQ24
15	A3	51	DQ9
16	A4	52	DQ25
17	A5	53	DQ10
18	A6	54	DQ26
19	A10	55	DQ11
20	DQ4	56	DQ27
21	DQ20	57	DQ12
22	DQ5	58	DQ28
23	DQ21	59	Vcc
24	DQ6	60	DQ29
25	DQ22	61	DQ13
26	DQ7	62	DQ30
27	DQ23	63	DQ14
28	A7	64	DQ31
29	A11	65	DQ15
30	Vcc	66	NC
31	A8	67	PD1
32	$\overline{\text{A9}}$	68	PD2
33	$\overline{\text{RAS1}}$	69	PD3
34	$\overline{\text{RAS0}}$	70	PD4
35	NC	71	NC
36	NC	72	Vss

PIN NAMES

Pin Name	Function
A0 - A11	Address Inputs(4K Ref)
A0 - A10	Address Inputs(2K Ref)
DQ0 - DQ31	Data In/Out
$\overline{\text{W}}$	Read/Write Enable
$\overline{\text{RAS0}}, \overline{\text{RAS1}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
PD1 -PD4	Presence Detect
Vcc	Power(+5V)
Vss	Ground
NC	No Connection

PRESENCE DETECT PINS (Optional)

Pin	50NS	60NS
PD1	NC	NC
PD2	Vss	Vss
PD3	Vss	NC
PD4	Vss	NC

* Pin connection changing available

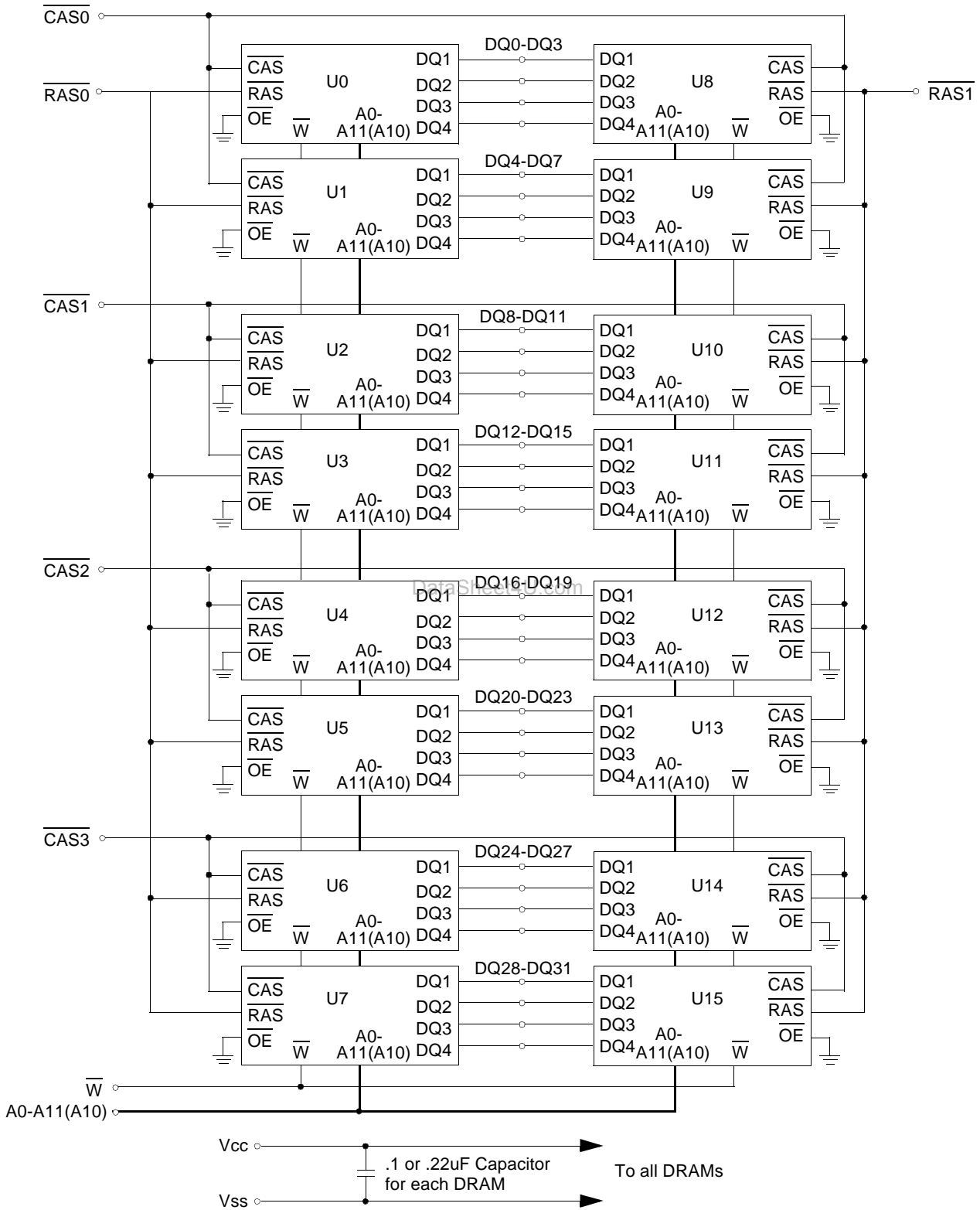
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* NOTE : A11 is used for only M53230800CW0/CB0 (4K ref.)



DRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



M53230800CW0/CB0

M53230810CW0/CB0

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ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1 to +7.0	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1 to +7.0	V
Storage Temperature	T _{stg}	-55 to +150	°C
Power Dissipation	P _d	16	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.4	-	V _{CC} +1 ^{*1}	V
Input Low Voltage	V _{IL}	-1.0 ^{*2}	-	0.8	V

*1 : V_{CC}+2.0V/20ns, Pulse width is measured at V_{CC}.

*2 : -2.0V/20ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M53230800CW0/CB0		M53230810CW0/CB0		Unit
		Min	Max	Min	Max	
I _{CC1}	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I _{CC2}	Don't care	-	32	-	32	mA
I _{CC3}	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I _{CC4}	-50	-	656	-	736	mA
	-60	-	576	-	656	mA
I _{CC5}	Don't care	-	16	-	16	mA
	-50	-	736	-	896	mA
I _{CC6}	-50	-	736	-	896	mA
	-60	-	656	-	816	mA
I _{I(L)}	Don't care	-80	80	-80	80	uA
		-10	10	-10	10	uA
V _{OH}	Don't care	2.4	-	2.4	-	V
		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{IH}$)

I_{CC3} : RAS Only Refresh Current * ($\overline{\text{CAS}}=V_{IH}$, $\overline{\text{RAS}}$ cycling @trc=min)

I_{CC4} : EDO Mode Current * ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$ Address cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=V_{CC}-0.2V$)

I_{CC6} : $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

V_{OH} : Output High Voltage Level (I_{OH} = -5mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 4.2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{\text{RAS}}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one EDO mode cycle, t_{HPC}.



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CAPACITANCE ($T_A = 25^\circ\text{C}$, $V_{CC}=5\text{V}$, $f = 1\text{MHz}$)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A11(A10)]	CIN1	-	100	pF
Input capacitance[W]	CIN2	-	130	pF
Input capacitance[RAS0, RAS1]	CIN3	-	70	pF
Input capacitance[CAS0 - CAS3]	CIN4	-	30	pF
Input/Output capacitance[$\overline{\text{DQ0-31}}$]	CDQ	-	20	pF

AC CHARACTERISTICS ($0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC}=5.0\text{V} \pm 10\%$. See notes 1,2.)Test condition : $V_{ih}/V_{il}=2.4/0.8\text{V}$, $V_{oh}/V_{ol}=2.0/0.8\text{V}$, Output loading $CL=100\text{pF}$

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t _{RC}	90		110		ns	
Access time from $\overline{\text{RAS}}$	t _{RAC}		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t _{CAC}		13		15	ns	3,4,5
Access time from column address	t _{AA}		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	t _{CEZ}	3	13	3	15	ns	6,11,12
Transition time(rise and fall)	t _T	2	50	2	50	ns	2
$\overline{\text{RAS}}$ precharge time	t _{RP}	30		40		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	13		15		ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	38		45		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	8	10K	10	10K	ns	13
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCd}	20	37	20	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t _{RAD}	15	25	15	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	5		5		ns	
Row address set-up time	t _{ASR}	0		0		ns	
Row address hold time	t _{RAH}	10		10		ns	
Column address set-up time	t _{ASC}	0		0		ns	
Column address hold time	t _{CAH}	8		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t _{RAL}	25		30		ns	
Read command set-up time	t _{RCS}	0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t _{RCH}	0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t _{RRH}	0		0		ns	8
Write command hold time	t _{WCH}	10		10		ns	
Write command pulse width	t _{WP}	10		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t _{RWL}	13		15		ns	
Write command to $\overline{\text{CAS}}$ lead time	t _{CWL}	8		10		ns	
Data-in set-up time	t _{DS}	0		0		ns	9
Data-in hold time	t _{DH}	8		10		ns	9
Refresh period (4K Ref)	t _{REF}		64		64	ms	
Refresh period (2K Ref)	t _{REF}		32		32	ms	
Write command set-up time	t _{WCS}	0		0		ns	7
$\overline{\text{CAS}}$ setup time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CSR}	5		5		ns	
$\overline{\text{CAS}}$ hold time($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh)	t _{CHR}	10		10		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t _{RPC}	5		5		ns	



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AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=5.0V±10%. See notes 1,2.)

Test condition : V_{Ih}/V_{il}=2.4/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading C_L=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
CAS precharge time (C-B-R counter test cycle)	t _{CPT}	20		20		ns	
Access time from CAS precharge	t _{CPA}		30		35	ns	3
Hyper page mode cycle time	t _{HPC}	25		30		ns	13
CAS precharge time(Hyper page cycle)	t _{CP}	8		10		ns	
RAS pulse width(Hyper page cycle)	t _{RASP}	50	200K	60	200K	ns	
RAS hold time from CAS precharge	t _{RHCP}	30		35		ns	
W to RAS precharge time(C-B-R refresh)	t _{WRP}	10		10		ns	
W to RAS hold time(C-B-R refresh)	t _{WRH}	10		10		ns	
Output data hold time	t _{DOH}	5		5		ns	
Output buffer turn off delay from RAS	t _{REZ}	3	13	3	15	ns	7,11,12
Output buffer turn off delay from W	t _{WEZ}	3	13	3	15	ns	7,11
W to data delay	t _{WED}	15		15		ns	
W pulse width (Hyper Page Cycle)	t _{WPE}	5		5		ns	

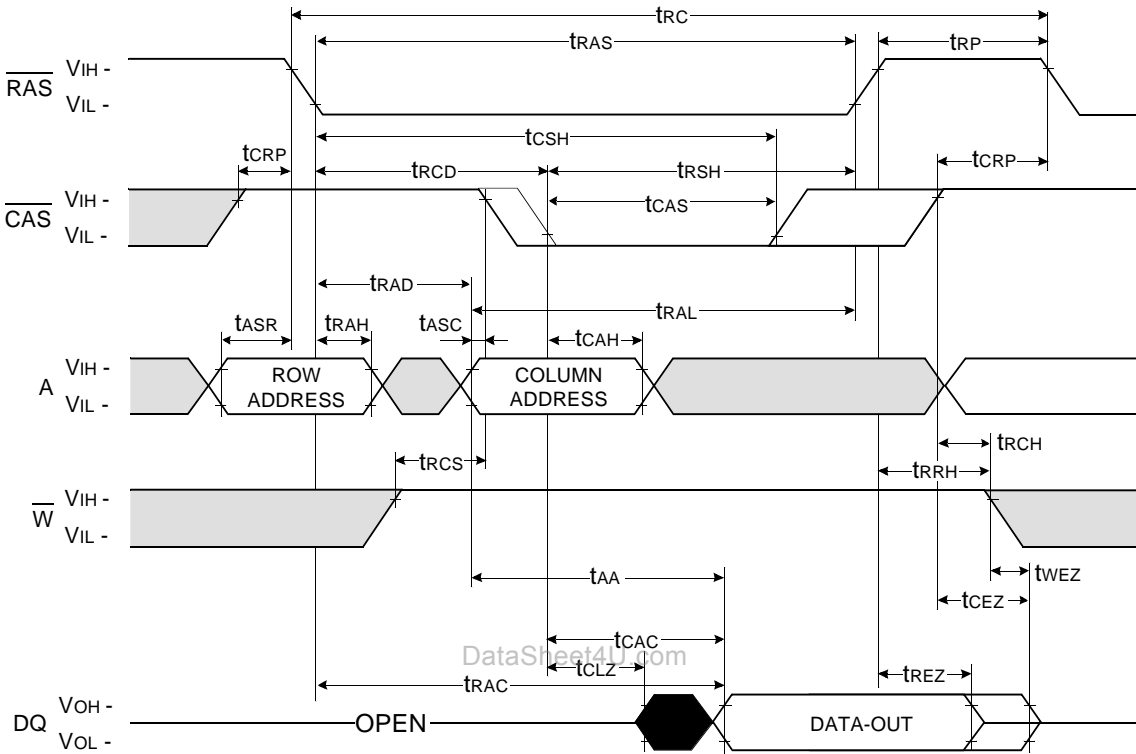
NOTES

- An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
- V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
- Measured with a load equivalent to 2 TTL loads and 100pF.
- Operation within the t_{RCd}(max) limit insures that t_{RC}(max) can be met. t_{RCd}(max) is specified as a reference point only. If t_{RCd} is greater than the specified t_{RCd}(max) limit, then access time is controlled exclusively by t_{CAC}.
- Assumes that t_{RCd}≥t_{RCd}(max).
- This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
- t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If t_{WCS}≥t_{WCS}(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
- Either t_{TRC} or t_{TRH} must be satisfied for a read cycle.
- These parameter are referenced to the CAS leading edge in early write cycles and to the W leading edge in read-write cycles.
- Operation within the t_{RAD}(max) limit insures that t_{RC}(max) can be met. t_{RAD}(max) is specified as reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
- t_{CEZ}(max), t_{REZ}(max), t_{WEZ}(max) and t_{OEZ}(max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
- If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.
- t_{ASC}≥t_{CP} min



DRAM MODULE

READ CYCLE



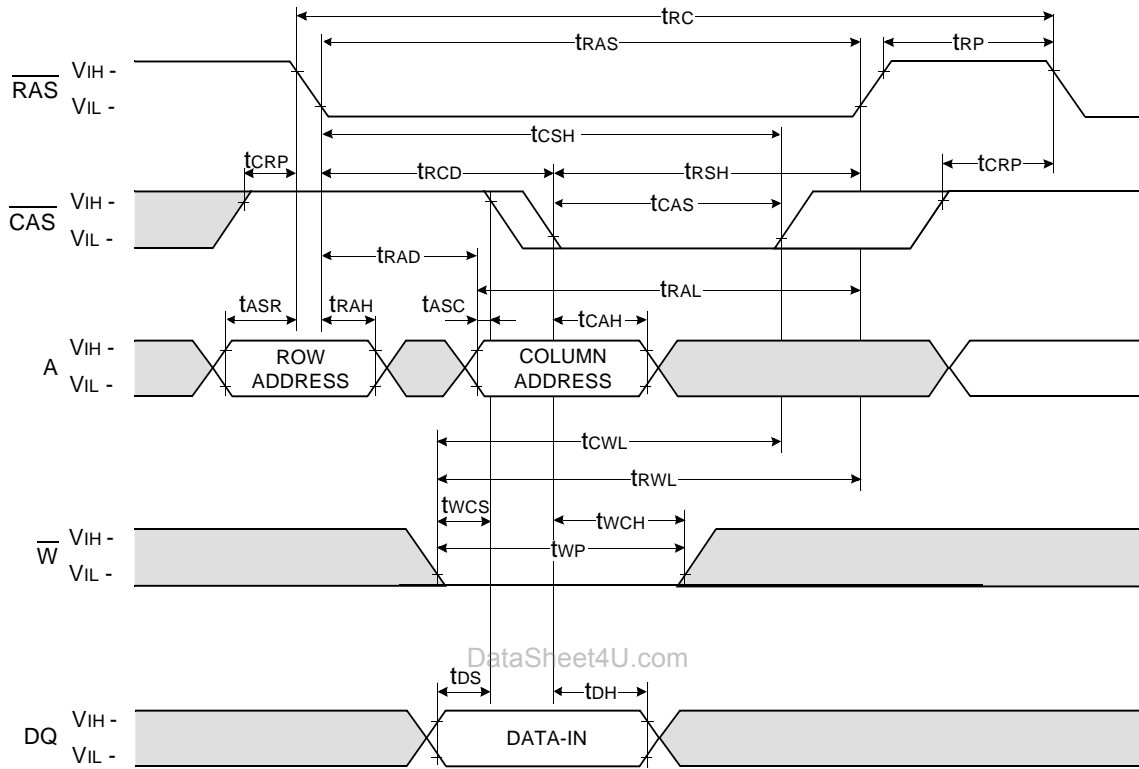
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DRAM MODULE

WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

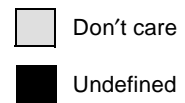
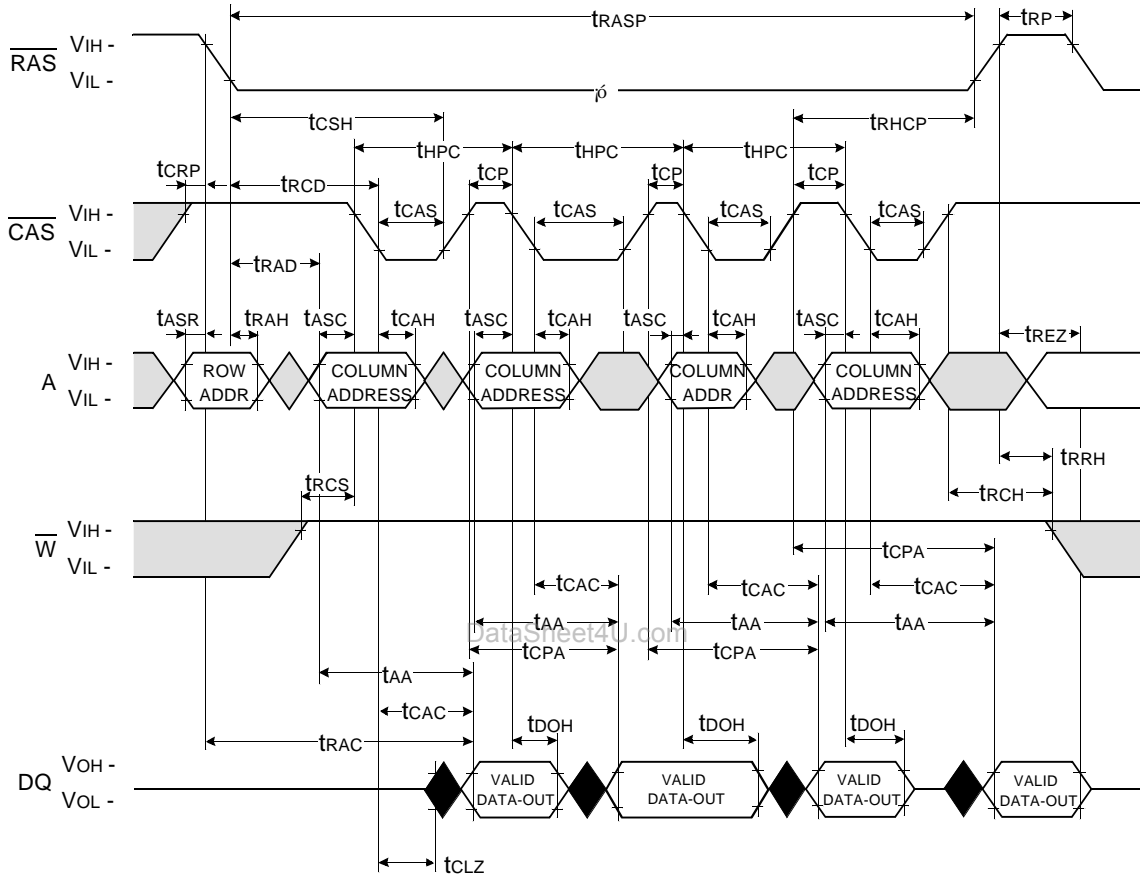


□ Don't care
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DRAM MODULE

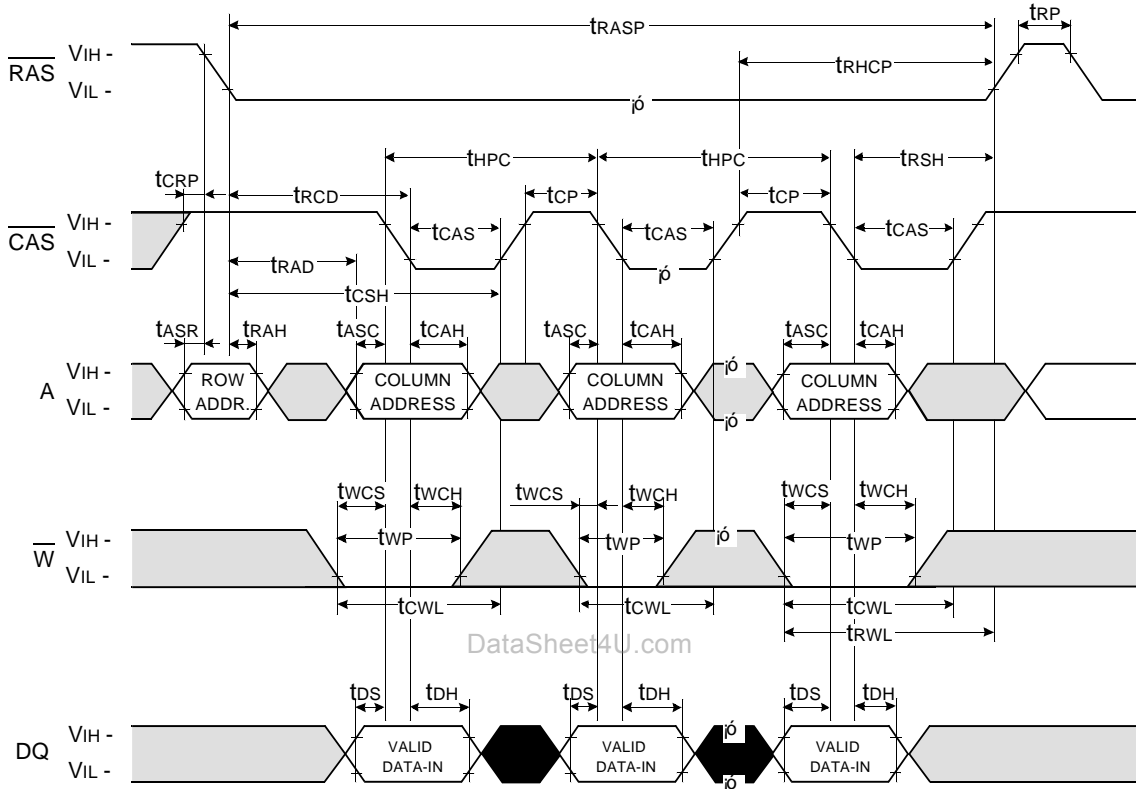
HYPER PAGE READ CYCLE



DRAM MODULE

HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

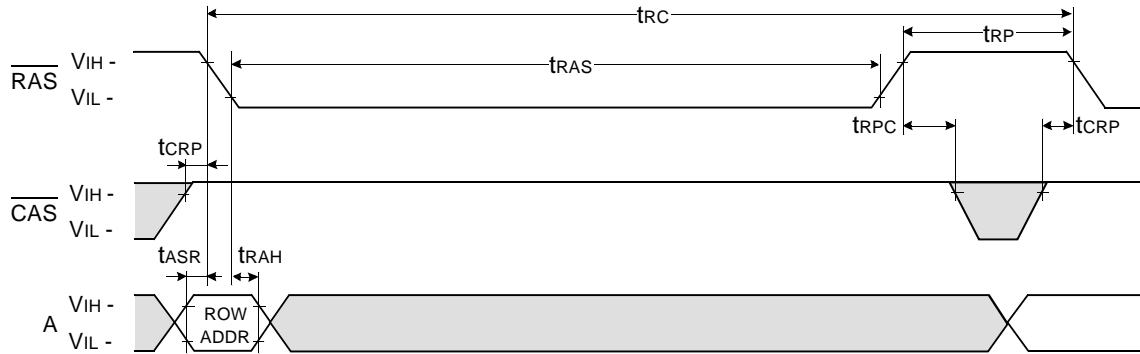


DRAM MODULE

$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

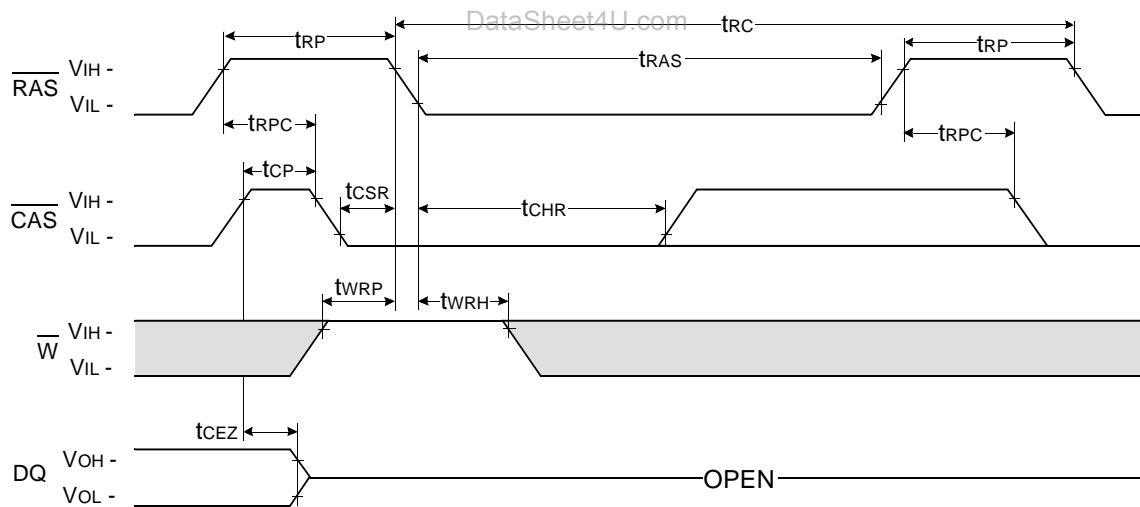
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



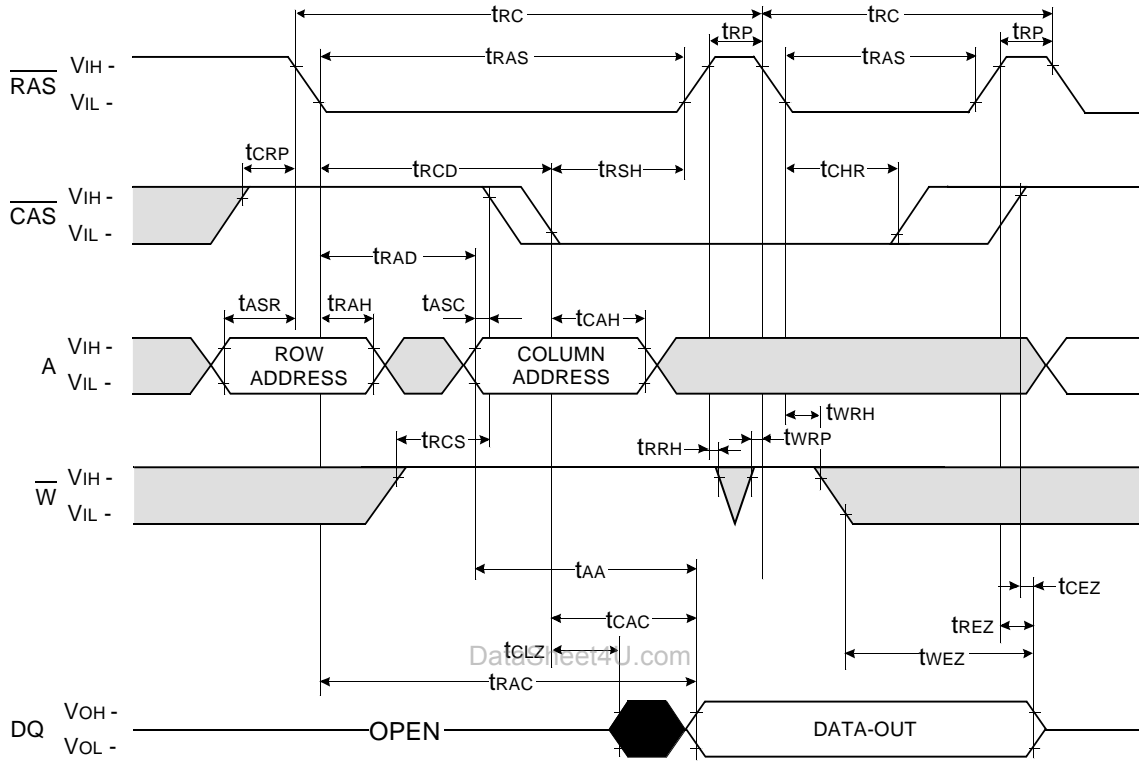
□ Don't care
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* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.



DRAM MODULE

HIDDEN REFRESH CYCLE (READ)

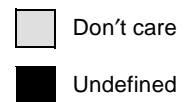
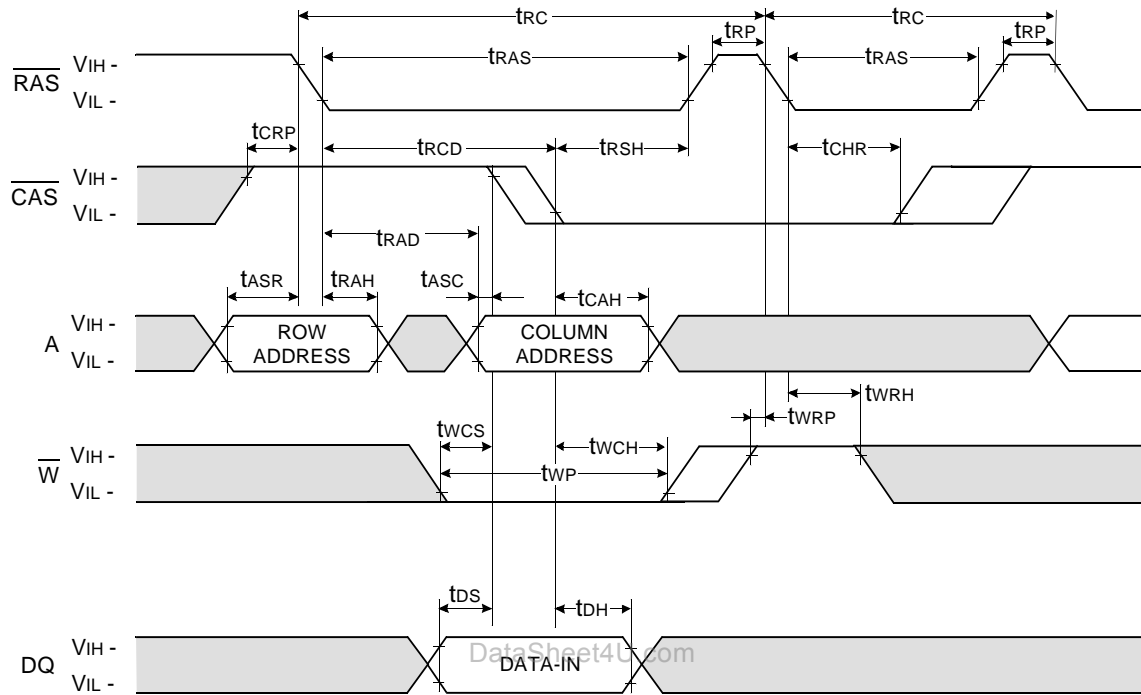


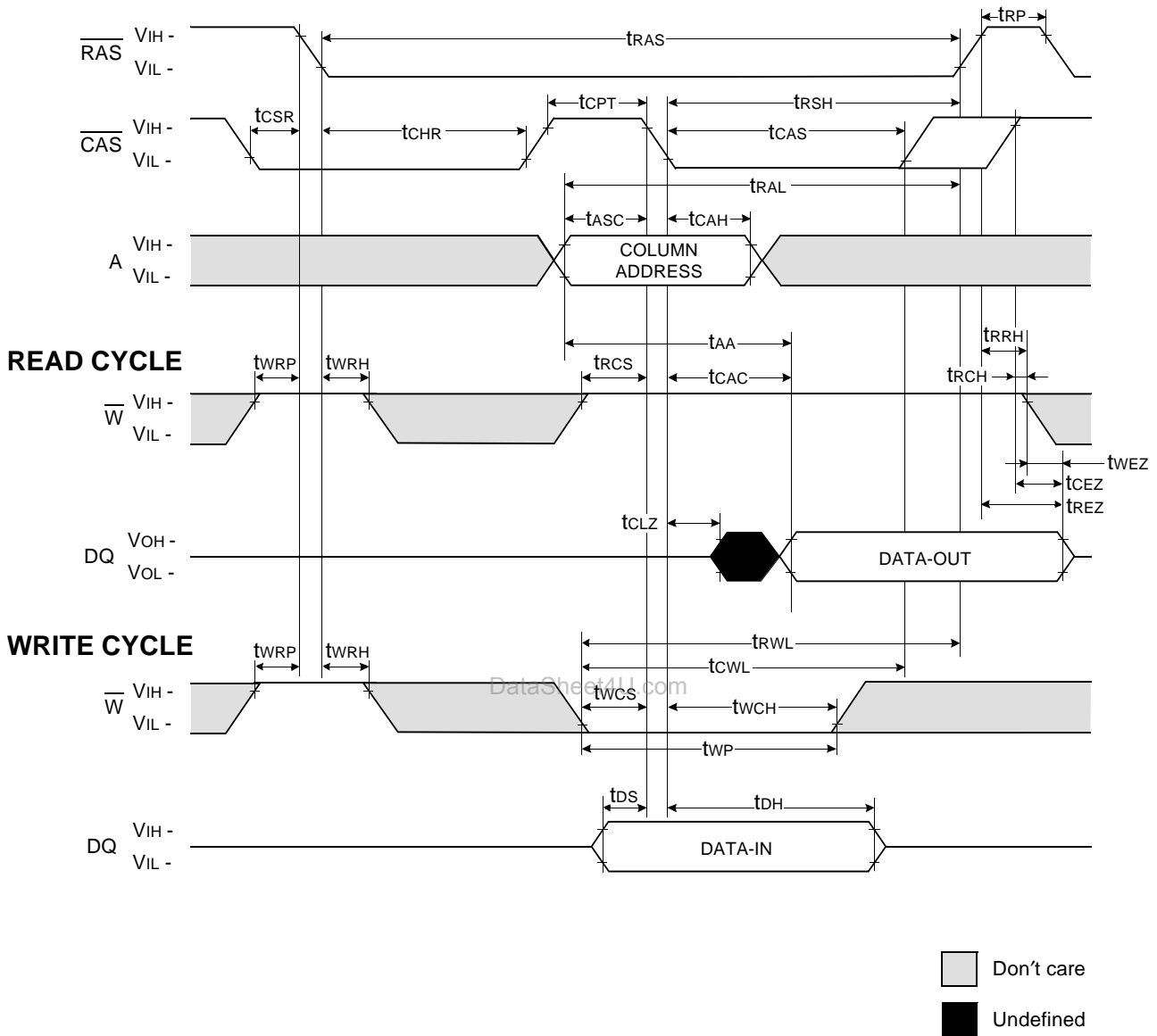
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DRAM MODULE
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



DRAM MODULE
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE


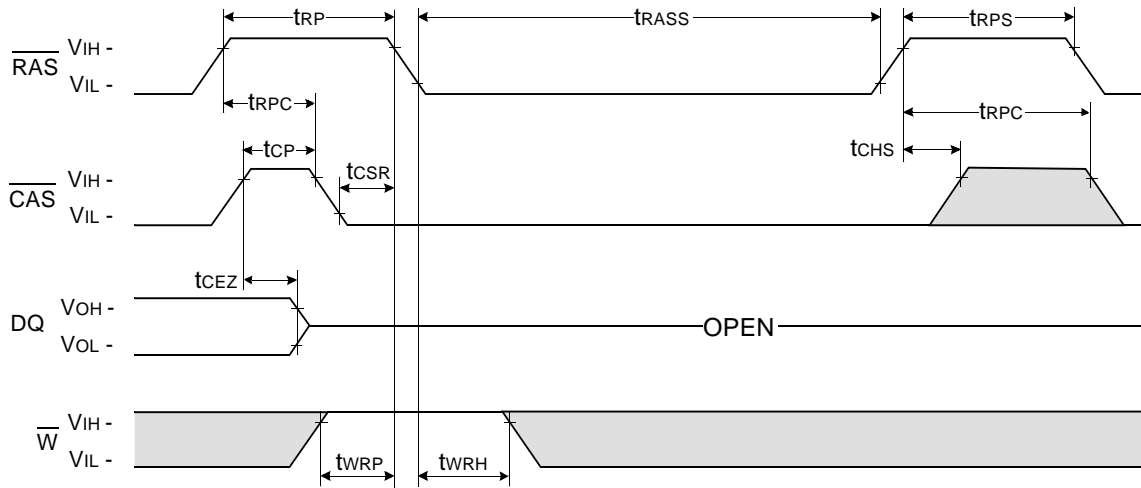
NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.



DRAM MODULE

CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : \overline{OE} , A = Don't care

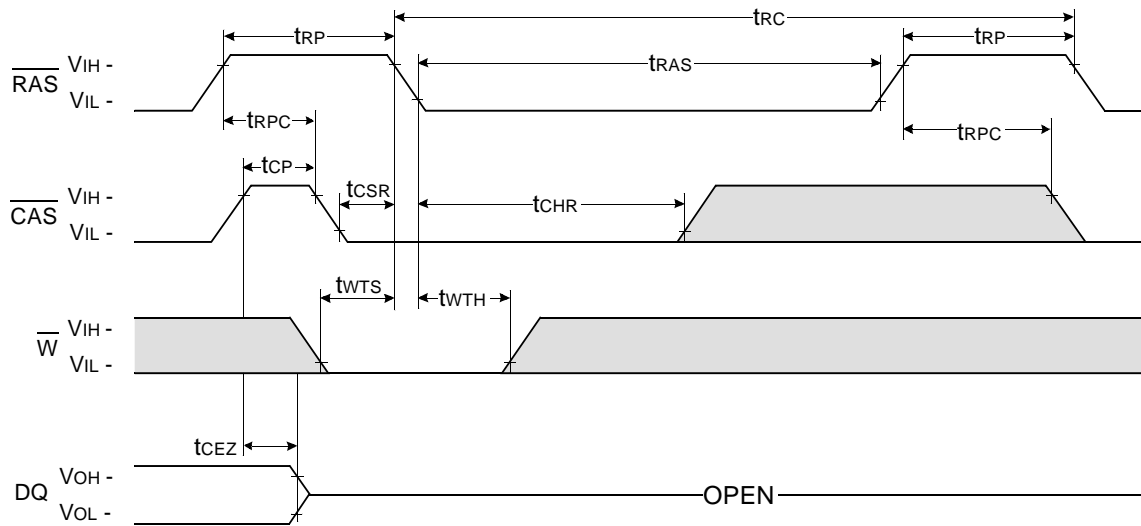


TEST MODE IN CYCLE

NOTE : \overline{OE} , A = Don't care

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□ Don't care
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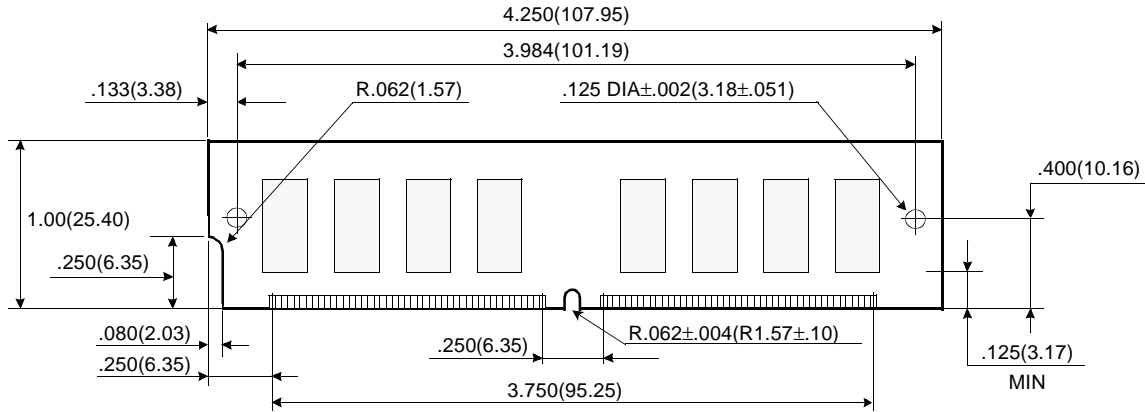


M53230800CW0/CB0
M53230810CW0/CB0

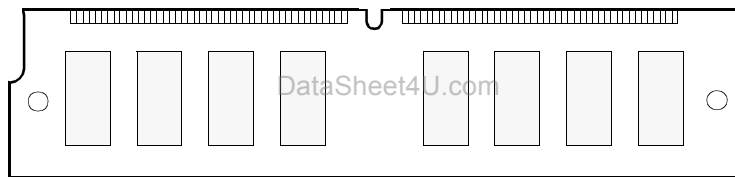
DRAM MODULE

PACKAGE DIMENSIONS

Units : Inches (millimeters)

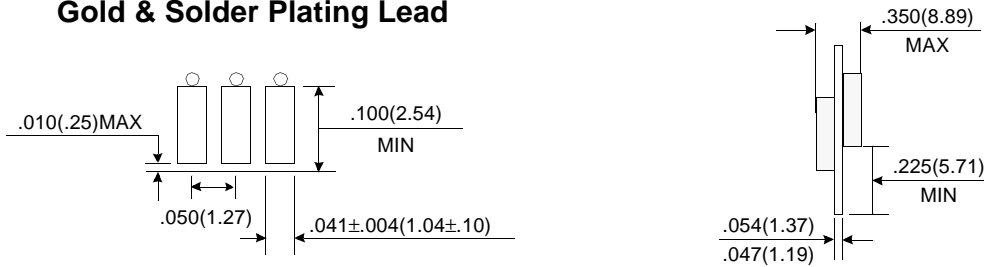


(Front view)



(Back view)

Gold & Solder Plating Lead



Tolerances : $\pm .005$ (.13) unless otherwise specified

NOTE : The used device are 4Mx4 EDO DRAM (SOJ & 300mil)
 DRAM Part No. : M53230800CW0/CB0 -- K4E170411C-B (300 mil)
 M53230810CW0/CB0 -- K4E160411C-B (300 mil)

Revision History
 Rev 0.0 : Oct. 1999

