

**DESCRIPTION**

The M54123L is a semiconductor integrated circuit with amplifier for a high-speed earth leakage circuit breaker.

**FEATURES**

- Suitable for JIS C 8371
- Good temperature characteristics of input sensitivity current
- High input sensitivity ( $V_T = 6.1\text{mV Typ.}$ )
- Low external component count
- High noise and surge-proof
- Low power dissipation ( $P_d = 5\text{mW Typ.}$ ) and may be used both as 100V and 200V.
- High mounting density by SIL package with 8 pins
- Wide temperature range ( $T_a = -20 \sim +80^\circ\text{C}$ )

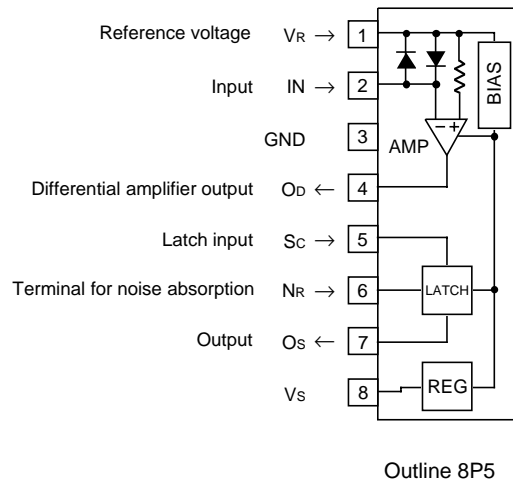
**APPLICATION**

High speed earth leakage circuit breaker

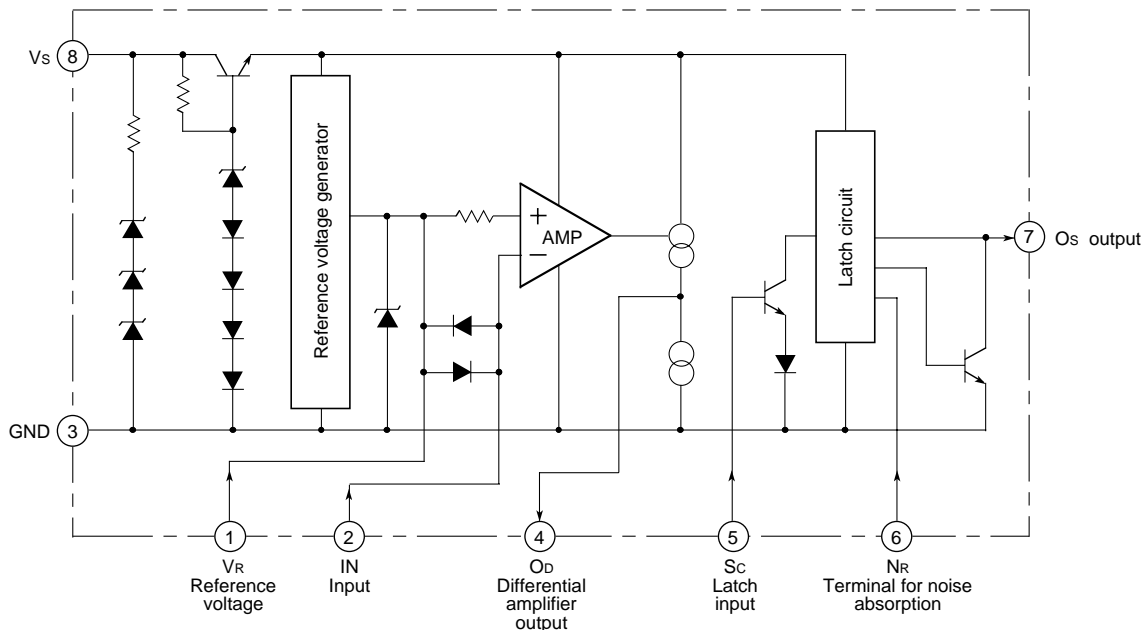
**FUNCTION**

The M54123L circuit for the amplifying parts of earth leakage circuit breaker consists of differential amplifier, latch circuit and voltage regulator. It is connected to the secondary side of the zero-current transformer (ZCT) which detects leakage current in the both input of the differential amplifier. Signals amplified by differential amplifier are integrated by an external capacitor, and connects to the input terminal of latch circuit with output suitable for the characteristics of high-speed earth leakage circuit breaker. Latch circuit keeps low in the output till the input voltage reaches the fixed level, and output becomes high when the leakage current more than fixed flows. It drives a thyristor connected to the output terminal of latch circuit.

**PIN CONFIGURATION (TOP VIEW)**



**BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS** (Ta = -20 – 80°C unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Is	Supply current		8	mA
I <sub>VR</sub>	V <sub>R</sub> pin current	Between V <sub>R</sub> -IN (Note 1)	250	mA
		Between V <sub>R</sub> -GND	30	
		Between IN-V <sub>R</sub> (Note 1)	-250	
I <sub>IN</sub>	IN terminal current	Between IN-V <sub>R</sub> (Note 1)	250	mA
		Between IN-GND	30	
		Between V <sub>R</sub> -IN (Note 1)	-250	
I <sub>SC</sub>	Sc terminal current		5	mA
P <sub>d</sub>	Power dissipation		200	mW
T <sub>opr</sub>	Operating temperature		-20 – 80	°C
T <sub>stg</sub>	Storage temperature		-55 – 125	°C

Note 1: Current value between V<sub>R</sub> and IN, and between IN and V<sub>R</sub> is less than 1ms in the pulse width, and duty cycle is less than 12%. In applying AC current continuously, it is 100mArms in the off-state.

Remarks: GND terminal (pin ③) of the circuit is a basis of all the voltages except differential input clamp voltage of DC electrical characteristics, and direction of current is plus (no signal) in flowing into the circuit and is minus (–signal) in flowing out of it. Maximum value and minimum one are shown as absolute value. Please don't apply voltage whose standard is GND terminal in V<sub>R</sub> and IN pin.

**RECOMMENDED OPERATING CONDITIONS** (Ta = -20 – 80°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>s</sub>	Supply voltage when latch circuit is off-state	12			V
C <sub>vs</sub>	External capacitor between V <sub>s</sub> and GND	1			μF
C <sub>os</sub>	External capacitor between O <sub>s</sub> and GND			1	μF

**ELECTRICAL CHARACTERISTICS** (Ta = -20 – 80°C unless otherwise noted)

Symbol	Parameter	Test conditions	Temperature (°C)	Test circuit	Limits			Unit	
					Min.	Typ.*	Max.		
I <sub>s1</sub>	Supply current	V <sub>s</sub> = 12V, V <sub>R</sub> -V <sub>I</sub> = 30mV	-20	1			580	μA	
			25	1		400	530		
			80	1			480		
V <sub>T</sub>	Trip voltage	V <sub>s</sub> = 16V, V <sub>R</sub> -V <sub>I</sub> (Note 2)	-20 – +80	2	4	6.1	9	mV <sub>rms</sub>	
I <sub>TD1</sub>	Timed current 1	V <sub>s</sub> = 16V, V <sub>R</sub> -V <sub>I</sub> = 30mV, V <sub>OD</sub> = 1.2V	25	3	-12		-30	μA	
I <sub>TD2</sub>	Timed current 2	V <sub>s</sub> = 16V, short circuit between V <sub>R</sub> and V <sub>I</sub> , V <sub>OD</sub> = 0.8V	25	4	17		37	μA	
I <sub>o</sub>	Output current	V <sub>SC</sub> = 1.4V V <sub>OS</sub> = 0.8V		I <sub>s1</sub> = 580μA	-20	5	-200		μA
				I <sub>s1</sub> = 530μA	25	5	-100		
				I <sub>s1</sub> = 480μA	80	5	-75		
V <sub>SC "ON"</sub>	Sc "ON" voltage (Note 3)	V <sub>s</sub> = 16V	25	6	0.7		1.4	V	
I <sub>SC "ON"</sub>	Sc input current	V <sub>s</sub> = 12V	25	7			5	μA	
I <sub>OSL</sub>	Output low-level current	V <sub>s</sub> = 12V, V <sub>OSL</sub> = 0.2V	-20 – +80	8	200			μA	
V <sub>IC</sub>	Input clamp voltage	V <sub>s</sub> = 12V, I <sub>IC</sub> = 20mA	-20 – +80	9	4.3		6.7	V	
V <sub>IDC</sub>	Differential input clamp voltage	I <sub>IDC</sub> = 100mA	-20 – +80	10	0.4		2	V	
V <sub>SM</sub>	Maximum current voltage	I <sub>SM</sub> = 7mA	25	11	20		28	V	
I <sub>s2</sub>	Supply current 2 (Note 4)	V <sub>R</sub> -V <sub>I</sub> V <sub>OS</sub> = 0.6V (Note 5)	-20 – +80	12			900	μA	
V <sub>S "OFF"</sub>	Latch circuit is off-state supply voltage (Note 6)		25	13	0.5			V	
T <sub>ON</sub>	Operating time (Note 7)	V <sub>s</sub> = 16V, V <sub>R</sub> -V <sub>I</sub> = 0.3V	25	14	2		4	ms	

\*: Typical values are at Ta = 25°C.

Note 2: When standard value of voltage (60Hz) between V<sub>R</sub> and V<sub>I</sub> is minimum, and output O<sub>s</sub> is low-level, or when standard value of voltage (60Hz) between V<sub>R</sub> and V<sub>I</sub> is maximum, and output O<sub>s</sub> is high-level, it is considered as a good one.

3: When standard value of voltage V<sub>SC "ON"</sub> is minimum, and output O<sub>s</sub> is low-level, or when standard value of voltage V<sub>SC "ON"</sub> is maximum, and output O<sub>s</sub> is high-level, it is considered as a good one.

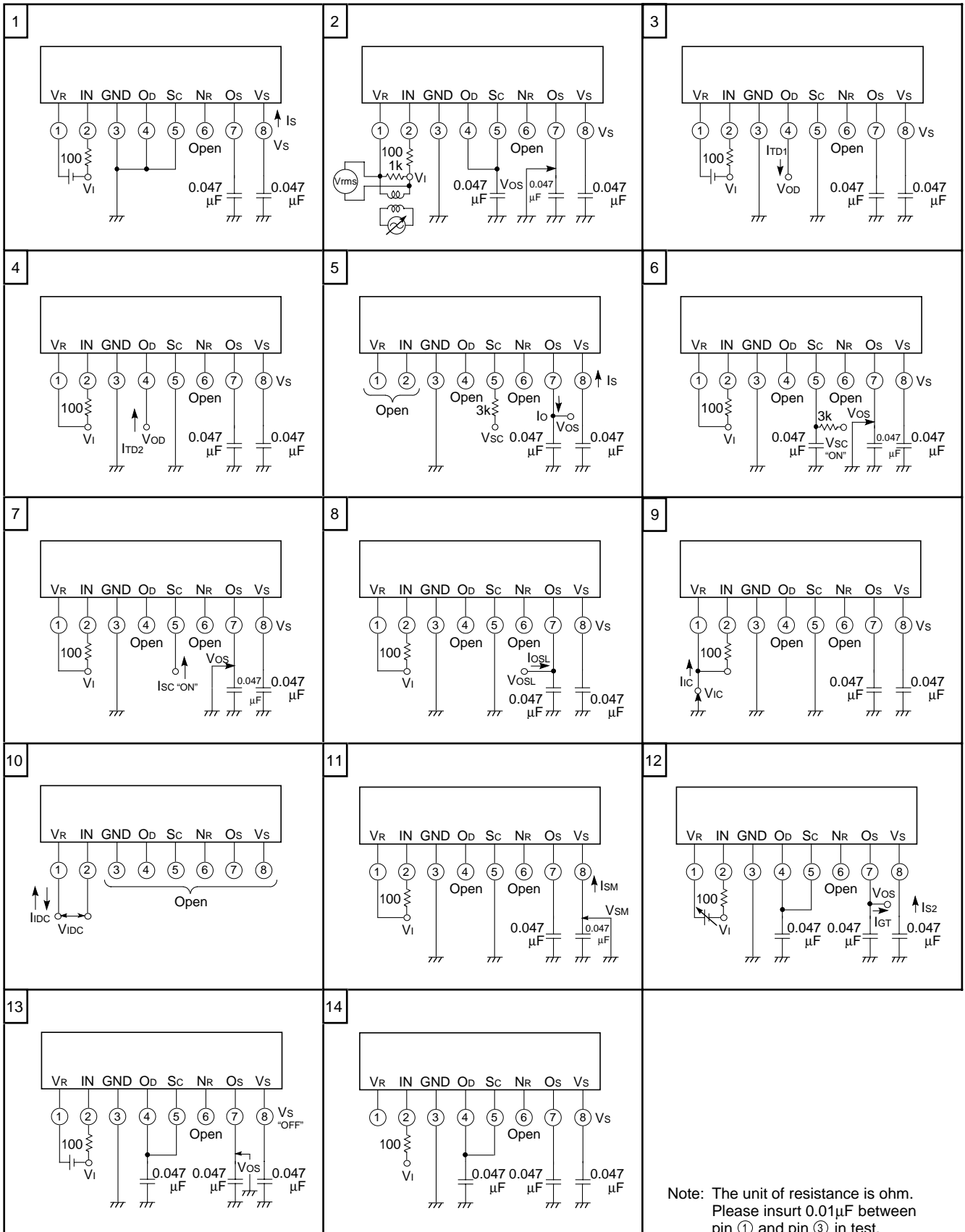
4: Supply current 2 is necessary to keep high in output O<sub>s</sub>.

5: After applying 30mV between V<sub>R</sub> and V<sub>I</sub> and shorting between them, it is considered as a good one if standard value of I<sub>IGT</sub> flows out of output O<sub>s</sub>.

6: After supply voltage applies 12V and output O<sub>s</sub> is high-level, it is considered as a good one in the standard value of supply voltage and in the low-level of output O<sub>s</sub>.

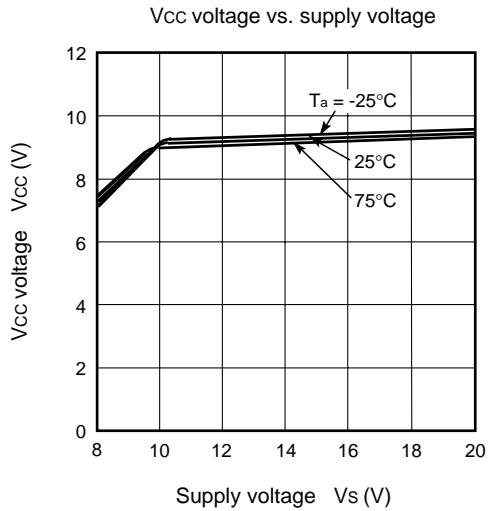
7: Operating time is a time from applying fixed input till operating latch circuit in 0.047μF between O<sub>D</sub> and GND.

**TEST CIRCUIT**

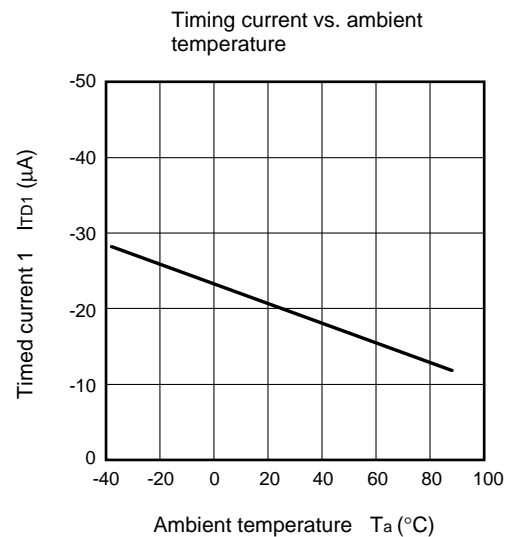
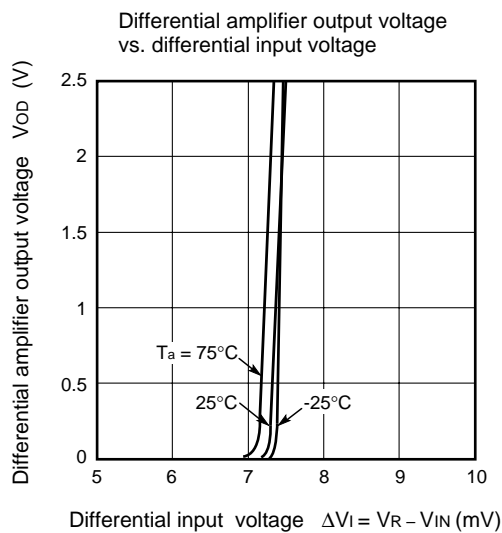
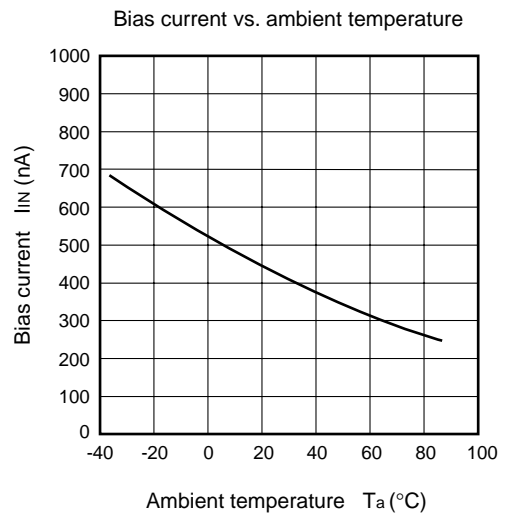
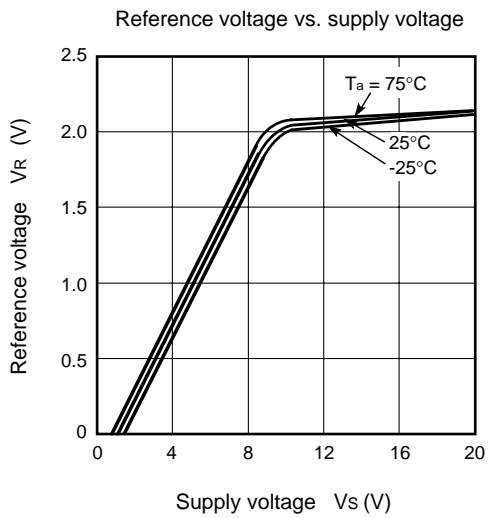
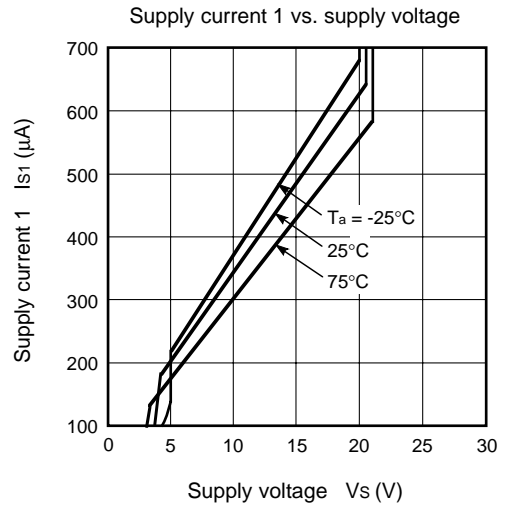


Note: The unit of resistance is ohm.  
Please insert 0.01μF between pin ① and pin ③ in test.

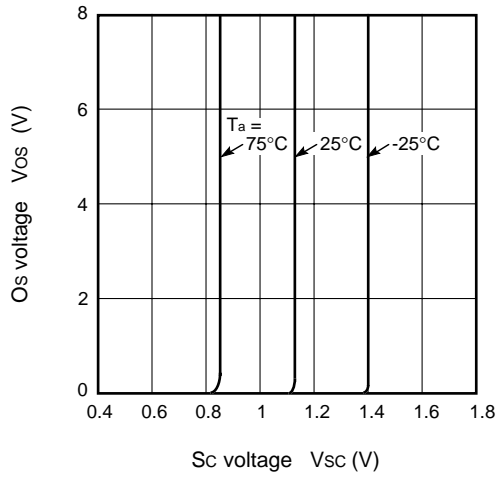
**TYPICAL CHARACTERISTICS**



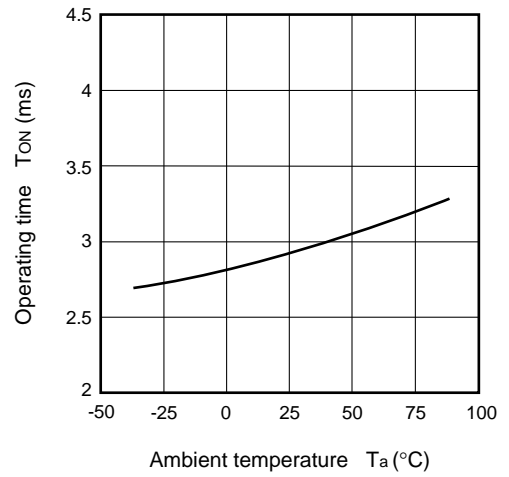
Vcc voltage generates by the constant voltage circuit in IC. This is measured not by M54122L but by a special element.



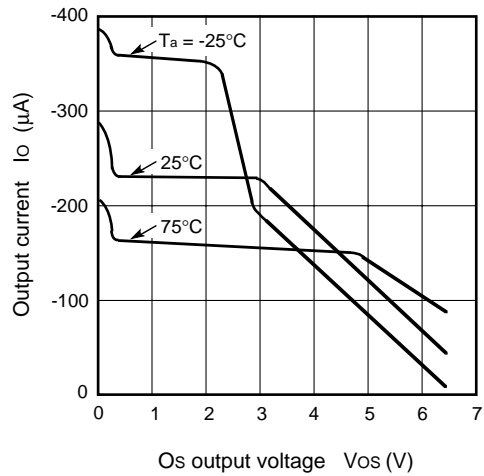
Os voltage vs. Sc voltage



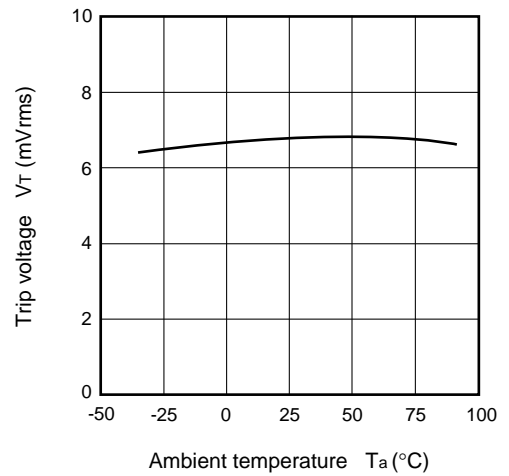
Operating time vs. ambient temperature



Output current vs. Os output voltage

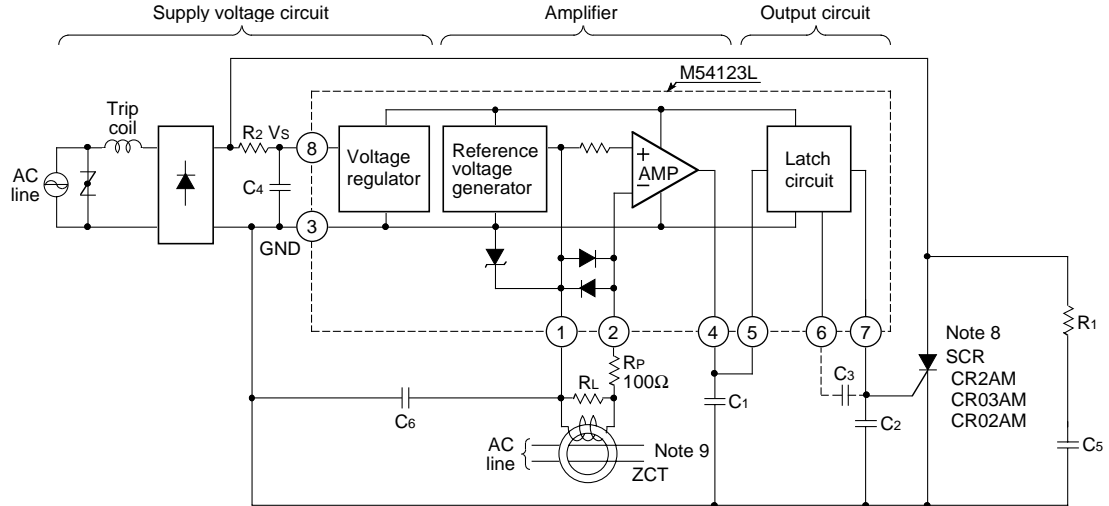


Trip voltage vs. ambient temperature



**APPLICATION EXAMPLE**

• HIGH-SPEED LEAKAGE CIRCUIT BREAKER WITH M54123L



Note 8 : Gate current must be selected.  
 Please select voltage resistance by AC supply voltage.  
 9 : MZ Core Series by Soryo Denshi Kagaku Co., Ltd (Mitsubishi Subsidiary)  
 Tel. +81-427-74-7813

Supply voltage circuit is connected as a previous diagram. Please decide constants  $R_1$ ,  $R_2$ ,  $C_4$ , and  $C_5$  of a filter in order to keep at least 12V in  $V_s$ , when normal supply current flows.

In this case, please connect  $C_4$  (more than  $1\mu\text{F}$ ) and  $C_2$  (less than  $1\mu\text{F}$ ). ZCT and load resistance  $R_L$  of ZCT are connected between input pin ① and ②. In this case protective resistance ( $R_P = 100\Omega$ ) must be inserted. Sensitivity current is regulated by  $R_L$ , and output of amplifier shows in pin ④. External capacitor  $C_1$  between pin ④ and GND is used for noise removal.

When large current is grounded in the primary side (AC line) of ZCT, the wave form in the secondary side of ZCT is distorted and some signals doesn't appear in the output of amplifier. So please connect a varistor or a diode (2 pcs.) to ZCT in parallel.

Latch circuit is used to inspect the output level of amplifier and to supply gate current on the external SCR. When input pin becomes more than 1.1V (Typ.), latch circuit operates and supply gate current in the gate of SCR connected to the output pin ⑦.

Pin ⑥ can be used in the open state, but please connect capacitor (about  $0.047\mu\text{F}$ ) between pin ⑥ and pin ⑦.

Capacitor  $C_6$  between pin ① and GND is used to remove noise and is about  $0.047\mu\text{F}$ .

