M54910P

F2F MAGNETIC STRIPE ENCORDING CARD READER

DESCRIPTION

The M54910P is an I^2L semiconductor intergrated circuit consisting of an F2F demodulator for magnetic stripe card readers.

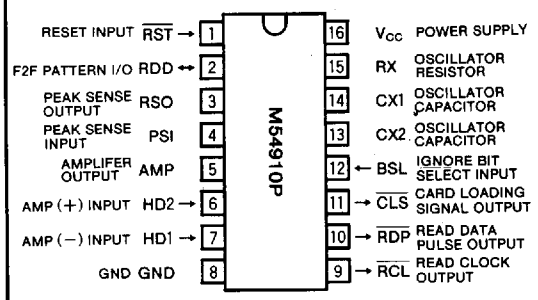
FEATURES

- Low power dissipation (18mA typ)
- Ignore bit select input (bits 2, 8)
- Open collecteor output
- Wide operating temperature range T_a=−20~+75℃

APPLICATION

Magnetic stripe card readers

PIN CONFIGURATION (TOP VIEW)



Outline 16P4

FUNCTION

The data signal from a magnetic stripe card is read by a magnetic head and enters the M54910P via inputs HD-1 and HD-2. The signal is analog processed by amplifier OP1, peak detector OP2 and waveform regenerator OP3 to demodulate the F2F pattern signal. The specific bit numbers set by input BSL are ignored, and the data is digitally processed to output card loading signal $\overline{CLS}$, demodulated clock signal $\overline{RCL}$, and demodulated data signal $\overline{RDP}$.

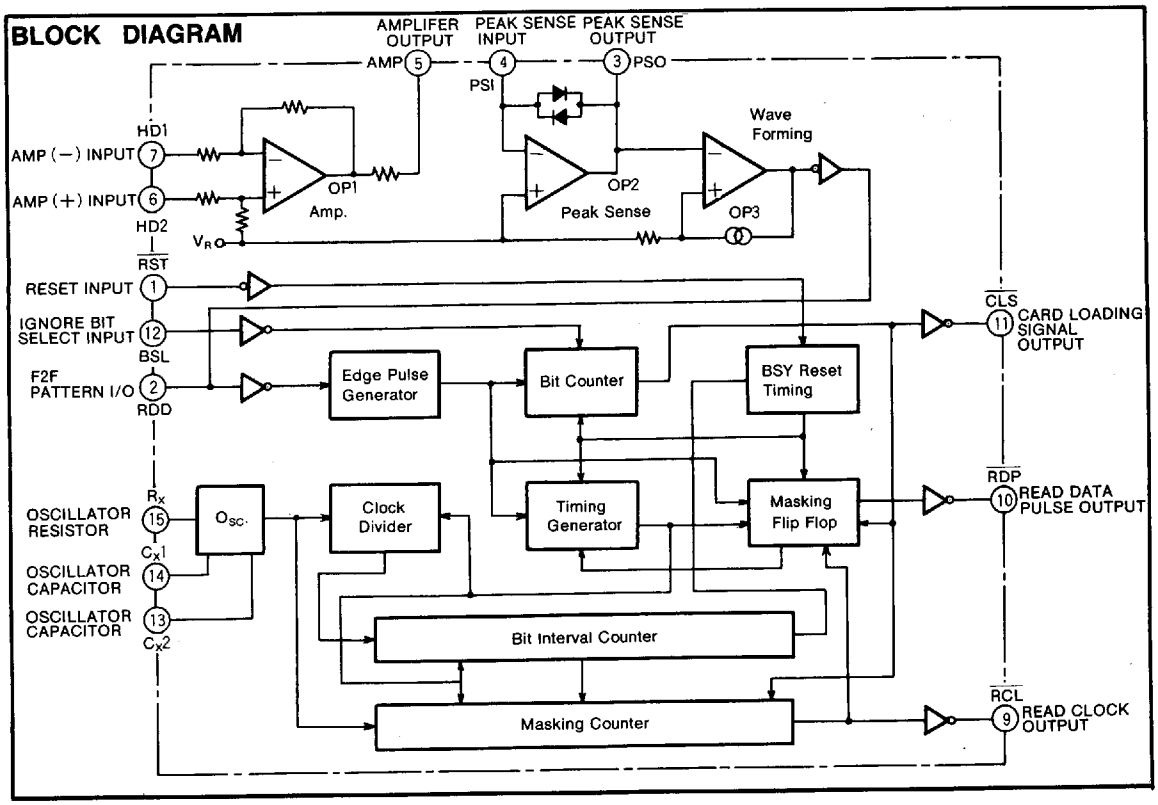
$\overline{CLS}$ becomes low when two rising and falling edges of the F2F pattern signal RDD are counted (eight if BSL is high). If no input data is detected for a specified period, $\overline{CLS}$ returns to high. $\overline{RCL}$ is a clock signal whose period corresponds to T_B, the duration of one data bit when the card speed is constant.

If T_{Bn} is the duration of a particular bit, $\overline{RCL}$ will be high for a period of 2/3 T_{Bn}-1. When the bit value is 1, $\overline{RDP}$ is set low by the timing of RDD. In other words, while $\overline{RCL}$ is high, it can respond to a change of state in RDD. This means that even if the card speed changes, (typically 10~150cm/s) where T_{Bn} satisfies the following formula.

$2/3\ T_{Bn}-1 < T_{Bn} < 4/3 T_{Bn}$

The T_B is counted by the oscillator period T_{OSC}.

BLOCK DIAGRAM



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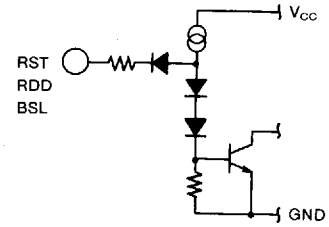
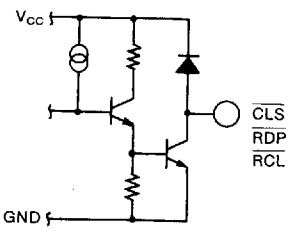
I/O CIRCUIT CHART

INPUT CIRCUIT



OUTPUT CIRCUIT



PIN DESCRIPTION

pin number	Symbol	Name	Description
1	$\overline{RST}$	Reset input	Resets when low. When not used, reset is performed as required by internal logic.
2	RDD	F2F pattern I/O	Monitor input/output of F2F pattern reformed magnetic head signal.
3	PSO	Peak sense output	A resistor and capacitor are connected in parallel between PSI and PSO to set the negative feedback impedance of the peak sense circuit.
4	PSI	Peak sense input	Refer to PSO and AMP
5	AMP	Amp output	A resistor and capacitor are connected between PSI and AMP to set the peak sense circuit.
6	HD2	Amp (+) input	The magnetic head is connected between HD1 and HD2.
7	HD1	Amp (−) input	Same as above.
8	GND	GND	
9	$\overline{RCL}$	Read clock output	Clock output after F2F demodulation.
10	$\overline{RDP}$	Read data pulse output	Data output after F2F demodulation.
11	$\overline{CLS}$	Card loading signal output	Becomes low while a card is running.
12	BSL	Ignore bit select input	2 bit are ignored when low, 8 bits when high.
13	CX2	Oscillator capacitance	A capacitor is connected between CX1 and CX2 to set the oscillator freqency.
14	CX1	Oscillator capacitance	Same as above
15	RX	Oscillator resistance	A resistor is connected between V_{CC} and RX to set the oscillator current.
16	V_{CC}	Power supply	

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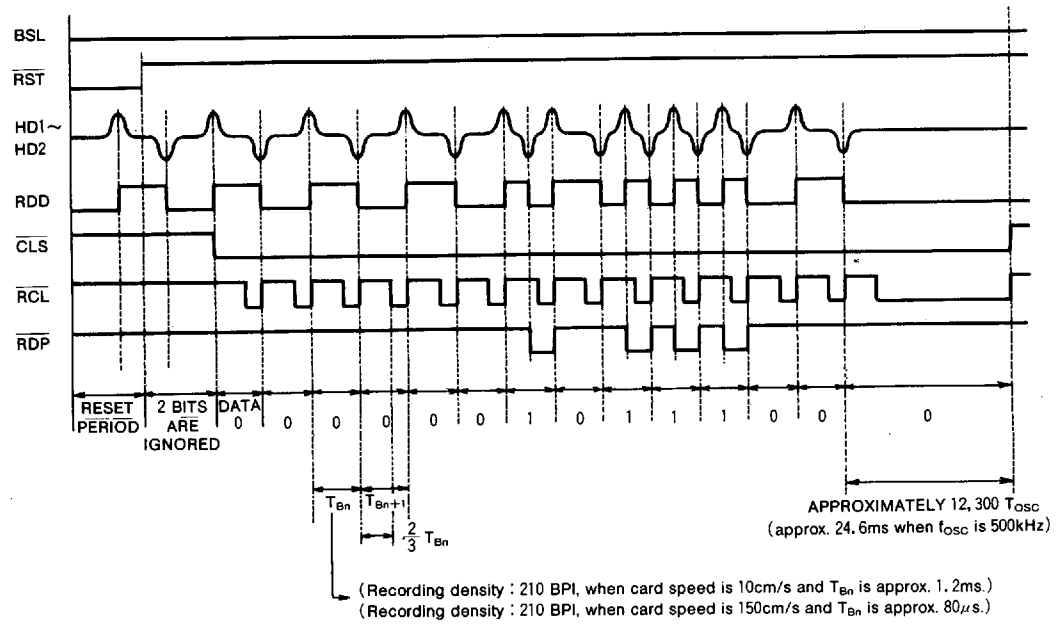
TIMING DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0. 5∼+6	V
V_I	Input voltage	RST, PDD, BSL	−0. 5∼V_{CC}	V
V_O	Output voltage	When CLS, RDP and RCL are high	−0. 5∼V_{CC}	V
P_d	Power dissipation		150	mW
T_{opr}	Operating temperature		−20∼+75	℃
Tstg	Storage temperature		−55∼+125	℃

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RECOMMENDED OPERATING CONDITIONS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage	$\overline{RST}$, RDD, BSL	2		V_{CC}	V
V_{IL}	Low-level input voltage	$\overline{RST}$, RDD, BSL	0		0.8	V
I_{OL}	Low-level output current	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$			16	mA
V_{OH}	High-level output voltage	When $\overline{CLS}$, $\overline{RDP}$ and $\overline{RCL}$ are high.			V_{CC}	V
V_{ID}	Differential input voltage	HD1, HD2	2.5		80	mV_{PP}
f_{IN}	Input frequency	HD1, HD2	0.4		20	kHz
f_{OSC}	Oscillator frequency	$f_{OSC}=\frac{1}{T_{OSC}}\fallingdotseq\frac{1}{2R_XC_X}$				kHz
R_X				15		kΩ
C_X		When recording density is 210 BPI		68		pF
C_{PS}		When recording density is 210 BPI		0.022		μF
C_{NF}		When recording density is 210 BPI		1000		pF
R_{NF}		When recording density is 210 BPI		680		kΩ

ELECTRICAL CHARACTERISTICS (T_a=−20∼+75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Test circuit	Limits			Unit
					Min	Typ	Max	
I_{CC}	Circuit current	V_{CC}	V_{CC}=5.5V, V_{IN}=80mV$_{PP}$, f_{IN}=20kHz	1			25	mA
I_{IL}	Low-level input current	RST, RDD, BSL	V_{CC}=5.5V, V_{IL}=0.4V	5	−50		−200	μA
I_{IH}	High-level input current	RST, RDD, BSL	V_{CC}=5.5V, V_{IN}=5.5V	5			40	μA
V_{OL}	Low-level output voltage	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$	V_{CC}=4.5, I_{OL}=16mA	6			0.4	V
I_{OL}	High-level output current	$\overline{CLS}$, $\overline{RDP}$, $\overline{RCL}$	V_{CC}=5.5V, V_{OH}=5.5V	6			200	μA
R_{IN}	Input resistance	HD1, HD2	V_{CC}=5V, ΔV_{IN}=40mV	3	1.7		4.2	kΩ
V_R	Reference voltage	AMP	V_{CC}=5V	4	2.25		2.75	V
G_{V1}	Voltage gain 1	Amplifier curcuit	V_{CC}=5V, V_{IN}=80mV$_{PP}$, f_{IN}=1kHz	2	24		30	V/V
G_{V2}	Voltage gain 2	Amplifier circuit	V_{CC}=5V, V_{IN}=80mV$_{PP}$, f_{IN}=20kHz	2	21		30	V/V
V_{OPP}	Maximum output voltage	Amplifier circuit	V_{CC}=5V, f_{IN}=20kHz	2	2.6			V_{PP}
I_{IB}	Input bias current	PSI	V_{CC}=5V	3			−0.2	μA
V_{CL}	Clamp voltage	Peak sense circuit	V_{CC}=5V, V_{IN}=80mV$_{PP}$, f_{IN}=1mkHz	1	0.8		2.4	V_{PP}
V_{TH}	Threshold voltage	Waveform regenerator circuit	V_{CC}=5V	4	±0.15		±0.26	V
DF	Duty factor	Peak sense circuit	V_{CC}=5V, V_{IN}=2.5mV$_{PP}$, f_{IN}=1kHz	1	40		60	%
f_{OSC}	Oscillator frequency	Oscillator circuit	V_{CC}=5V, R_X=15kΩ, C_X=68pF	4	380		600	kHz
T_{d1}	Delay time 1		V_{CC}=5V	7			T_{OSC}+2	μs
T_{d2}	Delay time 2		V_{CC}=5V	7			$3T_{OSC}$+2	μs
T_{d3}	Delay time 3		V_{CC}=5V	7			$3T_{OSC}$+4	μs
T_{d4}	Delay time 4		V_{CC}=5V	7			$12294T_{OSC}$ +0.5	μs

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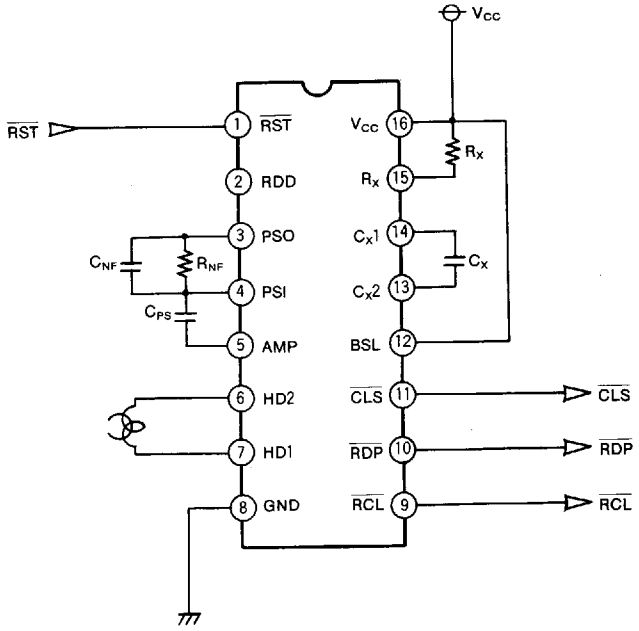
APPLICATION EXAMPLE



Note : The following procedure allows RDD to be used as an input.
1) Shout circuit HD1 and HD2.
2) Leave AMP and PSO open.
3) Connect resistor R_{PS} (5kΩ to 50kΩ) between PSI and GND.

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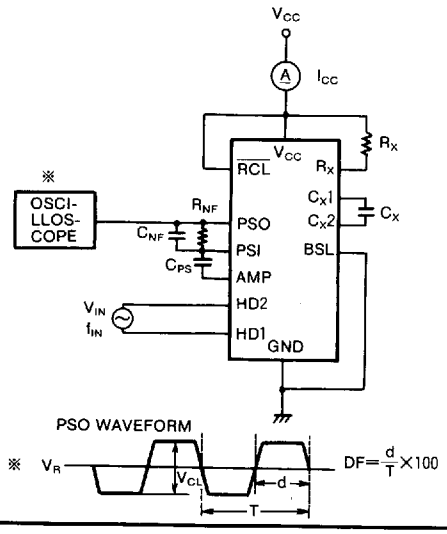
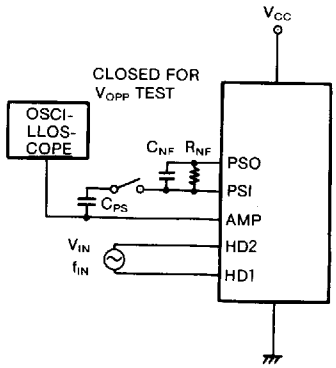
TEST CIRCUIT (R_X=15kΩ, C_X=68pF, C_{PS}=0.022μF, C_{NF}=1000pF, RNF=680kΩ, unless otherwise noted)

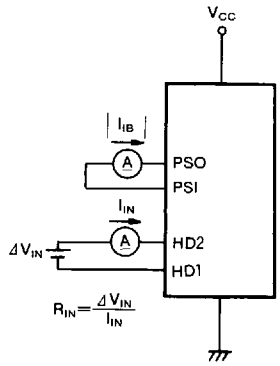
1 • I_{CC}, V_{CL}, DF TEST



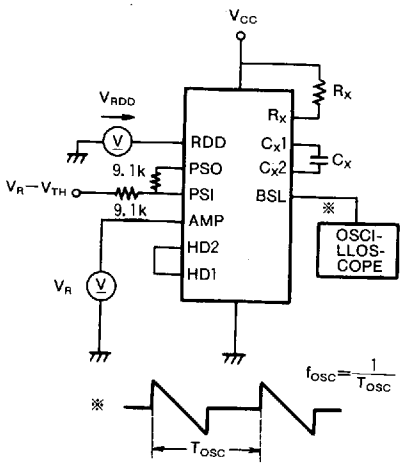
2 • G_{V1}, G_{V2}, V_{OPP} TEST



3 • R_{IN}, I_{IB} TEST



4 • V_R, V_{TH}, f_{OSC} TEST



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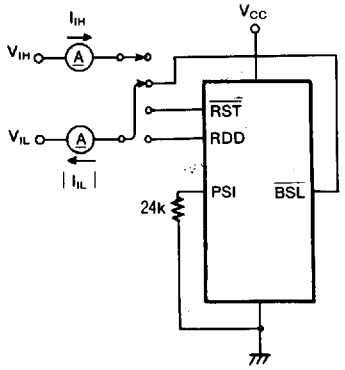
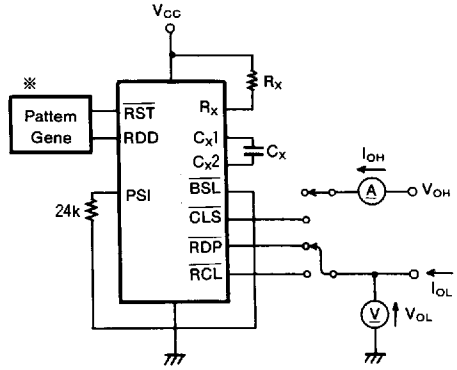
5 • I_{IL}, I_{IH} TEST

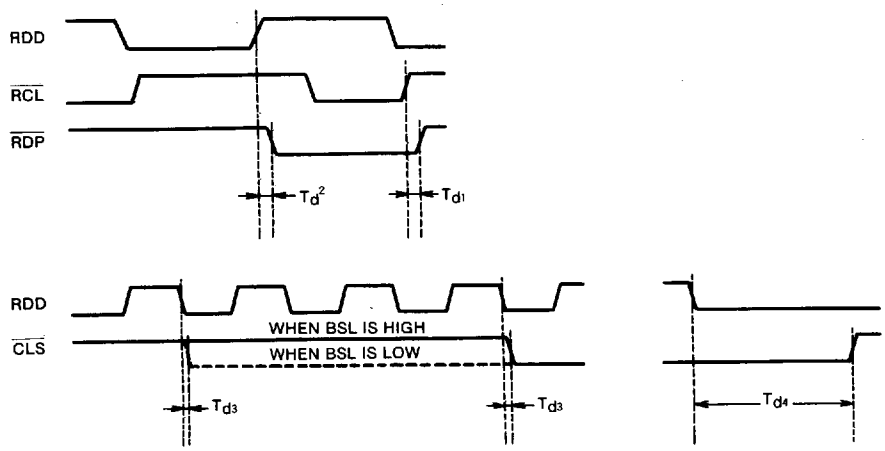


6 • V_{OL}, I_{OH} TEST



※ Apply the appropriate pattern to set the test pin either high or low.

7 • T_{d1}, T_{d2}, T_{d3}, T_{d4} TEST



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