

PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

DESCRIPTION

The M54959P is a semiconductor integrated circuit consisting of a PLL frequency synthesizer for use in personal radio equipment. It contains an 1/128 and 1/129 2-modulus prescaler allowing the direct synthesis of local oscillator frequency up to 500MHz.

The reference frequency is provided by a 12.8MHz crystal oscillator.

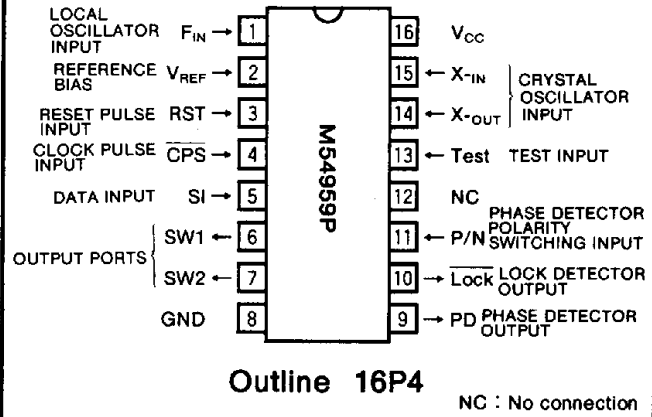
FEATURES

- Built-in 1/128 and 1/129 2-modulus prescaler ( $f_{max}=500MHz$ )
- Low power consumption ( $I_{CC}=20mA$ , at  $V_{CC}=5V$ )
- Reference frequency selectable from four values (25k, 12.5k, 6.25k, 5k)
- Wide range of division ratio (16384~131071, binary coded)
- Serial data input (3 data-transfer lines)
- PLL Lock/unlock status display output
- Output-ports state can be set by date from a controller

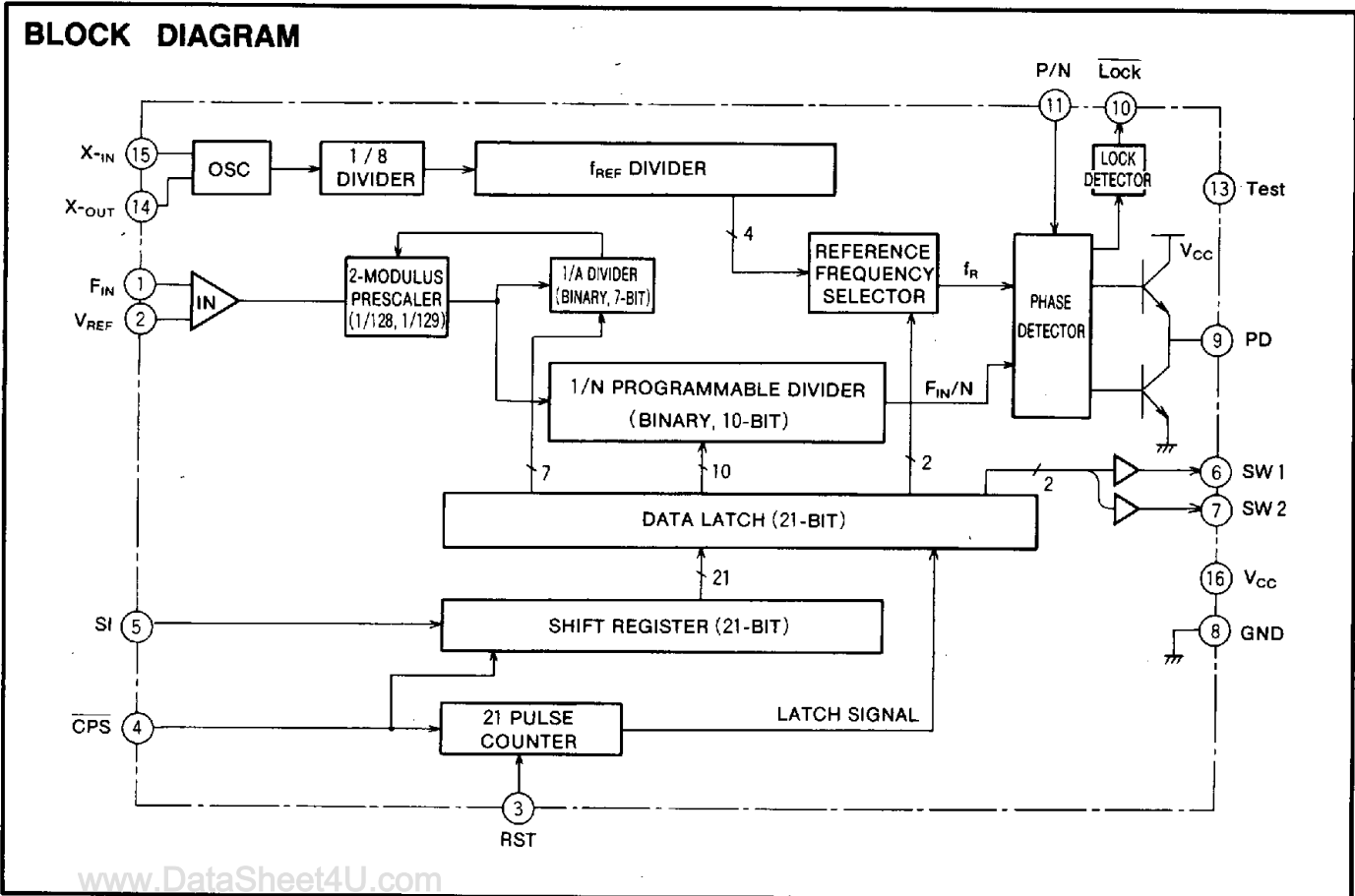
APPLICATION

Personal radio

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



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## PLL FREQUENCY SYNTHESIZER FOR PERSONAL RADIOS

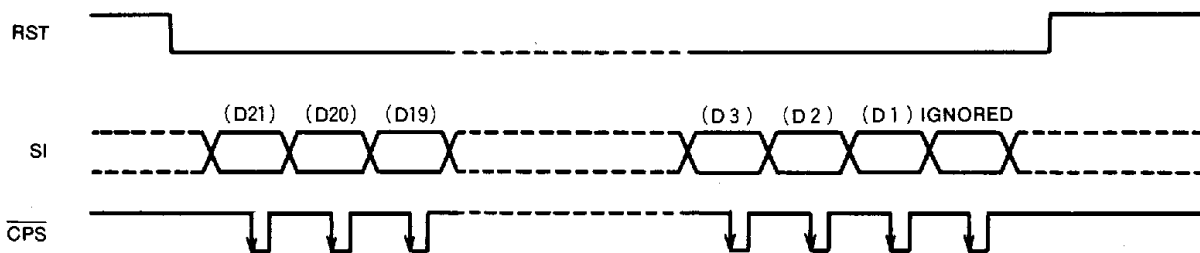
## PIN DESCRIPTION

No.	Symbol	Pin name	Description
1	$F_{IN}$	Local oscillator input	Local oscillator frequency (V.C.O) input. $f_{max}=500\text{MHz}$
2	$V_{REF}$	Reference bias	Ground through a 1000pF capacitor
3	RST	Reset pulse input	Reset pulse input for 21-pulse counter
4	$\overline{CPS}$	Clock pulse input	Clock pulse input for shift register
5	SI	Data input	Data input for shift register
6	SW1	Output port	Open collector output port. State can be set by data from a controller.
7	SW2		
8	GND	GND	0 V
9	PD	Phase detector output	Three-state
10	$\overline{Lock}$	Lock detector output	Low when PLL locked, and high when unlocked. Open collector.
11	P/N	Phase detector polarity switching	When high, PD goes high as the phase advances and low as the phase delays. When low, PD goes low as the phase advances, and high as the phase delays.
12	NC	No connection	Open or GND
13	Test	Test input	Normally set low. When set high, $f_R$ (reference frequency) is output from SW1 (pin 6), and $f_{IN}/N$ (programmable divider output) is output from SW2 (pin 7).
14	$X^{-}OUT$	Crystal oscillator input	Apply the output from the 12.8MHz reference oscillator to $X^{-}IN$ . A crystal resonator can also be connected.
15	$X^{-}IN$		
16	$V_{CC}$	Power supply pin	4.5~5.5V

## FUNCTION

## 1. DATA INPUT

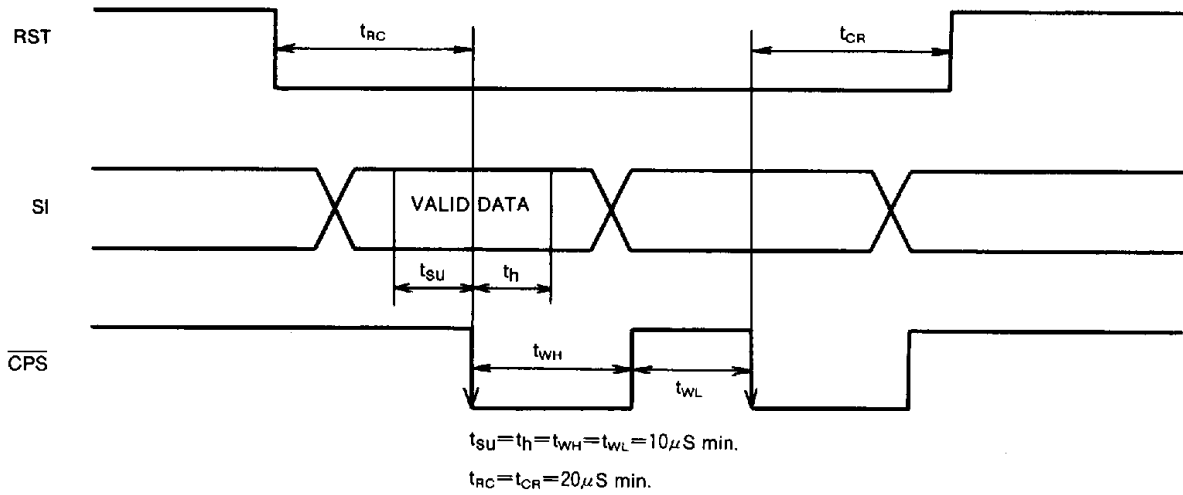
Configuration of input signal



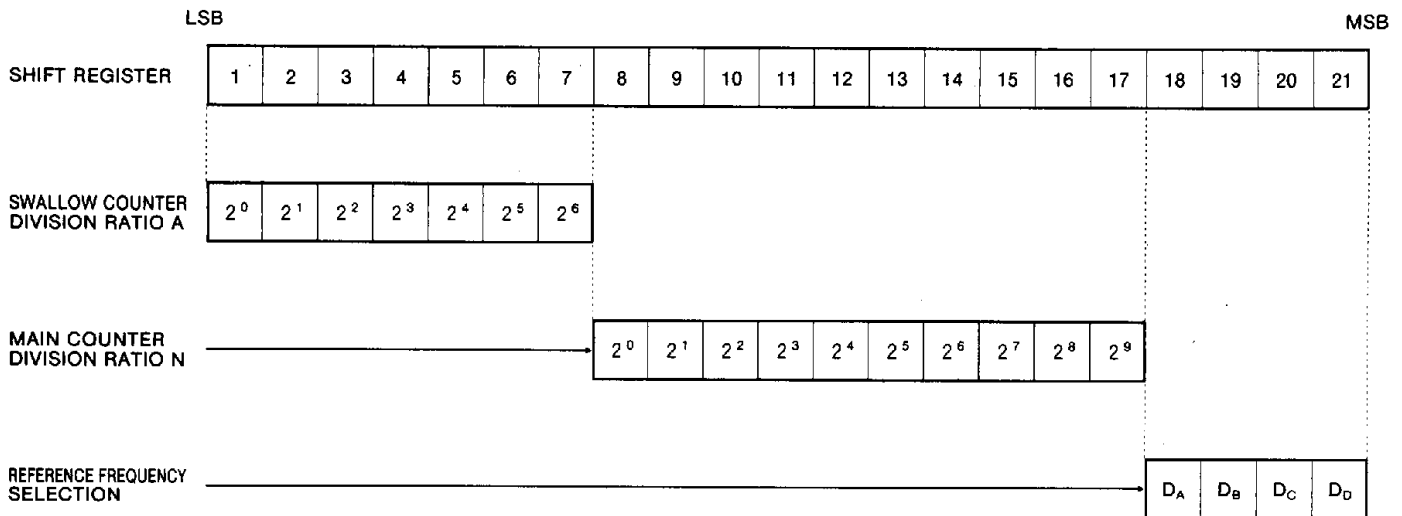
- Note 1 : Data at input SI is read into shift register sequentially by the falling edge of the clock signal at input  $\overline{CPS}$ .  
 2 : All data (N value, port, reference frequency) are set by the falling edge of the 21st clock pulse at  $\overline{CPS}$ .  
 Additional pulses at CPS are ignored.  
 3 : When RST is high, inputs are accepted at neither  $\overline{CPS}$  nor SI.

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Timing of input signal



2. BIT CONFIGURATION OF SHIFT REGISTER



Note 4 : Total division ratio M is given by  $M=A+128N$ .

Note 5 : The reference frequency is selected by D<sub>A</sub> and D<sub>B</sub>.

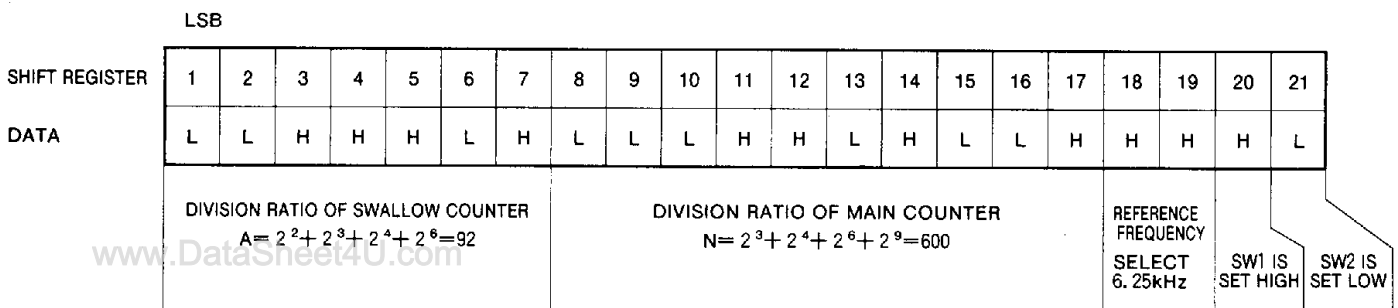
Note 6 : The output port is selected by D<sub>C</sub> and D<sub>D</sub>.

Data		Reference frequency
D <sub>A</sub>	D <sub>B</sub>	
L	L	50k
H	L	25k
L	H	12.5k
H	H	6.25k

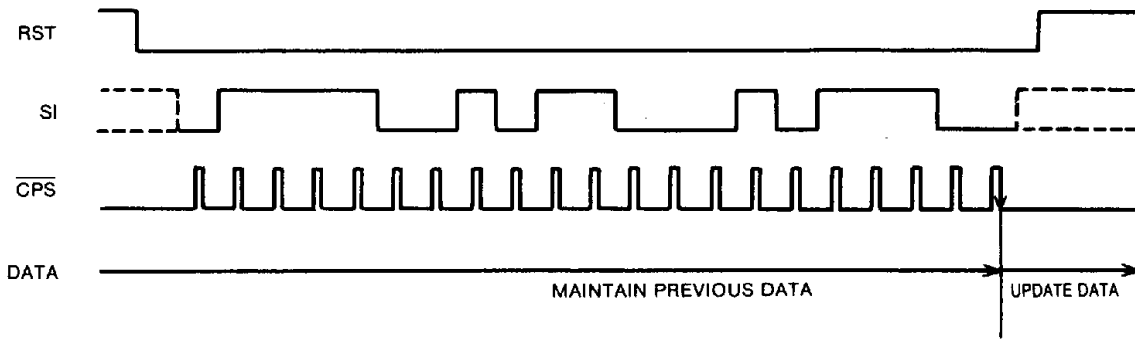
Data		Output port	
D <sub>C</sub>	D <sub>D</sub>	SW1	SW2
L	L	L	L
H	L	H	L
L	H	L	H
H	H	H	H

3. DATA CODING EXAMPLE

Reference frequency 6.25kHz, M=76892, SW1="H", SW2="L"



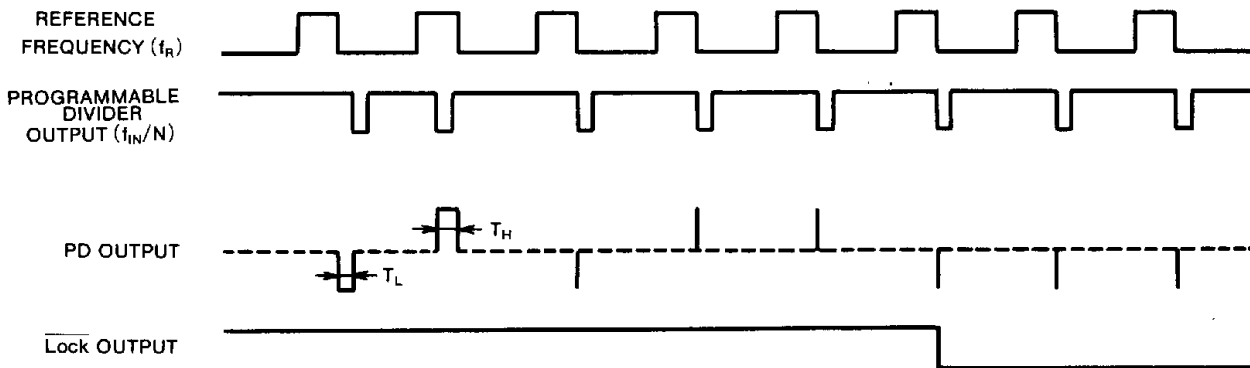
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Note 7 : Total division ratio is set by  $M=A+128N=92+128\times 600=76892$ .

8 : When PLL is locked,  $f_{v.c.o}=6.25\times 76892=480575\text{kHz}$   
 $=480.575\text{MHz}$

4. PD AND Lock WAVEFORMS



Note 9 : When the phase of programmable divider output  $f_{IN}/N$  is behind the phase of reference frequency  $f_R$ , PD is low; when  $f_{IN}/N$  is ahead of  $f_R$ , PD is high.

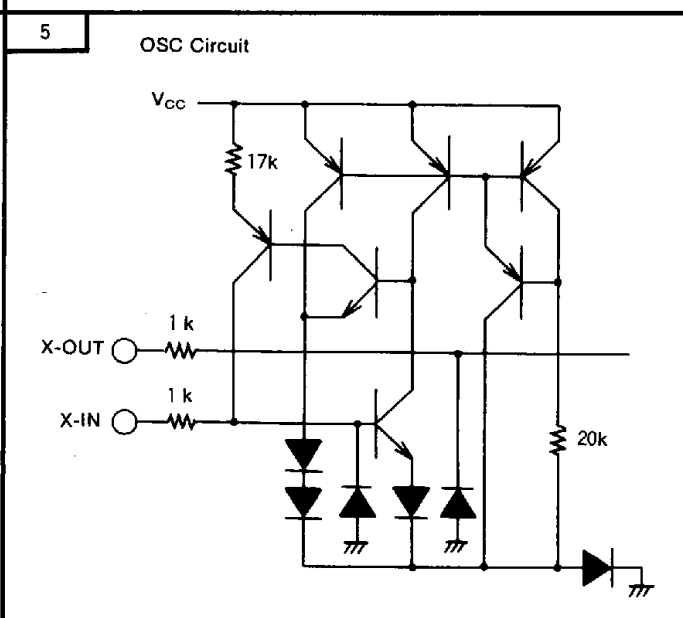
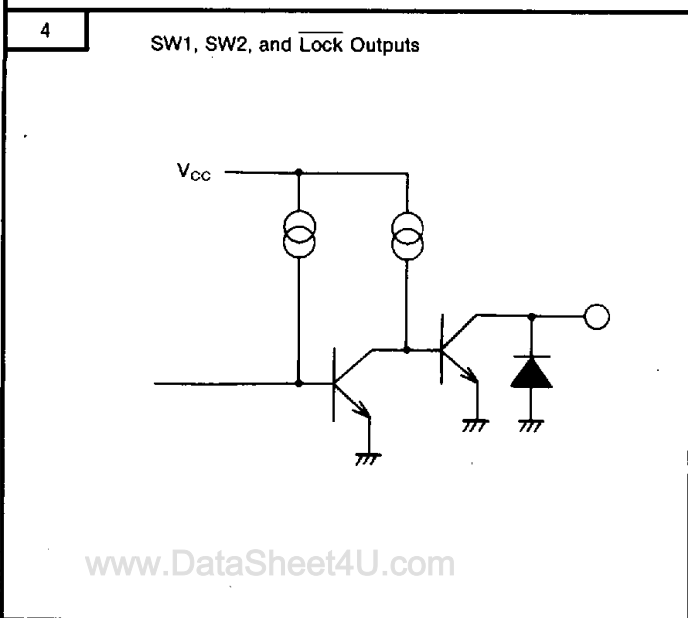
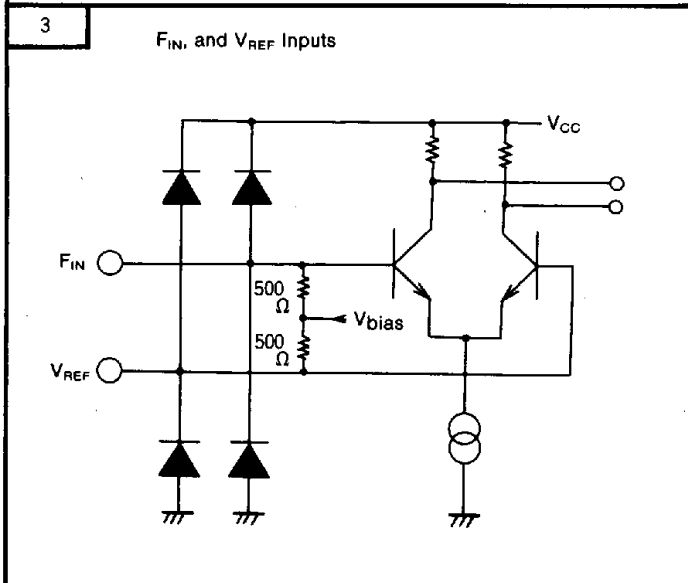
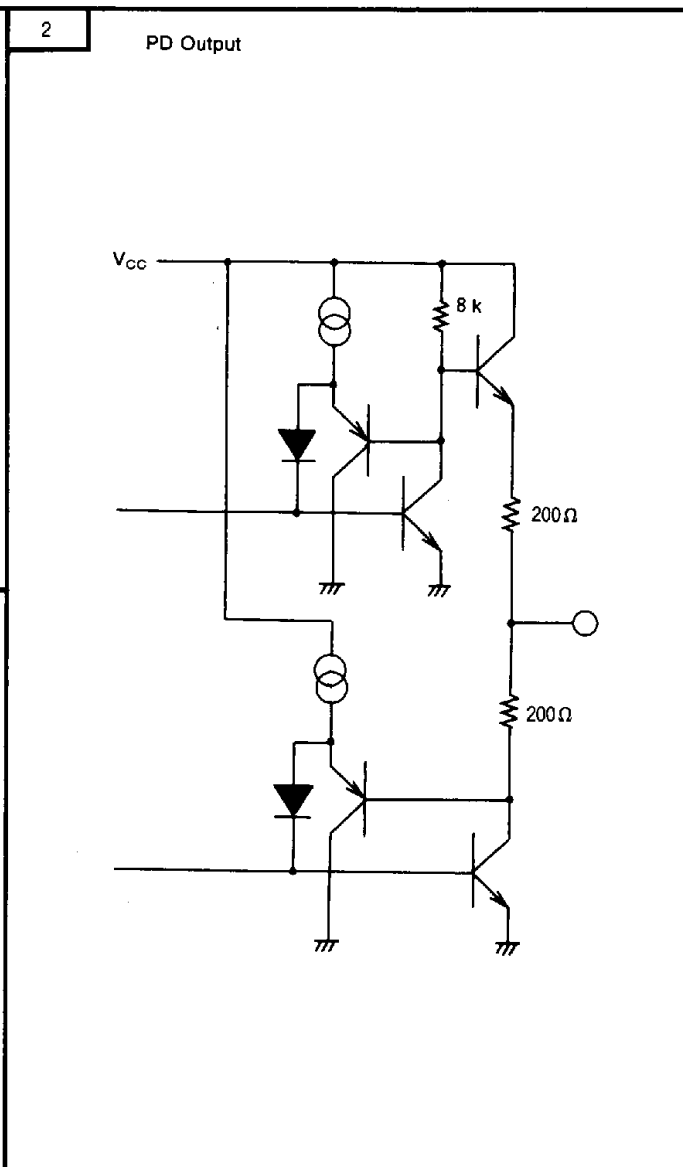
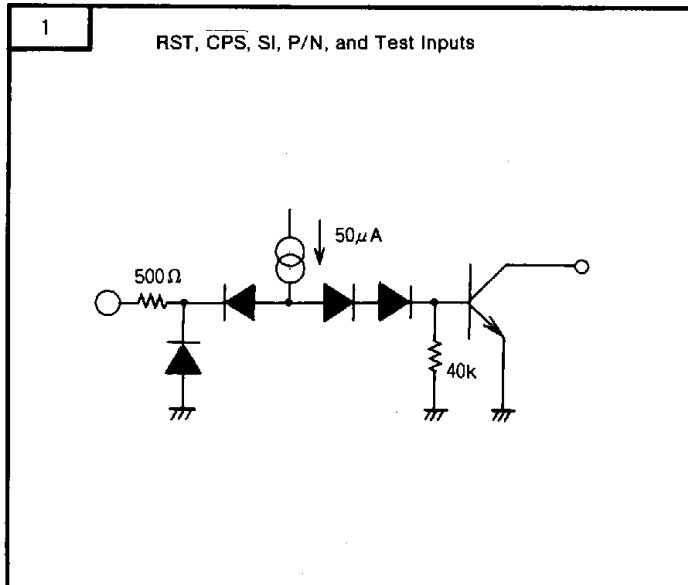
10 : Broken lines indicate the high impedance state.

11 : If phase differences  $T_L$  and  $T_H$  continue at less than 625ns for more than three cycles of reference frequency  $f_R$ , LOCK becomes low.

※The above description applies when input P/N (pin 11) is high.  
 When P/N is low, the output at PD is inverted.

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I/O CIRCUITS



Note 12 : Resistance and current values are typical at  $V_{\text{CC}}=5\text{ V}$ ,  $T_a=25^\circ\text{C}$ .

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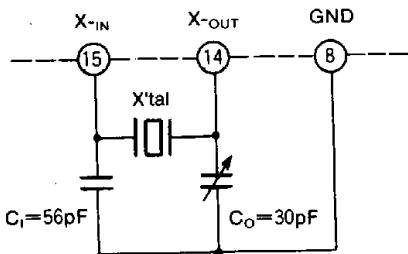
ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub> = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings		Unit	Remarks
			Min	Max		
V <sub>CC</sub>	Supply voltage		-0.5	6.0	V	
V <sub>I</sub>	Input voltage	All inputs	-0.5	6.0	V	
V <sub>O</sub>	Output voltage	All outputs	-0.5	6.0	V	
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 75°C		500	mW	Package permissible power dissipation
T <sub>opr</sub>	Operating temperature		-20	+75	°C	
T <sub>stg</sub>	Storage temperature		-40	+125	°C	

RECOMMENDED OPERATING CONDITIONS (V<sub>CC</sub> = 4.5~5.5V, T<sub>a</sub> = -20~+75°C unless otherwise noted)

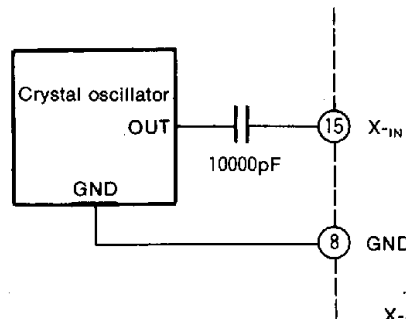
Symbol	Parameter	Conditions	Limits			Unit	Remarks
			Min	Typ	Max		
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	V	
V <sub>IN</sub>	Input amplitude	F <sub>IN</sub> = 100~1000MHz	200		800	mV <sub>P-P</sub>	
F <sub>IN1</sub>	Input frequency	V <sub>IN</sub> = 200~800mV <sub>P-P</sub>	100		500	MHz	
I <sub>OL</sub>	Low-level output current	SW1, SW2, and Lock outputs			5	mA	
V <sub>X-IN</sub>	X-IN input amplitude	Note 14	1		2	V <sub>P-P</sub>	Sine wave
f <sub>OSC</sub>	Reference oscillator frequency			12.8		MHz	

Note 13 : Cristal oscillator circuit



Lpad capacitance of crystal 20pF  
Effective resistance less than 100Ω

Note 14 : Cristal oscillator circuit



X-OUT (pin 14) is left open.

ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = -20~+75°C, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions	Limits			Unit
				Min	Typ	Max	
V <sub>IH</sub>	High-level input voltage	3, 4, 5, 11, 13	V <sub>CC</sub> =5.5V	2.0			V
V <sub>IL</sub>	Low-level input voltage	3, 4, 5, 11, 13	V <sub>CC</sub> =5.5V			0.6	V
I <sub>IH</sub>	High-level input current	3, 4, 5, 11, 13	V <sub>CC</sub> =5.5V, V <sub>IH</sub> =5.5V			30	μA
I <sub>IL</sub>	Low-level input current	3, 4, 5, 11, 13	V <sub>CC</sub> =4.5V, V <sub>IL</sub> =0V		-50	-100	μA
V <sub>OL</sub>	Low-level output voltage	6, 7, 10, 12	V <sub>CC</sub> =4.5V, I <sub>OL</sub> =5mA			0.5	V
V <sub>OHP1</sub>	PD high-level output voltage	9	V <sub>CC</sub> =4.5V, I <sub>OH</sub> =-1mA	3.0			V
V <sub>OHP2</sub>	PD high-level output voltage	9	V <sub>CC</sub> =5V, I <sub>OH</sub> =-0.1mA	4.0			V
V <sub>OLP1</sub>	PD low-level output voltage	9	V <sub>CC</sub> =4.5V, I <sub>OL</sub> =1mA			1.5	V
V <sub>OLP2</sub>	PD low-level output voltage	9	V <sub>CC</sub> =5V, I <sub>OL</sub> =0.1mA			1.0	V
I <sub>PD1</sub>	PD leakage current	9	V <sub>CC</sub> =5.5V, V <sub>O</sub> =0.8~4.7V			±1.0	μA
I <sub>PD2</sub>	PD leakage current	9	V <sub>CC</sub> =5V, V <sub>O</sub> =2.5V			±100	μA
I <sub>CC</sub>	Supply current		V <sub>CC</sub> =5.5V		20	30	mA
I <sub>OLK</sub>	Output leakage current	6, 7, 10	V <sub>CC</sub> =5.5V, V <sub>OH</sub> =5.5V			30	μA

Note 15 : All voltages are measured with respect to circuit ground (pin 8)

16 : Currents are taken to be positive (negative sign) when flowing out of the circuit.

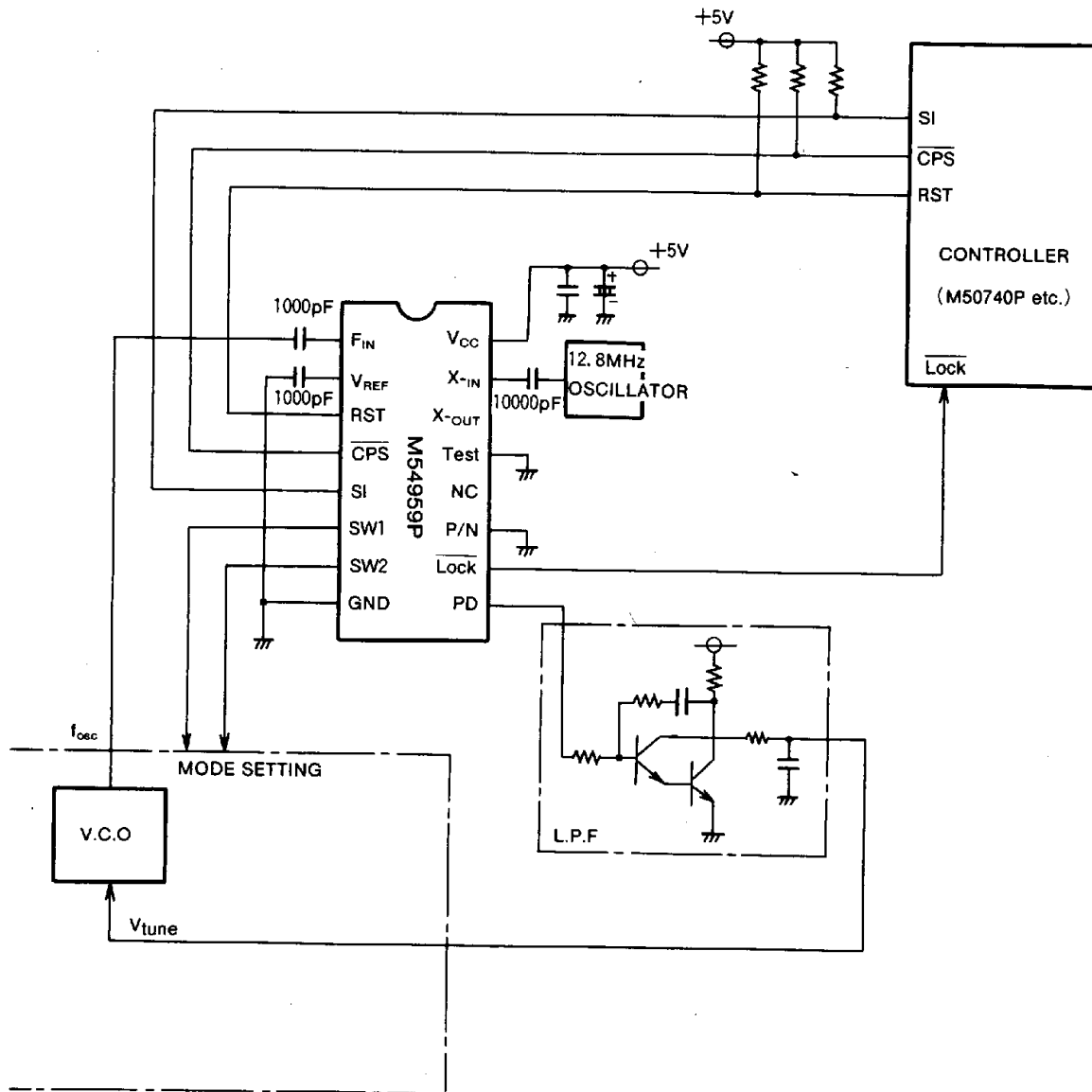
The minimum and maximum values are taken to be absolute values.

17 : Typical values are at V<sub>CC</sub>=5V, T<sub>a</sub>=25°C

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APPLICATION EXAMPLE



TYPICAL CHARACTERISTICS

INPUT AMPLITUDE VS INPUT FREQUENCY

