

M54974P

Bi-CMOS 12-BIT SERIAL-INPUT LATCHED DRIVER

DESCRIPTION

The M54974P is a semiconductor integrated circuit consisting of 12 stages of CMOS shift registers and latches with serial inputs and serial or parallel outputs. It is based on Bi-CMOS process technology, and has 12 bipolar drivers at the parallel outputs.

FEATURES

- Serial input and serial or parallel output
- Serial output enables cascade connection
- Built-in latch for each stage
- Enable input provides output control
- Low supply current (standby current $I_{cc} \leq 10\mu A$)
- Serial I/O level is compatible with typical CMOS devices
- Driver features: High withstand voltage ($BV_{CE0} \geq 30V$)
Capable of large drive currents ($I_{O(max)} = 300mA$)
- Wide operating temperature range $T_a = -20 - +75^\circ C$

APPLICATION

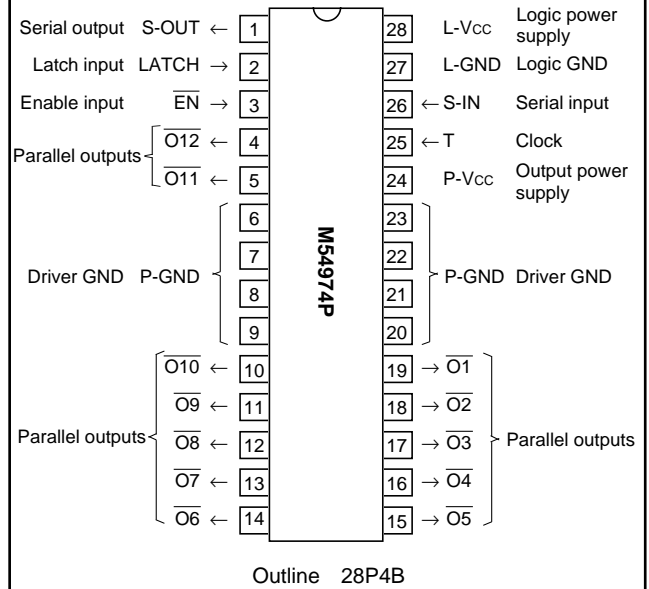
Dot drivers for thermal print heads. Serial/parallel conversion. Drivers for relay and solenoids.

FUNCTION

The M54974P consists of 12 stages of D-type flip flops connected to 12 latches.

Data is input to serial input S-IN, and clock pulses are applied to clock input T. When the clock changes from low to high, the input data enters the first shift register and data already in the shift

PIN CONFIGURATION (TOP VIEW)

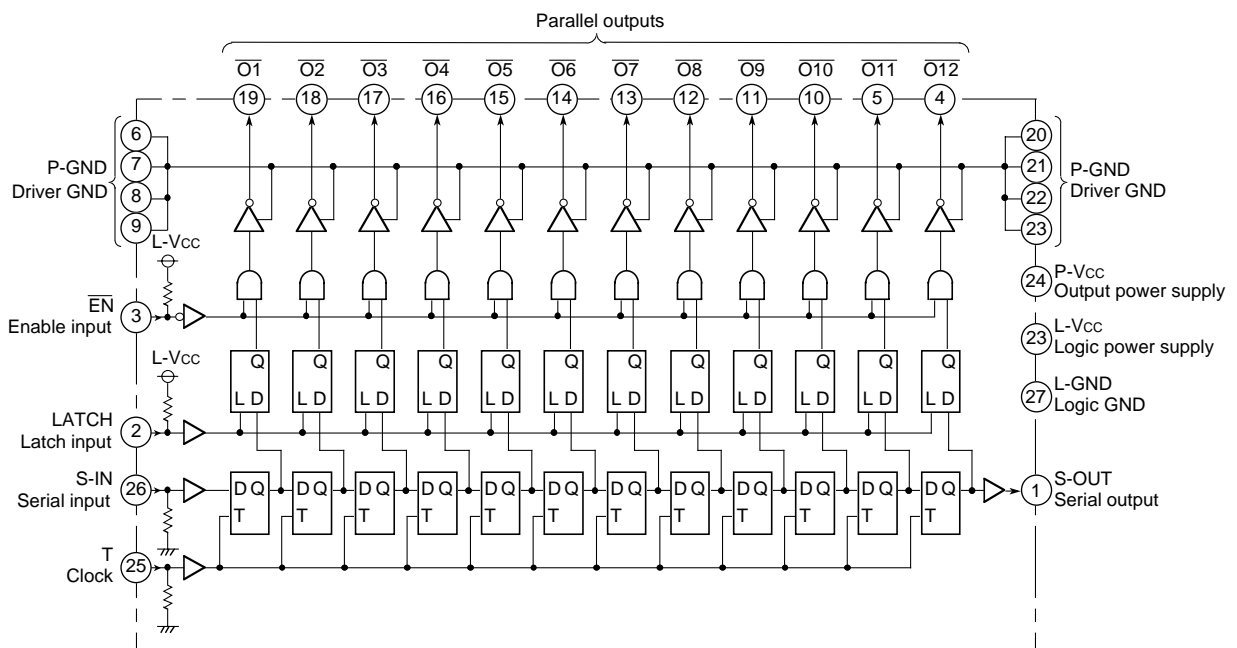


registers is shifted sequentially.

The serial output S-OUT is used to connect multiple M54974Ps to expand the number of parallel outputs. S-OUT is connected to S-IN of the next stage.

When the clock pulse changes from low to high, latch input (LATCH) is high and output enable input (\overline{EN}) is low the serial input data at S-IN appears at output $\overline{O1}$ and the other data already

BLOCK DIAGRAM



BI-CMOS 12-BIT SERIAL-INPUT LATCHED DRIVER

present is shifted sequentially to outputs $\overline{O2}$ through $\overline{O12}$.

The parallel outputs are inverted.

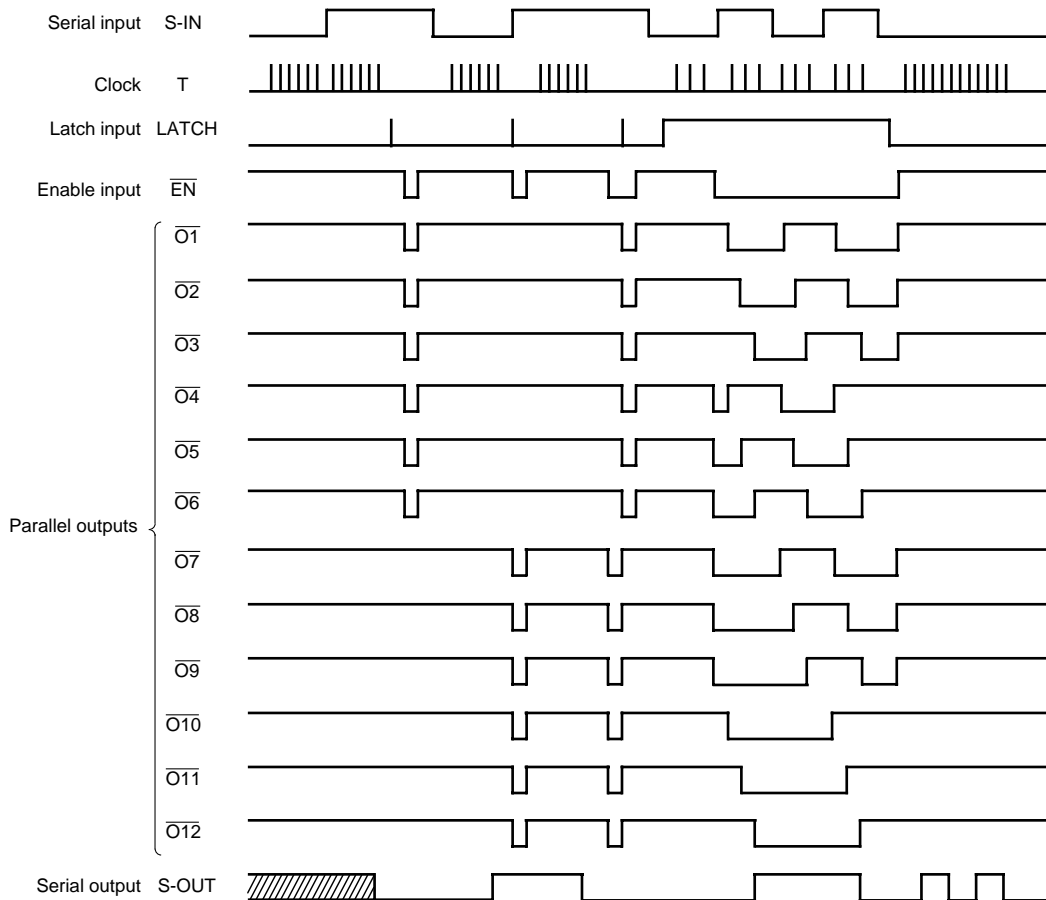
When the latch input is held low, the latch retains the stored data.

When the \overline{EN} input is high, outputs $\overline{O1}$ through $\overline{O12}$ all turn off. As the internal logic is unstable when the power is turned on, the \overline{EN}

input should be kept high (setting the outputs $\overline{O1}$ through $\overline{O12}$ off) until input data is set and the internal logic is initialized.

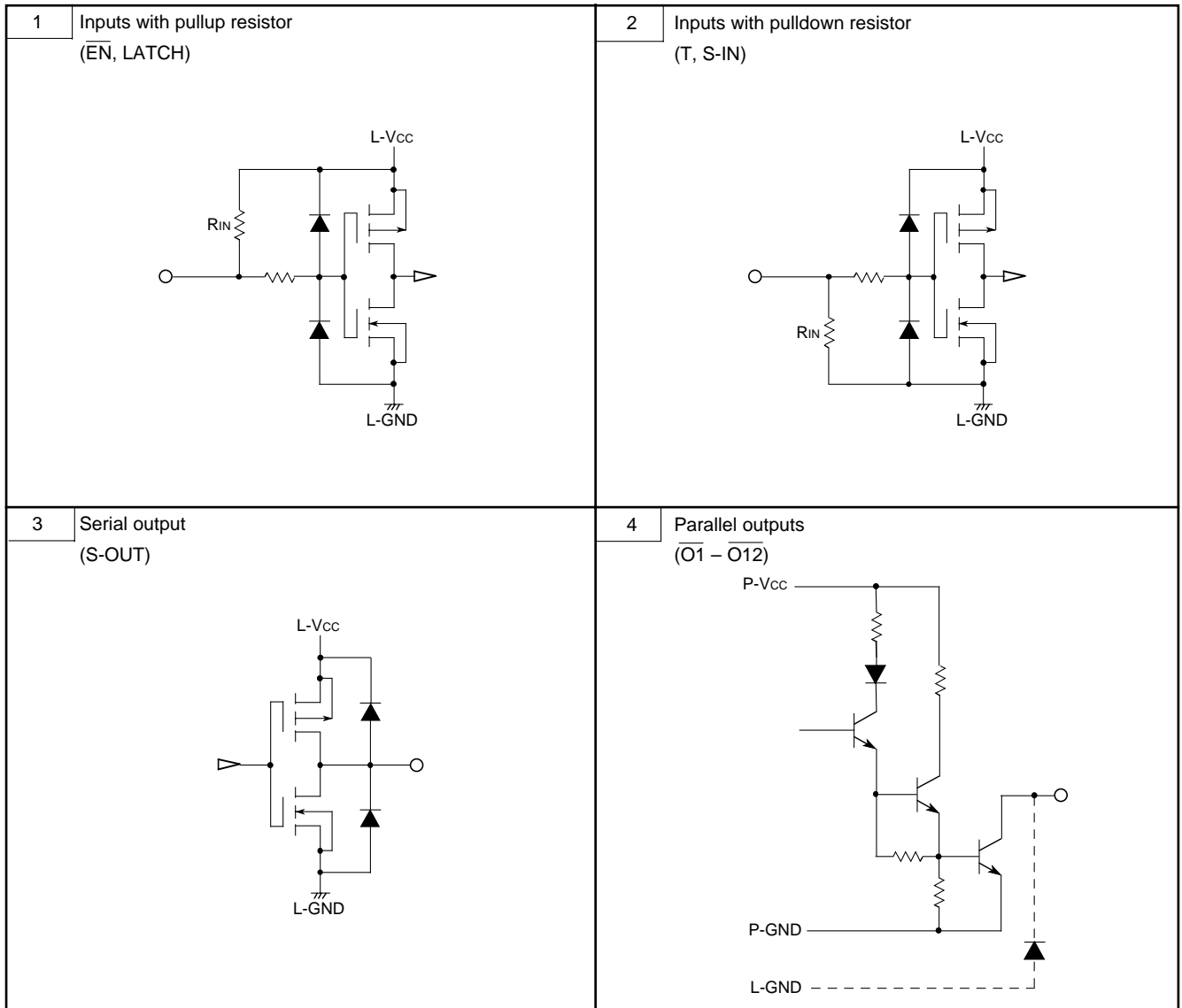
L-GND is the GND of CMOS logic circuit and P-GND is the GND of output driver circuits $\overline{O1}$ through $\overline{O12}$ which employ bipolar transistors capable of large drive currents.

TIMING CHART



* The shaded area shows the unstable state.

INPUT/OUTPUT CIRCUIT DIAGRAM



Bi-CMOS 12-BIT SERIAL-INPUT LATCHED DRIVER

ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	P-Vcc, L-Vcc	-0.5 – 8	V
Vi	Input voltage	S-IN, LATCH, T, \overline{EN}	-0.5 – Vcc+0.5	V
Vo	Output voltage	S-OUT	-0.5 – Vcc+0.5	V
		$\overline{O1} - \overline{O12}$: OFF	-0.5 – 30	
Io	Output current	$\overline{O1} - \overline{O12}$	400	mA
Pd	Power dissipation	Ta=25°C	2.5	W
Topr	Operating temperature		-20 – 75	°C
Tstg	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage	P-Vcc, L-Vcc	4	5	6	V
Vo	Output apply voltage	$\overline{O1} - \overline{O12}$: OFF			30	V
Io	Output current (per circuit)	All outputs go in the ON state simultaneously. Duty cycle < 50%, Ta < 25°C			300	mA

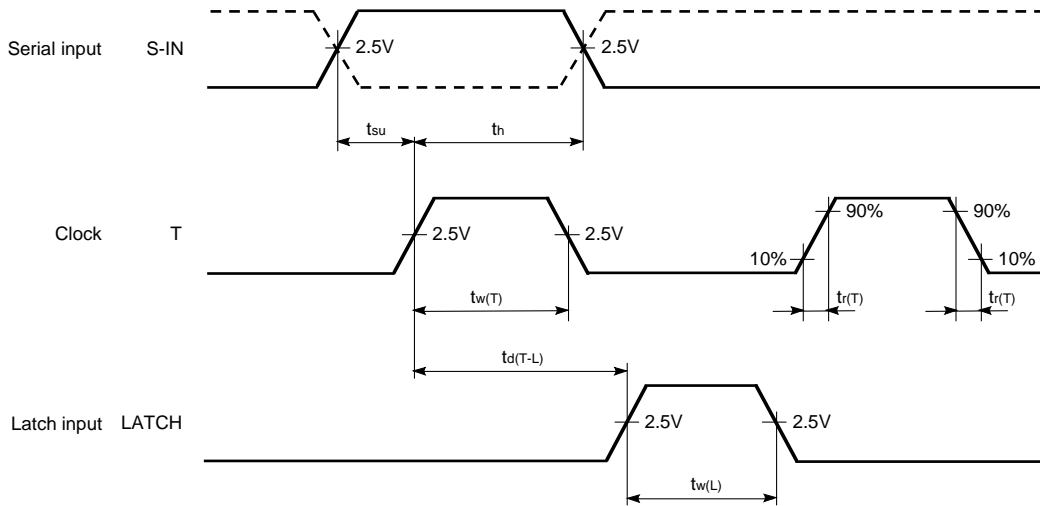
ELECTRICAL CHARACTERISTICS (Ta=25°C, L-Vcc=5V, P-Vcc=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit	
				Min.	Typ.	Max.		
VIH	High-level input voltage		Ta=-20 – 75°C	0.7Vcc		Vcc	V	
VIL	Low-level input voltage			0		0.3Vcc	V	
RIN	Input resistance			50			kΩ	
VOH	High-level output voltage	S-OUT	Io ≤1μA	4.9			V	
VOL	Low-level output voltage	S-OUT				0.1	V	
IOH	High-level output current	S-OUT	VOH=4.5V	-100			μA	
IOL	Low-level output current	S-OUT	VOL=0.4V	400			μA	
VOL1	Low-level output voltage	$\overline{O1} - \overline{O12}$	IoL=120mA			0.4	V	
VOL2								
VOL3								0.7
IOLK	Output leak current	$\overline{O1} - \overline{O12}$	Vo=30V			50	μA	
ICC1	Supply current (L-Vcc)		Input: open, All driver outputs: OFF			10	μA	
ICC2			One driver output is ON.			0.2	mA	
ICC3	Output supply current (P-Vcc)		One driver output is ON.			14	mA	

TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f(T)	Clock frequency	Input duty: 40 – 60%			2	MHz
tw(T)	Clock pulse width		200			ns
tw(L)	Latch pulse width		200			ns
tsu	Data setup time		100			ns
th	Data hold time		100			ns
td(T-L)	Clock-latch time		400			ns
tr(T)	Clock pulse rise time				500	ns
tf(T)	Clock pulse fall time				500	ns

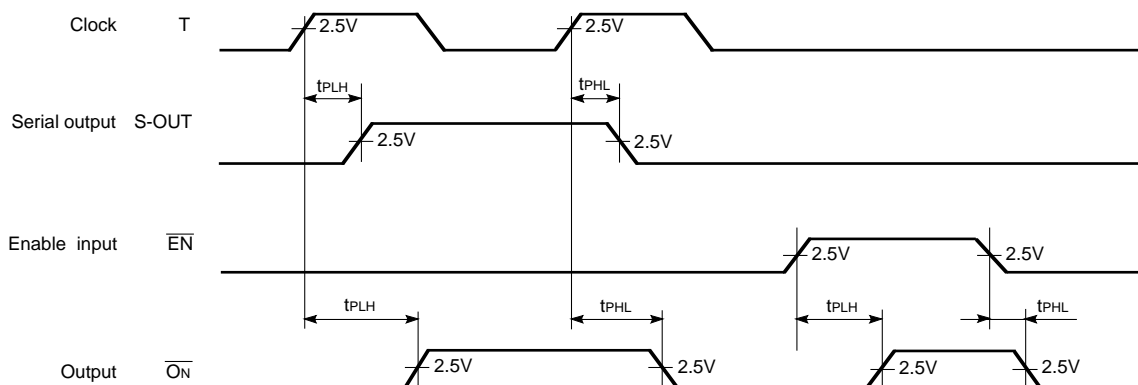
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, VCC=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tPLH	Low-to-high-level output propagation time, From input T to output S-OUT	VIH=5V VIL=0V RL(S-OUT)=∞ RL(ON)=100Ω (N=1-12) CL=15pF		(0.15)	0.3	μs
tPHL	High-to-low-level output propagation time, From input T to output S-OUT			(0.15)	0.3	μs
tPLH	Low-to-high-level output propagation time, From input T to output ON			(2)	10	μs
tPHL	High-to-low-level output propagation time, From input T to output ON			(1)	5	μs
tPLH	Low-to-high-level output propagation time, From input EN to output ON			(2)	10	μs
tPHL	High-to-low-level output propagation time, From input EN to output ON			(1)	5	μs

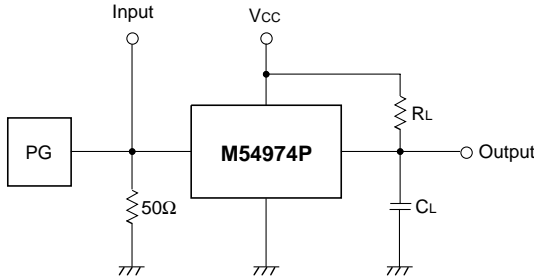
TIMING CHART



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TEST CIRCUIT



- The input waveform: $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
- The capacitance C_L includes the stray wiring capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

