

## 8 BIT SIPO SHIFT REGISTER

- HIGH SPEED  
 $t_{PD} = 20 \text{ ns (TYP.) AT } V_{CC} = 5 \text{ V}$
- LOW POWER DISSIPATION  
 $I_{CC} = 4 \mu\text{A (MAX.) AT } T_A = 25 \text{ }^\circ\text{C}$
- OUTPUT DRIVE CAPABILITY  
 10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS  
 $t_{PLH} = t_{PHL} = 4 \text{ nA (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE  
 $I_{OL} = |I_{OH}| = 4 \text{ mA (MIN.)}$
- COMPATIBLE WITH TTL OUTPUTS  
 $V_{IH} = 2 \text{ V (MIN.) } V_{IL} = 0.8 \text{ V (MAX.)}$
- WIDE OPERATING VOLTAGE RANGE  
 $V_{CC} \text{ (OPR)} = 2 \text{ V TO } 6 \text{ V}$
- PIN AND FUNCTION COMPATIBLE  
 WITH 54/74LS164

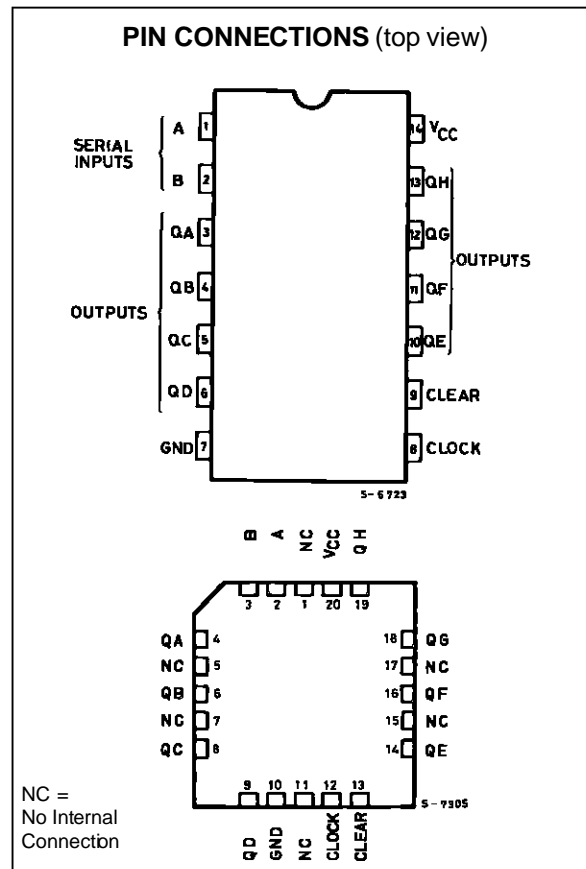
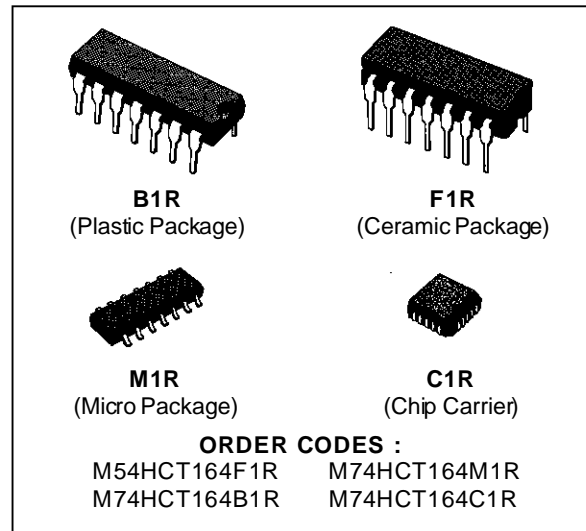
### DESCRIPTION

The M54/74HCT164 is a high speed CMOS 8 BIT SIPO SHIFT REGISTER fabricated in silicon gate C<sup>2</sup>MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

The HCT164 is an 8 bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B), either of these inputs can be used as an active high enable for data entry through the other input. An unused input must be high, or both inputs connected together. Each low-to-high transition on the clock input shifts data one place to the right and enters into QA, the logic NAND of the two data inputs ( $A \cdot B$ ), the data that existed before the rising clock edge. A low level on the clear input overrides all other inputs and clears the register asynchronously, forcing all Q outputs low.

All inputs are equipped with protection circuits against static discharge and transient excess voltage.

This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC<sup>2</sup>MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption.



# M54/M74HCT164

## INPUT AND OUTPUT EQUIVALENT CIRCUIT



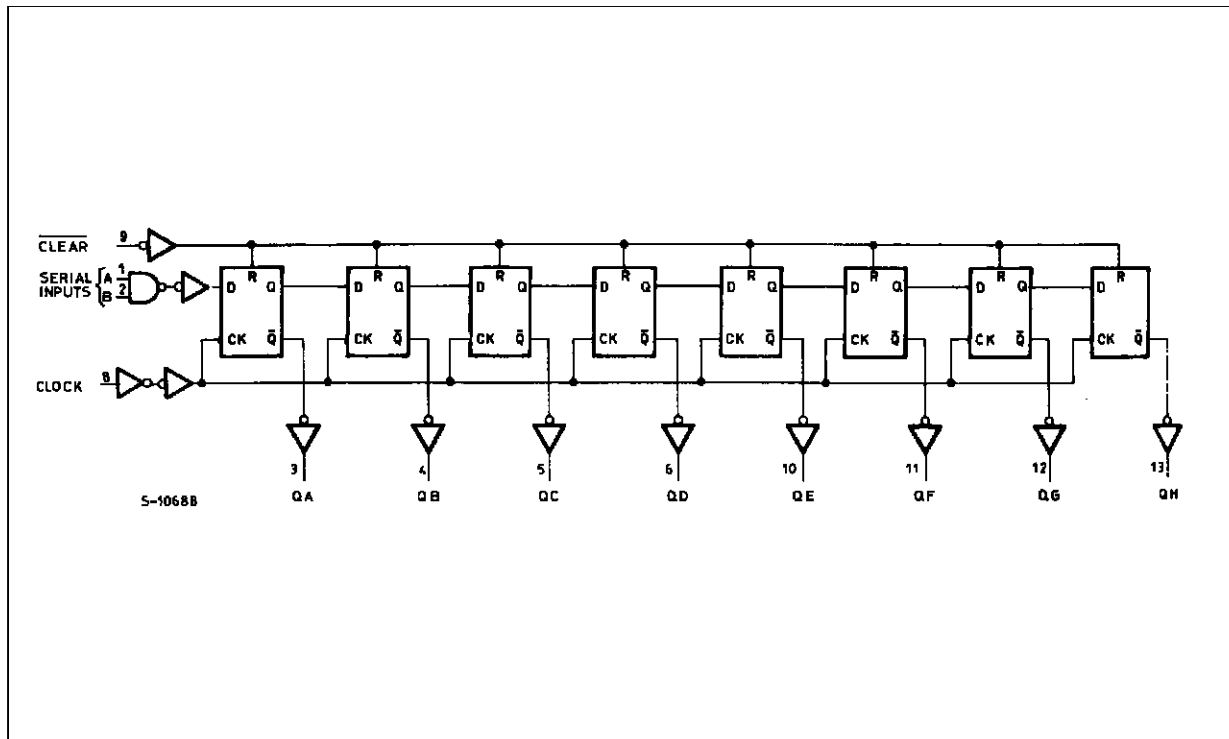
## TRUTH TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	SERIAL IN		QA	QB	.....	QH
		A	B				
L	X	X	X	L	L	.....	L
H		X	X	NO CHANGE			
H		L	X	L	QAn	.....	QGn
H		X	L	L	QAn	.....	QGn
H		H	H	H	QAn	.....	QGn

X: Don't Care

QAn - QGn : The level of QA -QG, respectively, before the most-recent transition of th clock.

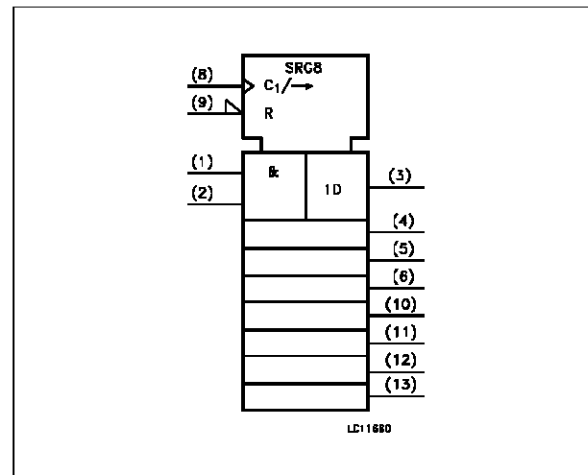
## LOGIC DIAGRAM



**PIN DESCRIPTION**

PIN No	SYMBOL	NAME AND FUNCTION
1, 2	A, B	Data Inputs
3, 4, 5, 6, 10, 11, 12, 13	QA to QH	Outputs
8	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
9	$\overline{\text{CLEAR}}$	Master Reset Input
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive Supply Voltage

**IEC LOGIC SYMBOL**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7	V
V <sub>I</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	± 20	mA
I <sub>OK</sub>	DC Output Diode Current	± 20	mA
I <sub>O</sub>	DC Output Source Sink Current Per Output Pin	± 25	mA
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	± 50	mA
P <sub>D</sub>	Power Dissipation	500 (*)	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.  
 (\*) 500 mW: ± 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	4.5 to 5.5	V
V <sub>I</sub>	Input Voltage	0 to V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	0 to V <sub>CC</sub>	V
T <sub>op</sub>	Operating Temperature: <b>M54HC Series</b> <b>M74HC Series</b>	-55 to +125 -40 to +85	°C °C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (V <sub>CC</sub> = 4.5 to 5.5V)	0 to 500	ns

**DC SPECIFICATIONS**

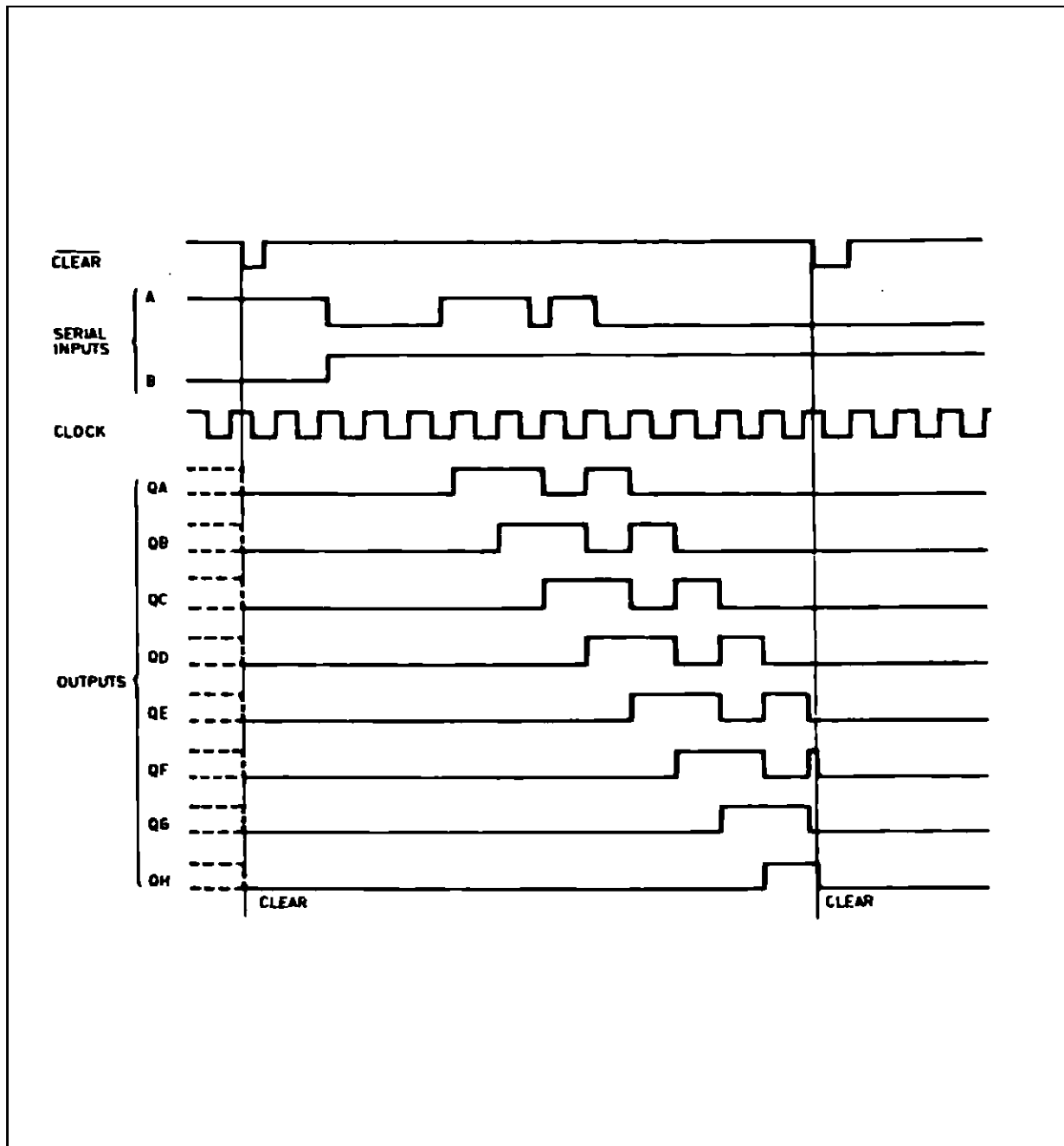
Symbol	Parameter	Test Conditions		Value						Unit		
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC			
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.	
V <sub>IH</sub>	High Level Input Voltage	4.5 to 5.5		2.0			2.0		2.0		V	
V <sub>IL</sub>	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V	
V <sub>OH</sub>	High Level Output Voltage	4.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = -20 μA	4.4	4.5		4.4		4.4	V	
				I <sub>O</sub> = -4.0 mA	4.18	4.31		4.13		4.10		
V <sub>OL</sub>	Low Level Output Voltage	4.5	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 μA		0.0	0.1		0.1		0.1	V
				I <sub>O</sub> = 4.0 mA		0.17	0.26		0.33		0.4	
I <sub>I</sub>	Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND				±0.1		±1		±1	μA
I <sub>CC</sub>	Quiescent Supply Current	5.5	V <sub>I</sub> = V <sub>CC</sub> or GND				4		40		80	μA
ΔI <sub>CC</sub>	Additional worst case supply current	5.5	Per Input pin V <sub>I</sub> = 0.5V or V <sub>I</sub> = 2.4V Other Inputs at V <sub>CC</sub> or GND I <sub>O</sub> = 0				2.0		2.9		3.0	mA

AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$  pF, Input  $t_r = t_f = 6$  ns)

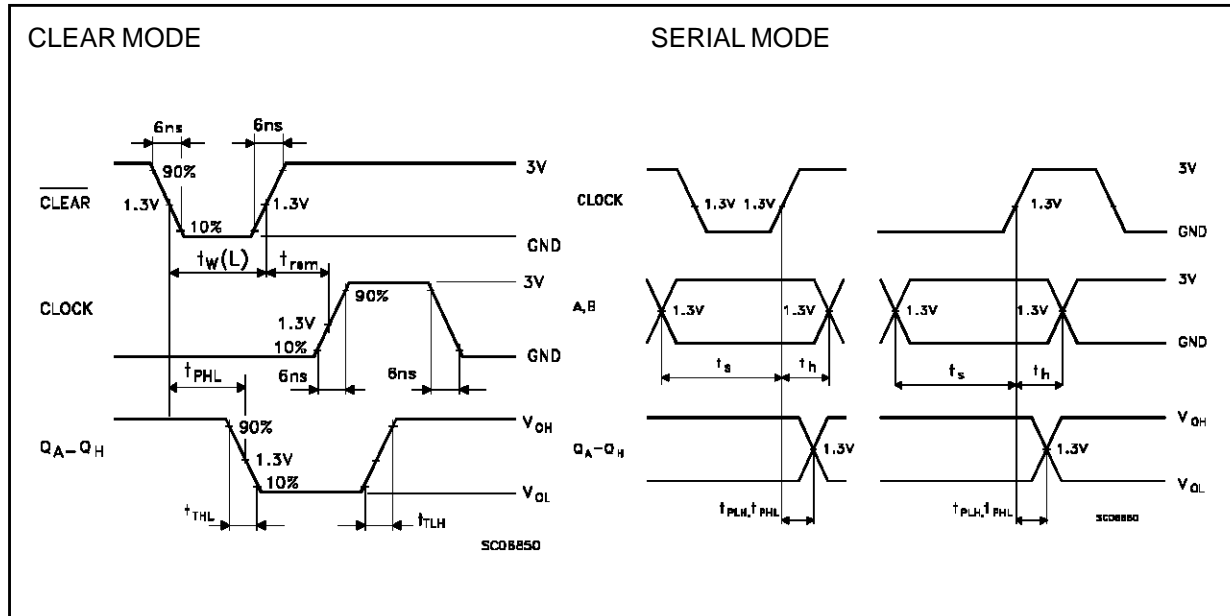
Symbol	Parameter	Test Conditions		Value						Unit	
		V <sub>CC</sub> (V)		T <sub>A</sub> = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t <sub>TLH</sub> t <sub>THL</sub>	Output Transition Time	4.5			8	15		19		22	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CLOCK - Q)	4.5			23	36		45		54	ns
t <sub>PHL</sub>	Propagation Delay Time (CLEAR - Q)	4.5			24	37		46		56	ns
f <sub>MAX</sub>	Maximum Clock Frequency	4.5		30	50		24		20		MHz
t <sub>W(H)</sub> t <sub>W(L)</sub>	Minimum Pulse Width (CLOCK)	4.5			8	15		19		22	ns
t <sub>W(L)</sub>	Minimum Pulse Width (CLEAR)	4.5			8	15		19		22	ns
t <sub>s</sub>	Minimum Set-up Time (A, B - CK)	4.5			4	10		13		15	ns
t <sub>h</sub>	Minimum Hold Time (A, B - CK)	4.5				0		0		0	ns
t <sub>REM</sub>	Minimum Removal Time					5		6		8	ns
C <sub>IN</sub>	Input Capacitance				5	10		10		10	pF
C <sub>PD</sub> (*)	Power Dissipation Capacitance				137						pF

(\*) C<sub>PD</sub> is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.  $I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

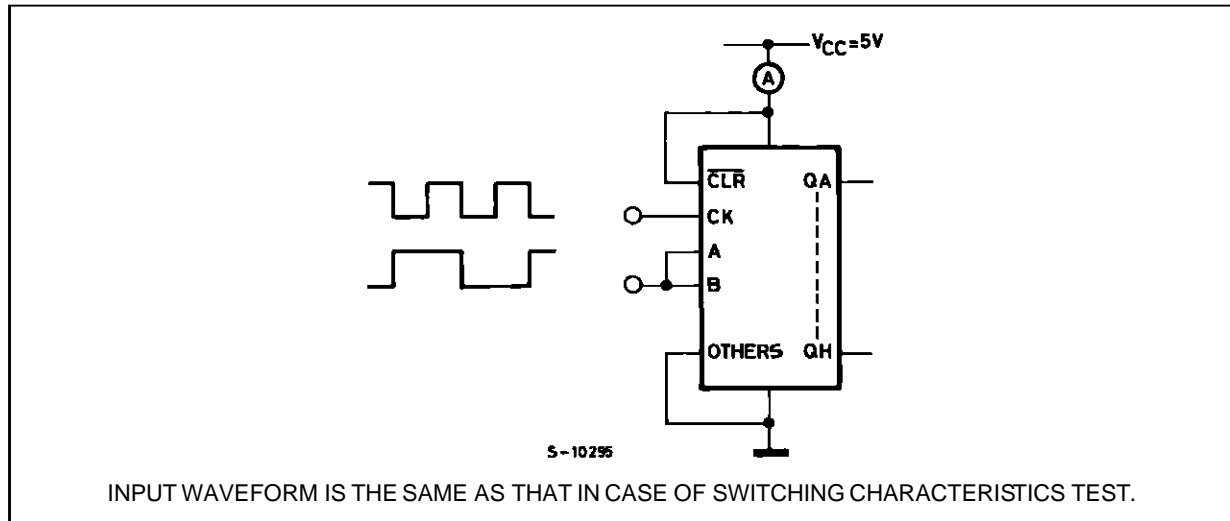
TIMING CHART



SWITCHING CHARACTERISTICS TEST WAVEFORM

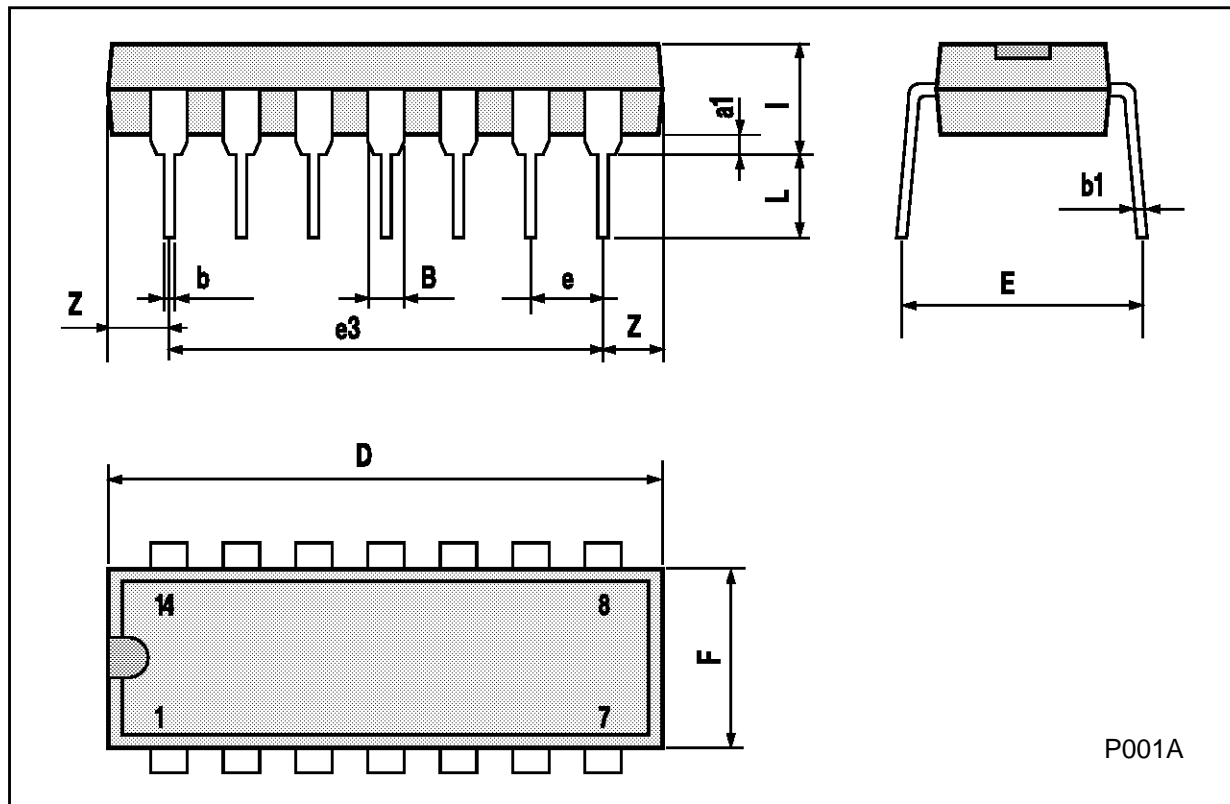


TEST CIRCUIT I<sub>cc</sub> (Opr.)



**Plastic DIP14 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

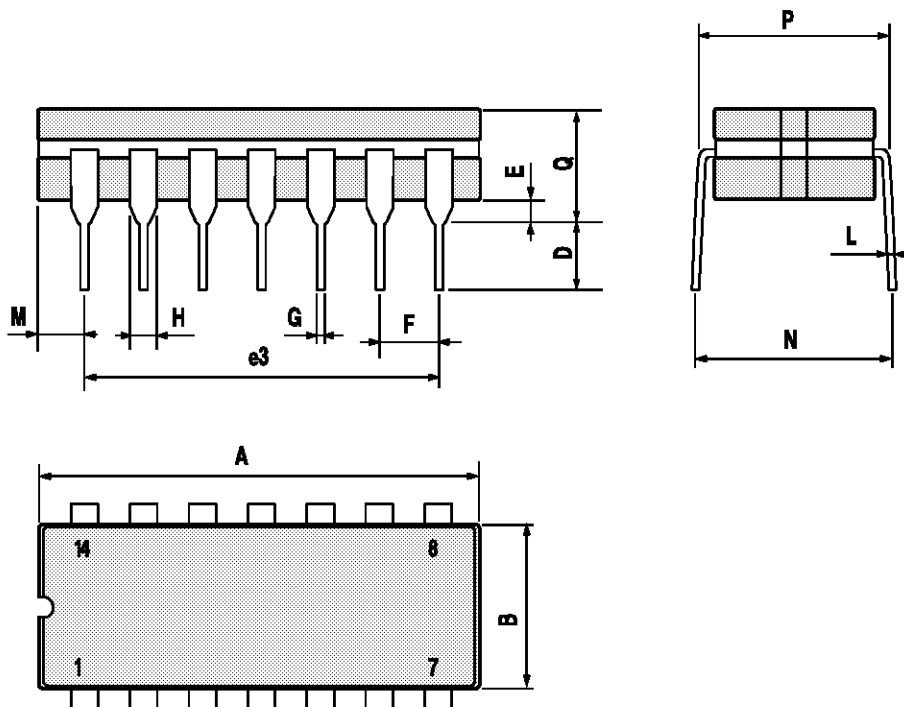


P001A



## Ceramic DIP14/1 MECHANICAL DATA

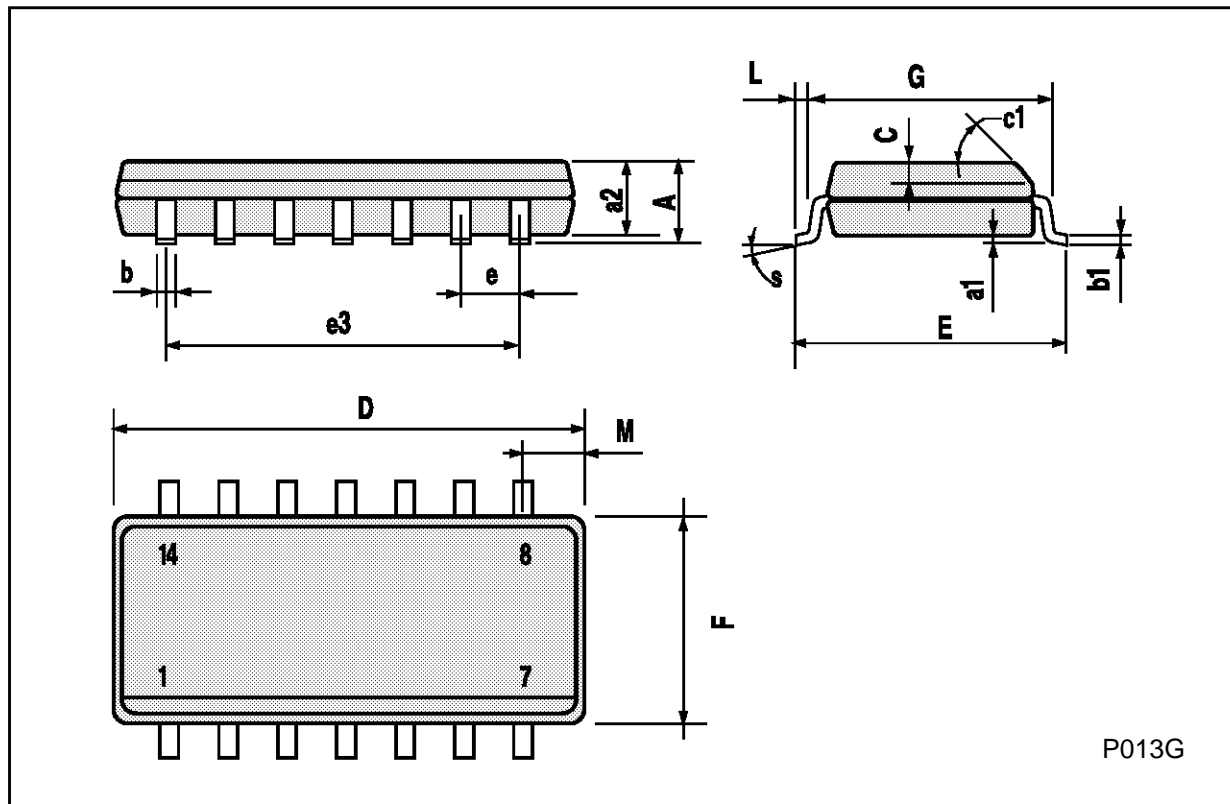
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			20			0.787
B			7.0			0.276
D		3.3			0.130	
E	0.38			0.015		
e3		15.24			0.600	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
H	1.17		1.52	0.046		0.060
L	0.22		0.31	0.009		0.012
M	1.52		2.54	0.060		0.100
N			10.3			0.406
P	7.8		8.05	0.307		0.317
Q			5.08			0.200



P053C

SO14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



P013G

## PLCC20 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	9.78		10.03	0.385		0.395
B	8.89		9.04	0.350		0.356
D	4.2		4.57	0.165		0.180
d1		2.54			0.100	
d2		0.56			0.022	
E	7.37		8.38	0.290		0.330
e		1.27			0.050	
e3		5.08			0.200	
F		0.38			0.015	
G			0.101			0.004
M		1.27			0.050	
M1		1.14			0.045	



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