M58479P
M58482P

CMOS COUNTER/TIMERS

DESCRIPTION

The M58479P and M58482P are electronic timer ICs developed by aluminum-gate CMOS technology. Use of these ICs makes possible timer devices without mechanical elements, which have reduced power dissipation, superior reliability, and higher noise immunity. The M58479P is specifically designed for high noise immunity while the M58482P particularly features low power dissipation.

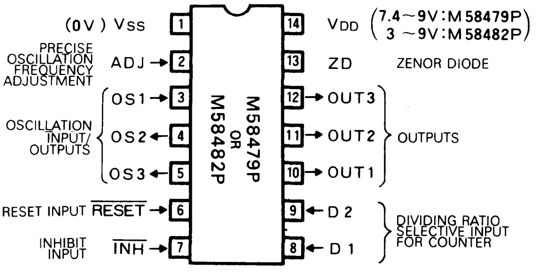
FEATURES

- Low power dissipation
  M58479P: 2mW (typ.), 7.5mW (max.)
  M58482P: 200μW (typ.), 750μW (max.)
- Superior noise immunity
- Single power supply with a zenor diode
- Internal RC oscillator
- Precise oscillation frequency regulating capability
- Extremely broad time-delay range (50ms~4800h)
- Time-delay settable to 10, 60, or 600 times fundamental time (1024 times oscillation period)
- M58479P has automatic-reset function during power engagement
- Built-in reset and inhibit functions
- Residual time display possible by adding Mitsubishi's M53290P and M53242P IC

APPLICATIONS

- Electronic timer or counter with broad time-delay range (50ms~4800h)

PIN CONFIGURATION (TOP VIEW)



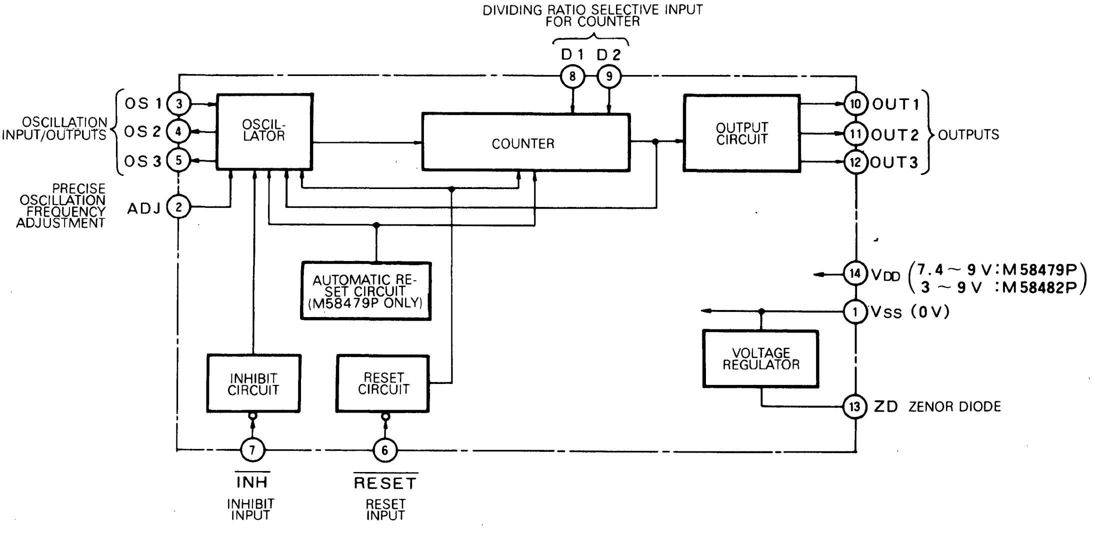
Outline 14P4

FUNCTION

These devices make possible extremely long clock performance, by counting pulse signals from the RC oscillator. It has precise oscillation frequency adjustment, automatic-reset, reset, and inhibit functions.

There are three outputs. When the time duration is up, OUT1 turns from low to high and OUT2 from high to low. OUT3 can be connected to M53290P and M53242P TTLs for residual time display.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{DD}	Supply voltage	With respect to V_{SS}	−0.3～9.5	V
V_I	Input voltage		$V_{SS} \leqq V_I \leqq V_{DD}$	V
Pd	Maximum power dissipation	Ta＝25°C	250	mW
Topr	Operating free-air temperature range		−30～75	°C
Tstg	Storage temperature range		−40～125	°C

RECOMMENDED OPERATING CONDITIONS (Ta＝−30～75°C, unless otherwise noted.)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit
V_{DD}	Supply voltage	M58479P	7.4		9	V
		M58482P	3		9	V
I_{ZD}	Zenor current				10	mA
R_{FC}	Feedback resistance		0.005		10	MΩ
C_{FC}	Oscillation capacitance		0.001		1	μF
R_{FC}	Resistance for fine-adjustment of oscillation frequency		0		100	kΩ
V_{IH}	High-level input voltage, $\overline{RESET}$, $\overline{INH}$, D_1, D_2		0.7×V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage, $\overline{RESET}$, $\overline{INH}$, D_1, D_2		0	0	0.3×V_{DD}	V

ELECTRICAL CHARACTERISTICS (Ta＝25°C, unless otherwise noted.)

Symbol	Parameter		Test conditions	Limits Min	Limits Typ	Limits Max	Unit
V_{ZD}	Zenor voltage		I_{ZD}＝2mA	7.4	8.2	9	V
			I_{ZD}＝10mA	7.5	8.2	9	V
I_{DD}	Supply current	M58479P	V_{DD}＝7.5V, C_{FC}＝0.01μF, R_{FC}＝1MΩ R_{ADJ}＝0Ω, Input/output open		0.25	1	mA
		M58482P	V_{DD}＝7.5V, C_{FC}＝0.01μF, R_{FC}＝1MΩ R_{ADJ}＝0Ω, Input/output open		25	100	μA
V_{RE}	Supply voltage at the time of automatic-reset release	M58479P		3.1		5.4	V
V_{TR}	Transition voltage of first inverter in the oscillator		V_{DD}＝7.5V, R_{ADJ}＝0Ω	2.9		4.8	V
R_I	Pull-up resistance: $\overline{RESET}$, $\overline{INH}$, D1, D2 inputs	M58479P		10	20	30	kΩ
		M58482P		25	50	75	kΩ
I_{OH}	High-level output current, OUT1 and OUT2 outputs		V_{DD}＝7.5V, V_O＝0V	5	10		mA
I_{OL}	Low-level output current, OUT1, OUT2, and OUT3 outputs		V_{DD}＝7.5V, V_O＝7.5V	10	20		mA
I_{OZH}	Off-state output current, OUT3 output		V_{DD}＝7.5V, V_O＝7.5V			1	μA
I_{OL}	Low-level output current: OUT1, OUT2, and OUT3 outputs		V_{DD}＝7.5V, V_O＝0.4V	1.6			mA
I_{OL}	Low-level output current: OUT1, OUT2, and OUT3 outputs	M58482P	V_{DD}＝4.5V, V_O＝0.4V	1.6			mA
V_{OL}	Low-level output voltage: OUT1, OUT2, and OUT3 outputs		V_{DD}＝7.5V			0.1	V

FUNCTIONAL DESCRIPTION

Voltage Regulator

A zenor diode is on-chip, making it easy to obtain a constant voltage regulator circuit. Since the zenor diode terminal (ZD) is independent of the power terminal (V_{DD}), it can be used as a constant voltage power supply for the total system.

Oscillator

Oscillation is obtained by connecting an external resistor (feedback resistor R_{FC}) between terminals OS1 and OS3 and an external capacitor (oscillation capacitor C_{FC}) between terminals OS1 and OS2. The values of the external resistor and capacitor can then be changed to vary the oscillation period and thus change the time delay. Oscillation period T_0 is obtained by the following equation:

$$T_0 = -R_{FC} \cdot C_{FC} \left\{ \ell n \frac{V_{TR}}{V_{DD}+V_{BE}} + \ell n \frac{V_{DD}-V_{TR}}{V_{DD}+V_{BE}} \right\} \cdots (1)$$

Where,

R_{FC} : Resistance of external resistor

C_{FC} : Capacitance of external capacitor

V_{TR} : Transition voltage of the first inverter in the oscillation circuit

V_{DD} : Supply voltage

V_{BE} : Forward rising voltage of the diode in terminal OS1 (0.3~0.7V)

Automatic-Reset Function

The M58479P has a power-supply voltage-detection circuit on-chip, so that the counter is automatically reset by the rising edge of the supply voltage when power is turned on. The reset is then released, making the oscillator ready to function and the counter ready to start counting.

The M58482P can also be provided with the same automatic-reset function by connecting capacitor between terminals $\overline{\text{RESET}}$ and V_{SS}.

Reset Function

When the $\overline{\text{RESET}}$ input turns low (V_{SS}), oscillation of the oscillator can be stopped and the counter reset.

Inhibit Function

When terminal $\overline{\text{INH}}$ turns low (V_{SS}) while the timer is in action, the oscillation halts. When input $\overline{\text{INH}}$ is turned high or returned to OPEN afterwards, it starts to count residual time.

Counter

This counter consists of an 11-stage 1/2 frequency divider, a 2-stage 1/10 frequency divider and a 1-stage 1/6 frequency divider. As shown in the table below, timer duration can be changed by varying the number of pulses counted according to the combination of the input levels on terminals D1 and D2.

D1	D2	Number of pulses counted	Time delay	Typical time delay applied
H	H	1024	T_1	1 min
L	H	1024 × 10	$T_1 \times 10$	10 min
H	L	1024 × 10 × 6	$T_1 \times 10 \times 6$	1h
L	L	1024 × 10 × 6 × 10	$T_1 \times 10 \times 6 \times 10$	10h

Where, $T_1 = T_0 \times 1024$

T_0 is the value obtained from equation (1)

Output Circuits

The chips have three outputs: OUT1 changes from low to high and OUT2 from high to low as soon as the time duration is up. Either can be used to drive a transistor by connecting it to the transistor base. OUT1 can drive a thyristor when connected to the thyristor gate.

OUT3 is an open-drain output with period 1/8 of the time delay, and can be used to drive a TTL in a separate (5V) power supply line. Thus, if a M53290P counter and a M53242P binary-to-decimal decoder are connected to OUT3, with their output connected to a light-emitting diode, residual time will be displayed on the LED. When not in use, OUT3 should be connected to V_{SS}.

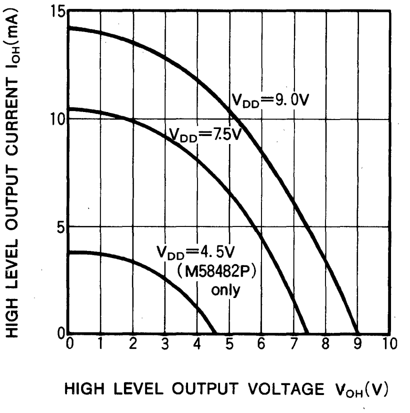
Fine Adjustment of Oscillation Period

A variable resistor can be connected between terminals ADJ and V_{SS}, enabling precise adjustment of the period of the oscillator. However, when not used for fine adjustment, ADJ should be connected to V_{SS}.

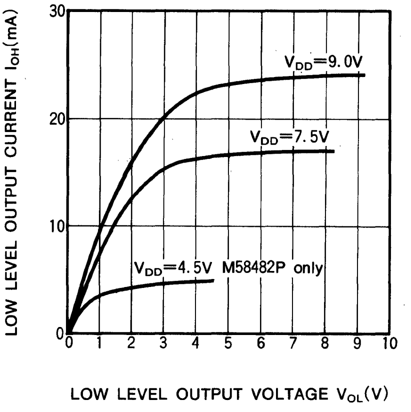
TYPICAL CHARACTERISTICS (T_a=+25℃, unless otherwise noted)

See "9. ELECTRICAL CHARACTERISTICS" for absolute values

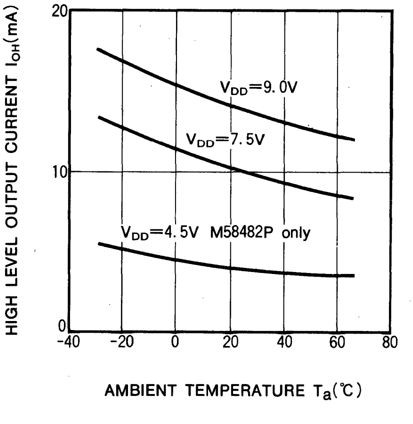
(1) $I_{OH}-V_{OH}$ (OUT 1, OUT 2)



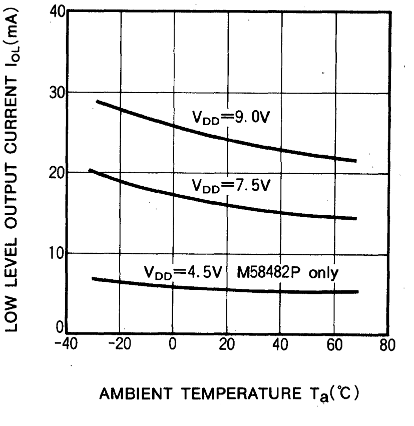
(2) $I_{OH}-V_{OL}$ (OUT 1, OUT 2, OUT 3)



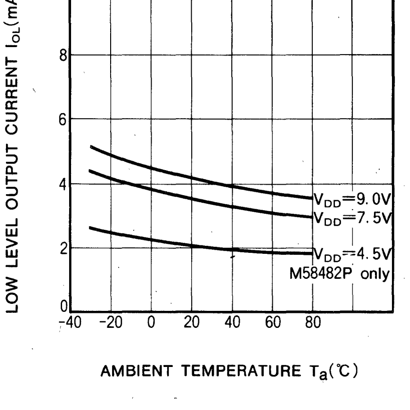
(3) $I_{OH}-T_a$ (OUT 1, OUT 2) V_{OH}=DV



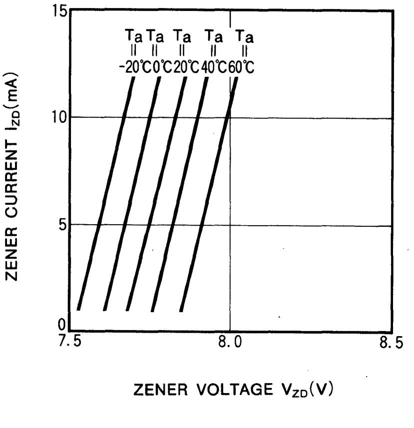
(4) $I_{OL}-T_a$ (OUT 1, OUT 2, OUT 3) $V_{OL}-V_{DD}$



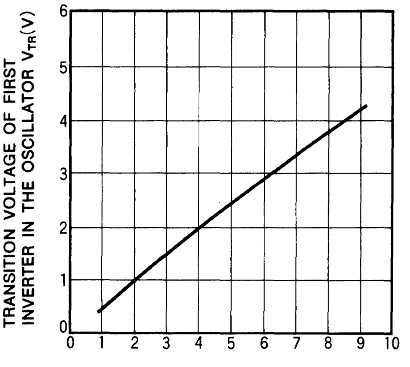
(5) $I_{OL}-T_a$(OUT 1, OUT 2, OUT 3) V_{OL}=0.4V



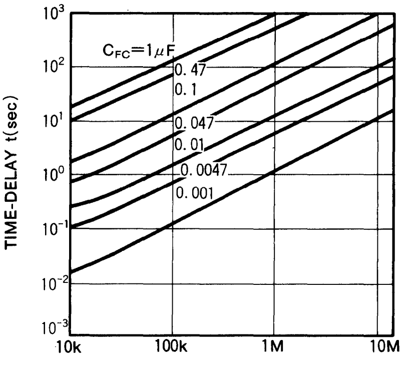
(6) I_{ZD} V_{ZD}



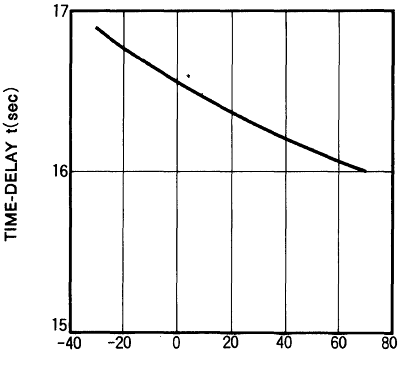
(7) $V_{TR}-V_{DD}$



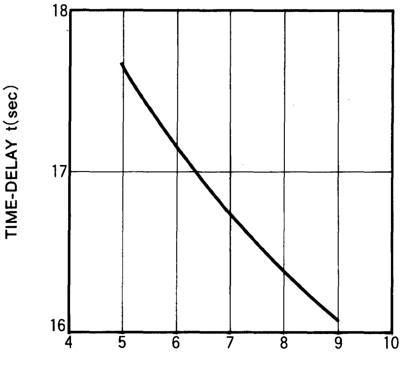
(8) $t=R_{FC}$
V_{DD}=7.5V, ADJ: SHORTED WITH V_{SS},
D1～D2: OPEN OR "H",
C_{FC}=0.001～1 μF



(9) t—Ta
V_{DD}=7.5V ADJ: SHORTED WITH V_{SS},
D1, D2: OPEN OR "H",
R_{FC}= 1 MΩ, C_{FC}=0.01μF



(10) t—V_{DD}
ADJ: SHORTED WITH V_{SS},
D1, D2:OPEN OR "H"
R_{FC}=1MΩ, C_{FC}=0.1μF



OSCILLATION FREQUENCY

The oscillation period of M58479P and M58482P are formularized as follows.

$$T_O = -R_{FC}C_{FC}\ \left\{\ell n\frac{V_{TR}}{V_{DD}+V_{BE}} + \ell n\frac{V_{DD}-V_{TR}}{V_{DD}+V_{BE}}\right\} \quad (1)$$

The value in { } of (1) takes the maximum value at $V_{TR}=V_{DD}/2$. For example, under the condition of $V_{DD}=7.5V$, the relation of the V_{TR} and the value in { } is shown in Figure 1 .

Regarding the Figure 1 , the value in { } of (1) at $V_{DD}=7.5V$ is, in a range of $V_{BE}=0.3\ell\sim0.7V$ and $V_{TR}=2.9\sim4.8V$, −1.647, −1.464.

The oscillation period can be figured out theoretically by the (1) formula; however, as 'the oscillation is executed by the charge and discharge of R_{FC}, C_{FC}, the correction parameter R_{FC} by the output impedence of OS 2 and OS 3 is added in the (1) formula as:

$$T_O = -(R_{FC}+\Delta R_{FC})C_{FC}\ \left\{\ell n\frac{V_{TR}}{V_{DD}+V_{BE}} + \ell n\frac{V_{DD}-V_{TR}}{V_{DD}+V_{BE}}\right\} \quad (2)$$

At this time, the value of the correction parameter ΔR_{FC} will be around $5.5\pm2.5k\Omega$.

For the circuit designing, set the oscillation constant regarding to the above matters.

TIMER ADJUSTMENT

Following is the method of adjusting time-delay keeping the external resistance R_{FC} and capacitor C_{FC} fixed.

(1) The method to verify R_{ADJ} value with inserting the parallelly connected R_{ADJ} and C_{ADJ} into ADJ-VSS

As described already, the oscillation period To is calculated with (1) formula, as the relation of V_{TR} and the minimum value when $V_{TR}=V_{DD}/2$. This means the To can be varied by changing the V_{TR} value. This method is performed by adjusting the time-delay by the V_{TR}.

The ADJ is connected to a N-Channel-FET source of the first inverter of oscillator as Figure 3 illustrates. When the parallelly connected resistance R_{ADJ} and capacitance C_{ADJ} are inserted between ADJ and V_{SS} and the R_{ADJ} changes its value, the voltage of the ADJ varies by the current in the R_{ADJ}, and this results the change of V_{TR}.

As the R_{ADJ} value gets larger, the value of the V_{TR} is increased from that at $R_{ADJ}=0\Omega$. The value of V_{TR} at $R_{ADJ}=0\Omega$ is in the range of $2.9\sim4.8V$ ($V_{DD}=7.5V$). Therefore, as Figure 2 indicates, the variation way and the variation rate of the oscillation period To when the resistance R_{ADJ} gets larger are found according to the V_{TR} value at $R_{ADJ}=0\Omega$ and are not constant.

The capacitance C_{ADJ} to be parallelly inserted into the resistance R_{ADJ} has a function of making a variation rate of the To toward R_{ADJ} large.

On the resistance R_{ADJ} and the capacitance C_{ADJ}, please follow the ranges below.

$R_{ADJ}=0\sim100k\Omega$

$C_{ADJ}=100\sim1000pF$

When the ADJ is not used for the oscillation period adjustment, short to the V_{SS}.

TRANSITION VOLTAGE OF FIRST INVERTER IN THE OSCILLATOR

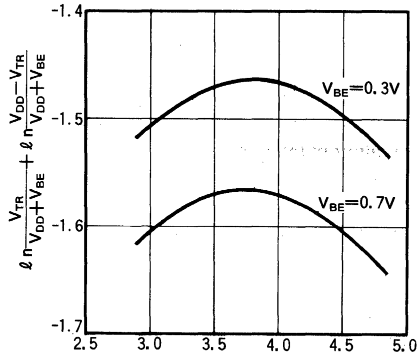


Fig. 1. V_{TR} VS $\ell n\frac{V_{TR}}{V_{DD}+V_{BE}} + \ell n\frac{V_{DD}-V_{TR}}{V_{DD}+V_{BE}}$

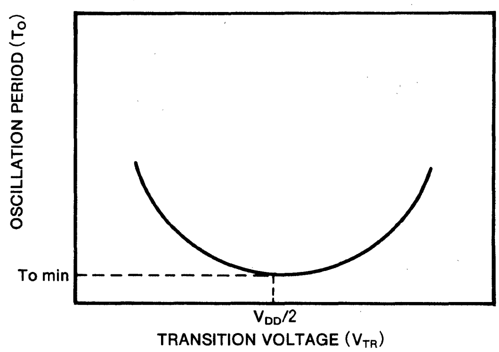


Fig. 2. Oscillation period (T_O) VS Transition Voltage (V_{TR})

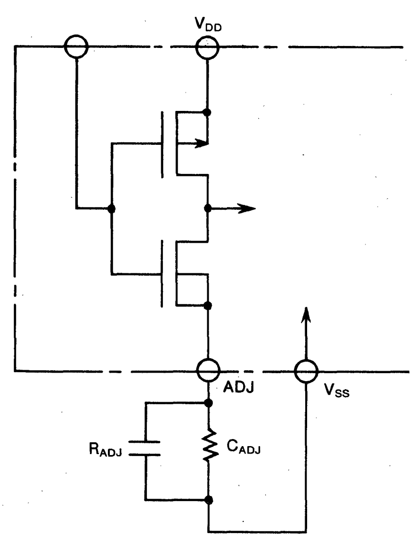


Fig.3 External connection diagram of oscillation frequency adjustment method (1)

(2) The method to verify resistance R_B value with inserting the resistance R_B and capacitance C_B connected in series between OS 1 and OS 2.

The oscillation period To is found by the same method as the (1) formula in principle, but a little more complicated.

In principle, the variation way, and the variation rate of the oscillation period To with the resistance R_B are constant, and not be different by process parameter (V_{TR} etc).

Figure 4 illustrates the external connection diagram of resistances R_{FC}, R_B and capacitance C_{FC}, C_B. In addition, the Figure 5 shows the relation of the time-delay T ($=T_O$ x 1024) with R_B at $C_{FC}=C_B$, $R_{FC}=1\ M\Omega$, and the time-delay variation rate ΔT at $R_B=250k\Omega$. As shown in Figure 6, the To takes the maximum value near $R_B=250k\Omega$ according to $C_{FC}=C_B=10^3$, 10^4, 10^5pF.

The change of the time-delay T with the resistance R_{FC} keeping the R_B constant will take poor linearity as the value of R_B increases. Therefore, try to keep the resistance R_B in a range of $0 \sim 150k\Omega$.

For that, take the $R_B=50k\Omega$ first and change its value in the range of $0 \sim 150k\Omega$ to adjust the time-delay at the maximum value of R_{FC}, so the adjustment of $\pm 7\%$ becomes possible.

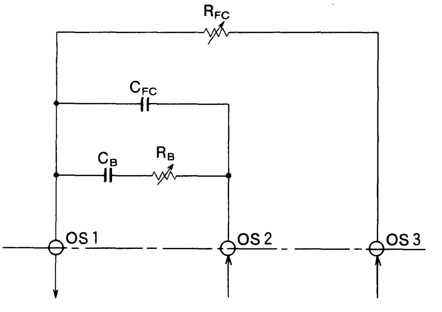


Fig. 4. External connection diagram of oscillation frequency adjustment method (2)

Fig. 5. (a) R_B—T (Method 2)
$C_{FC}=C_B=10^3$pF
$R_{FC}=1M\Omega$
ADJ is shorted with V_{SS}

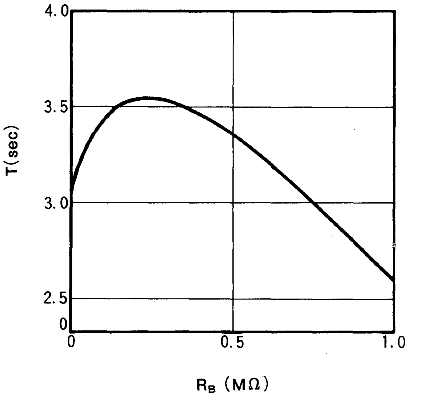


Fig. 5. (b) R_B—T (Method 2)
$C_{FC}=C_B=10^4$pF
$R_{FC}=1\ M\Omega$
ADJ is shorted with V_{SS}

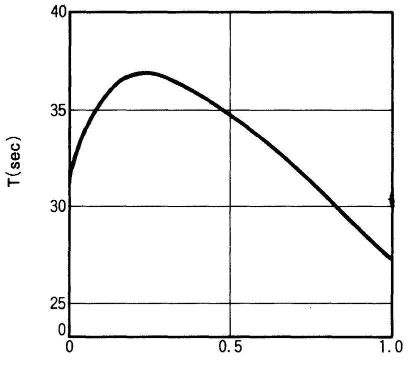


Fig. 5. (c) R_B—T (Method 2)
$O_{FC}=C_H=10^5$pF
$R_{FC}=1M\Omega$
ADJ is shorted with V_{SS}

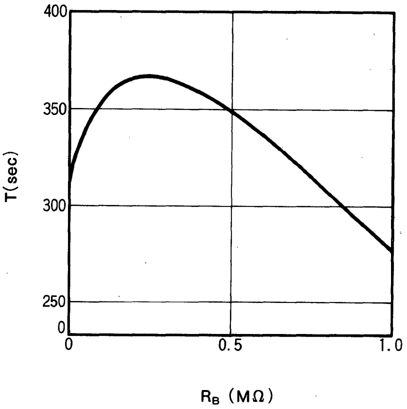
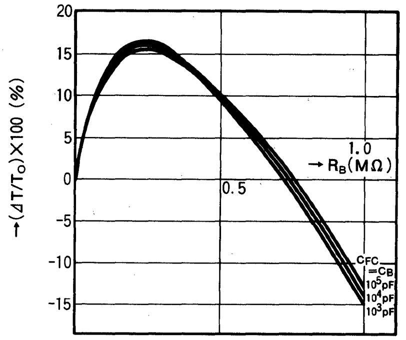


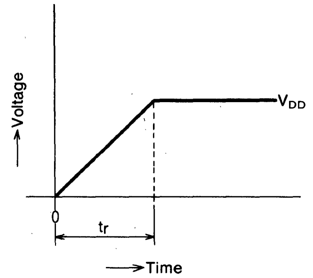
Fig. 6. R_B—($\Delta T/T_O$)×100(Method 2)
$R_{FC}=1M\Omega$
$\Delta T=T-T_O$
$T_O=T(Rb-0\Omega)$



POWER-ON FUNCTION

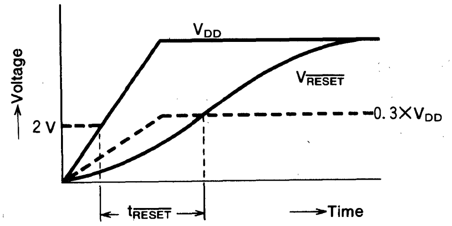
(1) M58479P

The power-on reset function will start when the power is on since the M58479P builts the supply voltage detection circuit in it; however, it is necessary to keep the rising time of power (tr) more than 1 ms as shown below.

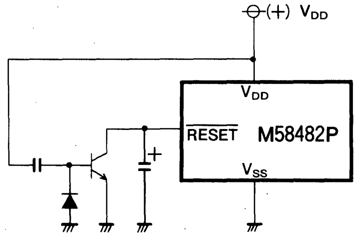


(2) M58482P

The power-on reset function will start by inserting the capacitance between the $\overline{\text{RESET}}$ and V_{SS} when the power is on as same as the M58479P. In order to have an accurate performance on the power-on reset function, keep $t_{\overline{RESET}}$ over 1msec on the condition of $V_{\overline{RESET}} \leqq 0.3 \times V_{DD}$ when V_{DD} is over 2 V, as illustrated below.

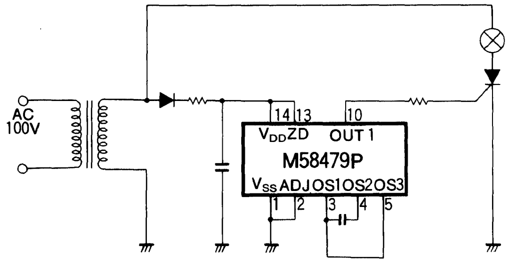


In case the power is on again after it is off and the voltage of $\overline{\text{RESET}}$ $V_{\overline{RESET}}$ is not perfectly down, the $t_{\overline{RESET}}$ must be also kept in over 1msec, which was mentioned in the above diagram. When the prescribed condition is not satisfied, add the circuit illustrated below to the $\overline{\text{RESET}}$and make the power-on reset function accurately. In this case, make sure to select an external capacitance to satisfy the $V_{\overline{RESET}} \geqq$ 1 msec.

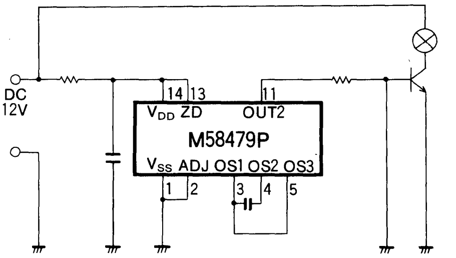


APPLICATION CIRCUITS

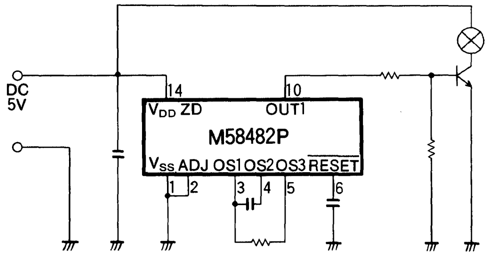
(1) Use of AC supply



(2) Use of DC supply



(3) Use of DC supply (low supply voltage)

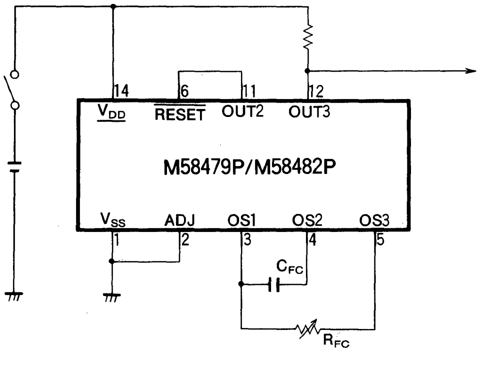


Both M58479P and M58483P build zenor diodes in them so that they can adopt AC supply (100V), DC supply (12V) according to external circuits.

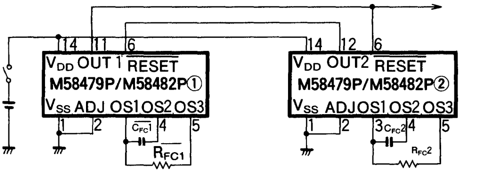
If the supply voltage is relatively high, when a power-on reset is required without an external circuit, employ the M58479P.

On the other hand, if a low supply voltage or low power dissipation is required, or if a power supply with a heavy fluctuation on lower voltage is used, employ the M58482P (M58479P may have a reset when V_{DD} is below 5. 4V).

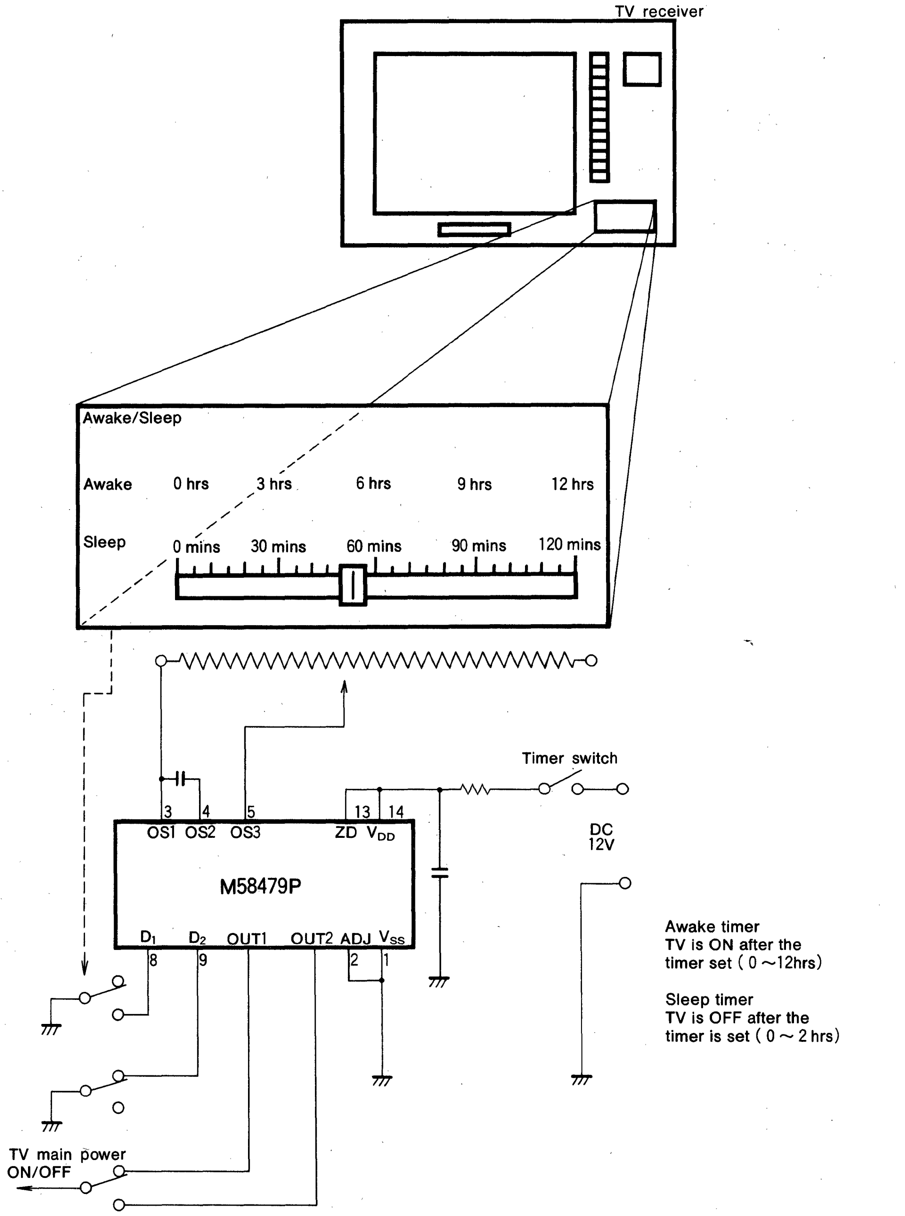
(4) While power is being on,
A pulse of 50% duty of which period is defined by R_{FC} and C_{FC}, is output from OUT 3 .



(5) While power is being on,
a (duty changeable) pulse of which a "L" period is defined by R_{FC1}, C_{FC1}, and a "H" period is by R_{FC2}, C_{FC2}, is output from OUT 1 of M58479P/M58482P①.



(6) An example of awake/sleep timer



Only one M58479P/M58482P is needed to have one switchover for awake/sleep timer

The application above is just a one example and the M58479P/M58482P can be widely used for home entertainment and industry.

(8) Circuit to display a timer in process