M58992P

CMOS CRT CONTROLLER

DESCRIPTION

The M58992P is a raster scan type CRT interface device, fabricated using silicon gate CMOS technology. This LSI is a one-chip type high-performance video display generator having the timing signal generator and attribute circuits required for CRT display so as to allow system configuration with a small number of components.

FEATURES

- Single 5V supply voltage.
- Can generate video display using simple external circuit
- 10 programmable display modes
- Some mode conditionally allows mixed use with other mode.
- Color display is programmable to use either 8 or 16 colors.
- The R, G and B signals are provided as video output signals.
- Can superimpose on TV screen
- A 16K or 64K DRAM is used as the video RAM under control of the built-in DRAM controller.
- The video RAM area can be used concurrently for storage of display data and microprocessor program.
- Paging and scrolling are possible.
- Cursor control; blinking, blanking, underline and reverse characters are possible.
- Light pen input control function is provided.
- Various interrupts generating function is provided.

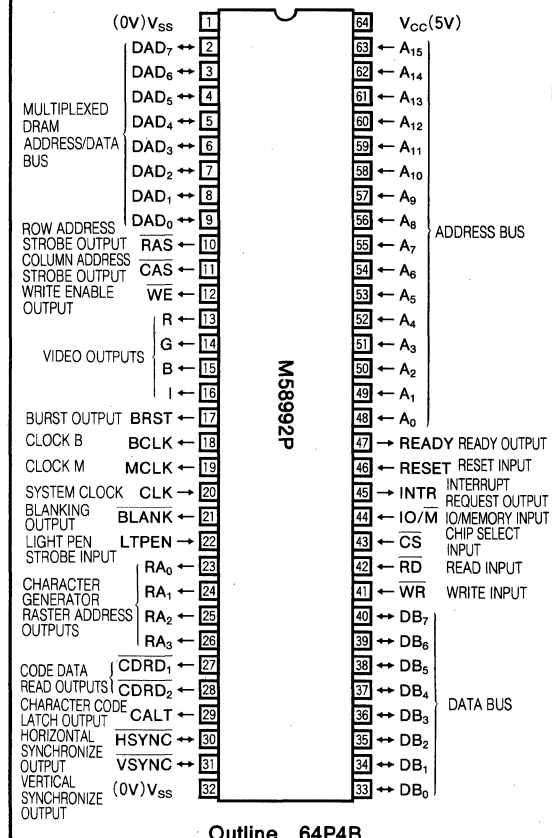
APPLICATION

Display unit using home TV set or monitor TV set

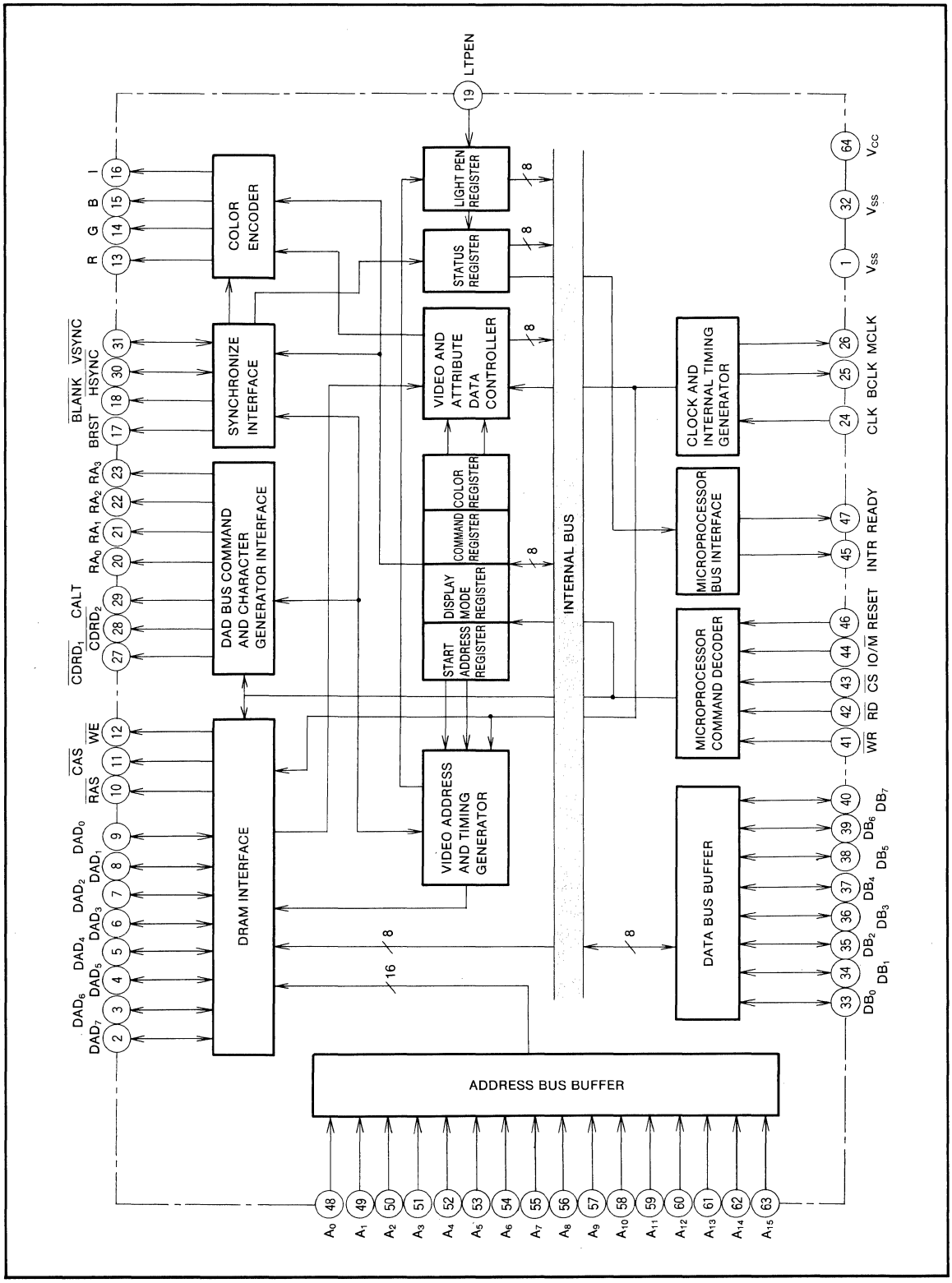
FUNCTION

The information or data to be displayed on the screen is written in the video RAM by the microprocessor. The M58992P can read the video RAM in the order of the CRT scan, and can generate synchronization signal for a CRT.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B


LTPEN
LIGHT PEN REGISTER
STATUS REGISTER
VIDEO AND ATTRIBUTE DATA CONTROLLER
COLOR REGISTER
COMMAND REGISTER
DISPLAY MODE REGISTER
START ADDRESS REGISTER
INTERNAL BUS
COLOR ENCODER
SYNCHRONIZE INTERFACE
DAD BUS COMMAND AND CHARACTER GENERATOR INTERFACE
DRAM INTERFACE
VIDEO ADDRESS AND TIMING GENERATOR
CLOCK AND INTERNAL TIMING GENERATOR
MICROPROCESSOR BUS INTERFACE
MICROPROCESSOR COMMAND DECODER
DATA BUS BUFFER
ADDRESS BUS BUFFER
R G B I
BLANK VSYNC
BRST HSYNC
CDRD1 CALT
CDRD2
RA0 RA1 RA2 RA3
DAD0 DAD1 DAD2 DAD3 DAD4 DAD5 DAD6 DAD7
RAS CAS WE
CLK BCLK MCLK
INTR READY
WR RD CS IO/M RESET
DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
Vss Vss Vcc

5

PIN DESCRIPTION

Pin	Name	Input/output	Functions
DAD_7~ DAD_0	Multiplexed DRAM address /data bus	Input/output	Causes data input from DRAM or data output for writing in DRAM by output of mltiplexed row and column address to DRAM.
$\overline{RAS}$	Row address strobe output	Output	DRAM address input is latched at falling edge of $\overline{RAS}$.
$\overline{CAS}$	Column address strobe output	Output	DRAM address input is latched at falling edge of $\overline{CAS}$.
$\overline{WE}$	Write enable output	Output	Data from microprocessor is written in DRAM when this signal is "L".
R	Video output R	Output	TTL level output of video signals R, G and B.
G	Video output G		
B	Video output B		
I	Video output luminance		Auxiliary output for R, G and B. By external Combination with R, G and B, up to 16 colors can be displayed. I = "H" indicates high luminance.
BRST	Burst output	Output	Signal to indicate color burst signal position or sub-carrier frequency phase-modulated by RGB in case of NTSC system.
BCLK	Clock B	Output	Frequency at 1/4 of clock input. Subcarrier frequency in NTSC color system.
MCLK	Clock M	Output	Internal timing clock. Indicates DRAM access by the M58992P for display when this signal is "L" in the text 1, text 2, graphic 1, graphic 2, graphic 3 or graphic 5 mode.
CLK	System clock	Input	14.31818MHz for display using NTSC system.
$\overline{BLANK}$	Blanking output	Output	Indicates around the synchronizing pulse in horizontal or vertical blanking period of the M58992P.
LTPEN	Light pen strobe input	Input	Signal to latch internal address value.
RA_3~ RA_0	Character generator raster address outputs	Output	Least significant 4 bits of address for use of character generater to be used in text mode.
$\overline{CDRD1}$ $\overline{CDRD2}$	Code data read outputs	Output	Signal to control external circuit for input of display code pattern to the M58992P. $\overline{CDRD1}$ is the timing for direct data input from DRAM to the M58992P, and $\overline{CDRD2}$ is the timing for input from character generator.
CALT	Character code latch output	Output	Signal to cause external latching of character generator pointer output from DRAM.
$\overline{HSYNC}$	Horizontal synchronize output	Open drain output	Setting synchronizing signal input mode by command causes no generation of internal synchronizing signal but internal counter reset by external signal.
$\overline{VSYNC}$	Vertical synchronize output		

PIN DESCRIPTION (CONTINUED)

<table>
<tr><th>Pin</th><th>Name</th><th>Input/output</th><th>Functions</th></tr>
<tr><td>$DB_7 \sim DB_0$</td><td>Data bus</td><td>Input/output</td><td>Data bus DB_7 : MSB</td></tr>
<tr><td>$\overline{WR}$</td><td>Write input</td><td>Input</td><td rowspan="4">
<table>
<tr><th>Function</th><th>$\overline{CS}$</th><th>IO/$\overline{M}$</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th></tr>
<tr><td>No LSI selection</td><td>1</td><td>—</td><td>—</td><td>—</td></tr>
<tr><td>DRAM Read</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>DRAM Write</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>The M58992P register read</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>The M58992P register write</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table>
The M58992P starts DRAM access or internal register read/write upon $\overline{CS}$.</td></tr>
<tr><td>$\overline{RD}$</td><td>Read input</td><td>Input</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip select input</td><td>Input</td></tr>
<tr><td>IO/$\overline{M}$</td><td>IO/memory input</td><td>Input</td></tr>
<tr><td>INTR</td><td>Interrupt request output</td><td>Output</td><td>Interrupt request output generated for any of four reasons in the M58992P can be masked. The status register detects the type of interrupt. The INTR signal is reset upon status read.</td></tr>
<tr><td>RESET</td><td>Reset input</td><td>Input</td><td>The M58992P system reset signal to initialize various registers.</td></tr>
<tr><td>READY</td><td>Ready output</td><td>Output</td><td>Normally "H" signal. Goes to "L" upon selection of DRAM and returns to "H" upon completion of DRAM read/write. This signal provides synchronism with the microprocessor.</td></tr>
<tr><td>$A_{15} \sim A_0$</td><td>Address bus</td><td>Input</td><td>Address input on the microprocessor side.
A_{15} is the MSB. A_0 to A_3 are used for register reading or writing.</td></tr>
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5

Table 1 The M58992P display mode list

Mode	Screen format (60Hz specification)	Character or dot composition	Color designation	Programming method				VRAM capacity (in bytes) (60Hz specification)	Cursor and blinking	VRAM access from microprocessor	Screen format (50Hz specification)	VRAM capacity (in bytes) (50Hz specification)
				VRAM	CLRG1	CLRG2	CLRG3					
Text 1	40 characters ×25 lines	8×8 dots	FG : 16 colors BG : 8 colors BD : 16 colors	16 bits/character (8 bits for character and 8 bits for color designation)	Border color designation, etc.	Unused	Unused	2000	Cursor allowed. Multiple blinking positions may be disignated in character units.	Always possible without flickering.	40 characters ×30 lines	2400
Text 2	40 characters ×20 lines	8×10 dots						1600			40 characters ×24 lines	1920
Text 3	80 characters ×25 lines	8×8 dots						4000		Always possible. Flickering is caused at other than blinking.	80 characters ×30 lines	4800
Text 4	80 characters ×20 lines	8×10 dots						3200			80 characters ×24 lines	3840
Graphic 1	160H ×100V	1 block : 2×2 dots	FG : 16 colors BD : 16 colors	4 bits/dot	Border color, etc.	MSB 4 bits, BG color	Unused	8000	No	Always Possible without flickering.	160H ×120V	9600
Graphic 2	160H ×200V	1 block : 2×1 dots						16000			160H ×240V	19200
Graphic 3	320H ×200V	1 block : 1×1 dot	FG : Semi 16 colors BD : 16 colors	2 bits/dot		Color pallet for FG		16000			320H ×240V	19200
Graphic 4	320H ×200V	1 block : 1×1 dot	FG : 16 colors BD : 16 colors	4 bits/dot		MSB 4 bits, BG color	Unused	32000		Same as text 3 and 4 modes	320H ×240V	38400
Graphic 5	640H ×200V	1 block : 1×1 dot	FG : One seleted color BD : 16 colors	1 bits/dot		BG and FG color designation		16000		Same as text 1 and 2 modes	640H ×240V	19200
Graphic 6	640H ×200V	1 block : 1×1 dot	Same as graphic 3	2 bits/dot		Color pallet for FG		32000		Same as text 3 and 4 modes	640H ×240V	38400

FG=Foreground BG=Background BD=Border CLRG1~3=Color register