

REJ03F0032-0100Z Rev.1.0 Sep.16.2003

# Description

The M59330P is an integrated circuit for two-line LAN transceivers, conforming to J1850 specifications.

The chip incorporates bus line anomaly detection functions; anomalous behavior causes the ERR signal to go to "L". A selector causes a normal bus signal to be output to  $R_x$ .

By setting the standby signal to "L", a low consumption current state is maintained. At this time, the drivers BUS (+) and BUS (-) are both turned off.

In standby mode, on input of "H" level to the ERR pin, error output reset occurs.

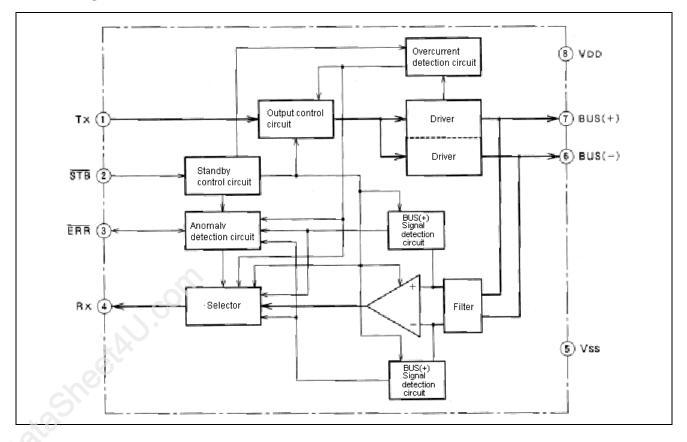
## Features

- Conforms to SAE J1850 specifications
- Internal bus line anomaly detection function

# Applications

• LAN transceiver for automotive use, generic LAN transceiver, transceiver for other communication applications

## **Block Diagram**





# **Pin Configuration (Top View)**

Datainput Standby input Erroor I/O Deta input	Tx 1 STB 2 ERR 3 Rx 4	M59330P	7 BUS(+)) 6 BUS(-))	Power supply Bus line I/O GND
	P	ackage <b>8</b>	P4	

# **Explanation of Functions**

# Pin Deiscription

Pin no.	Pin name	I/O	Function
1	Тх	I	Data signal input pin
2	STB	I	Standby signal input pin; L: standby mode, H: normal operation
3	ERR	I/O	Error signal output pin and error reset input pin; on detection of anomaly in transmission channel, outputs "L" level; in standby mode, error reset on input of "H" level
4	Rx	0	Pin for output of signal from transmission channel
5	Vss	I	Clamping pin
6	Bus(–)	I/O	Pin for signal output to transmission channel and for input of signal from transmission channel (negative logic)
7	Bus(+)	I/O	Pin for signal output to transmission channel and for input of signal from transmission channel (positive logic)
8	V <sub>DD</sub>	I	Power supply pin

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#### **Transmission Channel Anomaly Detection and Communication Functions**

The M59330P uses driver overcurrent detection functions and transmission signal logic error detection functions to detect anomalies in the transmission channel, and outputs an error signal (ERR (pin 3) = "L") accordingly. Also, by switching the signal output to pin  $R_X$  (pin 4) according to the anomalous state, communication is possible after anomaly occurrence.

### (1) Overcurrent detection

The drivers of the BUS(+) pin (pin 7) and BUS(-) pin (pin 6) of the M59330P are provided with overcurrent detection circuits. When excessive current flows in a driver, the driver is turned off, and an error signal (ERR (pin 3) = "L") is output. When overcurrent is detected, the driver is maintained in the off state until error reset.

The drivers for the BUS(+) pin (pin 7) and the BUS(-) pin (pin 6) are independent; depending on the circumstances of the anomaly, both may be turned off.

A filter is incorporated to prevent erroneous operation due to transient currents when a driver is turned on, and an overcurrent state is not detected for a short period of time (several hundred ns). The detection current is set at approx. 180 mA.

#### (2) Logical anomaly detection

M59330P transmission signals operate at opposite phases, and by comparing the signals, anomalies in the transmission channel are detected. The signals are compared at a preset time relative to an edge of the signals of the transmission channels (BUS(+), BUS(-)), and if they do not coincide, it is assumed that an anomaly has occurred in one of the transmission channels, and an error signal (ERR (pin 3) ="L") is output. When the next edge is detected within the preset time, this edge is taken as a new reference for timing, and if noncoincidence continues for longer than the preset time, an anomaly is detected. The time is set to approx. 4.2  $\mu$ s.

Logical anomaly detection does not support multiple error modes.

When only a logical anomaly is detected, the driver is not turned off. A driver is turned off upon anomaly detection only when overcurrent is detected.



### **(3)** Communication functions

The M59330P normally outputs differential signals on BUS (+) (pin 7) and BUS (-) (pin 6), but when an anomaly is detected, switches signal output to the  $R_x$  pin (pin 4) according to the anomaly state.

When overcurrent is detected, an anomaly with the driver or transmission channel for which the overcurrent was detected is assumed, and an error signal is output; at the same time, the signal for the other transmission channel is output to the  $R_X$  output (pin 4). As explained in (1) above, in some cases both drivers may be turned off; in such cases, the  $R_X$  output (pin 4) is fixed at "L".

When a logical anomaly is detected, an error signal (ERR (pin 3) = "L") is output, and at the same time the  $R_X$  output (pin 4) is driven to "L". After error signal output, a transmission channel for which a transmission signal edge is detected is regarded as normal, and the signal for the channel is output to the  $R_X$  output (pin 4).

Overcurrent detection takes precedence over logical anomaly detection in operations to switch the error signal output and  $R_x$  output.

_	Anomaly mode		Error output	Communication after anomaly detection	Method of anomaly detection
1	Bus(+)	GND short	Y	Y	(2)
2	-	VDD short	Y	Y	(1), (2)
3	_	Open	Y	Y	(2)
4	Bus(–)	GND short	Y	Y	(1), (2)
5	-	VDD short	Y	Y	(2)
6	_	Open	Y	Y	(2)
6	BUS(+), BUS(–) short		Y	Ν	(1)

#### Table 1. Anomaly modes and anomaly detection functions

### **Error Reset**

After standby mode is entered (the STB pin (pin 2) ="L"), the M59330P error output is reset by inputting level "H" to the ERR pin (pin 3). In this case, all operations relating to anomaly detection, such as overcurrent detection and  $R_X$  output switching, are canceled.

### Standby Mode

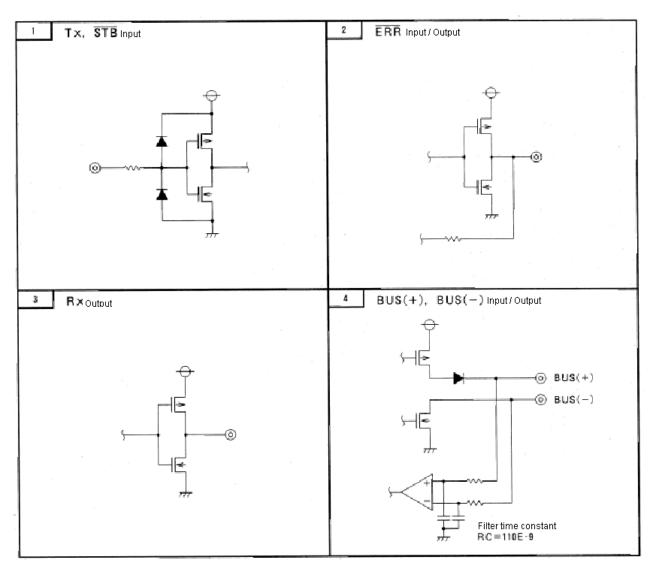
By driving the STB pin (pin 2) to "L" level, the M59330P can be put into a low consumption current mode.

In standby mode, the driver and overcurrent detection functions do not operate, but the logical anomaly detection function continues to operate, and except for overcurrent detection, detection of anomalies is possible. However, there is only error signal output, and  $R_x$  output signal switching is not performed.

In standby mode, the  $R_X$  output is the logical sum of the BUS(+) signal and the BUS(-) signal.



# **Input/Output Equivalent Circuits**





# **Electrical Characteristics**

Symbol	Quantity	Conditions	Rate	1	Unit	
			Min.	Тур.	Max.	_
I <sub>DD</sub> 1	Power supply current 1	RBUS = 105 Ω, Tx = "L", STB = "H"			5.0	mA
I <sub>DD</sub> 2	Power supply current 2	RBUS = 105 Ω, Tx = "H", STB = "H"			55	mA
I <sub>DD</sub> 3	Power supply current 3	RBUS = 105 Ω, Tx = STB = "H"			200	μA
V <sub>TH1</sub>	"H" input threshold voltage 1	ERR	2.2		3.2	V
V <sub>TH2</sub>	"H" input threshold voltage 2	Tx, STB	2.3		3.5	V
VTL	"L" input threshold voltage	Tx, STB	1.6		2.8	V
VHYSL	Hysteresis width	Tx, STB	0.4		1.0	V
V <sub>CIN</sub>	BUS input voltage range	BUS(+), BUS(-)	Vss		V <sub>DD</sub> -2.0	V
VHYS8	Input hysteresis width	BUS(+), BUS(-) differential input	70		300	mV
I <sub>IPP1</sub>	BUS(+) leakage current 1	with power supply off ( $V_{DD} = 0V$ ), BUS(+) = 0V			100	μA
I <sub>IPP1</sub>	BUS(+) leakage current 2	with power supply off ( $V_{DD} = 0V$ ), BUS(+) = 5V			100	μA
I <sub>IPP2</sub>	BUS(+) leakage current 3	with power supply onBUS(-) = 5V	-20			μA
I <sub>IDP2</sub>	BUS(+) leakage current 4	with power supply onBUS(–) = 0V			100	μA
I <sub>IPM1</sub>	BUS(-) leakage current 1	with power supply off–50mA			100	μA
I <sub>IDM1</sub>	BUS(-) leakage current 2	with power supply off+50mA			100	μA
I <sub>IPM2</sub>	BUS(-) leakage current 3	with power supply on			20	μA
V <sub>IDM2</sub>	BUS(-) leakage current 4	with power supply on			100	μA
V <sub>DROP1</sub>	Driver drop voltage	IBUS(+) = -50mA			1.0	V
V <sub>DROP2</sub>		IBUS(-) = +50mA			0.6	
V <sub>OH1</sub>	"H" output voltage 1	$R_X pin I_{OH} = -1mA$	4.5		5.0	V
V <sub>OL1</sub>	"L" output voltage 1	$R_X pin I_{OL} = +1mA$			0.6	V
V <sub>OH2</sub>	"H" output voltage 2	ERR pin I <sub>OH</sub> = –1mA	4.5		5.0	V
IPD	ERR pull-down current	ERR pin V <sub>OH</sub> = 3.0V		350	700	μΑ
C <sub>I1</sub>	Input capacitance 1	power supply OFF ( $V_{DD} = 0V$ )			150	pF
C <sub>I2</sub>	Input capacitance 2	power supply ON			150	pF
VTH1	Ground offset voltage	across two nodes			1.0	V

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# **Absolute Maximum Ratings**

Symbol	Quantity	Conditions	Rated	Unit		
			Min.	Тур.	Max.	_
V <sub>DD</sub>	Power supply voltage		-0.3		6.5	V
V <sub>1</sub>	Input voltage		-0.3		V <sub>DD</sub> +0.3	V
V <sub>0</sub>	Output voltage		-0.3		V <sub>DD</sub> +0.3	V
lo	Driver output current	BUS(+)			50	mA
		BUS(-)	-50			
P <sub>mex</sub>	Allowable power consumption				200	mW
T <sub>stg</sub>	Storage temperature		-50		125	°C

Note: All voltages use the circuit V<sub>SS</sub> pin as reference; maximum and minimum values are absolute values; and currents are positive when flowing into a circuit, and negative (preceded by a minus sign) when flowing outward.

# **Recommended Operating Conditions**

	Quantity	(	unless othe	40 to 85°C)			
Symbol		Conditions	Rated	Rated value			
			Min.	Тур.	Max.	-	
V <sub>DD</sub>	Power supply voltage		4.75		5.25	V	
RBUS	BUS resistance	transmission rate = 41.6Kbps	105			Ω	
		transmission rate = 125Kbps	105			_	
CBUS	BUS capacitance	transmission rate = 41.6Kbps RBUS = 378 $\Omega$			10000	pF	
		transmission rate = 125Kbps, RBUS = 378 $\Omega$			3000	_	
Topr	Operating ambient temperature		-40		85	°C	

# **Timing Characteristics**

(unless otherwise noted,  $Ta = 25^{\circ}C$ ,  $V_{DD}=5.0$  V, during normal operation)

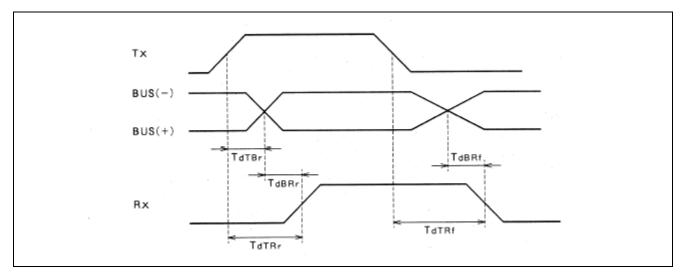
Symbol	Quantity	Conditions	Rated	Unit		
			Min.	Тур.	Max.	-
$T_{dTBr}$	$T_X \rightarrow BUS$ output delay time	CBUS = 10000pF,		0.25		μs
		RBUS = 378 Ω				
		transmission rate =41.6Kbps				
T <sub>dTRr</sub>	$T_X \rightarrow R_X$ rise delay time	CBUS = 10000pF,		0.6		μs
		RBUS = 378 Ω				
		transmission rate =41.6Kbps				
$T_{dBRf}$	$T_X \rightarrow R_X$ fall delay time	CBUS = 10000pF,		3.0		μs
		RBUS = 378 Ω				
		transmission rate =41.6Kbps				
$T_{dBRr}$	$BUS \rightarrow R_X$ rise delay time	transmission rate = 41.6Kbps		0.35		μs
$T_{dBRf}$	$BUS \to R_X$ fall delay time	transmission rate = 41.6Kbps		0.33		μs
TwS	Minimum STB input pulse width	standby mode	3.0			μs
TsS	STB input setup time	on error reset	1.0			μs
ThS	STB input hold time	on error reset	100			ns
TwE	ERR input pulse width	on error reset	200			ns



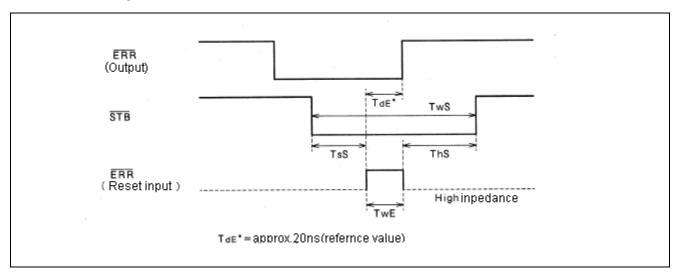
## M59330P

# **Timing Charts**

**Timing Waveforms** 



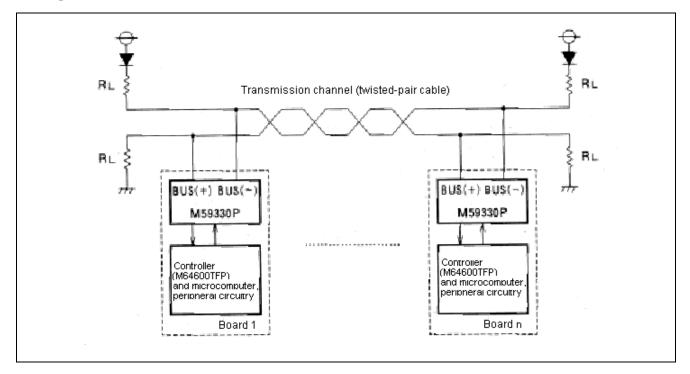
### **Error Reset Timing**



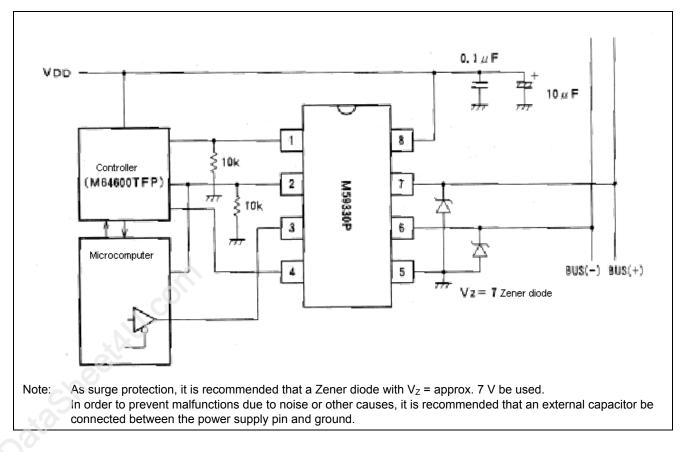


# **Application Circuit Example (One implementation example, which should be studied carefully)**



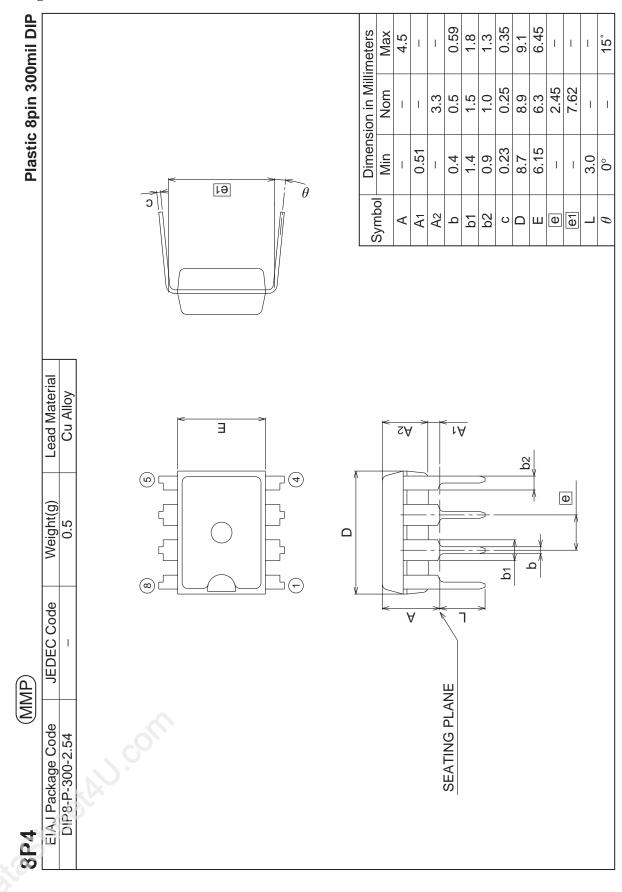


### **Peripheral Circuit Example**





**Package Dimensions** 





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