M5L8257P-5

PROGRAMMABLE DMA CONTROLLER

DESCRIPTION

The M5L8257P-5 is a programmable, 4-channel direct memory access (DMA) controller. It is produced using the N-channel silicon-gate ED-MOS process and is specifically designed to simplify data transfer at high speeds for microcomputer systems.

The LSI operates on a single 5V power supply.

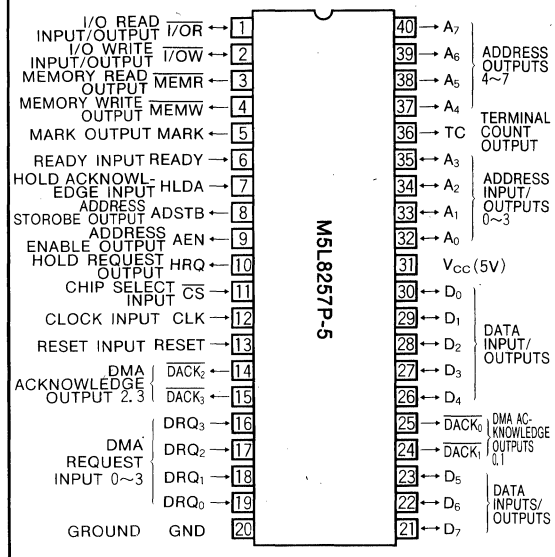
FEATURES

- Single 5V supply voltage
- Single TTL compatible
- Priority DMA request logic
- Channel-masking function
- Terminal count and Modulo 128 outputs
- 4-channel DMA controller
- Compatible with MELPS85 devices

APPLICATION

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

PIN CONFIGURATION (TOP VIEW)

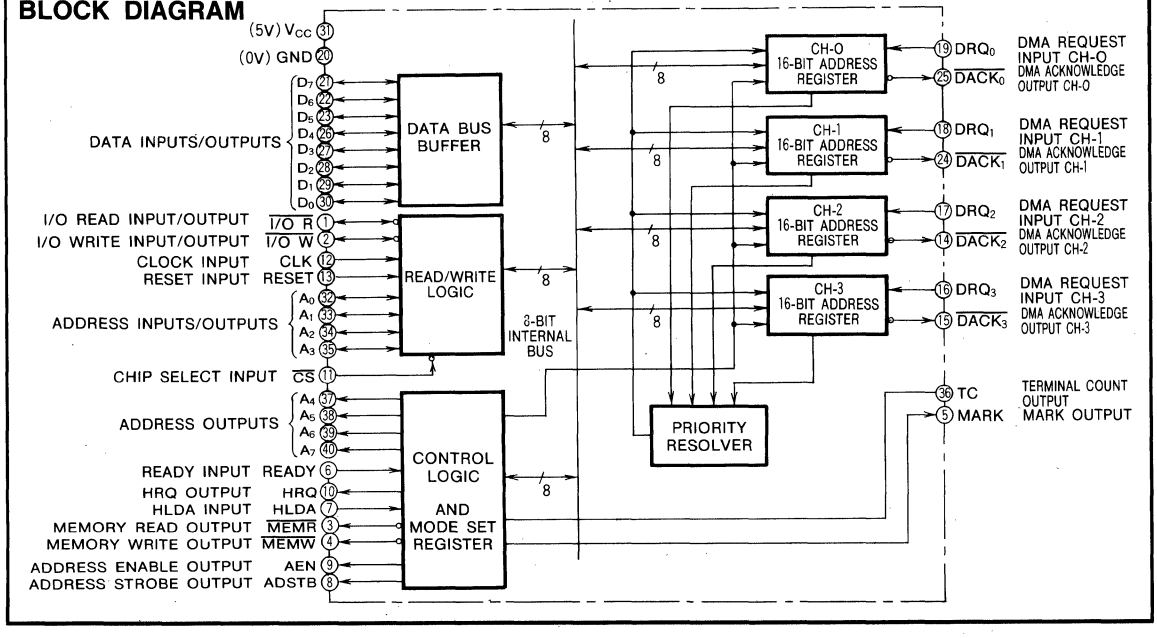


Outline 40P4

FUNCTION

The M5L8257P-5 controller is used in combination with the M5L8212P 8-bit input/output port in 8-bit microcomputer systems. It consists of a channel section to acknowledge DMA requests, control logic to exchange commands and data with the CPU, read/write logic, and registers to hold transfer addresses and count the number of bytes to be transferred. When a DMA request is made to an unmasked channel from the peripherals after setting of the transfer mode, transfer-start address and the number of transferred bytes for the registers, the M5L8257P-5 issues a priority request for the use of the bus to the CPU. On receiving an HLDA signal from the CPU, it sends a DMA acknowledge signal to the channel with the highest priority, starting DMA operation. During DMA operation, the contents of the high-order 8 bits of the transfer memory address are transmitted to the M5L8212P address-latch device through pins $D_0 \sim D_7$. The contents of the low-order 8 bits are transmitted through pins $A_0 \sim A_7$. After address transmission, DMA transfer can be started by dispatching read and write signals to the memories and peripherals.

BLOCK DIAGRAM



OPERATION

I/O Read Input/Output ($\overline{I/OR}$)
When the M5L8257P-5 is in slave-mode operation, this threestate, bidirectional pin serves for inputting and reads the upper/lower bytes of the 8-bit status register or 16-bit DMA address register and the high/low order bytes of the terminal counter.

In the master mode, the pin gives control output and is used to obtain data from a peripheral equipment during the DMA write cycle.

I/O Write Input/Output ($\overline{I/OW}$)
This pin is also of the three-state bidirectional type. When the M5L8257P-5 is in slave-mode operation, it serves for inputting and loads the contents of the data bus on the upper/lower bytes of the 8-bit status register or 16-bit DMA address register and the upper/lower bytes of the terminal counter.

Memory Read Output ($\overline{MEMR}$)
This active-low three-state output is used to read data from the addressed memory location during DMA read cycles.

Memory Write Output ($\overline{MEMW}$)
This active-low three-state output is used to write data into the addressed memory location during DMA write cycles.

Mark Output (MARK)
This signal notifies that the DMA transfer cycle for each channel is the 128th cycle since the previous MARK output.

Ready Input (READY)
This asynchronous input is used to extend the memory read and write cycles in the M5L8257P-5 with wait states if the selected memory requires longer cycles.

Hold Acknowledge Input (HLDA)
This input from the CPU indicates that the system bus is controlled by the M5L8257P-5.

Address Strobe Output (ADSTB)
This output strobes the most significant byte of the memory address into the M5L8212P 8-bit input/output port through the data bus.

Address Enable Output (AEN)
This signal is used to disable the system data bus and system control bus by means of the bus enable pin on the M5L8228P system controller. It may also be used to inhibit non-DMA devices from responding during DMA cycles.

Hold Request Output (HRQ)
This output requests control of the system bus. HRQ will normally be applied to the HOLD input on the CPU.

Chip-Select Input ($\overline{CS}$)
This pin is active on a low-level. It enable the IORD and IOWR signals output from the CPU, when the M5L8257P-5 is in slave-mode operation.

In the master mode, it is disabled to prevent the chip from selecting itself while performing the DMA function.

Clock Input (CLK)
This pin generates internal timing for the M5L8257P-5 and is connected to the $\phi_{2(TTL)}$ output of the M5L8224P-5 clock generator.

Reset Input (RESET)
This asynchronous input clears all registers and control lines inside the M5L8257P-5.

DMA Acknowledge Outputs ($\overline{DACK0}$~$\overline{DACK3}$)
These active-low outputs indicate that the peripheral equipment connected to the channel in question can execute the DMA cycle.

DMA Request Inputs (DRQ0~DRQ3)
These independent, asynchronous channel-request inputs are used to secure use of the DMA cycle for the peripherals.

Data-Bus Buffer
This three-state, bidirectional, 8-bit buffer interfaces the M5L8257P-5 to the CPU for data transfer. During a DMA cycle the upper 8 bits of the DMA address are output to the M5L8212P latch device through this buffer.

Address Inputs/Outputs (A_0~A_3)
The four bits of these input/output pins are bidirectional. When the M5L8257P-5 is in slave-mode operation, serve to input and address the internal registers. In the case of master operation, they output the low-order 4 bits of the 16-bit memory address.

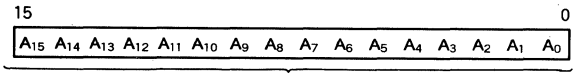
Terminal Count Output (TC)
This output signal notifies that the present DMA cycle is the last cycle for this data block.

Address Inputs/Outputs (A_4~A_7)
These four address lines are three-state outputs which constitute bits 4 through 7 of the memory address generated by the M5L8257P-5 during all DMA cycles.

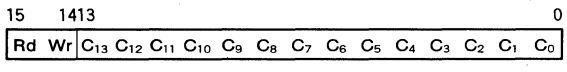
Register Initialization

Two 16-bit registers are provided for each of the 4 channels.

DMA Address register



Terminal count register

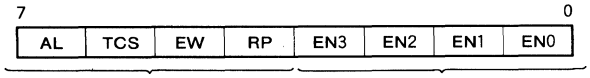


The DMA transfer starting address, number of transferred bytes, and DMA mode are written for each channel in 2 steps using the 8-bit data bus. The lower-order and upper-order bytes are automatically indicated by the firstlast flipflop for the writing and reading in 2 continuous steps.

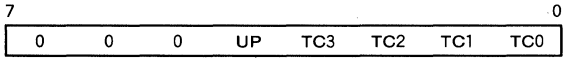
The DMA mode (read, write, or verify) is indicated by the upper 2 bits of the terminal count register. The read mode refers to the operation of peripheral devices reading data out of memory. The write mode refers to data from peripheral devices being written into memory. The verify mode sends neither the read nor the write signals and performs a date check at the peripheral device.

In addition to the above-mentioned registers, there is a mode set register and a status register.

Mode set register (write only)



Status Register (read only)



The upper-order 4-bits of the mode set register are used to select the added function, as described in Table 1. The lower-order 4-bits are mask kits for each channel. When set to 1, DMA requests are allowed. When the reset signal is input, all bits of the mode set and status registers are reset and DMA is inhibited for all channels. Therefore, to execute DMA operations, registers must first be initialized. An example of such an initialization is shown below.

MODESET:

```
MVI  A, ADDL
OUT  00#:   Channel 0 lower-order address
MVI  A, ADDH
OUT  00#:   Channel 0 upper-order address
MVI  A, TCL
OUT  01#:   Channel 0 terminal count lower-order
OUT  01#:   Channel 0 terminal count upper-order
MVI  A, XX
OUT  08#:   Mode set resister
```

As can be seen from the above example, until the contents of the address register and terminal count register become valid, the enable bit of the mode set register must not be set. This prevents memory contents from being destroyed by improper DRQ signals from peripheral devices.

DMA Operation Description

When a DMA request signal is received at the DRQ pin from a peripheral device after register initialization for a channel that is not masked, the M5L8257P-5 outputs a hold request signal to the CPU to begin DMA operation (S_1).

The CPU, upon receipt of the HRQ signal, outputs the HLDA signal which reserves capture of the bus after it has executed the present instruction to place this system in the hold state.

When the M5L8257P receives the HLDA signal, an internal priority determining circuit selects the channel with the highest priority for the beginning of data transfer (S_0).

Upon the next S_1 state, the address signal is sent. The lower-order 8-bits and upper-order 8-bits are sent by means of the $A_0 \sim A_7$ and $D_0 \sim D_7$ pins respectively, latched into the M5L8212P and output at pins $A_8 \sim A_{15}$. Simultaneous with this, the AEN signal is output to prohibit the selection of a device not capable of DMA.

In the S_2 state, the read, extended write, and DACK signals are output and data transferred from memory or a peripheral device appears on the data bus.

In the S_3 state, the write signal required to write data from the bus is output. At this time if the remaining number of bytes to be transferred from the presently selected channel has reached 0, the terminal count (TC) signal is output. Simultaneously with this, after each 128-byte data transfer a mark signal is output as required. In addition, in this state the READY pin is sampled and, if low, the wait state (S_W) is entered. This is used to perform DMA with slow access memory devices. In the verify mode, READY input is ignored.

In the S_4 state, the DRQ and HLDA pins are sampled at the end of a transferred byte as the address signal, control signals, and $\overline{DACK}$ signal are held to determine if transfer will continue.

As described above, transfer of 1 byte requires a minimum of 4 states for execution. For example, if a 2MHz clock input is used, the maximum transfer rate is 500k byte/s.

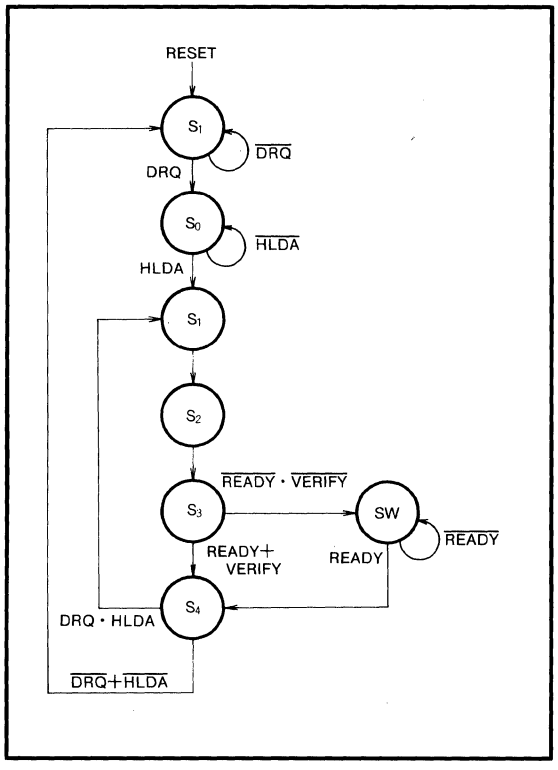


Fig. 1 DMA Operation state transition diagram

Memory Mapped I/O

When using memory mapped I/O, it is neccessary to change the connections for the control signals.

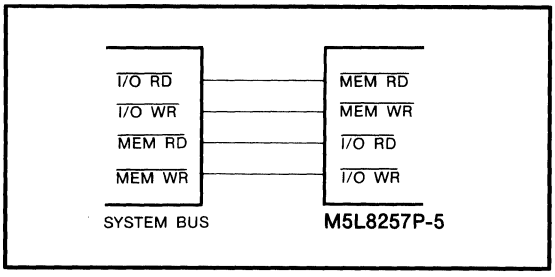


Fig. 2 Memory mapped I/O

Also, the read mode and write mode specifications for setting the mode of the terminal count are reversed.

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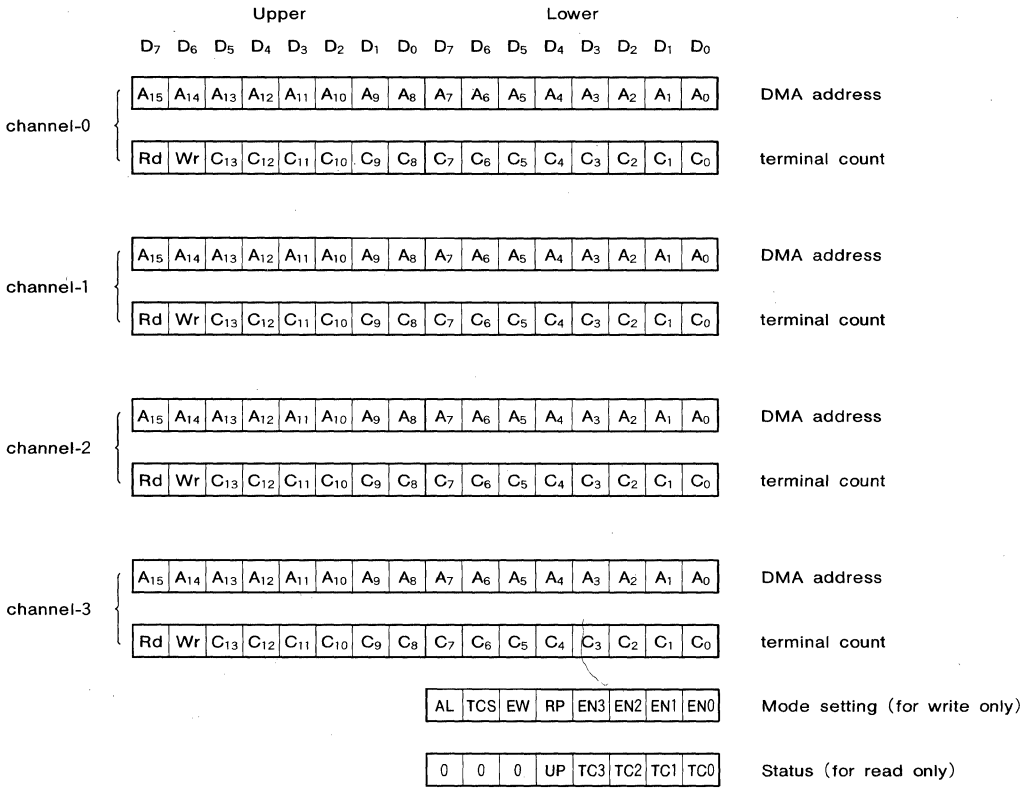
INTERNAL REGISTERS OF THE M5L8257P-5



A_0~A_{15} : Address of the memories for which DMA will be carried out from now on. In initialization, DMA start addresses must be written.
C_0~C_{13} : Terminal counts-in this IC (the number of remaining transfer bytes minus 1)
Rd. Wr : Used for DMA-mode-setting by the following convention:

Rd	Wr	Mode to be set
0	0	DMA verify
0	1	DMA write
1	0	DMA read
1	1	Prohibition

AL : Automatic load mode. When this bit has been set, contents of the channel 3 register are written, as are on the channel 2 register when channel 2 DMA transfer comes to an end. This mode allows quick, automatic chaining operations without intervention of the software.
EW : Extended write signal mode. When this bit has been set, write signals can be transmitted in advance to memories and peripheral equipment requiring long access time.
TCS : Terminal count stop. When a DMA transfer process is complete, with terminal-count output, the channel-enable mask of that channel is reset, prohibiting subsequent DMA cycles.
RP : Rotating priority mode. The setting of this mode allows the priority order to be rotated by each byte transfer.

Channel used for the present data transfer		CH-0	CH-1	CH-2	CH-3
Priority list for the next cycle	1	CH-1	CH-2	CH-3	CH-0
	2	CH-2	CH-3	CH-0	CH-1
	3	CH-3	CH-0	CH-1	CH-2
	4	CH-0	CH-1	CH-2	CH-3

EN0~EN3 : Channel-enable mask. This mask prohibits or allows the DMA request.
UP : Update flag. This is set when register contents are transferred in an automatic load mode from channel 3 to channel 2.
TC0~TC3 : Terminal-count status flags. At the time of terminal-count output, the flag corresponding to the channel is set.

REGISTER ADDRESS

Address input				F/L	Register
A_3	A_2	A_1	A_0		
0	0	0	0	0	channel 0 DMA address Low-order
0	0	0	0	1	channel 0 DMA address High-order
0	0	0	1	0	channel 0 terminal count Low-order
0	0	0	1	1	channel 0 terminal count High-order
0	0	1	0	0	channel 1 DMA address Low-order
0	0	1	0	1	channel 1 DMA address High-order
0	0	1	1	0	channel 1 terminal count Low-order
0	0	1	1	1	channel 1 terminal count High-order
0	1	0	0	0	channel 2 DMA address Low-order
0	1	0	0	1	channel 2 DMA address High-order
0	1	0	1	0	channel 2 terminal count Low-order
0	1	0	1	1	channel 2 terminal count High-order
0	1	1	0	0	channel 3 DMA address Low-order
0	1	1	0	1	channel 3 DMA address High-order
0	1	1	1	0	channel 3 terminal count Low-order
0	1	1	1	1	channel 3 terminal count High-order
1	0	0	0	0	Mode Setting (for Write Only)
1	0	0	0	0	Status (for Read Only)

F/L : First/last flip-flop. This is toggled when program and register-read operations for each channel are finished, and specifies whether the next program or read operation is to be for the upper bytes or the lower bytes. This means that write and read operations for each register must be carried out for a set of lower and higher bytes.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Power-supply voltage	With respect to GND	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Power dissipation (max.)	T_a=25℃	1000	mW
Topr	Operating free-air temperature range		−20～75	℃
Tstg	Storage temperature range		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−20～75℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Power-supply voltage	4.75	5	5.25	V
V_{SS}	Power-supply voltage (GND)		0		V
V_{IH}	High-level input voltage	2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V

ELECTRICAL CHARACTERISTICS (T_a=−20～75℃, V_{CC}=5 V±5 %, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OL}	Low-level output voltage	I_{OL}=1.6mA			0.45	V
V_{OH1}	High-level output voltage for AB, DB and AEN	I_{OH}=−150μA	2.4		V_{CC}	V
V_{OH2}	High-level output voltage for HRQ	I_{OH}=−80μA	3.3		V_{CC}	V
V_{OH3}	High-level output voltage for others		2.4		V_{CC}	V
I_{CC}	Power-supply current from V_{CC}				120	mA
I_I	Input current	V_I=V_{CC}～0V	−10		10	μA
I_{OZ}	Off-state output current	V_I=V_{CC}～0V	−10		10	μA
C_I	Input capacitance	T_a=25℃, V_{CC}=V_{SS}=0V Pins other than that under measurement are set to 0V, f_C=1MHz			10	pF
$C_{I/O}$	Input/output terminal capacitance				20	pF

TIMING REQUIREMENTS (T_a=−20～75℃, V_{CC}=5 V±5 %, V_{SS}=0 V, V_{IH}=V_{OH}=2 V, V_{IL}=V_{OL}=0.8V, unless otherwise noted)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{w(R)}$	Read pulse width	T_{RR}	C_L=150pF	250			ns
$t_{su(A-R)}$ $t_{su(CS-R)}$	Address or $\overline{CS}$ setup time before read	T_{AR}		0			ns
$t_{h(R-A)}$ $t_{h(R-CS)}$	Address or $\overline{CS}$ hold time after read	T_{RA}		0			ns
$t_{su(R-DQ)}$	Date setup time before read	T_{RD}		0		200	ns
$t_{h(R-DQ)}$	Data hold time after read	T_{DF}		20		100	ns
$t_{w(W)}$	White pulse width	T_{WW}		200			ns
$t_{su(A-W)}$	Address setup time before write	T_{AW}		20			ns
$t_{h(W-A)}$	Address hold time after write	T_{WA}		0			ns
$t_{su(DQ-W)}$	Data setup time before write	T_{DW}		200			ns
$t_{h(W-DQ)}$	Data hold time after write	T_{WD}		0			ns
$t_{w(RST)}$	Reset pulse width	T_{RSTW}		300			ns
$t_{su(Vcc-RST)}$	Supply voltage setup time before reset	T_{RSTD}		500			μs
t_r	Input signal rise time	T_r				20	ns
t_f	Input signal fall time	T_f				20	ns
$t_{su(RST-W)}$	Reset setup time before write	T_{RSTS}		2			$t_{C(\phi)}$
$t_{C(\phi)}$	Clock cycle time	T_{CY}		0.32		4	μs
$t_{w(\phi)}$	Clock pulse width	T_e		80		$0.8t_{C(\phi)}$	ns
$t_{su(DRQ-\phi)}$	DRQ setup time before clock	T_{QS}		70			ns
$t_{h(HLDA-DRQ)}$	DRQ hold time after HLDA	T_{QH}		0			ns
$t_{su(HLDA-\phi)}$	HLDA setup time before clock	T_{HS}		100			ns
$t_{su(RDY-\phi)}$	Ready setup time before clock	T_{RS}		30			ns
$t_{h(\phi-RDY)}$	Ready hold time after clock	T_{RH}		20			ns

Note 1 : Measurement conditions: M5L8257P C_L=100pF, M5L8257P-5 C_L=150pF

SWITCHING CHARACTERISTICS (T_a=−20~75℃, V_{CC}=5V±5%, V_{SS}=0V, V_{OH}=2V, V_{OL}=0.8V, unless otherwise noted) (Note2)

Symbol	Parameter	Alternative symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ (Note3)	T_{DQ}				160	ns
$t_{PLH(\phi-HRQ)}$ $t_{PHL(\phi-HRQ)}$	Propagation time from clock to HRQ (Note5)	T_{DQI}				250	ns
$t_{PLH(\phi-AEN)}$	Propagation time from clock to AEN (Note3)	T_{AEL}				300	ns
$t_{PHL(\phi-AEN)}$	Propagation time from clock to AEN (Note3)	T_{AET}				200	ns
$t_{PZV(AEN-A)}$	Propagation time from AEN to address active (Note6)	T_{AEA}		20			ns
$t_{PZV(\phi-A)}$	Propagation time from clock to address active (Note4)	T_{FAAB}				250	ns
$t_{PVZ(\phi-A)}$	Propagation time from clock to address floating (Note4)	T_{AFAB}				150	ns
$t_{PLH(\phi-A)}$	Address setup time after clock (Note4)	T_{ASM}				250	ns
$t_{h(\phi-A)}$	Address hold time after clock (Note4)	T_{AH}		$t_{PLH(\phi-A)}-50$			ns
$t_{h(R-A)}$	Address hold time after read (Note6)	T_{AHR}		60			ns
$t_{h(W-A)}$	Address hold time after write (Note6)	T_{AHW}		300			ns
$t_{PZV(\phi-DQ)}$	Propagation time from clock to data active	T_{FADB}				300	ns
$t_{PVZ(\phi-DQ)}$	Propagation time from clock to data floating (Note4)	T_{AFDB}		$t_{PHL(\phi-ASTB)}+20$		170	ns
$t_{PHL(A-ASTB)}$	Propagation time from address to address strobe (Note4)	T_{ASS}		100			ns
$t_{h(ASTB-A)}$	Propagation time from address strobe to address hold (Note6)	T_{AHS}		50			ns
$t_{PLH(\phi-ASTB)}$	Propagation time from clock to address strobe (Note3)	T_{STL}				200	ns
$t_{PHL(\phi-ASTB)}$	Propagation time from clock to address strobe (Note3)	T_{STT}				140	ns
$t_{W(ASTB)}$	Address strobe pulse width (Note6)	T_{SW}		$t_{C(\phi)}-100$			ns
$t_{PHL(AS-R)}$ $t_{PHL(AS-WE)}$	Propagation time from address strobe to read or extended write (Note6)	T_{ASC}		70			ns
$t_{h(DQ-R)}$ $t_{h(DQ-WE)}$	Read or extended write hold time after data (Note6)	T_{DBC}		20			ns
$t_{PLH(\phi-DACK)}$ $t_{PHL(\phi-TC/MARK)}$ $t_{PLH(\phi-TC/MARK)}$	Propagation time from clock to DACK or TC/MARK (Note3, 7)	T_{AK}				250	ns
$t_{PHL(\phi-R)}$ $t_{PHL(\phi-W)}$ $t_{PHL(\phi-WE)}$	Propagation time from clock to read, write or extended write (Note4, 8)	T_{DCL}				200	ns
$t_{PLH(\phi-R)}$ $t_{PLH(\phi-W)}$	Propagation time from clock to read or write (Notes4, 9)	T_{DCT}				200	ns
$t_{PZV(\phi-R)}$ $t_{PZV(\phi-W)}$	Propagation time from clock to read active or write active (Note4)	T_{FAC}				300	ns
$t_{PVZ(\phi-R)}$ $t_{PVZ(\phi-W)}$	Propagation time from clock to read floating or write floating (Note4)	T_{AFC}				150	ns
$t_{W(R)}$	Read pulse width (Note6)	T_{RAM}		$2t_{C(\phi)}+t_{W(\phi)}-50$			ns ns
$t_{W(W)}$	Write pulse width (Note6)	T_{WWM}		$t_{C(\phi)}-50$			ns
$t_{W(WE)}$	Extended write pulse width	T_{WWME}		$2t_{C(\phi)}-50$			ns

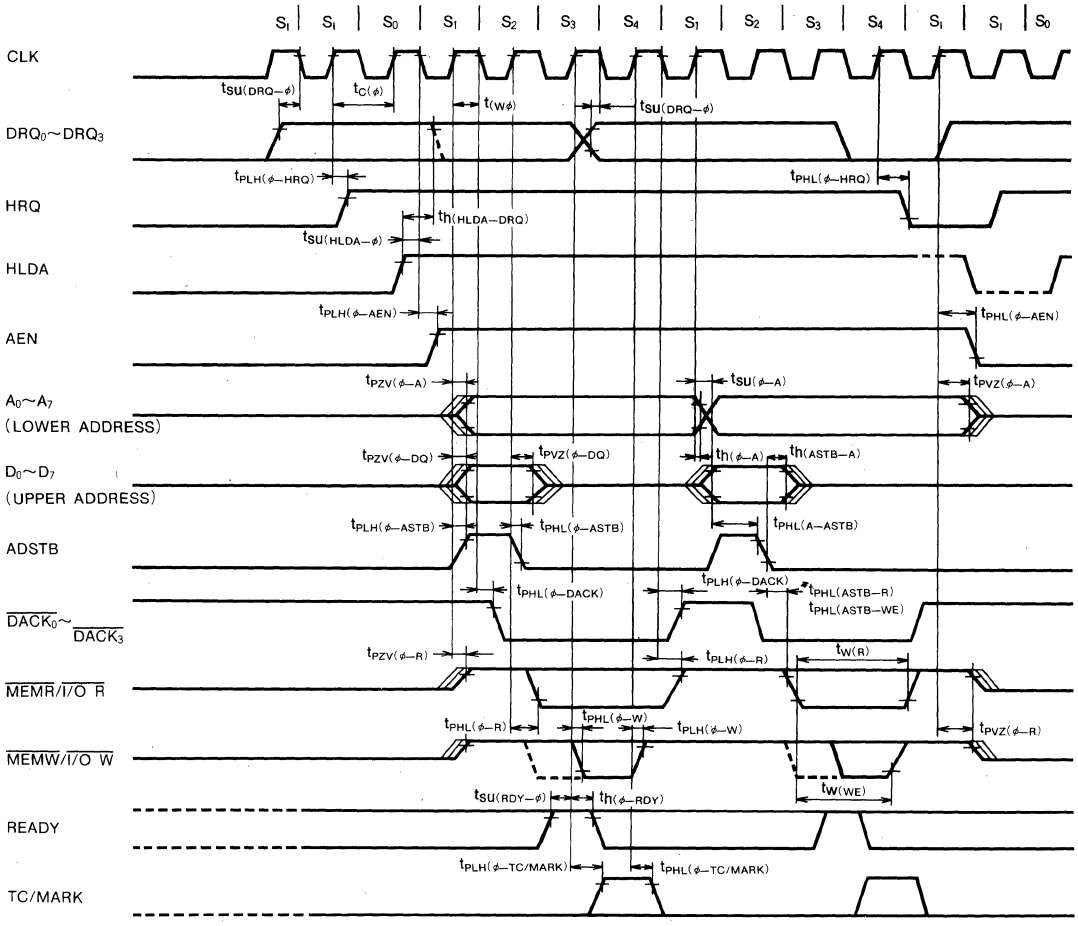
Note 2 : Reference level is V_{OH}=3.3V
3 : Load=1TTL
4 : Load=1TTL+50pF
5 : Load=1TTL+(R_L=3.3kΩ), V_{OH}=3.3V

Note 6 : Tracking specification
7 : $\Delta t_{PLH(\phi-DACK)}<50ns$, $\Delta t_{PHL(\phi-TC/MARK)}<50ns$, $\Delta t_{PLH(\phi-TC/MARK)}<50ns$
8 : $\Delta t_{PHL(\phi-R)}<50ns$, $\Delta t_{PHL(\phi-W)}<50ns$, $\Delta t_{PHL(\phi-WE)}<50ns$
9 : $\Delta t_{PLH(\phi-R)}<50ns$, $\Delta t_{PLH(\phi-W)}<50ns$

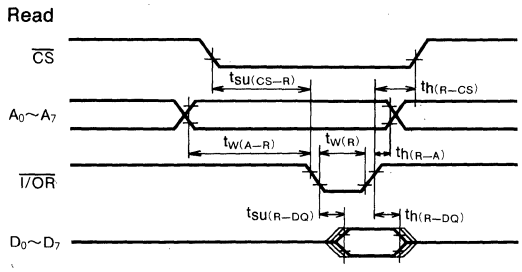
4

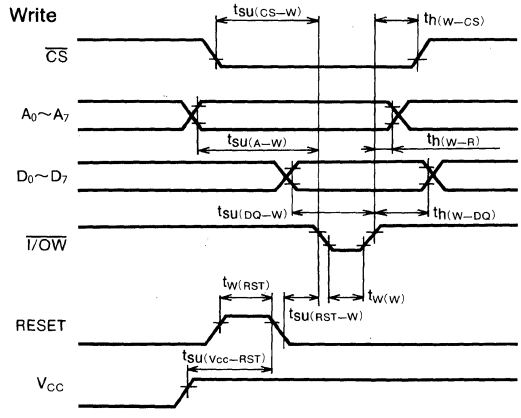
TIMING DIAGRAMS

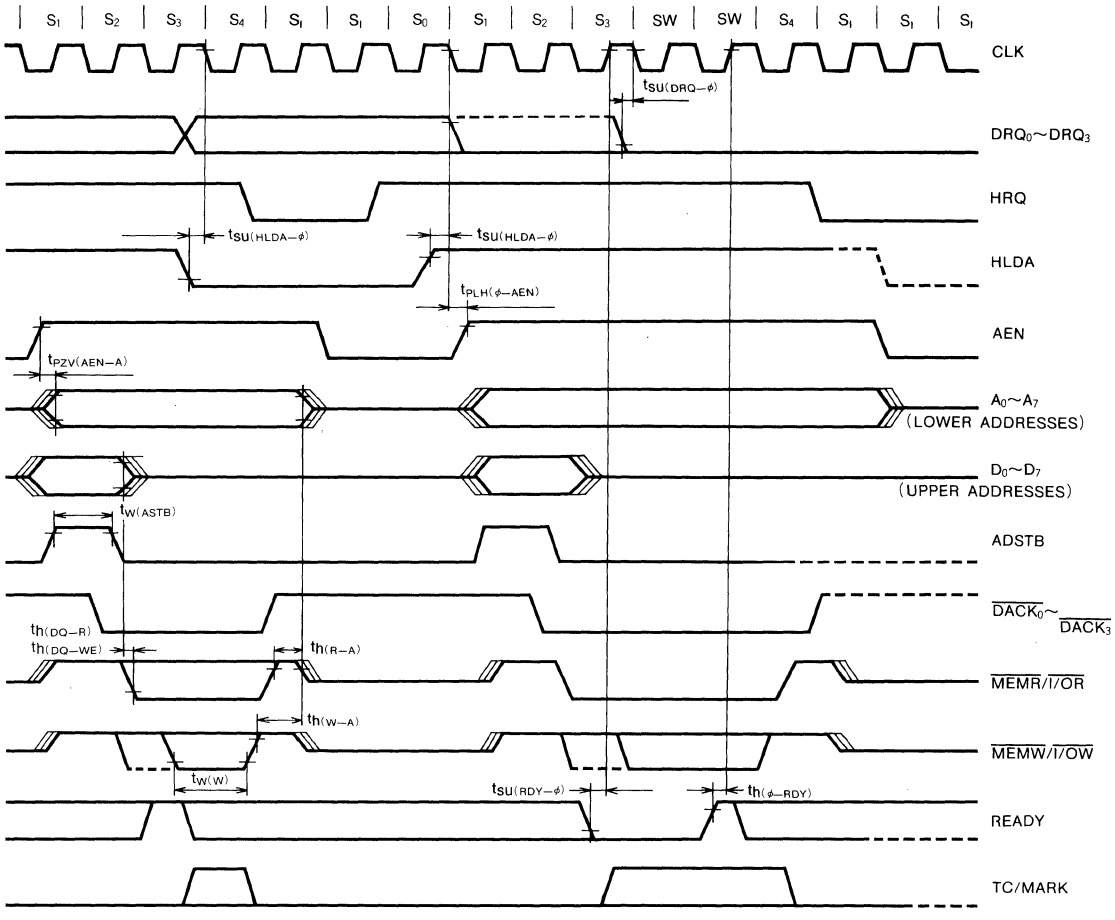
DMA Mode



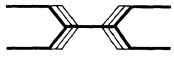
Slave Mode (Reference voltage: "H"=2V "L"=0.8V)







Note 1 :



The center line indicates a floating (high-impedance) state.