

M5L8282P/M5L8283P

T.46-07-11

OCTAL LATCH

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DESCRIPTION

The M5L8282P and M5L8283P are semiconductor integrated circuits consisting of sets of eight 3-state latches for use with various types of microprocessors.

FEATURES

- 3-state, high-fanout output ($I_{OL}=32\text{mA}$, $I_{OH}=-5\text{mA}$)
- Low power dissipation

APPLICATION

Data latches for various microcomputer systems

FUNCTION

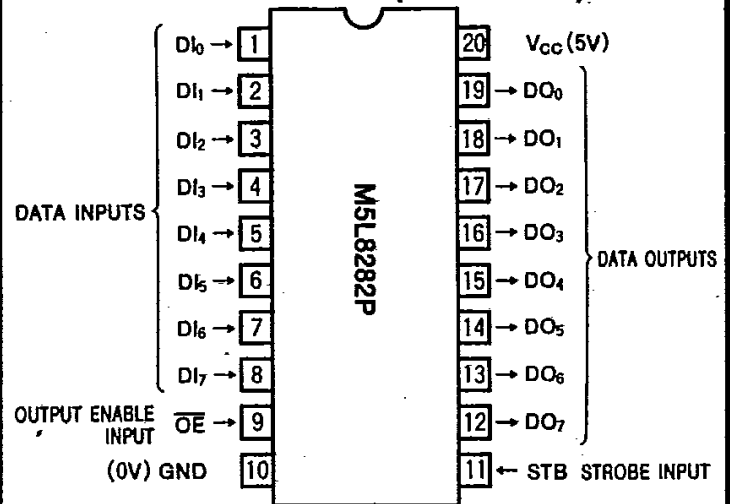
The M5L8282P and M5L8283P are latches with non-inverted and inverted outputs, respectively.

When the strobe input STB is high, the data inputs $DI_0 \sim DI_7$ are passed through the data outputs $DO_0 \sim DO_7$ (M5L8282P) or to the data outputs $\overline{DO}_0 \sim \overline{DO}_7$ (M5L8283P), changes in the $DI_0 \sim DI_7$ signals being reflected in the data outputs.

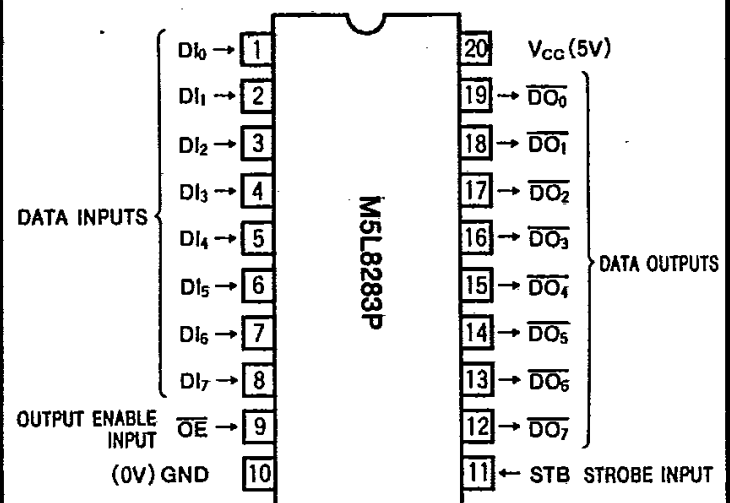
If the STB is changed from high to low, the data $DI_0 \sim DI_7$ just before the change is latched. If the DI data is changed while STB is low, this change is not reflected in the data outputs.

When \overline{OE} is made high, all the data outputs go into the high-impedance state, the data latched prior to \overline{OE} going high being held.

PIN CONFIGURATION (TOP VIEW)

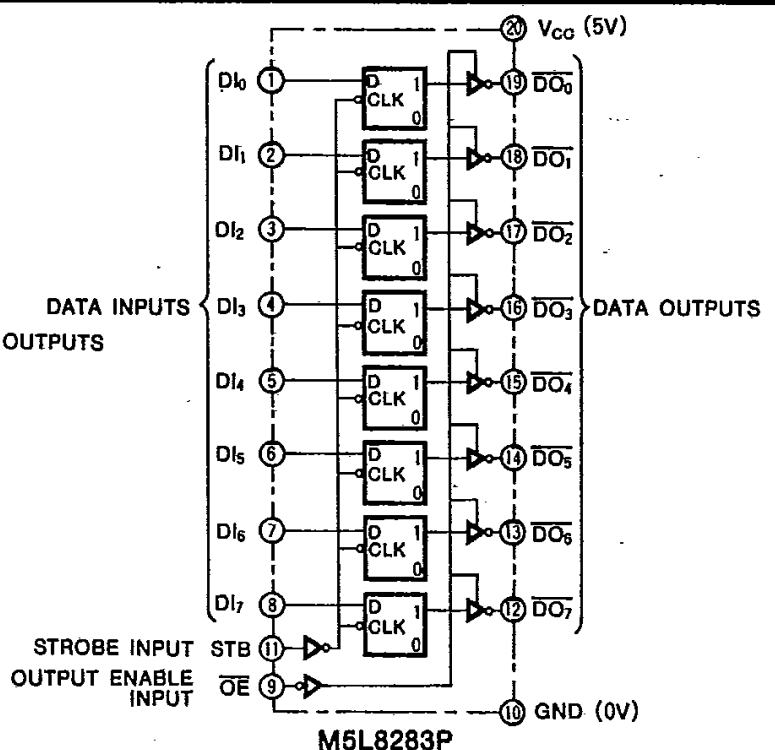
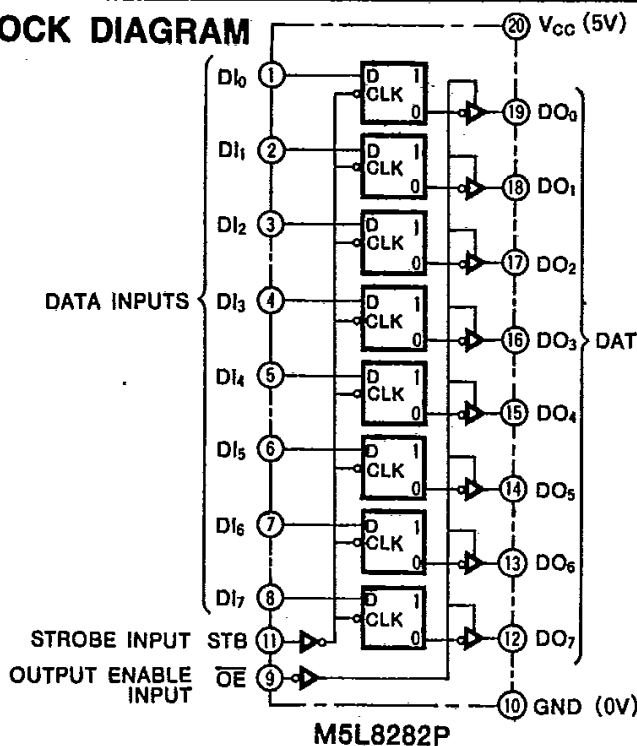


Outline 20P4



Outline 20P4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a=0\sim 75^{\circ}\text{C}$, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|-----------|--------------------------------------|------------|-------------------|--------------------|
| V_{CC} | Supply voltage | | $-0.5\sim +7$ | V |
| V_I | Input voltage | | $-0.5\sim +5.5$ | V |
| V_O | Output voltage | | $-0.5\sim V_{CC}$ | V |
| T_{opr} | Operating free-air temperature range | | $0\sim +75$ | $^{\circ}\text{C}$ |
| T_{stg} | Storage temperature range | | $-65\sim +150$ | $^{\circ}\text{C}$ |

RECOMMENDED OPERATING CONDITIONS ($T_a=0\sim 75^{\circ}\text{C}$, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|----------|---------------------------|---------------------------|--------|-----|-----|------|
| | | | Min | Nom | Max | |
| V_{CC} | Supply voltage | | 4.5 | 5 | 5.5 | V |
| I_{OH} | High-level output current | $V_{OH}\geq 2.4\text{V}$ | 0 | | -5 | mA |
| I_{OL} | Low-level output current | $V_{OL}\leq 0.45\text{V}$ | 0 | | 32 | mA |

ELECTRICAL CHARACTERISTICS ($T_a=0\sim 75^{\circ}\text{C}$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------|--|---|--------|-----|------|---------------|
| | | | Min | Typ | Max | |
| V_{IH} | High-level input voltage | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.8 | V |
| V_{IC} | Input clamp voltage | $V_{CC}=4.5\text{V}$, $I_{IC}=-5\text{mA}$ | | | -1 | V |
| V_{OH} | High-level output voltage | $V_{CC}=4.5\text{V}$, $I_{OH}=-5\text{mA}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage | $V_{CC}=4.5\text{V}$, $I_{OL}=32\text{mA}$ | | | 0.45 | V |
| I_{OZH} | Off-state output current, high-level applied to the output | $V_{CC}=5.5\text{V}$, $V_I=2\text{V}$, $V_O=5.25\text{V}$ | | | 50 | μA |
| I_{OZL} | Off-state output current, low-level applied to the output | $V_{CC}=5.5\text{V}$, $V_I=2\text{V}$, $V_O=0.4\text{V}$ | | | -50 | μA |
| I_{IH} | High-level input current | $V_{CC}=5.5\text{V}$, $V_I=5.25\text{V}$ | | | 50 | μA |
| I_{IL} | Low-level input current | $V_{CC}=5.5\text{V}$, $V_I=0.45\text{V}$ | | | -0.2 | mA |
| I_{CC} | Supply current | $V_{CC}=5.5\text{V}$ | | | 80 | mA |
| C_{IN} | Input capacitance | $F=1\text{MHz}$, $V_{BIAS}=2.5\text{V}$ $V_{CC}=5\text{V}$, $T_a=25^{\circ}\text{C}$ | | | 12 | pF |

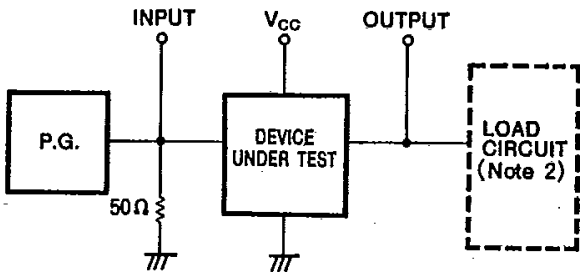
SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}\pm 10\%$, $T_a=0\sim 75^{\circ}\text{C}$, unless otherwise noted)

| Symbol | Parameter | Alternate symbol | Test conditions | M5L8282P | | | M5L8283P | | | Unit |
|------------------------|--|------------------|-----------------|----------|-----|-----|----------|-----|-----|------|
| | | | | Limits | | | Limits | | | |
| | | | | Min | Typ | Max | Min | Typ | Max | |
| t_{PLH} t_{PHL} | Propagation time from DI input to DO or $\overline{\text{DO}}$ for low-to-high or high-to-low change | T_{IVOV} | (Note 1) | 5 | | 30 | 5 | | 22 | ns |
| t_{PLH} t_{PHL} | Propagation time from STB input to DO or $\overline{\text{DO}}$ for low-to-high and high-to-low change | T_{SHOV} | | 10 | | 45 | 10 | | 40 | ns |
| t_{PZH} t_{PZL} | Propagation time from $\overline{\text{OE}}$ input to DO or $\overline{\text{DO}}$ output when output is enabled | T_{ELOV} | | 10 | | 30 | 10 | | 30 | ns |
| t_{PHZ} t_{PLZ} | Propagation time from $\overline{\text{OE}}$ input to DO or DO output when the output is disabled | T_{EHOV} | | 5 | | 18 | 5 | | 18 | ns |

TIMING REQUIREMENTS ($V_{CC}=5V\pm 10\%$, $T_a=0\sim 75^\circ C$, unless otherwise noted)

| Symbol | Parameter | Alternate symbol | Test conditions | Limits | | | Unit |
|--------------------|---|-------------------|-----------------|--------|-----|-----|------|
| | | | | Min | Typ | Max | |
| $t_w(\text{STBH})$ | Strobe STB high pulse width | T_{SHSL} | | 15 | | | ns |
| t_{su} | Strobe STB setup time for $D_0\sim D_7$ | T_{IVSL} | | 0 | | | ns |
| t_h | STB hold time for $D_0\sim D_7$ | T_{SLIX} | | 25 | | | ns |

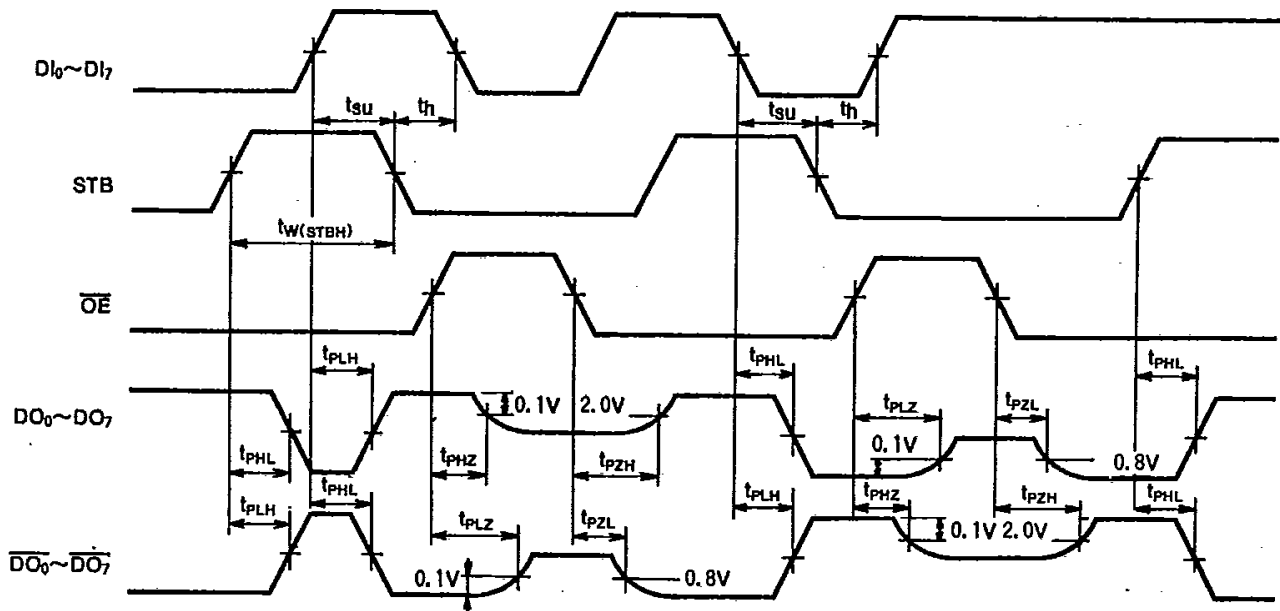
Note 1 : Test Circuit



Note 2 :

| TEST ITEM | $t_{\text{PLH}}, t_{\text{PHL}}$ | $t_{\text{PLZ}}, t_{\text{PZL}}$ | $t_{\text{PHZ}}, t_{\text{PZH}}$ |
|--------------|----------------------------------|----------------------------------|----------------------------------|
| LOAD CIRCUIT | | | |

TIMING DIAGRAM (Reference voltage=1.5V)

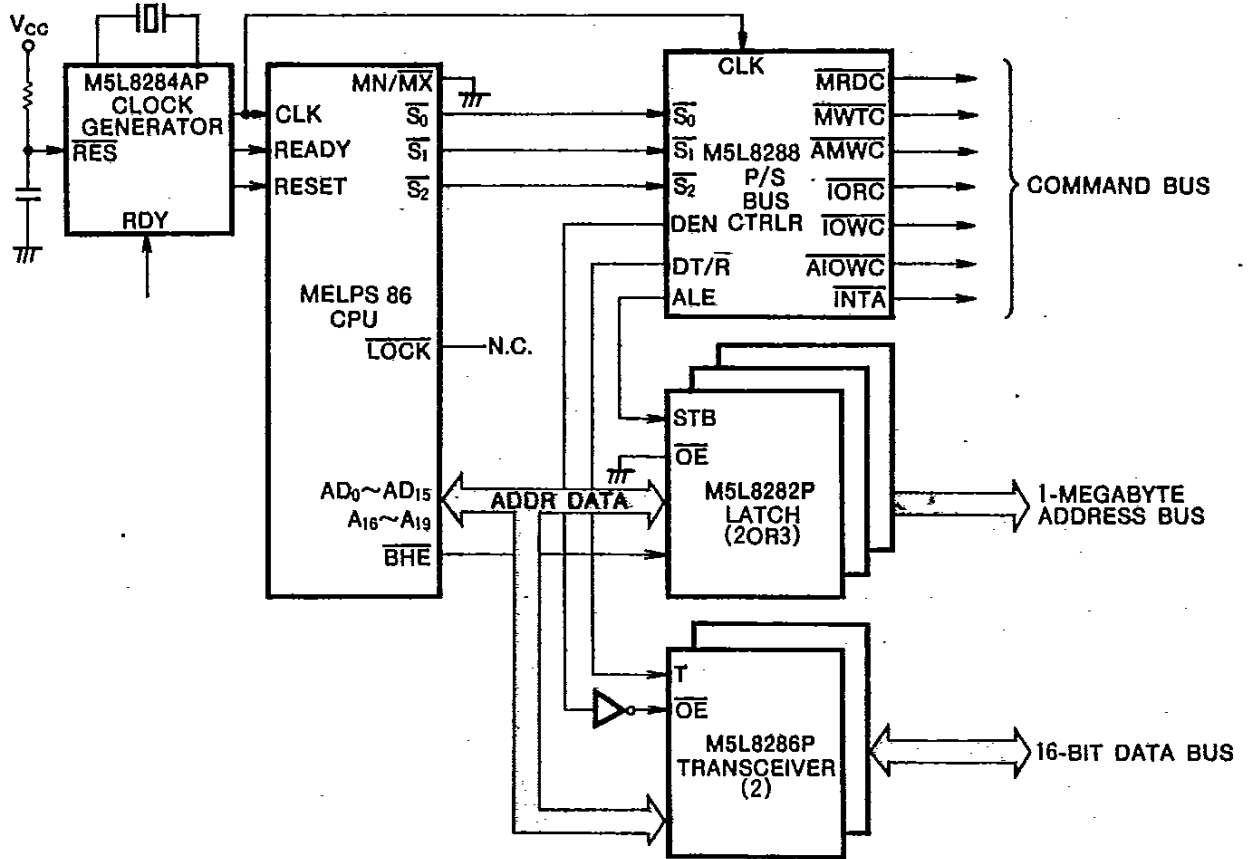


PRECAUTIONS FOR USE

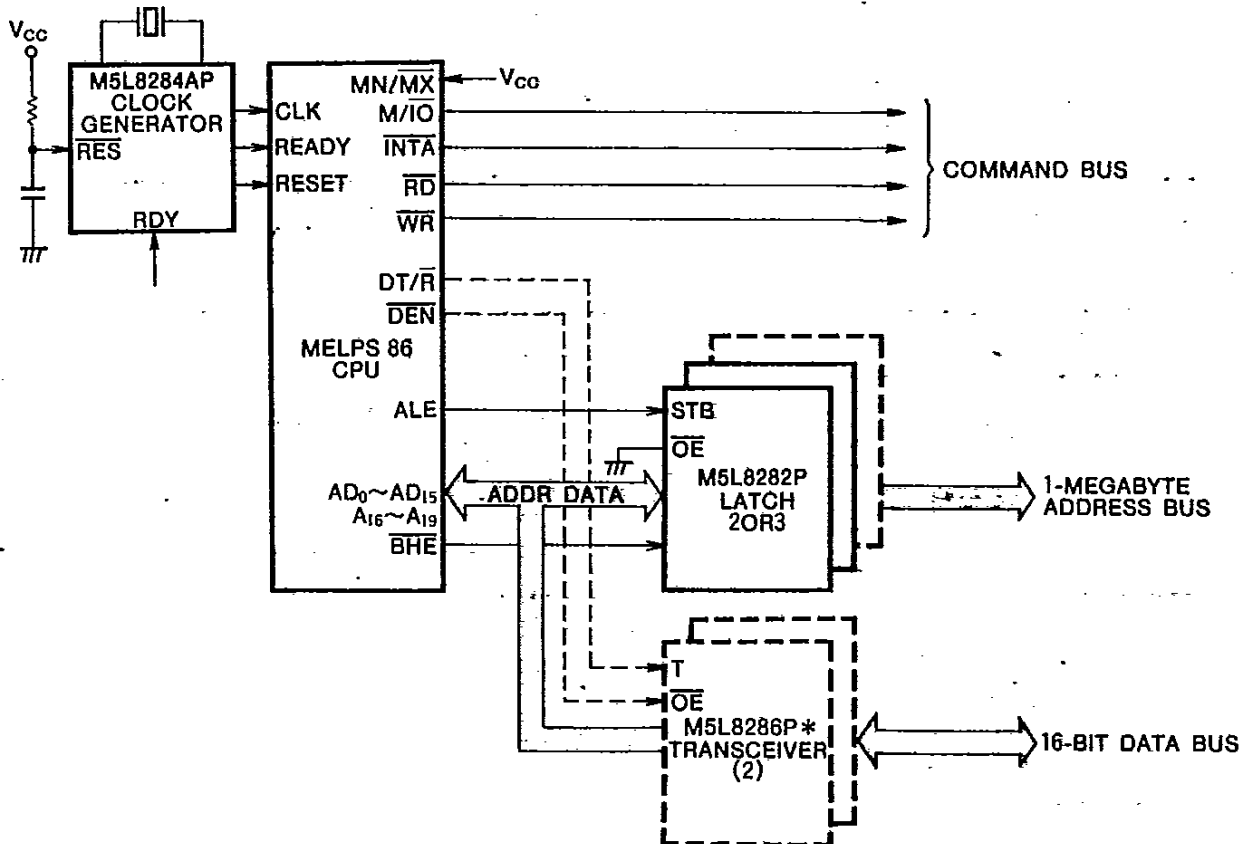
Care should be taken to accommodate the glitch that is generated when STB goes from low to high with the output low for the M5L8283P.

APPLICATION EXAMPLES

(1) Use in the maximum mode



(2) Use in the minimum mode



* : Option
Required when the number of devices
driving the bus increases