M5M5279P,J-20,-25,-35, -25L,-35L

294912-BIT (32768-WORD BY 9-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5279 is a family of 32768-word by 9-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time
  - M5M5279P,J-20 ····· 20ns(max)
  - M5M5279P,J-25,-25L ····· 25ns(max)
  - M5M5279P,J-35,-35L ····· 35ns(max)
- Low power dissipation
  - Active ····· 300mW(typ)
  - Stand by(-20,-25,-35) ····· 5mW(typ)
  - Stand by(-25L,-35L) ····· 50 μW(typ)
- Power down by $\overline{S_1}$
- Single 5V power supply
- Fully static operation
- Requires neither extenal clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S_1}$, S_2) input
- Output enable ($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other

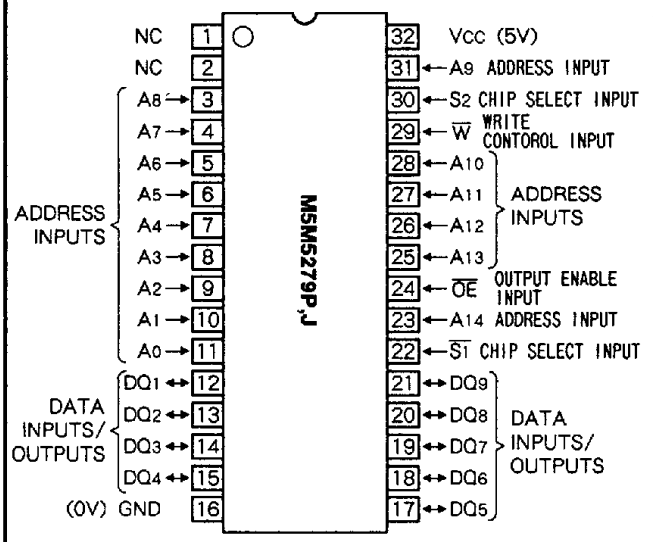
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S_1}$ low, S_2 high, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 32P4Y(DIP)
32P0J(SOJ)

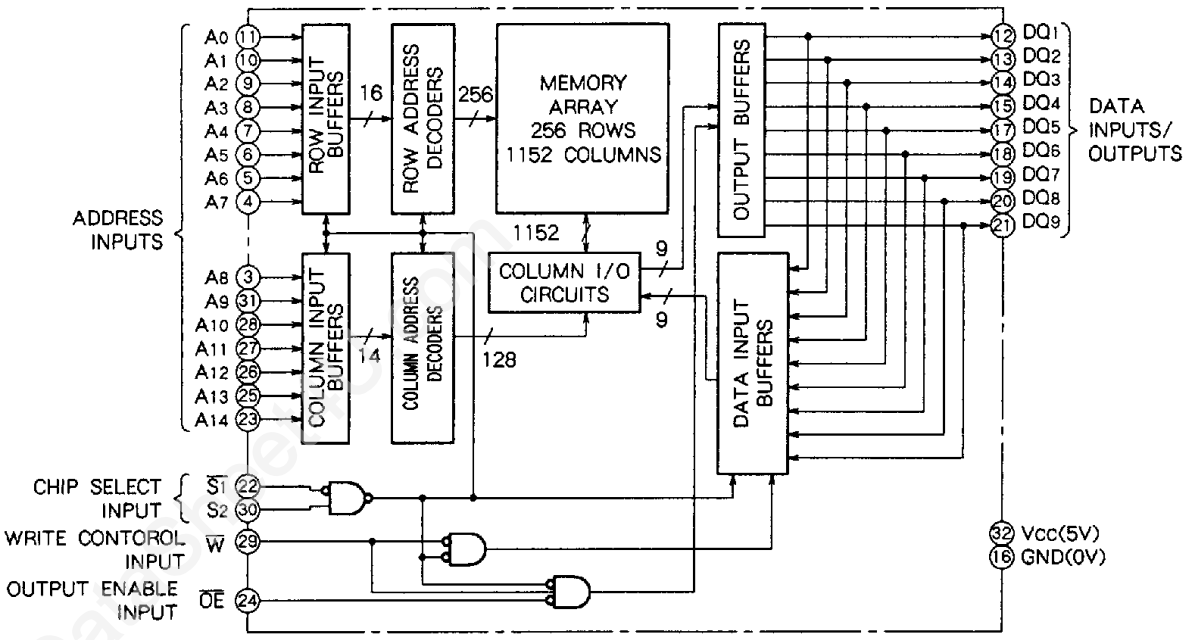
NC : NO CONNECTION

In a read operation, after setting $\overline{W}$ to high, $\overline{S_1}$ to low S_2 high and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S_1}$ is high, or S_2 is low, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S_1}$ controls the power-down feature. When $\overline{S_1}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S_1}$ is equivalent to the address access time.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

MODE SELECTION

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	Data input/output	Icc
H	X	X	X	Non selection	High-impedance	Stand by
L	L	X	X	Non selection	High-impedance	Active
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

H : V_{IH} L : V_{IL} X : V_{IH} or V_{IL}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5* ~7	V
V_I	Input voltage		−3.5* ~7	V
V_O	Output voltage		−3.5* ~7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		0~70	℃
$T_{stg(bias)}$	Storage temperature (bias)		−10~85	℃
T_{stg}	Storage temperature		−65~150	℃

* Pulse width ≦ 20ns, In case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.2		V_{CC}+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~V_{CC}				2	μA
| I_{OZ} |	Off-state output current	$V_{I(\overline{S})} = V_{IH}$, V_O = 0~V_{CC}				10	μA
I_{CC1}	Supply current from V_{CC}	$V_{I(\overline{S})} = V_{IL}$ Output open	AC(20ns cycle)			140	mA
			AC(25ns cycle)			130	
			AC(35ns cycle)			120	
			DC		75	100	
I_{CC2}	Stand by current	$V_{I(\overline{S})} = V_{IH}$	AC(20, 25, 35ns cycle)			40	mA
			Other $V_I \geqq V_{IH}$ or $\leqq V_{IL}$			30	
I_{CC3}	Stand by current	$V_{I(\overline{S})} = V_{CC}$−0.2V Other $V_I \leqq$ 0.2V or $V_I \geqq V_{CC}$−0.2V	-20, -25, -35		1	10	mA
			-25L, -35L		10	100	μA

Note 1. Current flow into an IC is positive, out is negative. * −3.0V in case of AC(Pulse width ≦ 20ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· V_{IH} = 3V, V_{IL} = 0V

Input rise and fall time ····· 3ns

Input timing reference levels ····· V_{IH} = 2.4V, V_{IL} = 0.6V

Output timing reference levels ····· V_{OH} = 2.0V, V_{OL} = 0.8V

Output loads ····· Fig.1, Fig.2

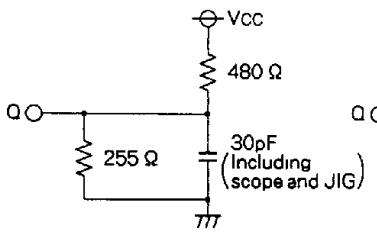


Fig.1 Output load

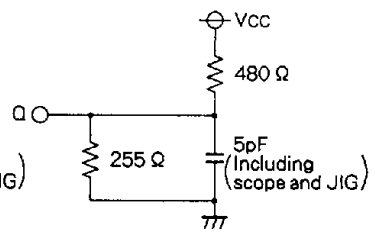


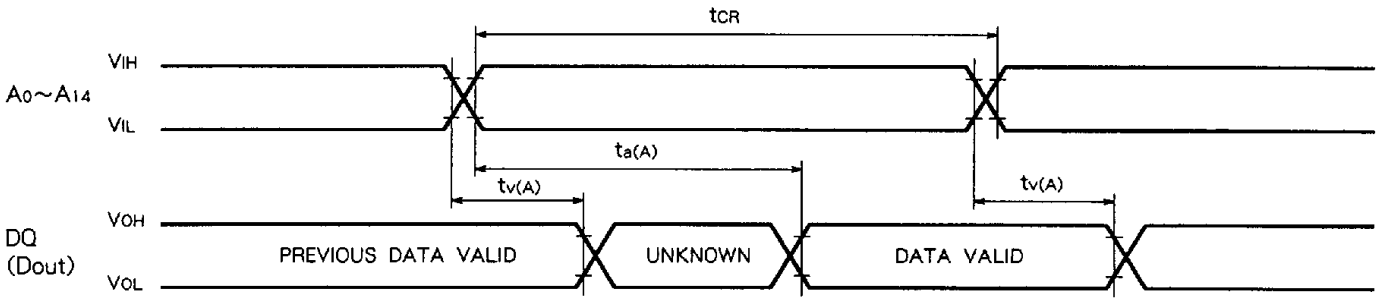
Fig. 2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M5279-20		M5M5279-25,-25L		M5M5279-35,-35L		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	20		25		35		ns
$t_{a(A)}$	Address access time		20		25		35	ns
$t_{a(S1)}$	Chip select 1 access time		20		25		35	ns
$t_{a(S2)}$	Chip select 2 access time		17		22		27	ns
$t_{a(OE)}$	Output enable access time		10		12		15	ns
$t_{v(A)}$	Data valid time after address change	3		5		5		ns
$t_{en(S1)}$	Output enable time after $\overline{S_1}$ low	3		5		5		ns
$t_{en(S2)}$	Output enable time after S_2 high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{dis(S1)}$	Output disable time after $\overline{S_1}$ high	0	8	0	10	0	10	ns
$t_{dis(S2)}$	Output disable time after S_2 low	0	8	0	10	0	10	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	8	0	10	0	10	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		20		25		35	ns

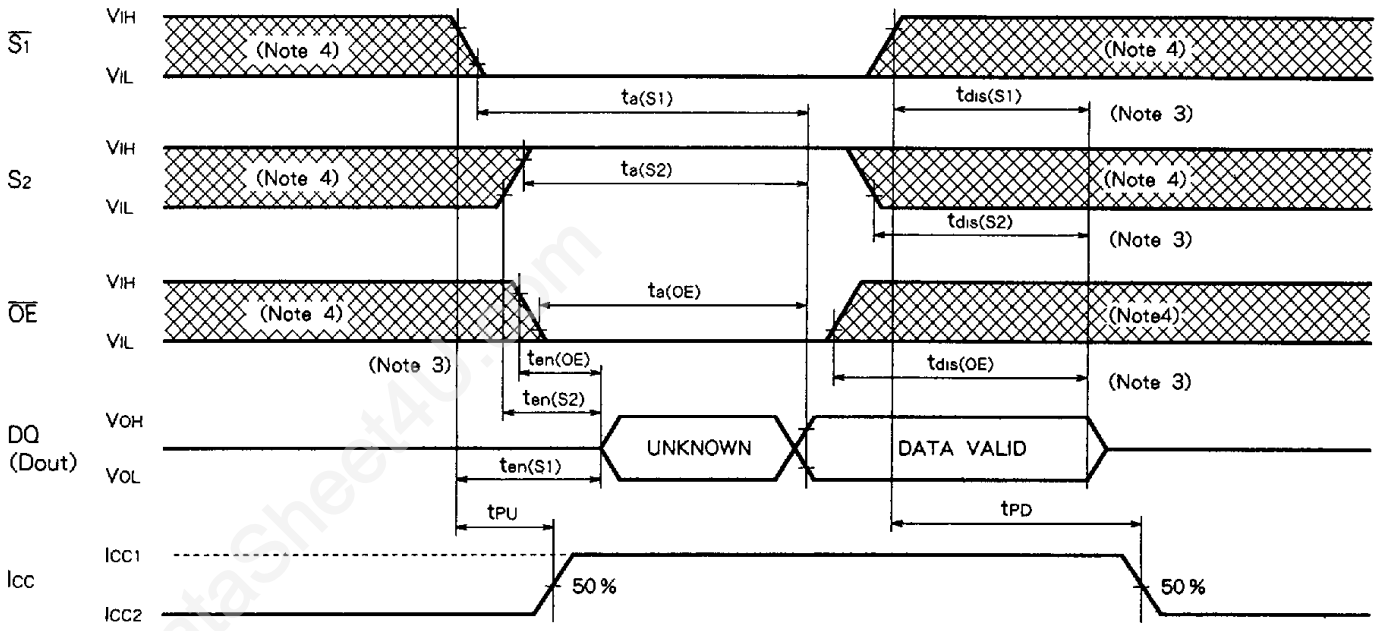
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{W}$ = H $\overline{S_1}$ = L S_2 = H $\overline{OE}$ = L

Read cycle 2 (Note 2)



$\overline{W}$ = H

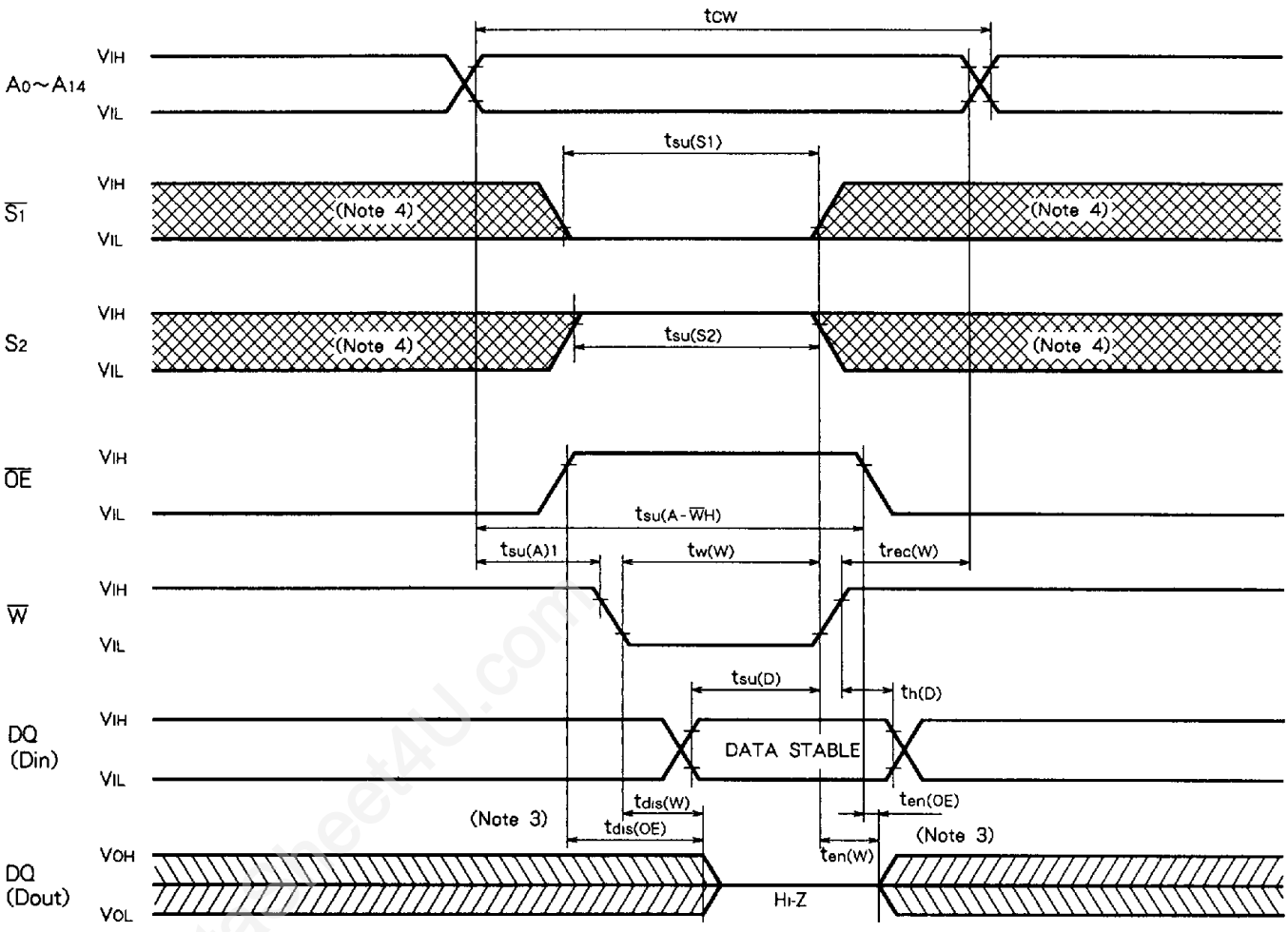
Note 2. Addresses valid prior to or coincident with $\overline{S_1}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.
4. Hatching indicates the state is don't care.

(4) WRITE CYCLE

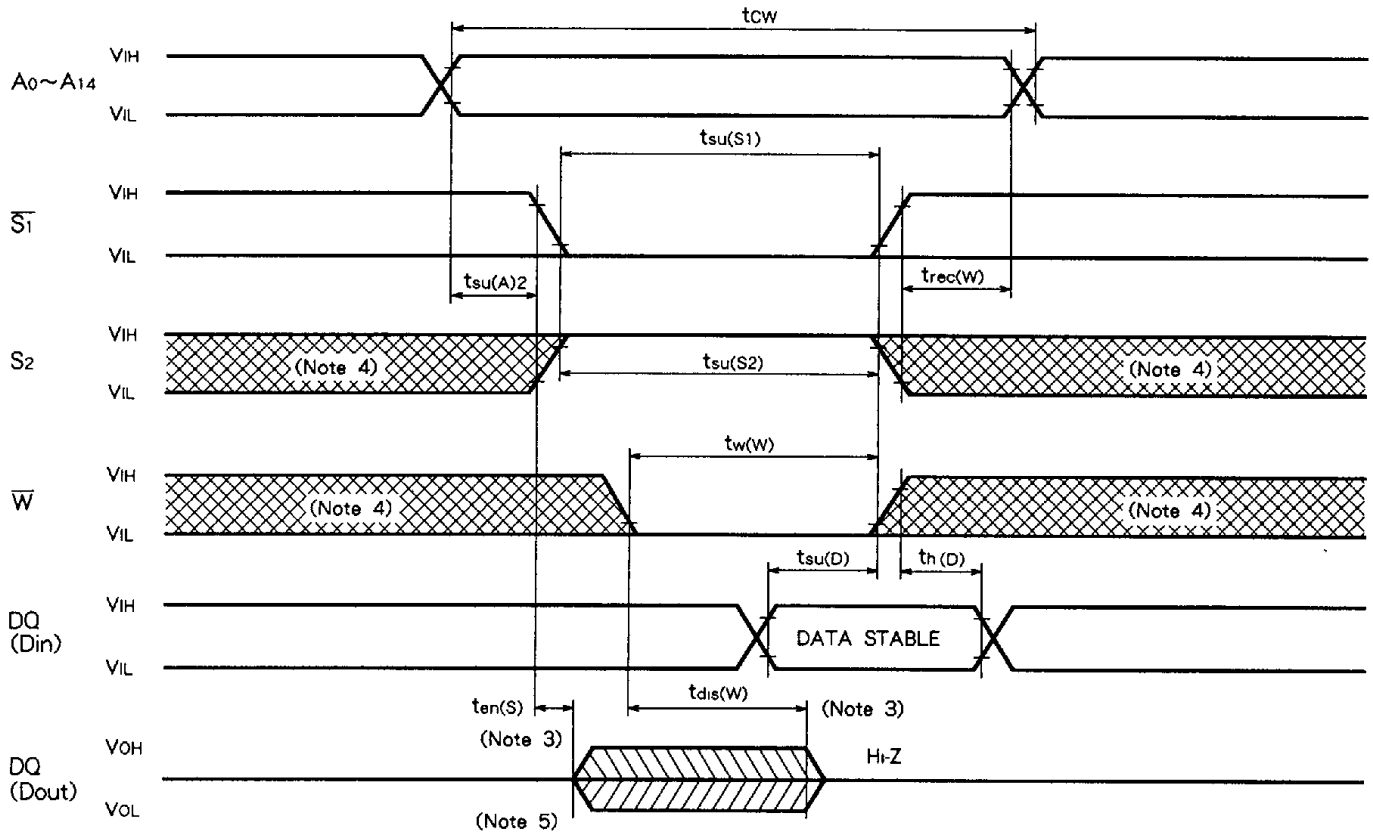
Symbol	Parameter	Limits						Unit
		M5M5279-20		M5M5279-25,-25L		M5M5279-35,-35L		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	20		25		35		ns
$t_{su(S1)}$	Chip select 1 setup time	15		20		30		ns
$t_{su(S2)}$	Chip select 2 setup time	15		20		30		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S1}$, S2)	0		0		0		ns
$t_{w(W)}$	Write pulse width	15		20		25		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	8		10		15		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time after $\overline{W}$ low	0	8	0	10	0	10	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0	8	0	10	0	10	ns
$t_{en(W)}$	Output enable time after $\overline{W}$ high	0		0		0		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0		0		0		ns
$t_{su(A-\overline{WH})}$	Address to $\overline{W}$ high	15		20		30		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S_1}$, S_2 control mode)



Note 5 When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S_1}$ S_2,the output is maintained in the high impedance.

POWER DOWN CHARACTERISTICS (Ta = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
$V_{CC(PD)}$	Power down supply voltage	$V_{I(\overline{S})} \geq V_{CC} - 0.2V$ $V_I \geq V_{CC} - 0.2V$ or $0V \leq V_I \leq 0.2V$		2			V
$V_{I(\overline{S})}$	Chip select input voltage			$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time			0			ns
$t_{rec(PD)}$	Power down recovery time		-25L	25			ns
			-35L	35			
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3.0V				50	μA
		V_{CC} = 5.5V				100	

Note 6. This is only M5M5279P, J-25L, -35L

TIMING WAVEFORM FOR POWER DOWN