*Preliminary*
*Notice: This is not final specification.*
*Some parametric limits are subject to change.*

# M5M5T5672TG – 20

**18874368-BIT(262144-WORD BY 72-BIT) NETWORK SRAM**

## DESCRIPTION

The M5M5T5672TG is a family of 18M bit synchronous SRAMs organized as 262144-words by 72-bit. It is designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Renesas's SRAMs are fabricated with high performance, low power CMOS technology, providing greater reliability. M5M5T5672TG operates on a single 2.5V power supply and are 2.5V CMOS compatible.

## FEATURES

- **Fully registered inputs and outputs for pipelined operation**
- **Fast clock speed: 200 MHz**
- **Fast access time: 3.2 ns**
- **Single 2.5V –5% and +5% power supply $V_{DD}$**
- **Individual byte write (BWa# - BWh#) controls may be tied LOW**
- **Single Read/Write control pin (W#)**
- **Snooze mode (ZZ) for power down**
- **Linear or Interleaved Burst Modes**
- **JTAG boundary scan support**

## APPLICATION

High-end networking products that require high bandwidth, such as switches and routers.

## FUNCTION

Synchronous circuitry allows for precise cycle control triggered by a positive edge clock transition.

Synchronous signals include : all Addresses, all Data Inputs, all Chip Enables (E1#, E2, E3#), Address Advance/Load (ADV), Byte Write Enables (BWa#, BWb#, BWc#, BWd#, BWe#, BWf#, BWg#, BWh#) and Read/Write (W#).

Write operations are controlled by the eight Byte Write Enables (BWa# - BWh#) and Read/Write(W#) inputs. All writes are conducted with on-chip synchronous self-timed write circuitry.

Asynchronous inputs include Output Enable (G#), Clock (CLK) and Snooze Enable (ZZ).

The HIGH input of ZZ pin puts the SRAM in the power-down state.

The Linear Burst order (LBO#) is DC operated pin. LBO# pin will allow the choice of either an interleaved burst, or a linear burst.

All read, write and deselect cycles are initiated by the ADV Low input. Subsequent burst address can be internally generated as controlled by the ADV HIGH input.

## PACKAGE

| | Bump | Body Size | Bump Pitch |
|---|---|---|---|
| M5M5T5672TG | 209(11X19) bump BGA | 14mm X 22mm | 1mm |

## PART NAME TABLE

| Part Name | Access | Cycle | Active Current (max.) | Standby Current (max.) |
|---|---|---|---|---|
| M5M5T5672TG -20 | 3.2ns | 5.0ns | 450mA | 30mA |

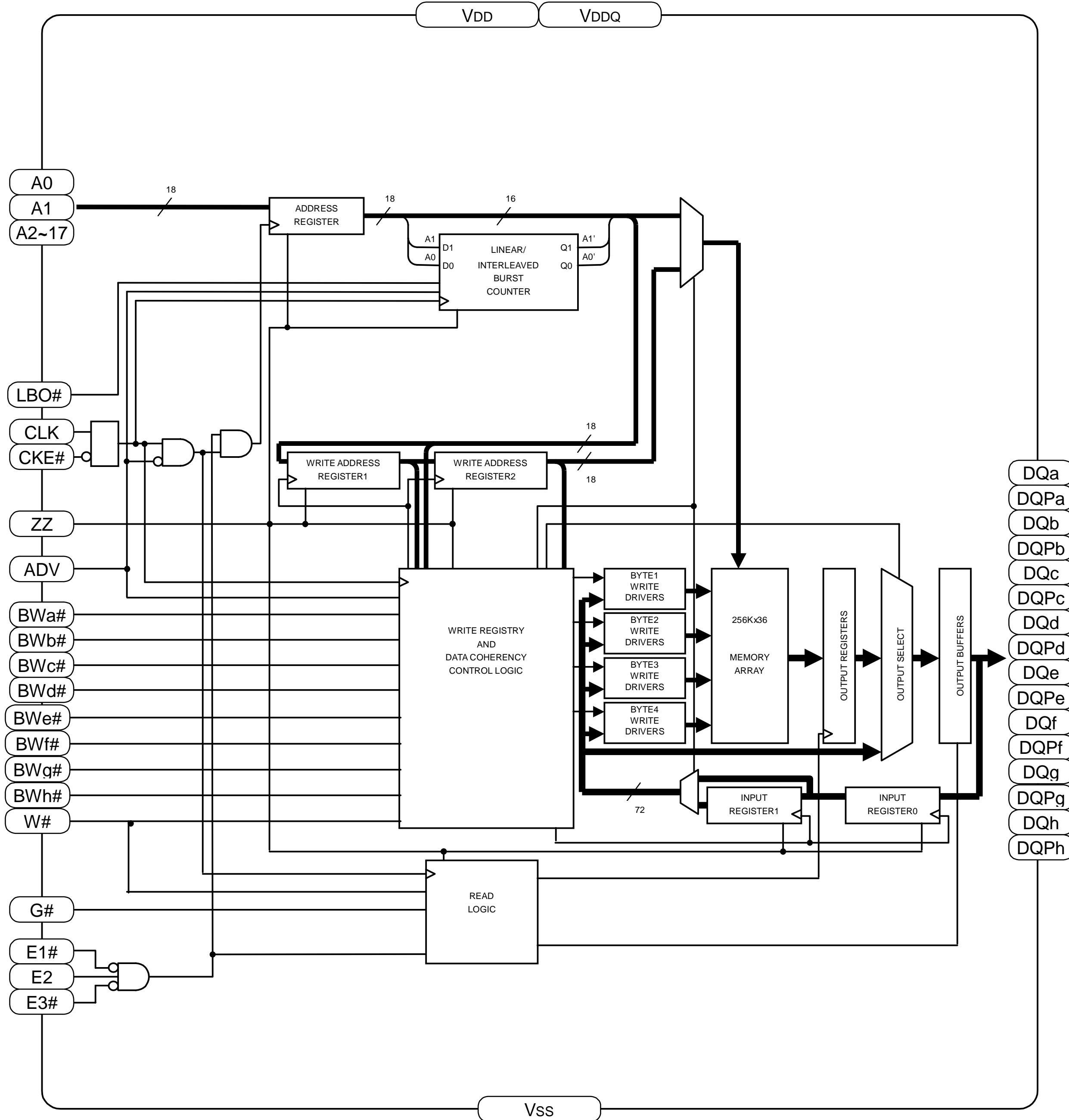
## BUMP LAYOUT(TOP VIEW)

**209 bump BGA**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DQg | DQg | A6 | E2 | A7 | ADV | A8 | E3# | A9 | DQb | DQb |
| B | DQg | DQg | BWc# | BWg# | NC | W# | A17 | BWb# | BWf# | DQb | DQb |
| C | DQg | DQg | BWh# | BWd# | NC | E1# | NC | BWe# | BWa# | DQb | DQb |
| D | DQg | DQg | Vss | NC | NC | G# | NC | NC | Vss | DQb | DQb |
| E | DQPg | DQPc | VDDQ | VDDQ | VDD | VDD | VDD | VDDQ | VDDQ | DQPf | DQPb |
| F | DQc | DQc | Vss | Vss | Vss | NC | Vss | Vss | Vss | DQf | DQf |
| G | DQc | DQc | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQf | DQf |
| H | DQc | DQc | Vss | Vss | Vss | NC | Vss | Vss | Vss | DQf | DQf |
| J | DQc | DQc | VDDQ | VDDQ | VDD | MCH | VDD | VDDQ | VDDQ | DQf | DQf |
| K | NC | NC | CLK | NC | Vss | CKE# | Vss | NC | NC | NC | NC |
| L | DQh | DQh | VDDQ | VDDQ | VDD | MCH | VDD | VDDQ | VDDQ | DQa | DQa |
| M | DQh | DQh | Vss | Vss | Vss | MCH | Vss | Vss | Vss | DQa | DQa |
| N | DQh | DQh | VDDQ | VDDQ | VDD | NC | VDD | VDDQ | VDDQ | DQa | DQa |
| P | DQh | DQh | Vss | Vss | Vss | ZZ | Vss | Vss | Vss | DQa | DQa |
| R | DQPd | DQPh | VDDQ | VDDQ | VDD | VDD | VDD | VDDQ | VDDQ | DQPa | DQPe |
| T | DQd | DQd | Vss | NC | NC | LBO# | NC | NC | Vss | DQe | DQe |
| U | DQd | DQd | NC | A3 | NC | A15 | NC | A11 | NC | DQe | DQe |
| V | DQd | DQd | A5 | A4 | A16 | A1 | A13 | A12 | A10 | DQe | DQe |
| W | DQd | DQd | TMS | TDI | A2 | A0 | A14 | TDO | TCK | DQe | DQe |

Note1. MCH means “Must Connect High”. MCH should be connected to HIGH.

## BLOCK DIAGRAM




Note2. The BLOCK DIAGRAM does not include the Boundary Scan logic. See Boundary Scan chapter.
Note3. The BLOCK DIAGRAM illustrates simplified device operation. See TRUTH TABLE, PIN FUNCTION and timing diagrams for detailed information.

## PIN FUNCTION

| Pin | Name | Function |
|---|---|---|
| **A0~A17** | Synchronous Address Inputs | These inputs are registered and must meet the setup and hold times around the rising edge of CLK. A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired. |
| **BWa#, BWb#, BWc#, BWd#, Bwe#, BWf#, BWg#, BWh#** | Synchronous Byte Write Enables | These active LOW inputs allow individual bytes to be written when a WRITE cycle is active and must meet the setup and hold times around the rising edge of CLK. BYTE WRITEs need to be asserted on the same cycle as the address. BWs are associated with addresses and apply to subsequent data. BWa# controls DQa, DQPa pins; BWb# controls DQb, DQPb pins; BWc# controls DQc, DQPc pins; BWd# controls DQd, DQPd pins; BWe# controls DQe, DQPe pins; BWf# controls DQf, DQPf pins; BWg# controls DQg, DQPg pins; BWh# controls DQh, DQPh pins. |
| **CLK** | Clock Input | This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge.<br>All synchronous inputs must meet setup and hold times around the clock's rising edge. |
| **E1#** | Synchronous Chip Enable | This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). |
| **E2** | Synchronous Chip Enable | This active HIGH input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion. |
| **E3#** | Synchronous Chip Enable | This active LOW input is used to enable the device and is sampled only when a new external address is loaded (ADV is LOW). This input can be used for memory depth expansion. |
| **CKE#** | Synchronous Clock Enable | This active LOW input permits CLK to propagate throughout the device. When HIGH, the device ignores the CLK input and effectively internally extends the previous CLK cycle. This input must meet setup and hold times around the rising edge of CLK. |
| **G#** | Output Enable | This active LOW asynchronous input enable the data I/O output drivers. |
| **ADV** | Synchronous Address Advance/Load | When HIGH, this input is used to advance the internal burst counter, controlling burst access after the external address is loaded. When HIGH, W# is ignored. A LOW on this pin permits a new address to be loaded at CLK rising edge. |
| **ZZ** | Snooze Enable | This active HIGH asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When active, all other inputs are ignored. When this pin is LOW or NC, the SRAM normally operates. |
| **W#** | Synchronous Read/Write | This active input determines the cycle type when ADV is LOW. This is the only means for determining READs and WRITEs. READ cycles may not be converted into WRITEs (and vice versa) other than by loading a new address. A LOW on the pin permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK. Full bus width WRITEs occur if all byte write enables are LOW. |
| **DQa,DQPa,DQb,DQPb, DQc,DQPc,DQd,DQPd, DQe,DQPe,DQf,DQPf, DQg,DQPg,DQh,DQPh** | Synchronous Data I/O | Byte “a” is DQa , DQPa pins; Byte “b” is DQb, DQPb pins; Byte “c” is DQc, DQPc pins; Byte “d” is DQd,DQPd pins; Byte “e” is DQe, DQPe pins; Byte “f” is DQf, DQPf pins; Byte “g” is DQg, DQPg pins; Byte “h” is DQh, DQPh pins. Input data must meet setup and hold times around CLK rising edge. |
| **LBO#** | Burst Mode Control | This DC operated pin allows the choice of either an interleaved burst or a linear burst. If this pin is HIGH or NC, an interleaved burst occurs. When this pin is LOW, a linear burst occurs, and input leak current to this pin. |
| **VDD** | VDD | Core Power Supply |
| **Vss** | Vss | Ground |
| **VDDQ** | VDDQ | I/O buffer Power supply |
| **TDI** | Test Data Input | These pins are used for Boundary Scan Test. |
| **TDO** | Test Data Output | |
| **TCK** | Test Clock | |
| **TMS** | Test Mode Select | |
| **NC** | No Connect | These pins are not internally connected and may be connected to ground. |

## DC OPERATED TRUTH TABLE

| Name | Input Status | Operation |
|---|---|---|
| LBO# | HIGH or NC | Interleaved Burst Sequence |
| | LOW | Linear Burst Sequence |

Note4. LBO# is DC operated pin.
Note5. NC means No Connection.
Note6. See BURST SEQUENCE TABLE about interleaved and Linear Burst Sequence.

## BURST SEQUENCE TABLE

(1) Interleaved Burst Sequence (when LBO# = HIGH or NC)

| Operation | A17~A2 | A1,A0 | | | |
|---|---|---|---|---|---|
| First access, latch external address | A17~A2 | 0 , 0 | 0 , 1 | 1 , 0 | 1 , 1 |
| Second access(first burst address) | latched A17~A2 | 0 , 1 | 0 , 0 | 1 , 1 | 1 , 0 |
| Third access(second burst address) | latched A17~A2 | 1 , 0 | 1 , 1 | 0 , 0 | 0 , 1 |
| Fourth access(third burst address) | latched A17~A2 | 1 , 1 | 1 , 0 | 0 , 1 | 0 , 0 |

(2) Linear Burst Sequence (when LBO# = LOW)

| Operation | A17~A2 | A1,A0 | | | |
|---|---|---|---|---|---|
| First access, latch external address | A17~A2 | 0 , 0 | 0 , 1 | 1 , 0 | 1 , 1 |
| Second access(first burst address) | latched A17~A2 | 0 , 1 | 1 , 0 | 1 , 1 | 0 , 0 |
| Third access(second burst address) | latched A17~A2 | 1 , 0 | 1 , 1 | 0 , 0 | 0 , 1 |
| Fourth access(third burst address) | latched A17~A2 | 1 , 1 | 0 , 0 | 0 , 1 | 1 , 0 |

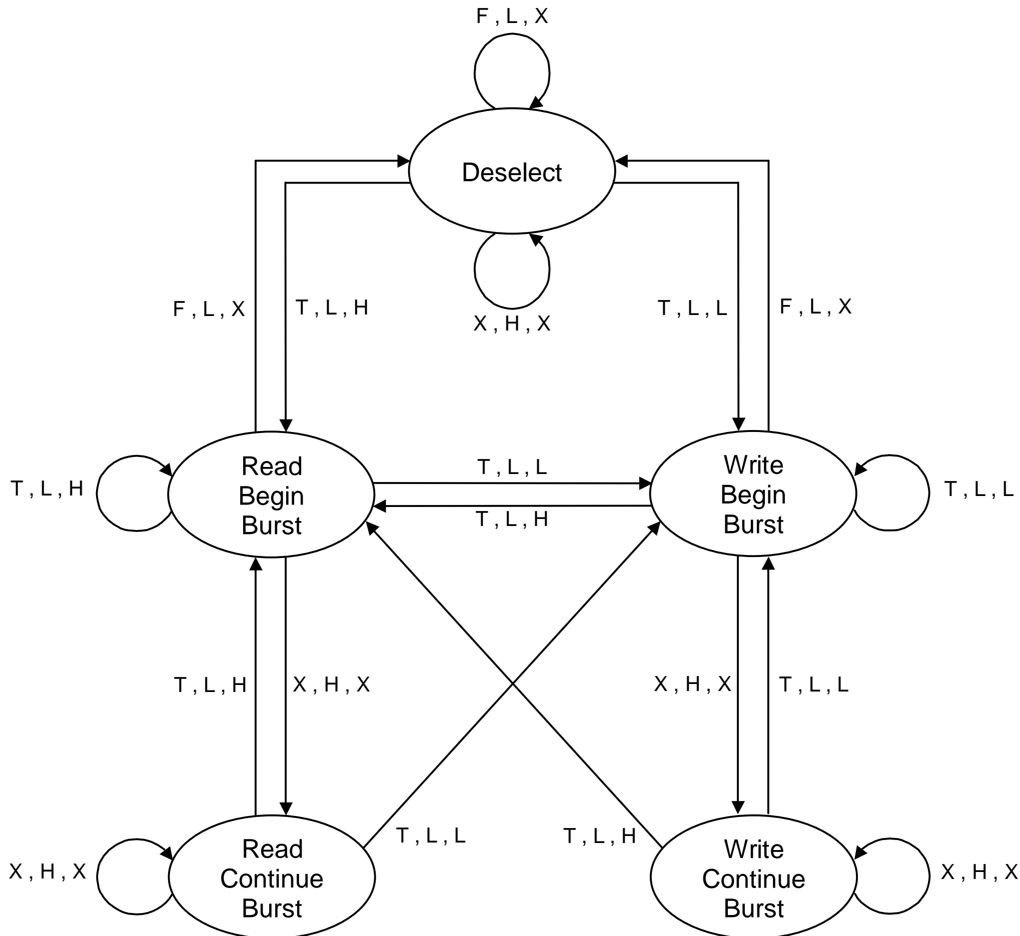
Note7. The burst sequence wraps around to its initial state upon completion.

## TRUTH TABLE

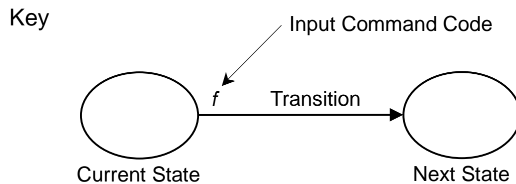
| E1# | E2 | E3# | ADV | W# | BWx# | G# | CKE# | ZZ# | CLK | Address used | Operation |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | X | X | L | X | X | X | L | L | L->H | None | Deselect Cycle |
| X | L | X | L | X | X | X | L | L | L->H | None | Deselect Cycle |
| X | X | H | L | X | X | X | L | L | L->H | None | Deselect Cycle |
| X | X | X | H | X | X | X | L | L | L->H | None | Continue Deselect Cycle |
| L | H | L | L | H | X | L | L | L | L->H | External | Read Cycle, Begin Burst |
| X | X | X | H | X | X | L | L | L | L->H | Next | Read Cycle, Continue Burst |
| L | H | L | L | H | X | H | L | L | L->H | External | NOP/Dummy Read, Begin Burst |
| X | X | X | H | X | X | H | L | L | L->H | Next | Dummy Read, Continue Burst |
| L | H | L | L | L | L | X | L | L | L->H | External | Write Cycle, Begin Burst |
| X | X | X | H | X | L | X | L | L | L->H | Next | Write Cycle, Continue Burst |
| L | H | L | L | L | H | X | L | L | L->H | None | NOP/Write Abort, Begin Burst |
| X | X | X | H | X | H | X | L | L | L->H | Next | Write Abort, Continue Burst |
| X | X | X | X | X | X | X | H | L | L->H | Current | Ignore Clock edge, Stall |
| X | X | X | X | X | X | X | X | H | X | None | Snooze Mode |

Note8. “H” = input VIH; “L” = input VIL; “X” = input VIH or VIL.
Note9. BWx#=H means all Synchronous Byte Write Enables (BWa#,BWb#,BWc#,BWd#) are HIGH. BWx#=L means one or more Synchronous Byte Write Enables are LOW.
Note10. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

## STATE DIAGRAM




Key




Note11. The notation "x , x , x" controlling the state transitions above indicate the state of inputs E, ADV and W# respectively.
Note12. If (E1# = L and E2 = H and E3# = L) then E="T" else E="F".
Note13. “H” = input VIH; “L” = input VIL; “X” = input VIH or VIL; “T” = input “true”; “F” = input “false”.

## WRITE TRUTH TABLE

| W# | BWa# | BWb# | BWc# | BWd# | BWe# | BWf# | BWg# | BWh# | Function |
|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | X | X | X | Read |
| L | L | H | H | H | H | H | H | H | Write Byte “a” |
| L | H | L | H | H | H | H | H | H | Write Byte “b” |
| L | H | H | L | H | H | H | H | H | Write Byte “c” |
| L | H | H | H | L | H | H | H | H | Write Byte “d” |
| L | H | H | H | H | L | H | H | H | Write Byte “e” |
| L | H | H | H | H | H | L | H | H | Write Byte “f” |
| L | H | H | H | H | H | H | L | H | Write Byte “g” |
| L | H | H | H | H | H | H | H | L | Write Byte “h” |
| L | L | L | L | L | L | L | L | L | Write All Bytes |
| L | H | H | H | H | H | H | H | H | Write Abort / NOP |

Note14. “H” = input VIH; “L” = input VIL; “X” = input VIH or VIL.
Note15. All inputs must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| VDD | Power Supply Voltage | With respect to Vss | -1.0*~3.6 | V |
| VDDQ | I/O Buffer Power Supply Voltage | | -1.0*~3.6 | V |
| VI | Input Voltage | | -1.0~VDDQ+1.0 ** | V |
| VO | Output Voltage | | -1.0~VDDQ+1.0 ** | V |
| PD | Maximum Power Dissipation (VDD) | | 1050 | mW |
| TOPR | Operating Temperature | | 0~70 | °C |
| TSTG(bias) | Storage Temperature(bias) | | -10~85 | °C |
| TSTG | Storage Temperature | | -55~125 | °C |

Note16. * This is -1.0V when pulse width≤2ns, and -0.5V in case of DC.
** This is -1.0V~VDDQ+1.0V when pulse width≤2ns, and –0.5V~VDDQ+0.5V in case of DC.

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $V_{DD}$ | Power Supply Voltage | | 2.375 | 2.625 | V |
| $V_{DDQ}$ | I/O Buffer Power Supply Voltage | | 2.375 | 2.625 | V |
| $V_{IH}$ | High-level Input Voltage | | 1.7 | $V_{DDQ}$+0.3* | V |
| $V_{IL}$ | Low-level Input Voltage | | -0.3* | 0.7 | V |
| $V_{OH}$ | High-level Output Voltage | $I_{OH}$ = -2.0mA | $V_{DDQ}$-0.4 | | V |
| $V_{OL}$ | Low-level Output Voltage | $I_{OL}$ = 2.0mA | | 0.4 | V |
| $I_{LI}$ | Input Leakage Current except ZZ and LBO# | $V_I$ = 0V ~ $V_{DDQ}$ | | 10 | μA |
| | Input Leakage Current of LBO# | $V_I$ = 0V ~ $V_{DDQ}$ | | 100 | |
| | Input Leakage Current of ZZ | $V_I$ = 0V ~ $V_{DDQ}$ | | 100 | |
| $I_{LO}$ | Output Leakage Current | $V_{I/O}$ = 0V ~ $V_{DDQ}$ | | 10 | μA |
| $I_{CC1}$ | Power Supply Current : Operating | Device selected; Output Open, $V_I \le V_{IL}$ or $V_I \ge V_{IH}$, ZZ$\le V_{IL}$ | | 450 | mA |
| $I_{CC2}$ | Power Supply Current : Deselected | Device deselected $V_I \le V_{IL}$ or $V_I \ge V_{IH}$, ZZ$\le V_{IL}$ | | 180 | mA |
| $I_{CC3}$ | CMOS Standby Current (CLK stopped standby mode) | Device deselected; Output Open $V_I \le V_{SS}$+0.2V or $V_I \ge V_{DDQ}$-0.2V CLK frequency=0Hz, All inputs static | | 30 | mA |
| $I_{CC4}$ | Snooze Mode Standby Current | Snooze mode ZZ$\ge V_{DDQ}$-0.2V, LBO#$\ge V_{DD}$-0.2V | | 30 | mA |
| $I_{CC5}$ | Stall Current | Device selected; Output Open, CKE#$\ge V_{IH}$ $V_I \le V_{SS}$+0.2V or $V_I \ge V_{DDQ}$-0.2V | | 140 | mA |

Note17.*$V_{ILmin}$ is –1.0V and $V_{IH\ max}$ is $V_{DDQ}$+1.0V in case of AC(Pulse width≤2ns).
Note18."Device Deselected" means device is in power-down mode as defined in the truth table.

## CAPACITANCE

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $C_I$ | Input Capacitance | $V_I$=GND, $V_I$=25mVrms, f=1MHz | | | 6 | pF |
| $C_O$ | Input / Output (DQ) Capacitance | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 8 | pF |

Note19. This parameter is sampled.

## THERMAL RESISTANCE

### 4-Layer PC board mounted (70x70x1.6mmT)

| Symbol | Parameter | Condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $\theta_{JA}$ | Thermal resistance Junction Ambient | Air velocity=0m/sec | | 26 | | °C/W |
| | | Air velocity=2m/sec | | 18 | | °C/W |
| $\theta_{JC}$ | Thermal resistance Junction to Case | | | 6 | | °C/W |

## AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, $V_{DD}$=$V_{DDQ}$=2.375~2.625V, unless otherwise noted)

### (1) MEASUREMENT CONDITION

Input pulse levels ........................................ $V_{IH}$=$V_{DDQ}$, $V_{IL}$=0V
Input rise and fall times ................................ faster than or equal to 1V/ns
Input timing reference levels ........................ $V_{IH}$=$V_{IL}$=$V_{DDQ}$ / 2
Output reference levels ................................ $V_{IH}$=$V_{IL}$=$V_{DDQ}$ / 2
Output load ................................................... Fig.1

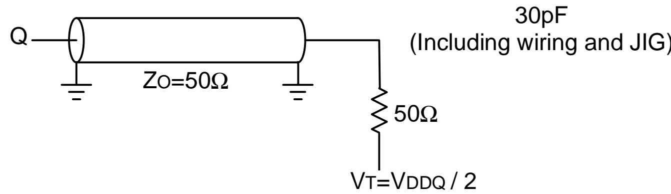



Fig.1 Output load

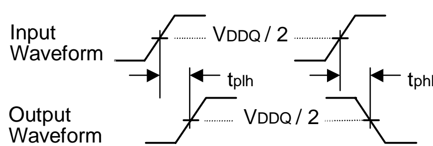



Fig.2 Tdly measurement

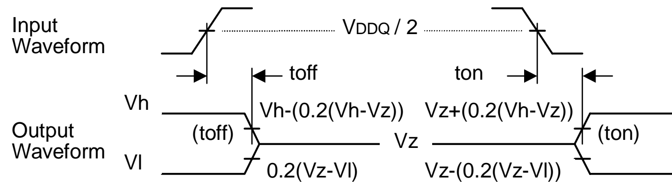



Fig.3 Tri-State measurement

Note20.Valid Delay Measurement is made from the $V_{DDQ}$/2 on the input waveform to the $V_{DDQ}$/2 on the output waveform.
Input waveform should have a slew rate of faster than or equal to 1V/ns.
Note21.Tri-state toff measurement is made from the $V_{DDQ}$/2 on the input waveform to the output waveform moving 20% from its initial to final Value $V_{DDQ}$/2.
Note:the initial value is not $V_{OL}$ or $V_{OH}$ as specified in DC ELECTRICAL CHARACTERISTICS table.
Note22. Tri-state ton measurement is made from the $V_{DDQ}$/2 on the input waveform to the output waveform moving 20% from its initial Value $V_{DDQ}$/2 to its final Value.
Note:the final value is not $V_{OL}$ or $V_{OH}$ as specified in DC ELECTRICAL CHARACTERISTICS table.
Note23.Clocks,Data,Address and control signals will be tested with a minimum input slew rate of faster than or equal to 1V/ns.

## (2)TIMING CHARACTERISTICS

| Symbol | Parameter | Limits 200MHz -20 Min | Max | Unit |
|---|---|---|---|---|
| Clock | | | | |
| tKHKH | Clock Cycle Time | 5.0 | | ns |
| tKHKL | Clock HIGH Time | 2.0 | | ns |
| tKLKH | Clock LOW Time | 2.0 | | ns |
| Output times | | | | |
| tKHQV | Clock HIGH to Output Valid | | 3.2 | ns |
| tKHQX | Clock HIGH to Output Invalid | 1.5 | | ns |
| tKHQX1 | Clock HIGH to Output in Low-Z | 1.5 | | ns |
| tKHQZ | Clock HIGH to Output in High-Z | 1.5 | 3.2 | ns |
| tGLQV | G# to output valid | | 3.2 | ns |
| tGLQX1 | G# to output in Low-Z | 0.0 | | ns |
| tGHQZ | G# to output in High-Z | | 3.2 | ns |
| Setup Times | | | | |
| tAVKH | Address Valid to Clock HIGH | 1.0 | | ns |
| tadvVKH | ADV Valid to Clock HIGH | 1.0 | | ns |
| tWVKH | Write Valid to Clock HIGH | 1.0 | | ns |
| tBxVKH | Byte Write Valid to Clock HIGH (BWa#~BWh#) | 1.0 | | ns |
| tEVKH | Enable Valid to Clock HIGH (E1#,E2,E3#) | 1.0 | | ns |
| tDVKH | Data In Valid Clock HIGH | 1.0 | | ns |
| Hold Times | | | | |
| tKHAX | Clock HIGH to Address don't care | 0.8 | | ns |
| tKHadvX | Clock HIGH to ADV don't care | 0.8 | | ns |
| tKHWX | Clock HIGH to Write don't care | 0.8 | | ns |
| tKHBxX | Clock HIGH to Byte Write don't care (BWa#~BWh#) | 0.8 | | ns |
| tKHEX | Clock HIGH to Enable don't care (E1#,E2,E3#) | 0.8 | | ns |
| tKHDX | Clock HIGH to Data In don't care | 0.8 | | ns |
| ZZ | | | | |
| tZZS | ZZ standby | | 2*tKHKH | ns |
| tZZREC | ZZ recovery | | 2*tKHKH | ns |

Note24.All parameter except tZZS, tZZREC in this table are measured on condition that ZZ=LOW fix.
Note25.Test conditions is specified with the output loading shown in Fig.1 unless otherwise noted.
Note26. tKHQX1, tKHQZ, tGLQX1, tGHQZ are sampled.
Note27.LBO# is static and must not change during normal operation.

**(3)READ TIMING**

CLK CKE# E# ADV W# BWx# ADD DQ G#

tKHKH tKHKL tKLKH tckeVKH tKHckeX tEVKH tKHEX tadvVKH tKHadvX tWVKH tKHWX tAVKH tKHAX tKHQX1 tKHQV tKHQX tGLQV tGHQZ tGLQX1 tKHQZ

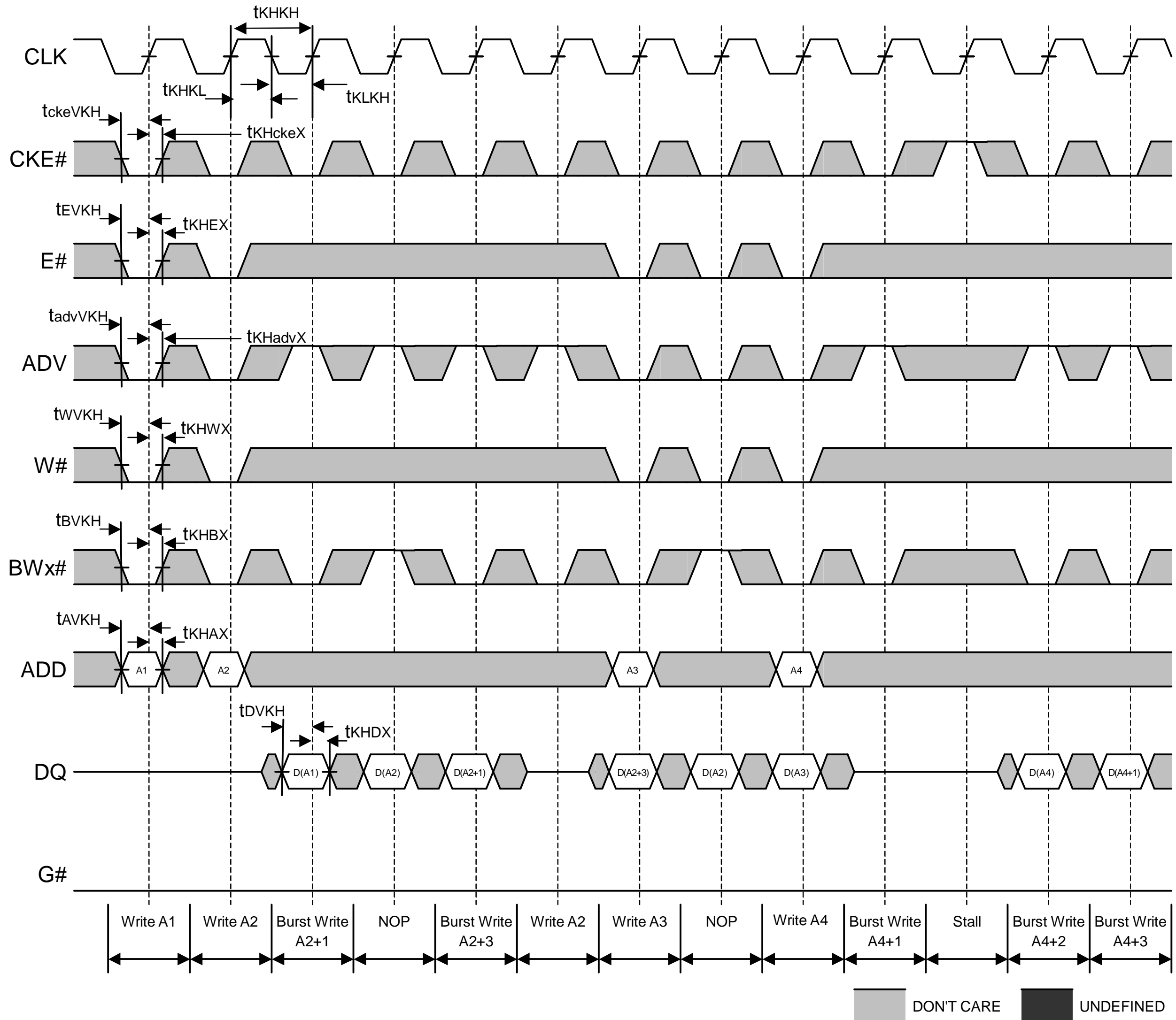
A1 A2 A3 Q(A1) Q(A2) Q(A2+1) Q(A2+2) Q(A2+3) Q(A2) Q(A3) Q(A3+1)

Read A1 | Read A2 | Burst Read A2+1 | Stall | Burst Read A2+2 | Burst Read A2+3 | Burst Read A2 | Deselect | Continue Deselect | Read A3 | Burst Read A3+1 | Burst Read A3+2 | Burst Read A3+3

DON'T CARE UNDEFINED

Note28.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note29. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note30.ZZ is fixed LOW.

## (4)WRITE TIMING




Note31.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note32. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note33.ZZ is fixed LOW.

## (5)READ/WRITE TIMING

CLK
CKE#
E#
ADV
W#
BWx#
ADD
DQ
G#

tKHKH, tKHKL, tKLKH, tckeVKH, tKHckeX, tEVKH, tKHEX, tadvVKH, tKHadvX, tWVKH, tKHWX, tBVKH, tKHBX, tAVKH, tKHAX, tKHQX1, tDVKH, tKHDX, tKHQV, tKHQV

A1 A2 A2 A3 A3 A4 A5

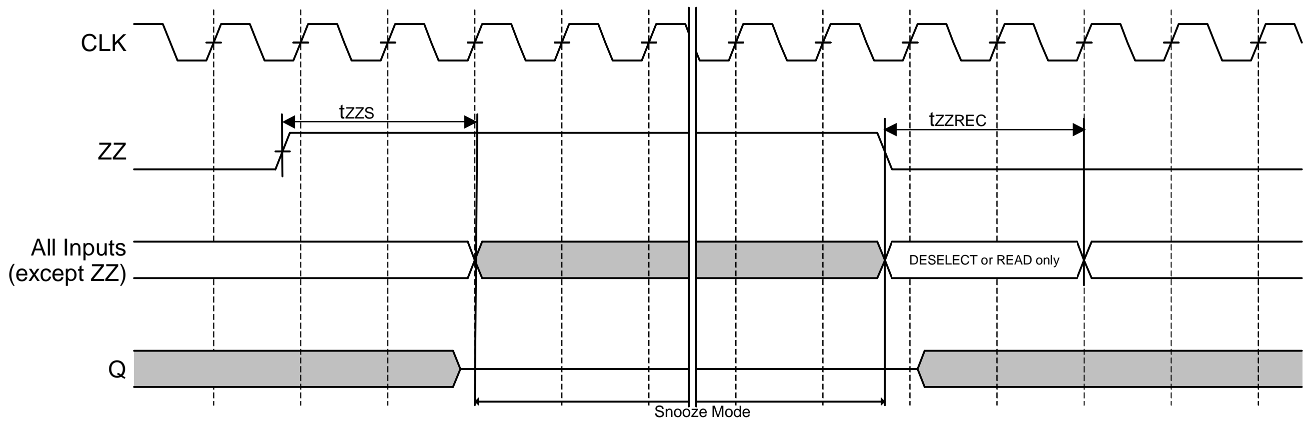
Q(A1) D(A2) Q(A2) D(A3) D(A3+1) Q(A3) Q(A3+1) D(A4) Q(A5)

Read A1 | Write A2 | Read A2 | Write A3 | Burst Write A3+1 | Read A3 | Burst Read A3+1 | Deselect | Write A4 | Stall | Read A5 | Burst Read A5+1 | Burst Read A5+2

DON'T CARE
UNDEFINED

Note34.Q(An) refers to output from address An. Q(An+1) refers to output from the next internal burst address following An.
Note35. E# represents three signals. When E# is LOW, it represents E1# is LOW, E2 is HIGH and E3# is LOW.
Note36.ZZ is fixed LOW.

## (6)SNOOZE MODE TIMING



## JTAG PORT OPERATION

### Overview

The JTAG Port on this SRAM operates in a manner consistent with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG), but dose not implement all of the function required for 1149.1 compliance. Unlike JTAG implementations that have been common among SRAM vendors for the last several years, this implementation dose offer a form of EXTEST, known as Clock Assisted EXTEST, reducing or eliminating the "hand coding" that has been required to overcome the test program compiler errors caused by previous non-compliant implementation. The JTAG Port interfaces with conventional CMOS logic level signaling.

### Disabling the JTAG port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. To assure normal operation of the SRAM with the JTAG Port unused, the TCK, TDI and TMS pins may be left floating or tied to High. The TDO pin should be left unconnected.

### JTAG Pin Description

| Pin | Name | Function |
|---|---|---|
| **TCK** | Test Clock | The TCK input is clock for all TAP events. All inputs are captured on the rising edge of TCK and the Test Data Out (TDO) propagates from the falling edge of TCK. |
| **TMS** | Test Mode Select | The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP Controller state machine. An undriven TMS input will produce the same result as a logic one input level. |
| **TDI** | Test Data In | The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between the TDI and TDO pins. the register placed between the TDI and TDO pins is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Resister (refer to the TAP Controller State Diagram). An undriven TDI Input will produce the same result as a logic one input level. |
| **TDO** | Test Data Out | The TDO output is active depending on the state of the TAP Controller state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between the TDI and TDO pins. |

**Note:**
This device dose not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

### JTAG Port Registers

#### Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequence of 1s and 0s applied to TMS as TCK is strobed. Each of TAP Registers are serial shift registers that capture serial input data on the rising edge of TCK and push serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

#### Instruction Register

The Instruction Register holds the instructions that are executed by the TAP Controller when it is moved into the Run-Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Resister can be loaded when it is placed between the TDI and TDO pins. The Instruction Resister is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in the Test-Logic-Reset state.

**Bypass Register**
The Bypass resister is a single-bit register that can be placed between the TDI and TDO pins. It allows serial test data to be passed through the SRAM's JTAG Port to another device in the scan chain with as little delay as possible.

**Boundary Scan Register**
The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the SRAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pins. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the SRAM's I/O ring when the controller is in the Capture-RD state and then is placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instruction can be used to activate the Boundary Scan Register.

**Identification (ID) Register**
The ID register is a 32-bit register that is loaded with a device and vender specific 32-bit code when the controllers put in the Capture-DR state with the IDCODE Instruction loaded in the Instruction Register. The code is loaded from 32-bit on-chip ROM. It describes various attributes of the SRAM (see page 25). The register is then placed between the TDI and TDO pins when the controller is moved into the Shift-DR state. Bit 0 in the register is the LSB and the first to reach the TDO pin when shifting begins.

## TAP Controller Instruction Set

**Overview**
There are two classes of instructions defined in the Standard 1149.1-1990; standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. Although the TAP Controller in this device follows the 1149.1 conventions, it is not 1194.1-compliant because one of the mandatory instructions, EXTEST, is uniquely implemented. The TAP on this device may be used to monitor all input and I/O pads. This device will not perform INTEST but can perform the preload portion of the SAMPLE/PRELOAD command.
When the TAP controller is placed in the Capture-IR state, the two least significant bits of the instruction register are loaded with 01. When the TAP controller is moved to the Shift-IR state, the Instruction Register is placed between the TDI and TDO pins. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at the TDO output). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to the Update-IR state. The TAP Instruction Set for this device is listed in the following table.

**Instruction Descriptions**

**BYPASS**
When the BYPASS instruction is loaded in the Instruction Register, the Bypass Register is placed between the TDI and TDO pins. This occurs when the TAP Controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

**SAMPLE/PRELOAD**
SAMPLE/PRELOAD is a Standard1149.1 mandatory public instruction. When the SAMPLE/PRELOAD instruction is loaded in the Instruction Register, moving the TAP Controller into the Capture-DR state loads the data in the SRAM's input and I/O buffers into the Boundary Scan Register. Some Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the BSDL file. Because the SRAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. SRAM input signals must be stabilized for long enough to meet the TAP's input data capture set-up plus hold time (tTS plus tTH). The SRAM's clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to the Shift-DR state then places the Boundary Scan Register between the TDI and TDO pins.

**EXTEST**

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the Instruction Register is loaded with all logic 0s. EXTEST is not implemented in the TAP Controller, and therefore this device is not compliant to the 1149.1 Standard. When the EXTEST instruction is loaded into the Instruction Register, the device responds as if the SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST place the SRAM outputs in a High-Z state.

**IDCODE**

The IDCODE instruction cause the ID ROM to be loaded into the ID register when the controller is in the Capture-DR state and places the ID Register between the TDI and TDO pins in the Shift-DR state. The IDCODE instruction is the default instruction loaded in at power-up and any time the controller is placed in the Test-Logic-Reset state.

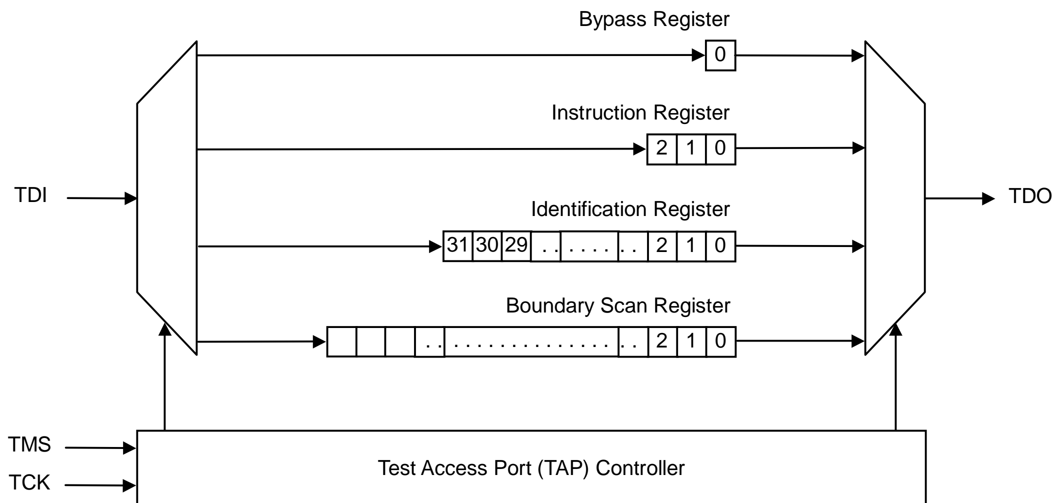
**SAMPLE-Z**

If the SAMPLE-Z instruction is loaded in the Instruction Register, all SRAM outputs are forced to an inactive drive state (High-Z) and the Boundary Scan Register is placed between the TDI and TDO pins when the TAP Controller is moved to the Shift-DR state.

**RFU**

These instructions are reserved for future use. Do not use these instructions.

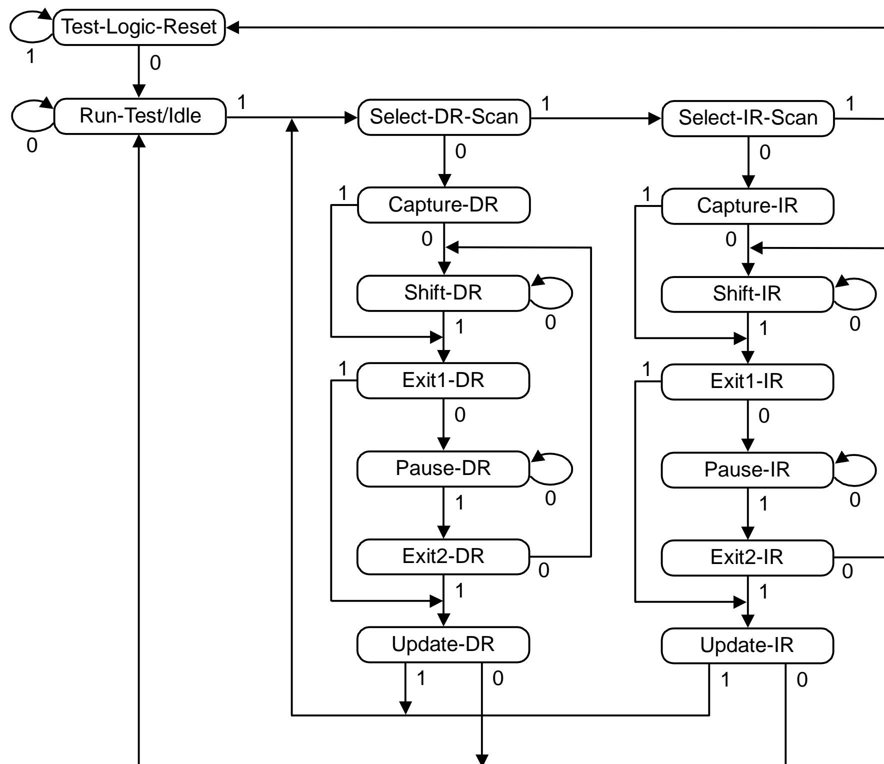
## JTAG TAP BLOCK DIAGRAM



## BOUNDARY SCAN ORDER

| Bit | Bump | Pin Name | Bit | Bump | Pin Name | Bit | Bump | Pin Name |
|---|---|---|---|---|---|---|---|---|
| 0 | 5V | A16 | 40 | 11B | DQb | 80 | 1H | DQc |
| 1 | 6U | A15 | 41 | 11A | DQb | 81 | 2H | DQc |
| 2 | 8U | A11 | 42 | 10C | DQb | 82 | 1J | DQc |
| 3 | 7V | A13 | 43 | 10B | DQb | 83 | 2J | DQc |
| 4 | 7W | A14 | 44 | 10A | DQb | 84 | 6L | MCH |
| 5 | 8V | A12 | 45 | 9A | A9 | 85 | 6M | MCH |
| 6 | 9V | A10 | 46 | 7A | A8 | 86 | 2L | DQh |
| 7 | 10W | DQe | 47 | 7B | A17 | 87 | 1L | DQh |
| 8 | 10V | DQe | 48 | 8C | BWe# | 88 | 2M | DQh |
| 9 | 10U | DQe | 49 | 9C | BWa# | 89 | 1M | DQh |
| 10 | 11W | DQe | 50 | 9B | BWf# | 90 | 2N | DQh |
| 11 | 11V | DQe | 51 | 8B | BWb# | 91 | 1N | DQh |
| 12 | 11U | DQe | 52 | 6A | ADV | 92 | 2P | DQh |
| 13 | 11T | DQe | 53 | 6D | G# | 93 | 1P | DQh |
| 14 | 10T | DQe | 54 | 6K | CKE# | 94 | 2R | DQPh |
| 15 | 11R | DQPe | 55 | 6B | W# | 95 | 1R | DQPd |
| 16 | 10R | DQPa | 56 | 3K | CLK | 96 | 2T | DQd |
| 17 | 11P | DQa | 57 | 8A | E3# | 97 | 1T | DQd |
| 18 | 10P | DQa | 58 | 4B | BWg# | 98 | 1U | DQd |
| 19 | 11N | DQa | 59 | 3B | BWc# | 99 | 1V | DQd |
| 20 | 10N | DQa | 60 | 3C | BWh# | 100 | 1W | DQd |
| 21 | 11M | DQa | 61 | 4C | BWd# | 101 | 2U | DQd |
| 22 | 10M | DQa | 62 | 4A | E2 | 102 | 2V | DQd |
| 23 | 11L | DQa | 63 | 6C | E1# | 103 | 2W | DQd |
| 24 | 10L | DQa | 64 | 5A | A7 | 104 | 6T | LBO# |
| 25 | 6P | ZZ | 65 | 3A | A6 | 105 | 3V | A5 |
| 26 | 6J | MCH | 66 | 2A | DQg | 106 | 4V | A4 |
| 27 | 10J | DQf | 67 | 2B | DQg | 107 | 4U | A3 |
| 28 | 11J | DQf | 68 | 2C | DQg | 108 | 5W | A2 |
| 29 | 10H | DQf | 69 | 1A | DQg | 109 | 6V | A1 |
| 30 | 11H | DQf | 70 | 1B | DQg | 110 | 6W | A0 |
| 31 | 10G | DQf | 71 | 1C | DQg | | | |
| 32 | 11G | DQf | 72 | 1D | DQg | | | |
| 33 | 10F | DQf | 73 | 2D | DQg | | | |
| 34 | 10E | DQPf | 74 | 1E | DQPg | | | |
| 35 | 11F | DQf | 75 | 1F | DQc | | | |
| 36 | 11E | DQPb | 76 | 2E | DQPc | | | |
| 37 | 10D | DQb | 77 | 2F | DQc | | | |
| 38 | 11D | DQb | 78 | 1G | DQc | | | |
| 39 | 11C | DQb | 79 | 2G | DQc | | | |

## JTAG TAP CONTROLLER STATE DIAGRAM




**TAP CONTROLLER DC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, VDD=2.375~2.625V, unless otherwise noted)

| Symbol | Parameter | Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| VIHT | Test Port Input High Voltage | | 1.7 | VDDQ+0.3 ** | V |
| VILT | Test Port Input Low Voltage | | -0.3 ** | 0.7 | V |
| VOHT | Test Port Output High Voltage | IOH=-100μA | VDDQ-0.1 | - | V |
| VOLT | Test Port Output Low Voltage | IOL=+100μA | - | 0.1 | V |
| IINT | TMS, TCK and TDI Input Leakage Current | | -10 | 10 | μA |
| IOLT | TDO Output Leakage Current | Output Disable, VOUT=0V~VDDQ | -10 | 10 | μA |

Note37. **Input Undershoot/Overshoot voltage must be –1.0V<Vi<VDDQ+1V with a pulse width not to exceed 20% tTCK.

**TAP CONTROLLER AC ELECTRICAL CHARACTERISTICS** (Ta=0~70°C, $V_{DD}$=2.375~2.625V, unless otherwise noted)

**(1)MEASUREMENT CONDITION**

Input pulse levels ........................................ $V_{IH}=V_{DDQ}$, $V_{IL}$=0V
Input rise and fall times ................................ faster than or equal to 1V/ns
Input timing reference levels ........................ $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output reference levels ................................ $V_{IH}=V_{IL}=V_{DDQ}$ / 2
Output load .................................................... Fig.4

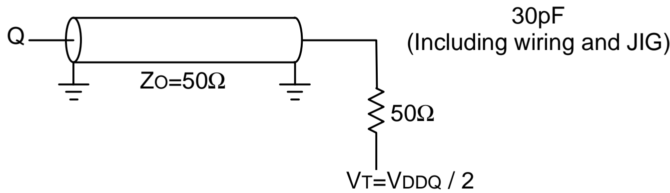
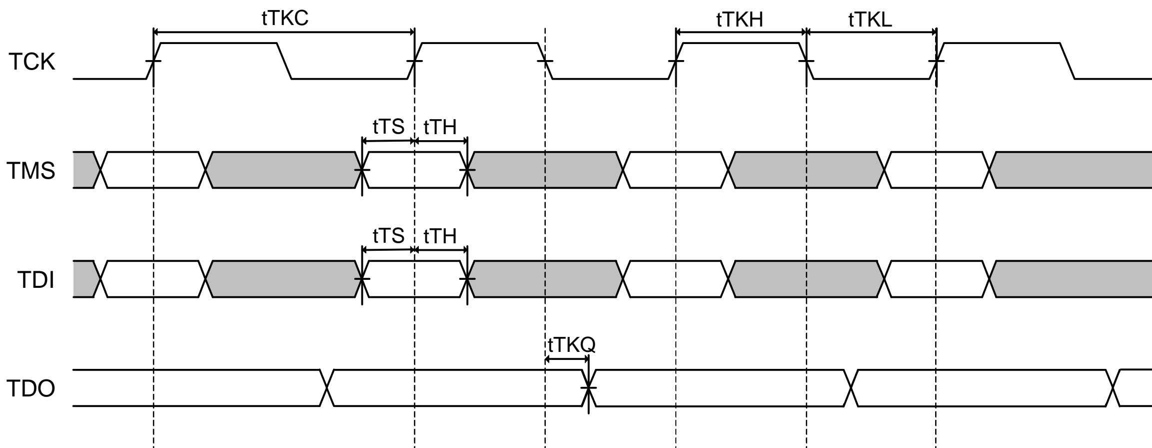



Fig.4 Output load

**(2)TIMING CHARACTERISTICS**

| Symbol | Parameter | Limits | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tTF | TCK Frequency | | 20 | MHz |
| tTKC | TCK Cycle Time | 50 | | ns |
| tTKH | TCK High Pulse Width | 20 | | ns |
| tTKL | TCK Low Pulse Width | 20 | | ns |
| tTS | TDI, TMS setup time | 10 | | ns |
| tTH | TDI, TMS hold time | 10 | | ns |
| tTKQ | TCK Low to TDO valid | | 20 | ns |

**(3) TIMING**





RENESAS
Renesas Technology Corp.

## JTAG TAP INSTRUCTION SET SUMMARY

| Instruction | Code | Description |
|---|---|---|
| EXTEST | 000 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant. |
| IDCODE | 001 | Preloads ID Register and places it between TDI and TDO |
| SAMPLE-Z | 010 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z |
| RFU | 011 | Do not use this instruction; Reserved for Future Use. |
| SAMPLE/PRELOAD | 100 | Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. |
| RFU | 101 | Do not use this instruction; Reserved for Future Use. |
| RFU | 110 | Do not use this instruction; Reserved for Future Use. |
| BYPASS | 111 | Places the BYPASS Register between TDI and TDO. |

## STRUCTURE OF IDENTIFICATION REGISTER

| | Revision | | | | Device Information | | | | | | | | | | | | | | | | JEDEC Vendor Code of RENESAS | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit No. | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| M5M5T5672 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| | MSB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | LSB |

**PACKAGE OUTLINE**

209(11x19) bump Ball Grid Array(BGA) Pin Pitch 1.0mm

Refer to JEDEC Standard MS-028, Variation BC,

which can be seen at:

http://www.jedec.org/download/search/MS-028C.pdf

**REVISION HISTORY**

| Rev.No. | History | Date | |
|---|---|---|---|
| 0.0 | First revision | September 25, 2002 | Preliminary |
| 0.1 | DC ELECTRICAL CHARACTERISTICS<br>Changed ILI limit from 10uA to 100uA<br>(Input Leakage Current of ZZ and LBO#)<br>Changed Icc3 and Icc4 limit from 20mA to 30mA<br>(Standby Current) | January 31, 2003 | Preliminary |
| 1.0 | Fixed PART NAME TABLE<br><br>AC ELECTRICAL CHARACTERISTICS<br>(2)TIMING CHARACTERISTICS<br>Changed tKHKL limit from 1.8ns to 2.0ns.<br>Changed tKLKH limit from 1.8ns to 2.0ns.<br>Changed all Setup times from 1.2ns to 1.0ns.<br>Changed all Hold times from 0.5ns to 0.8ns.<br><br>STRUCTURE OF IDENTIFICATION REGISTER<br>Fixed JEDEC Vender Code as follows.<br>The semiconductor operations of HITACHI and MITSUBISHI Electric were transferred to RENESAS Technology Corporation on April 1st 2003.<br>Both RENESAS and MITSUBISHI JEDEC vendor code are as follows | August 1, 2003 | Preliminary |

| Bit No. | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RENESAS | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| MITSUBISHI | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |

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REJ03C0072
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