# M5W1791-02P

## FLOPP DISK FORMATTER/CONTROLLER

## 1. DESCRIPTION

The M5W1791-02P is a floppy disk formatter/controller device which accommodates single and double density formats.

The device is designed for use with microprocessors or microcomputers.

The device is fabricated with the Nchannel silicon gate EDMOS technology is packaged in a 40-pin DIL package.

## 2. FEATURES

- Single 5V supply voltage
- Accommodate singe and double density formats
  IBM 3740 single density format
  IBM system 34 double density format
- Selectable sector length (128, 256, 512 or 1024 bytes/sector)
- Side select compare
- Single/multiple sector read or write with automatic sector search
- Selectable track to track stepping time
- Write precompensation
- DMA or programmed data transfers
- Window extension

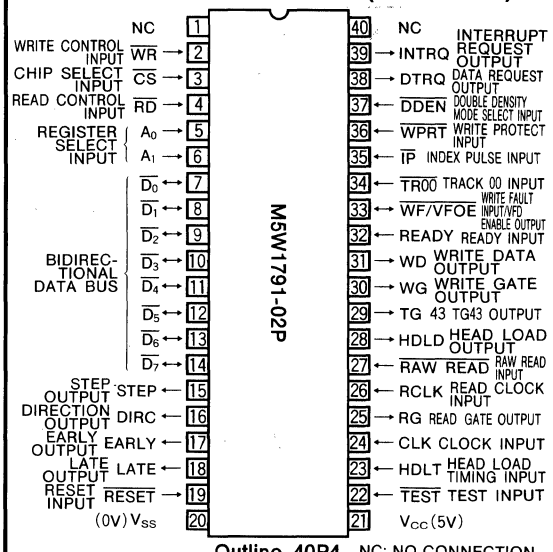
## 3. APPLICATION

- Single or double density floppy disk drive formatter/controller
- 8-inch or mini floppy disk interface

## 4. FUNCTION

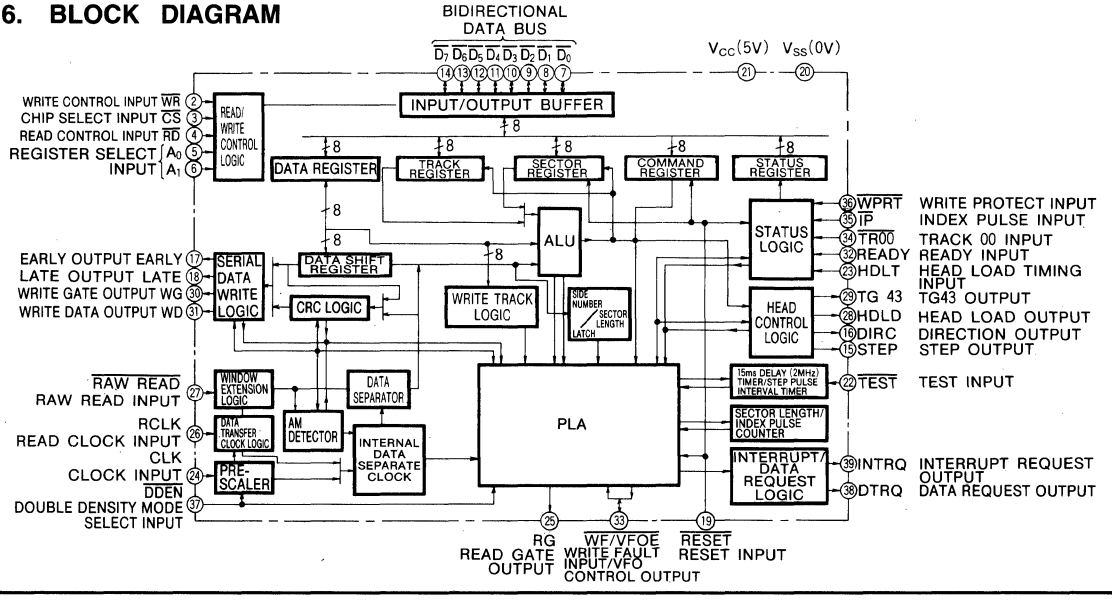
The M5W1791-02P is a floppy disk formatter/controller that can be used with most microprocessor or microcomputer systems. The hardware of the M5W1791-02P consists of a floppy disk interface, a CPU interface and a PLA control logic. The total chip can be programmed by eleven 8-bit commands. The floppy disk interface portion performs the communication with floppy disk drive under control of the PLA control logic. The CPU interface portion has five registers — command, data, status, track and sector register — and communicates with the CPU through the data bus. These functions are also controlled by the PLA.

## 5. PIN CONFIGURATION (TOP VIEW)




Outline 40P4 NC: NO CONNECTION

## 6. BLOCK DIAGRAM



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## 7. PIN DESCRIPTION

| Pin | Name | Input or output | Functions |
|---|---|---|---|
| NC | No internal connection | | NC(pin 1) is not internally connected |
| $\overline{WR}$ | Write control input | Input | Write signal from a master CPU (Active low). |
| $\overline{CS}$ | Chip select input | Input | Chip select (Active low). |
| $\overline{RD}$ | Read control input | Input | Read signal from a master CPU (Active low). |
| $A_0$, $A_1$ | Register select input | Input | Register select inputs. These inputs select the register under the control of the $\overline{RD}$ and $\overline{WR}$.<br>$A_1$ $A_0$ $\overline{RD}$ $\overline{WR}$<br>0 0 STATUS REGISTER COMMAND REGISTER<br>0 1 TRACK REGISTER TRACK REGISTER<br>1 0 SECTOR REGISTER SECTOR REGISTER<br>1 1 DATA REGISTER DATA REGISTER |
| $\overline{D_0}$~$\overline{D_7}$ | Bidirectional data bus | In/Out | Three-state, inverted bidirectional data bus. |
| STEP | Step output | Output | Step pulse output (Active high). |
| DIRC | Direction output | Output | Direction output. High level means the head is stepping in and low level means the head is stepping out. |
| EARLY | Early output | Output | This signal is used for write precompensation. It indicates that the write data pulse should be shifted earty. |
| LATE | Late output | Output | This signal is also used for write precompensation. It indicates that the write data pulse should be shifted late. |
| $\overline{RESET}$ | Reset input | Input | Reset input (Active low). The device is reset by this signal and automaticaily loads "03" (hexadecimal) into the command register. The not-ready-status bit is also reset by this signal. When reset input is made to be high, the device executes restore command even unless READY is active and the device loads "01" (hexadecimal) to the sector register. |
| $\overline{TEST}$ | Test input | Input | This input is only used for test purposes, so user must tie it to $V_{CC}$ or leave it open unless using voice coll actuated motors. |
| HDLT | Head load timing input | Input | When the device finds high level on this input, the device assumes that the head is engaged on the media. Active high. |
| CLK | Clock input | Input | Clock input to generate internal timing. 2MHz for 8-inch drives, 1MHz for mini drives. |
| RG | Read gate output | Output | This signal shows the external data separator that the syncfield is detected. |
| RCLK | Read clock input | Input | This signal is internally used for the data window. Phasing relation to raw read data is specified but polarity (RCLK high or low) is not important. |
| $\overline{RAW}$ $\overline{READ}$ | Raw read input | Input | This input signal from the drive shall be low for each recorded flux transition. |
| HDLD | Head load output | Output | This output signal controls the loading of the head of the drive. The head must be loaded on the media by this high-level output. |

6

| Pin | Name | Input or output | Functions |
|---|---|---|---|
| TG43 | TG 43 output | Output | This output is valid only during disk read/write operation and it shows the position of the head. High level on this output indicates that head is positioned between track 44 to 76. |
| WG | Write gate output | Output | This signal becomes active before disk write operations are to occur. |
| WD | Write data output | Output | This signal consists of data bits and clock bits. It becomes active for every flux transition. Active high. |
| READY | Ready input | Input | This signal shows the device the drive is ready. In the disk read/write operation except for TYPE 1 command operation, low level input terminates current operation and the device generates the INTRQ. In the TYPE 1 command operation, this signal is neglected. Not ready bit in the status register is the inverted form of this input. |
| $\overline{WF}/\overline{VFOE}$ | Write fault input/ VFO enable output | In/Out | This is a bidirectional signal. It becomes write fault input when WG is active. In the disk write operation, low level signal on this input terminates the write operation and makes INTRQ active. This signal also appears in the status register as the write fault bit. When WG is inactive, this signal works as VFO enable output. $\overline{VFOE}$ output is also an open drain type, so pull it up to $V_{CC}$ and never input active write fault signal write WG is inactive. |
| $\overline{TR00}$ | Track 00 input | Input | This signal indicates that the head is located on the track 00 to the device. Active low. |
| $\overline{IP}$ | Index pulse input | Input | This input indicates to the device that an index hole of the diskette has been encountered. |
| $\overline{WPRT}$ | Write protect input | Input | Low level signal on this input informs the device that the drive is in the write protected state. Before disk write operations, this signal is sampled and an active low signal will terminate the current command and set INTRQ. The write protect status bit in the status register is also set. |
| $\overline{DDEN}$ | Double density mode select input | Input | This input determines the device operation mode. When $\overline{DDEN}$=0, double density mode is selected. When $\overline{DDEN}$=1, single density mode is selected. |
| DTRQ | Data request output | Output | DTRQ is an open drain output, so pull up to $V_{CC}$ by the 10k resistor. In the disk read mode, DTRQ indicates that data is assembled in the data register. In the disk write mode, it indicates that the data register is empty. DTRQ is reset by the read data or write data operation. |
| INTRQ | Interrupt request output | Output | INTRQ is also a open drain output, so pull up to $V_{CC}$ by the 10k resistor. INTRQ becomes active at the completion of any command and is reset when the CPU reads the status or writes the command. |
| NC | No internal connection | | NC (pin 40) is not internally connected. |

## 8. HARDWARE CONFIGURATION

The following explanation is based on the block diagram is Section 6.

The registers which are accessible by the CPU system through the input/output buffer of the M5W1791-02P are the command, status, track, sector and data registers. These are all 8-bit registers.

The register select inpus $A_0$ and $A_1$ select one register under $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ control as described in Section 7.

### 8.1 Retister Descriptions

### (1) Command Register

This register is write-only, so the contents of the command register cannot be read onto the bi-directional data bus. The CPU system writes the command code into this register to be executed by the M5W1791-02P. Except the force interrupt command, the command register should not be loaded while the busy status bit is set.

### (2) Status Register

This is the read-only register and holds the status information about the device and a connected floppy disk drive. The meaning of each status bit is varied by the executing command.

### (3) Track Register

This register is bi-directional, so the CPU system can read or write the data through the data bus. The track register has the track number of the floppy disk's current head position. The type 1 commands have the update flag option according to this register. When this flag is set, the contents of the track register are updated by one for each step. They are incremented when the head is stepped in and decremented when the head is stepped out.

When the type 2 command which performs the read/write operation for the floppy disk is executed, the track address of the floppy disk's ID field and the contents of the track register are compared. If they match, M5W1791-02P continues to check whether the sector address is the one appointed by the sector register.

When the restore command is performed automatically by the $\overline{RESET}$ input transition from "0" to "1" or when the CPU system executes the restore command, FF (HEX) is at first loaded into the track register and every time the step pulse is issued, the value of this register is decremented by one. The contents of the track register are set to 00 (HEX) when the $\overline{TR00}$ input is activated before the 255th step pulse issued or after the step pulse was generated 255 times.

### (4) Sector Register

This is also a bi-directional register.

For disk read or write operation, the CPU system must set the desired sector address into this register.

By forcing the $\overline{RESET}$ input from "0" to "1", M5W1791-02P also sets 01 (HEX) into the sector register, then begins the restore operation.

In the type 2 command execution, the sector address of the disk's ID field and the contents of the sector register are also compared as mentioned above.

When the m flag bit of the type 2 command code is set to perform the multi-sector read/write operation, the sector register value is automatically incremented by one upon completion of the read/write operation of the one sector.

When the read address command of the type 3 command has been executed, the track address which is read out from the first encountered ID field is loaded into the sector register.

### (5) Data Register

This register is bi-directional.

During disk data read operation, the data read from the floppy disk is held in this register. During the write operation, byte of data from the CPU system is held.

Prior to seek command execution, the desired track position must be written into the data register.

By executing the restore command or the $\overline{RESET}$ input transition from "0" to "1", M5W1791-02P automatically loads 00 (HEX) into the data register.

The hardware blocks of access to the user are only the reigsters mentioned above. Descriptions of inaccesible internal hardware blocks follow.

### 8.2 Control Circuit

### (1) ALU (Arithmetic Logic Unit)

This one-bit serial ALU executes the comparisons of the serial data and is used for the modification and comparison of registers.

### (2) Status Control Logic

The status control logic generates the status information for the status register. It is divided into two sections: one reflects the state of the M5W1791-02P and the other reflects the state fo the disk system. Disk states inclued write protect, index pulse, track 00, ready, head loak timing and write fault.

### (3) Head Control Logic

This circuit generates the signal which controls head movement of the floppy disk. It provides the head load signal, direction signal, step signal and TG43 signal. The TG43 output controls the disk's write current.

When the type 1 command with the head load flag h at "1" is executed, the head load output is set to "1" at the beginning of the command execution. The command execution where the head load flag h is initially at "0" makes the head load output "0" whether it has been "0" or "1".

After issuing the step pulses, the M5W1791-02P checks

the verify flag V in the command code. If V is "0", the command is terminated and the interrupt request output signal is sent. If V is "1", the head load output is set to "1" (if h ="1" , HDLD is already set to "1" at the beginning of this command), and after an internal 15 ms delay (CLK = 2MHz, $\overline{TEST}$ =1), the head load timing input HDLT is sampled until HDLD and HLDT ="1" (logic true). Then M5W1791-02P updates the TG43 output signal and commences the disk read operation. This means that during the type 1 command, the TG43 signal is not updated unless the V flag is set to "1". The TG43 output is set to "1"when the floppy disk head is positioned beyond the 43rd track.

The type 2 and 3 commands confirm the ready input logic high, and after a 15 ms delay (if flag E is set; if E = 0, no internal delay is initiated), HDLT is sampled until HDLD and HDLT = "1" as mentioned above. M5W1791-02P then updates the TG43 output signal and begins the disk read/write operation. If the ready input is low, then the command is terminated and INTRQ is generated.

The head load output which was set to "1" is reset to "0" under the following two conditions:

- If the M5W1791-02P is idle for 15 disk revolutions after the prevous command terminates, the head load signal resets to "0".
- If the type 1 command is executed when h = "0", the head is also automatically disengaged.

## (4) Head Engage Timer/Step Speed Timer

The M5W1791-02P can generate an internal 15 ms wait time (CLK = 2MHz) before the head load timing input is sampled. The HDLT signal shows M5W1791-02P that the floppy disk head is completely engaged after loading into the media. The step speed can be selected at 3 ms, 6 ms, 10 ms or 15 ms (CLK = 2MHz) by the stepping motor rate bits $r_1$ and $r_0$ in the type 1 command.

These operations are controlled by the 1 ms timer and presettable 4-bit binary counter inside the M5W1791-02P.

This 1 ms timer is disabled by setting the test input $\overline{TEST}$ to "0", which initiates step pulse intervals of about 400$\mu$s in the single-density mode and about 200$\mu$s in the double-density mode (CLK = 2MHz). The 15 ms wait time is also reduced in the two modes to about 60$\mu$s and 30$\mu$s, respectively.

The test input signal is used only for interfacing with the floppy disk drives and a voice coil motor.

Table 8.1 shows the relationship between the stepping motor rate flags and the step pulse intervals.

Table 8.1 Step Pulse Intervals

(unit: ms)

| CLK (MHz) | 2MHz | | 1MHz | |
|---|---|---|---|---|
| $r_{1,0}$ \ $\overline{DDEN}$ | 0 | 1 | 0 | 1 |
| 0, 0 | 3 | 3 | 6 | 6 |
| 0, 1 | 6 | 6 | 12 | 12 |
| 1, 0 | 10 | 10 | 20 | 20 |
| 1, 1 | 15 | 15 | 30 | 30 |

## (5) Index Pulse Counter/Sector Counter/ Step Pulse Counter

As mentioned in Section 8.2 (3), the M5W1791-02P has an index pulse counter that returns the head load output to "0" in the idle state after command execution. This index pulse counter is used to terminate the command when the M5W1791-02P does not complete it within 5 index pulses. There are 12 reasons why the command may be terminated prematurely:

- The synchronize pattern of the ID field is not found.
- The synchronize pattern of the ID field is too short.
- AM1 of the ID field is not found.
- AM1 of the ID field is not complete.
- The ID track address is not equal to the contents of the track register.
- The ID sector address is not equal to the contents of the sector register.
- The side number of the ID field is not equal to the side select flag s in the command code when the side comparison flag C is set to "1".
- The ID field CRC error occurs.
- The synchronize pattern of the data field is not found.
- The synchronize pattern of the data field is too short.
- AM2 of the data field cannot be found.
- AM2 of the data field not complets.

When a CRC error of the data field occurs, an interrupt is generated without a retry.

The index counter is also used as the sector counter/ step pulse counter. When this counter is used as a step pulse counter, it counts a maximum of 255 step pulses during the restore command as described in Section 8.1(3)

This counter is used as a sector counter in the type 2 command to count the data length of the data field for the destination sector. In this sense, it is more appropriate to call this counter the data length counter.

The M5W1791-02P allows one of four different data length configurations in one sector: 128 bytes, 256 bytes, 512 bytes and 1024 bytes. The data length of the sector to be read or written by the M5W1791-02P is decided by the "sector length" parameter at the 4th byte of the ID field. When the read/write operation is commenced for the desired data field, the M5W1791-02P uses this sector counter to generate the data request signal at specified times in accordance with the ID sector length byte.

## (6) Interrupt Request Control Logic, Data Request Control Logic

The interrupt request output INTRQ is an open drain output that notifies the CPU of command termination.

Once set, the interrupt request output INTRQ is not reset to "0" until the status is read out from the status register or the command is written into the command register by the CPU.

Refer to Section 11.5 concerning the response of the INTRQ during the type 4 command.

The INTRQ output is not reset by the reset input signal. This state is undefined after power is applied.

The data request control output DTRQ is also an open drain output that requests the CPU to read out the data from the data register or write the data into the data register during the disk read or write operation.

The DTRQ output is reset to "0" by writing the data into or reading the data out from the data register.

The DTRQ output is changed to "0" by the reset input.

### (7) Write Control Logic

The M5W1791-02P provides frequency-modulated(FM) data in the single-density mode or modified FM (MFM) data in the double-density mode.

The data written into the data register from the CPU is sent to the data shift register and then it is modulated by the write control logic in accordance with the modulation type selected by the $\overline{\text{DDEN}}$ input. This modulated data is sent to the write data output WD.

The special patterns including the missing clock required for disk formatting are also produced in the write control logic under the control of the write command control circuit.

During the disk write operation, M5W1791-02P can predict the occurrence of the peak shift, depending on the previous bit pattern, so the write control logic provides the early and late output signals for write precompensation.

### (8) Write Track Command Control Logic

The internal PLA program controls almost all the operations of the M5W1791-02P. However, when the write track command is executed, the PLA program control speed is too slow to perform the command. Therefore, the write track command control logic implements the write track operation directly.

When the CPU writes the data into the data register for disk initialization, the contents are sent to the internal data shift register and the write track command control logic. When a special data byte is sent to the data register from the CPU, the write control logic operates under the control of the write track command control logic the provide the designated write data pattrern. When the other data bytes are written into the data register, they are first sent to the data shift register, then to the write control logic serially to be modulated according to the $\overline{\text{DDEN}}$ input.

## 8.3 Internal Control Logic

### (1) Data Shift Register

During the disk write operation, the data bytes written into the data register from the CPU are loaded into this register in parallel. The data shift register transfers the serial data to the write control logic for modulation.

During the disk read operation, the internal data separator circuit demodulates the raw read data stream and produces the true data bit pattern. This demodulated data bit is shifted into the data shift register in series and transferred to the data register in parallel byte by byte.

### (2) CRC Logic

The CRC (Cyclic Redundancy Check) circuit generates the cyclic redundancy check code. The polymonial is $X^{16} + X^{12} + X^5 + 1$.

The CRC code, generated by the CRC circuit from the write data stream, is written onto the floppy disk during the disk write operation.

During the disk read operation, the last two CRC bytes read out in the ID or data field are checked for errors by the CRC logic.

### (3) Prescaler

A pair of internal clocks are required to drive the M5W1791-02P's logic circuitry. During the disk read operation, these clocks are derived from the read clock input RCLK from the differential circuit, the data transfer clock logic and the internal clock control logic.

At all times except for disk read operations, such as during type 1 commands or disk write operations, these two internal clocks are produced by the prescaler and the internal clock control logic from the CLK input signal.

The prescaler generates the data transfer clock and the data separator clock by dividing the CLK input clock by 2 and 4 in the double density mode and by 4 and 8 in the single density mode.

The internal PLA logic is driven by this data separator clock.

### (4) Differential Circuit, Data Transfer Clock Logic

The differential circuit and the data transfer clock logic generate the internal data transfer clock by multiplying the PCLK clock input and shaping its waveform.

### (5) Window Extension Logic

When disk read operations are executed in the double-density mode, the raw read input occurs in both RCLK clock windows. At this time, the window extension logic samples the raw read input at the edge of the internal data transfer clock which is derived from the RCLK input to provide that the read clock input RCLK window width is extended substantially.

### (6) AM Detector Logic

The raw read signal input $\overline{\text{RAW READ}}$ from the floppy disk is a signal which has been modulated by either FM or MFM. M5W1791-02P should synchronize the internal data separator clock with the data bit of the input data stream. For this

6

purpose, the AM detector logic is employed to detect the special patterns which contain the missing clocks from the input raw read stream.

### (7) Internal Clock Control Logic

This logic generates the data transfer clock and data separator clock.

### (8) Data Separator

This separates the data bit from the raw read input signal by using the data separator clock.

### (9) PLA

This is the programmable logic array which controls the M5W1791-02P. The size of this PLA ROM is approximately 230 × 19 bits.

## 9. DESCRIPTION OF COMMANDS

There are 11 different commands. By setting $\overline{CS}$ to "0", $A_0$ to "0" and $A_1$ to "0" the commands are written inside the M5W1791-02P from the data bus at the rising edge of the $\overline{WR}$ signal.

The commands are classified into four types: type 1, type 2, type 3 and type 4.

Table 9.1 List of Commands

| Command type | Command | MSB | | | Code | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|
| Type 1 commands | Restore command | 0 | 0 | 0 | 0 | h | V | $r_1$ | $r_0$ |
| | Seek command | 0 | 0 | 0 | 1 | h | V | $r_1$ | $r_0$ |
| | Step command | 0 | 0 | 1 | u | h | V | $r_1$ | $r_0$ |
| | Step-in command | 0 | 1 | 0 | u | h | V | $r_1$ | $r_0$ |
| | Step-out command | 0 | 1 | 1 | u | h | V | $r_1$ | $r_0$ |
| Type 2 commands | Read sector command | 1 | 0 | 0 | m | S | E | C | 0 |
| | Write sector command | 1 | 0 | 1 | m | S | E | C | $a_0$ |
| Type 3 commands | Read address command | 1 | 1 | 0 | 0 | 0 | E | 0 | 0 |
| | Read track command | 1 | 1 | 1 | 0 | 0 | E | 0 | 0 |
| | Write track command | 1 | 1 | 1 | 1 | 0 | E | 0 | 0 |
| Type 4 commands | Force interrupt command | 1 | 1 | 0 | 1 | $I_3$ | $I_2$ | $I_1$ | $I_0$ |

Note 1 : Although the codes are written in TRUE form, the M5W1791-02P features a negative logic data bus. This means codes with 0 and 1 reversed are written into the M5W1791-02P.

Each command comes with a flag option. These are identified in Table 9.2.

6

## Table 9.2 Flag Options

| | Flag | Description |
|---|---|---|
| Type 1 commands | h : Head load flag | When h =1: The head is loaded at the beginning of the command execution.<br>When h =0: The head is loaded when the verify operation starts if the V flag is "1". It is not loaded if the V flag is "0". |
| | V : Verify flag | When V =1: The contents of the track register are compared with the ID track address after head positioning. The seek error status bit is set if the desired track address is not found by the time the diskette has gone through 6 rotations.<br>When V =0: The track verification is not performed. |
| | $r_1$, $r_0$ : Stepping rate flag | The stepping rate is determined by the value of these 2 bits as well as by the CLK frequency and $\overline{TEST}$ input pin. |
| | u : Update flag | When u = 1: The track register is updated with each step pulse: It is incremented (or decremented) by 1 for each step-in (or step-out) pulse.<br>When u =0: Track register is not updated. |
| Type 2/Type3 Commands | E : 15ms delay flag(at 2MHz clock) | When E =1: Sampling of the head load timing input starts with the 15ms delay after the head load output has been set to "1". An advance is made to the next step when HDLD·HLDT = "1" is established.<br>When E =0: Sampling of the head load timing input starts immediately after the head load output has been set to "1". An advance is made to the next step when HDLD·HLDT = "1" is established.<br>The "next step" is the TG43 output update. |
| Type 2 commands | m : Multi-sector read/write flag | When m =1: Multi-sector read/write is performed. Upon completion of one sector read/write, the sector register value is incremented by 1, the next sector is sought and read/write is performed again. Upon completion of the final sector read/write operation, the next sector is not found even when sought and so at the sixth rotation of the diskette the RNF error bit is set and the operation is concluded. This command can also be concluded with the Type 4 command.<br>When m =0: Read/write for single sector is performed. |
| | S : Side select flag | When S =1: "1" is compared with the ID side number when the C flag is "1".<br>When S =0: "0" is compared with the ID side number when the C flag is "1".<br>No comparison is performed when C =0. |
| | C : Side compare flag | When C =1: The S flag and ID side number are compared.<br>When C =0: The ID side number is not compared. |
| | $a_0$ : Data address mark flag | When $a_0$ =1: The deleted data mark "F8" (hexadecimal) is written into the data field address mark.<br>When $a_0$ =0: The data mark "FB" (hexadecimal) is written into the data field address mark. |
| Type 4 command | I : Interrupt condition flag | When $I_0$ =1: The interrupt request output is set to "H" at the ready input rising edge.<br>When $I_1$ =1: The interrupt request output is set to "H" at the ready input falling edge.<br>When $I_2$ =1: The interrupt request output is set to "H" with the index pulse input.<br>When $I_3$ =1: The command being executed is terminated and the interrupt request output is set to "H" immediately.<br>When $I_0$ =$I_1$ =$I_2$ =$I_3$ =0: No interrupt request is generated but the command being executed is terminated. This command is executed so that the interrupt request output, which has been set by the Type 4 command, is reset by the following command write or status read. |

## 10. DESCRIPTION OF OPERATION

The M5W1791-02P is provided with an interface section for the CPU system and an interface section for the floppy disk system.

### 10.1 CPU System Interface Section

The CPU interface section is composed of the input/output buffer, input/output control logic, five internal registers, interrupt request control logic and data request control logic.

The CPU reads/writes the contents of the internal registers through the M5W1791-02P's data bus.

Upon the completion of each command, and interrupt to the CPU is generated by the interrupt control logic. INTRQ is reset by command register write or status register read.

The M5W1791-02P generates the data request output DTRQ for the CPU system using its data request control circuit while reading or writing floppy disk data.

The time required to transfer one byte of serial data when CLK is 2MHz is 32$\mu$s in the single-density mode and 16$\mu$s in the double-density mode. However, the maximum time from when DTRQ is set to "H" until the CPU system reads or writes the data is actually shorter than 32$\mu$s (or 16$\mu$s) and if the service is not completed whithin this time, the lost data status bit is set. When the CPU system does not respond to the first data request for write sector command or write track command within the required time, the subsequent operation of the commands are theminated and the interrupt request output is set.

For instance, the service time $T_{service}$ (WR) for DTRQ when a write sector command is being executed in the single-density mode is 23.5$\mu$s maximum. This is because it takes 4$\mu$s for the DTRQ output to be set after the contents of the data register have been transferred to the data shift register, and 4.5$\mu$s at most for the M5W1791-02P to transfer data into the data register which has been written in response to DTRQ. In other words, unless the data is serviced within 23.5$\mu$s (i.e. 32 — 4 — 4.5 = 23.5$\mu$s), there will no longer be time to begin transfer of data from the next data register to the data shift register.

For further details, refer to the section dealing with the description of the commands.

### 10.2 Floppy Disk Interface Section

The floppy disk interface section is composed mainly of the floppy disk head control section which relates to the head positioning control and the floppy disk read/write control section which controls the serial data transfer.

#### (1) Floppy Disk Head Control Section

For details on the operation of the floppy disk head control section, refer to Section 8.2(3) on the read control circuit, Section 8.2(4) on the head load time timer/stepping rate timer, and Section 8.2(5) on the index pulse counter/sector counter/step pulse counter as well as to Table 9.2 which lists the flag options.

#### (2) Floppy Disk Read/Write Control Section

The floppy disk read/write control section executes the disk read and disk write operations.

The disk read and disk write operations have no direct relation to the read and write commands. For instance, when a write sector command is executed, the disk read operation is performed first to find the desired ID. After the ID is found, the M5W1791-02P writes the sync pattern, data field address mark, data and CRC, after which the command is terminated.

#### Disk Read Operation

The M5W1791-02P is applicable to both the single- and double-density recording formats, and selection between these is performed by the $\overline{DDEN}$ double-density select input.

When the disk read operation starts, the write fault input/VFOE control output $\overline{WF}/\overline{VFOE}$ is set to "L". (This pin is pulled up by a 10-kohm resistance since it serves as an open-drain output during signal output.
The pin serves as the $\overline{VFOE}$ output when the write gate output WG = "L".) This output is kept at "L" until the disk read operation is terminated. The $\overline{VFOE}$ output can be used as the signal that indicates that the PLL circuit employed as the external RCLK generator should enter into lock-in operation from its free-running state.

The following description is for the single-density mode which is almost the same as the double-density mode. When the disk read operation starts and the 2-byte 00 (HEX) is found, this is treated as a sync pattern and the read gate output RG is set to "H". Address mark FE, FB or F8 (HEX) are retrieved within the 10-byte period that follows. When the address mark is not found, RG is reset to "L" and a retry is made to retrieve the 2-byte 00 (HEX). If the address mark is found on the ID field and if the ID track address and sector address (and side number also when side compare bit C = "1") are correct, RG is held at "H" until CRC reading is completed and checked.

Whether there is a CRC error or not, RG is then reset to "L". When there is no error, the sync pattern of the data field is retrieved. When ID is not found properly, that is, when AM1 cannot be read properly, the values of the track register and track address do not match, the values of the sector register and sector address do not match, the side select flag of the command and side number do not match (when C = 1), or when there is a CRC error in th ID field, RG is reset to "0" and a retry is made to retrieve the 2-byte 00 (HEX).

However, when the read address command is executed, the data is read as far as the CRC byte if the sync pattern and AM1 are found properly, and the command is terminated

regardless of whether there is a CRC error. When the data address mark is found, RG is held at "1" until the data and the CRC are read and CRC check is performed. RG is then reset to "0" regardless of whether there is a CRC error. If the command is single sector read or if a data field CRC error occurs, the INTRQ interrupt request output is set to "1" and the command is terminated. The CRC error status bit is set with a CRC error.

The read gate output is active during reading of the valid data stream from the sync field to the CRC. It is the signal that controls the read data tracking sensitivity for the external PLL RCLK generator circuit.

Operation in the double-density mode is the same as that for the single density mode except for the following points. In the double density mode the 4-byte "00" or "FF" (HEX) is treated as the sync pattern and the adress marks "A1" "A1" "A1" "FE", "A1" "A1" "A1" "FB", or "A1" "A1" "A1" "F8" (HEX) are retrieved within the following 16-byte period.

Note that the $\overline{\text{VFOE}}$ output is active when the read track command among the type 3 commands is executed but the RG output remains at "0".

Also bear in mind the following points relating to the disk read operation.

Even during the disk read operation, TG43 is updated in accordance with the track register contents before $\overline{\text{VFOE}}$ is made active.

During the disk read or write operations mentioned below (the execution of type 2 and 3 commands), the READY input is checked at the beginning of the command's execution and if the input is not ready, the command is terminated, the interrpt request output is set to "1" and an interrupt is generated (this does not apply to type 1 and type 4 commands). In this case, the not ready status bit is set.

## Disk Write Operation

During the disk write operation, the write gate output WG is first set to "1". This enables the user to apply the write fault input to the write fault input/VFOE VFO control output pin. Then write data are output from output WD. If the write fault input is made active when WG = "1", the command is immediately terminated, interrupt reqest output INTRQ is set to "1", an interrupt is generated, and the write fault status bit is set.

When the disk write operation is about to be suspended by the type 4 command and when the type 4 command is accepted into the M5W1791-02P's command register before the data field AM2 data mark or deleted data mark is written, the command is terminated when the type 4 command is written and an interrupt is generated. The type 4 command, which is written during disk write operation for the data field subsequent to the above mark writing, is also acknowledged immediately and the disk write operation is terminated.

The CPU system must write the data into the data register during the service period mentioned at the beginning of Section 10 dealing with the Description of Operation with data request output DTRQ during the disk write operation. When the data is not written during the same service period, the command is continued with 00 (HEX) as the data which is written. The lost data status bit is set at this time. DRTQ is not reset if it is not serviced.

During the disk write operation, the early output or the late output is made active in accordance with the write data. Both output signals are used when the user provides write pre-compensation for the write data output, and they predict late or early peak shifts of the disk write data which is output at the same time.

The TG43 output is used to control the writing current of the floppy disk system. It is "0" at the time when the track register contents are 0 to 43, while it is "1" at 44 or above (up to 255).

# 11. DESCRIPTION OR COMMANDS

## 11.1 Command Standby Condition

After the execution of a command has been completed, the M5W1791-02P stands by for the next command to be executed. If the head load HDLD has been set to "1" by the previous command and 15 index pulses are counted in the standby condition, the head is unloaded from the media. After this the M5W1791-02P remains into the command standby condition. When a command is written in the command register, the M5W1791-02P comes into operation according to the execution flow for the command.

## 11.2 Type 1 Commands

### (1) Restore Command

This command is used to position the head to track 00. This command is automatically executed when the reset input is set from "0" to "1". During reset, the h = "0", V = "0" and $r_1$, $r_0$ = "1, 1" flags are set automatically.

Refer to Section 8 dealing with the hardware configuration and in particular to Section 8.1(3) on the track register for details on the execution of the command. When the V flag is "1", the verify operation is performed after the head opsitioning operation. 00 (HEX) is automatically set in the data register.

### (2) Seek Command

This command is used to move the head onto the desired track. After the destination track number is written into the data register and the seek command is written into the command register, step pulses are generated until the contents of both the track register and data register match. The direction of head movement is indicated by direction output DIRC.

The contents of the track register are updated every time a step pulse is output. When the V flag = "1", the verify operation is perfomed after the head positioning operation.

### (3) Step Command

This generates a single step pulse. Direction output DIRC is not changed. Therefore, the head moves toward the same direction as it did the previous time. When the update flag u is "1", the contents of the track register are updated. When the V flag is "1", the verify operation is performed after the head positioning operation.

### (4) Step-in Command

This command sets direction output DIRC to "1" and generates a single step pulse. When the u flag is "1", the contents of the track regsiter are incremented by 1. When the V flag is "1", the verify operation is performed after the head positioning operation.

### (5) Step-out Command

This command sets direction output DIRC to "0" and generates a single step pulse. When the u flag is "1", the contents of the track register are decremented by 1. When the V flag is "1", the verify operation is performed after the head positioning operation.

## 11.3 Type 2 Commands

Using the type 2 commands, reading/writing the data in the disk's data field is performed. When the desired sector is found, the data is transferred into/from the CPU system using the data request output DTRQ as the data transfer timing signal.

Side number comparison and multi-sector read/write can be performed by setting the command flag.

### (1) Read Sector Command

When the read sector command is executed, once the ID field is found properly, the data is sent from the data shift register to the data register and the M5W1791-02P requests through DTRQ that the CPU system read out the data from the data register. (For details on the service time for DTRQ, refer to Section 10 dealing with the Description of Operation.)

Unless the CPU reads out the data within the service time, the next data is written from the data shift register into the data register. The data which has not been read is destroyed and the lost data status bit is set. DTRQ is reset by the data register readout, but when the data has not been read out during the service time, DTRQ remains at "1".

The length of the data fields in each sector is indicated by the sector length of the disk ID. This value is saved inside the M5W1791-02P and DTRQ is generated for the necessary number of times in accordance with this value.

The relationship between the number of data in a single sector and the data byte length is shown below.

Table 11.3 Data Byte Length

| Sector length of the disk ID | Bytes/sector |
|---|---|
| 00H | 128 bytes |
| 01H | 256 bytes |
| 02H | 512 bytes |
| 03H | 1024 bytes |

When, for instance, the sector length, i.e. the 4th byte of ID is 00 (HEX), data request output DTRQ is "1" for 128 times unless lost data occurs. If, for example, lost data occurs once, DTRQ is "1" for 127 times.

For multi-sector read, refer to the section on flag option m in Table 9.2.

Depending upon the data address mark of the data field, the record type status bit can be set. When the data mark is FB (HEX), the record type status bit is set to "0" and when the deleted data mark is F8 (HEX), it is set to "1".

6

### (2) Write Sector Command

When the ID field is found properly upon execution of the write sector command and the CRC check is completed without any errors detected, the M5W1791-02P generates a single data request output DTRQ. In response to this DTRQ, the CPU must write the data into the data register during the 8-byte time (1-byte time is 32$\mu$s in the single-density mode and 16$\mu$s in the double-density mode with CLK = 2MHz).

Whether or not the service has been performed during the specified time is then determined.

When the service has not been performed in the specified time, the lost data status bit is set, the execution of the command is terminated and interrupt request output INTRQ is set to "1".

When the first service has been performed, the data is written after the sync pattern and AM2 have been written.

After a lost data check, there is a 1-byte time delay (with the single-density mode), then the write gate output WG is set to "1", the 6-byte sync field 00 (HEX) is written into the disk, and FB or F8 (HEX) is written depending on the value of the command's data address mark flag $a_0$. DTRQ is generated and data is written in succession until the number per sector indicated by the ID data length in that sector is reached.

In the double-density mode, the write gate output WG is set to "1" after 12-byte time delay following the lost data check, the 12-byte sync field 00 (HEX) is written, and the 3-byte A1 (HEX) is written, after which the same operation is peformed as for the single-density mode.

Unless the data are written into the data register from the CPU system within the prescribed service time for the second and further DTRQ data request outputs, data 00 (HEX) is written on the disk and the lost data status bit is set. The behavior of the DTRQ output when lost data is generated is the same as that described in the section on the read sector command.

Operations for multi-sector writing are the same as those during the read sector command.

## 11.4 Type 3 Commands

Type 3 commands consist of 3 commands: read address, read track and write track.

### (1) Read Address Command

The 6 bytes of the ID field found first are read out with the execution of the read address command. These 6 bytes in order are: 1) track number, 2) side number, 3) sector number, 4) data length and 5) 2-byte CRC. When data is sent to the data register, data request output DTRQ is generated from the M5W1791-02P and the CPU system is requested to read out the data from the data register. If DTRQ is not serviced within the service time, the lost data status bit is set and the next data is written from the data shift register into the data register as with the read sector command. When the read address command is executed, the track number which has been read out is also written into the sector regsiter of M5W1791-02P along with the CRC check.

### (2) Read Track Command

The read track command serves to read out all the data of an entire track, beginning and ending upon detection of the index pulse. Unlike the read sector or read address commands, all the data including the gaps and sync pattern are read out. The data are synchronized when the index mark, ID address mark and data address mark are detected. "Data synchronization" refers to reading the data string from the floppy disk in 1-byte units. Read gate output RG, which gives notification that the sync pattern has been detected, is not output with this command.

Neither side number comparison nor CRC check is conducted with the read track command. Unless the CPU read out data within the specified service time as with the other disk read command, the data is lost.

### (3) Write Track Command

The write track command formats the tracks on the disk. Disk formatting requires not only that the gaps, sync pattern, ID and data are written, but also that the marker including the missing clock and the CRC are written.

When this command is executed, the first data request output DTRQ is generated after the head has been loaded into the media. In response to this, the CPU must complete the writing of the data whithin the 3-byte time.

Unless the data are serviced during this time, the lost data status bit is set, subsequent commands are terminated the interrupt request output INTRQ is set to "1". When the data is serviced during the specified time, data write starts with the arrival of the index pulse. Then the CPU writes the data into the data register in accordance with the data request output.

When data written by the CPU are values from F5 to FE (HEX), M5W1791-02P performs special processing consisting of writing the markers and generating and writing the CRC. When other data from 00 to F4 and FF (HEX) are written into the data register, the value is modulated as it is and written onto the disk.

The write track command continues until the next index pulse input $\overline{IP}$ is detected.

If the CPU hasn't loaded the data into the data register within the service time, 00 (HEX) is written and the lost data status bit is set.

Table 11.4 shows the control bytes of the write track command.

Table 11.4 Write Track Command Control Bytes

| Data register contents | Single-density format | | | Double-density format | | |
|---|---|---|---|---|---|---|
| | Function | Data pattern | Clock pattern | Function | Data written onto disk | Missing clock |
| 00~F4 | Data ragister values are written onto the disk without modification. | 00~F4 | FF | Data register values are written onto the disk without modification. | 00~F4 | Not generated |
| F5 | Non-usable | | | Marker A1 is written. CRC is preset. | A1 | Generated |
| F6 | Non-usable | | | Marker C2 is written. | C2 | Generated |
| F7 | 2 calculated CRC bytes are written. | 2-byte CRC | FF | 2 calculated CRC bytes are written. | 2-byte CRC | Not generated |
| F8~FB | Writing as data. Used for writing data address mark. CRC is preset. | F8~FB | C7 | Writing as data. Used for writing data address mark. CRC is preset. | F8~FB | Not generated |
| FC | Index mark FC is written. | FC | D7 | Index mark FC is written. | FC | Not generated |
| FA | Writing as data. | FD | FF | Writing as data. | FD | Not generated |
| FE | ID address mark is written. CRC is preset. | FE | C7 | ID address mark is written. CRC is preset. | FE | Not generated |
| FF | Writing as data. | FF | FF | Writing as data. | FF | Not generated |

Note : Hexadecimal notation is used throughout.

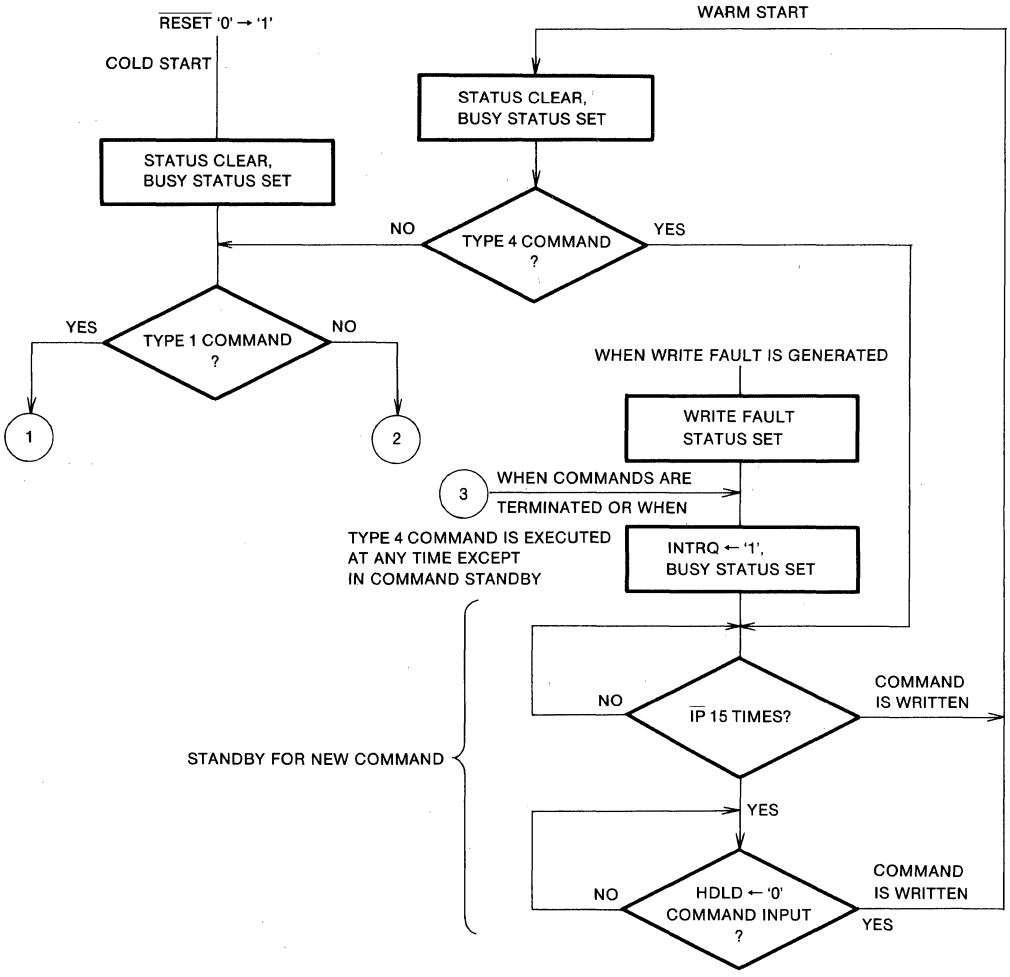
## 11.5 Type 4 Commands

This command generates the interrupt through detection of conditions or generates the unconditional interrupt other commands may be executed only it the M5W1791-02P is in the standby condition (busy status bit is "0"), but the type 4 command may be executed at any time.

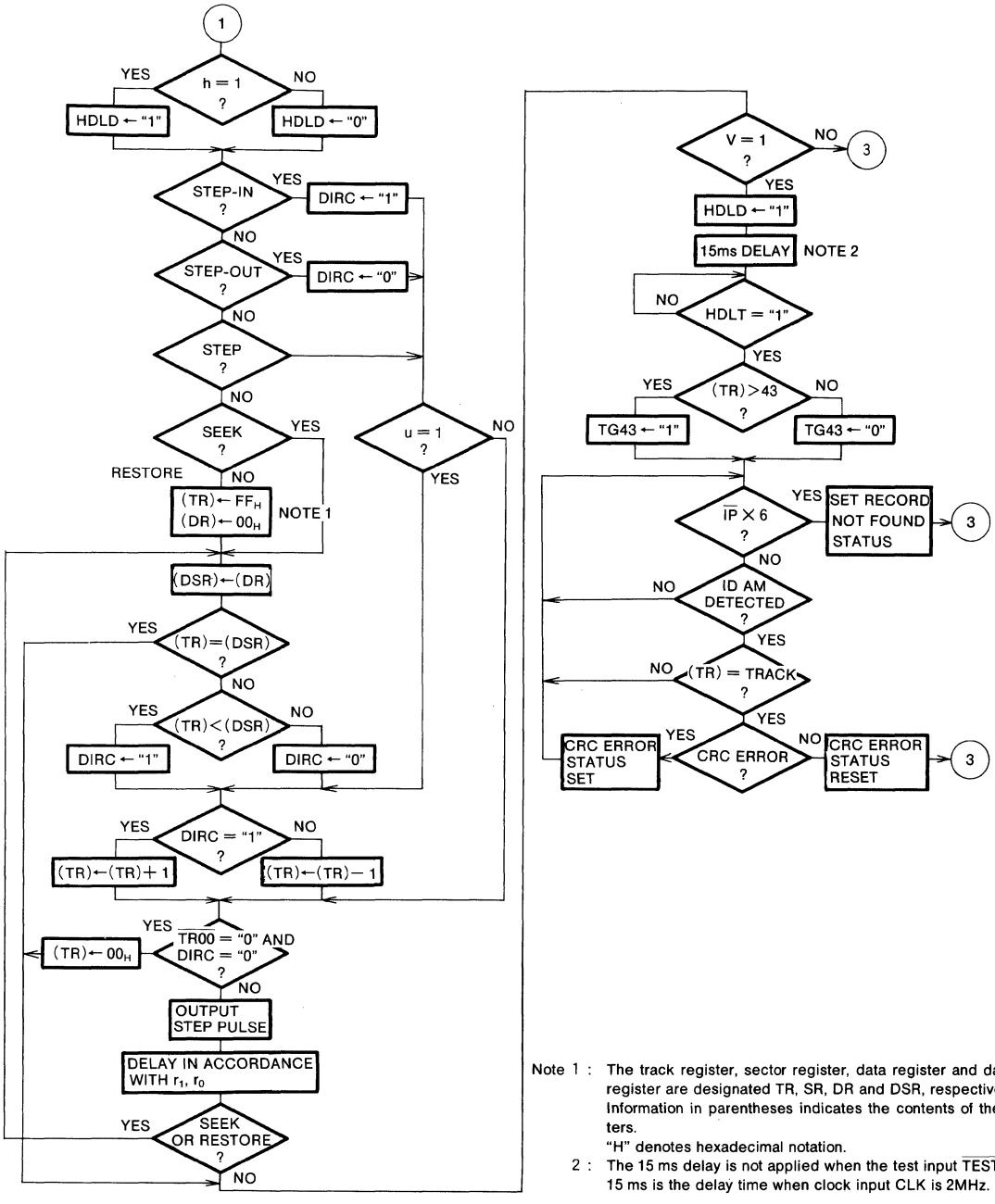
When a preceding command is being executed, it is suspended and operation is keyed to the flag bit of the type 4 command. Refer to Table 9.2 for the flag bits.

Interrupt request output INTRQ generated by the type 4 command is reset by reading the stauts register data or executing a command after the execution of the type 4 command with $I_0 \sim I_3 =$ "0".

## COMMAND STANDBY CONDITION



## TYPE 1 COMMAND

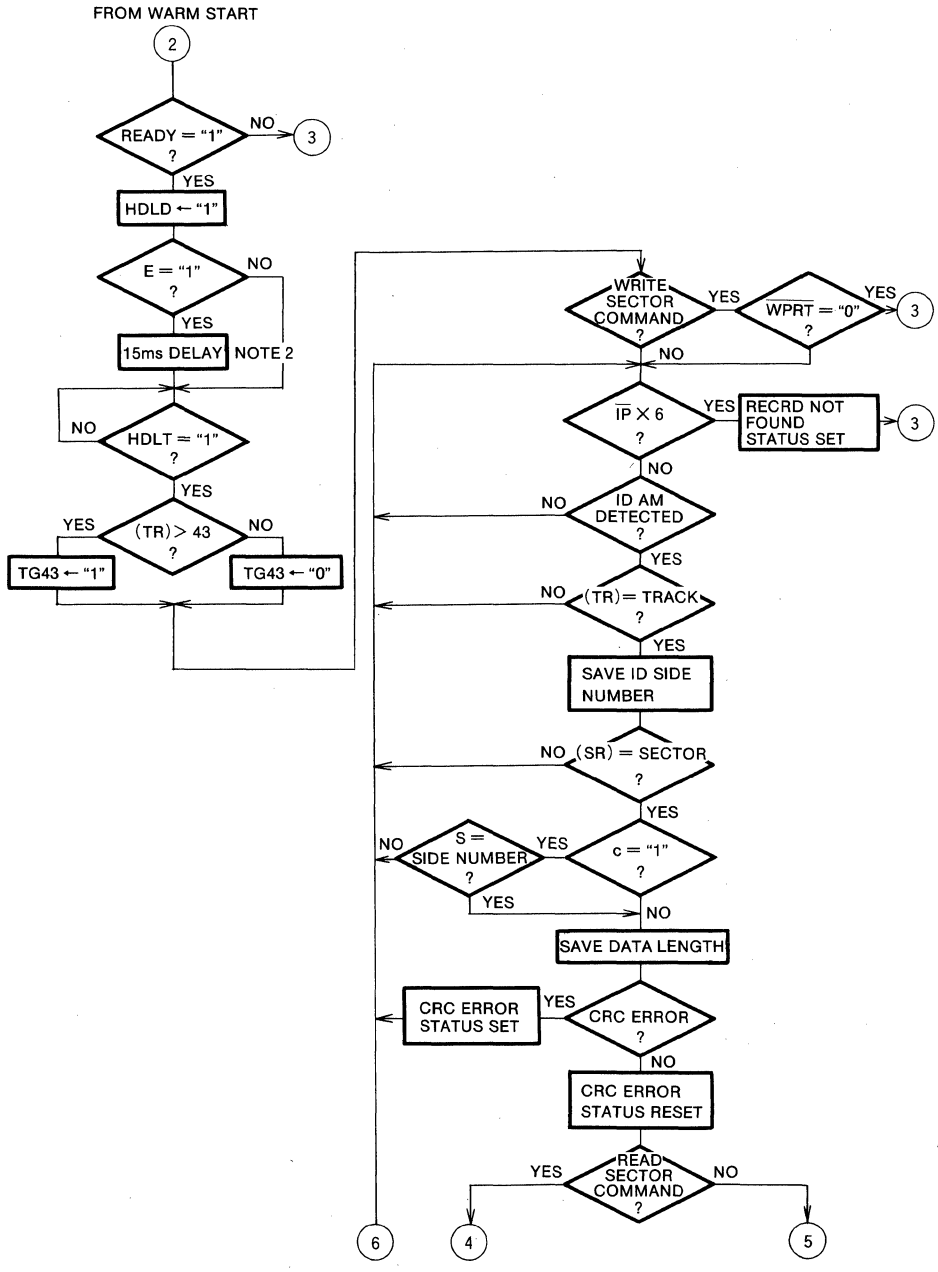


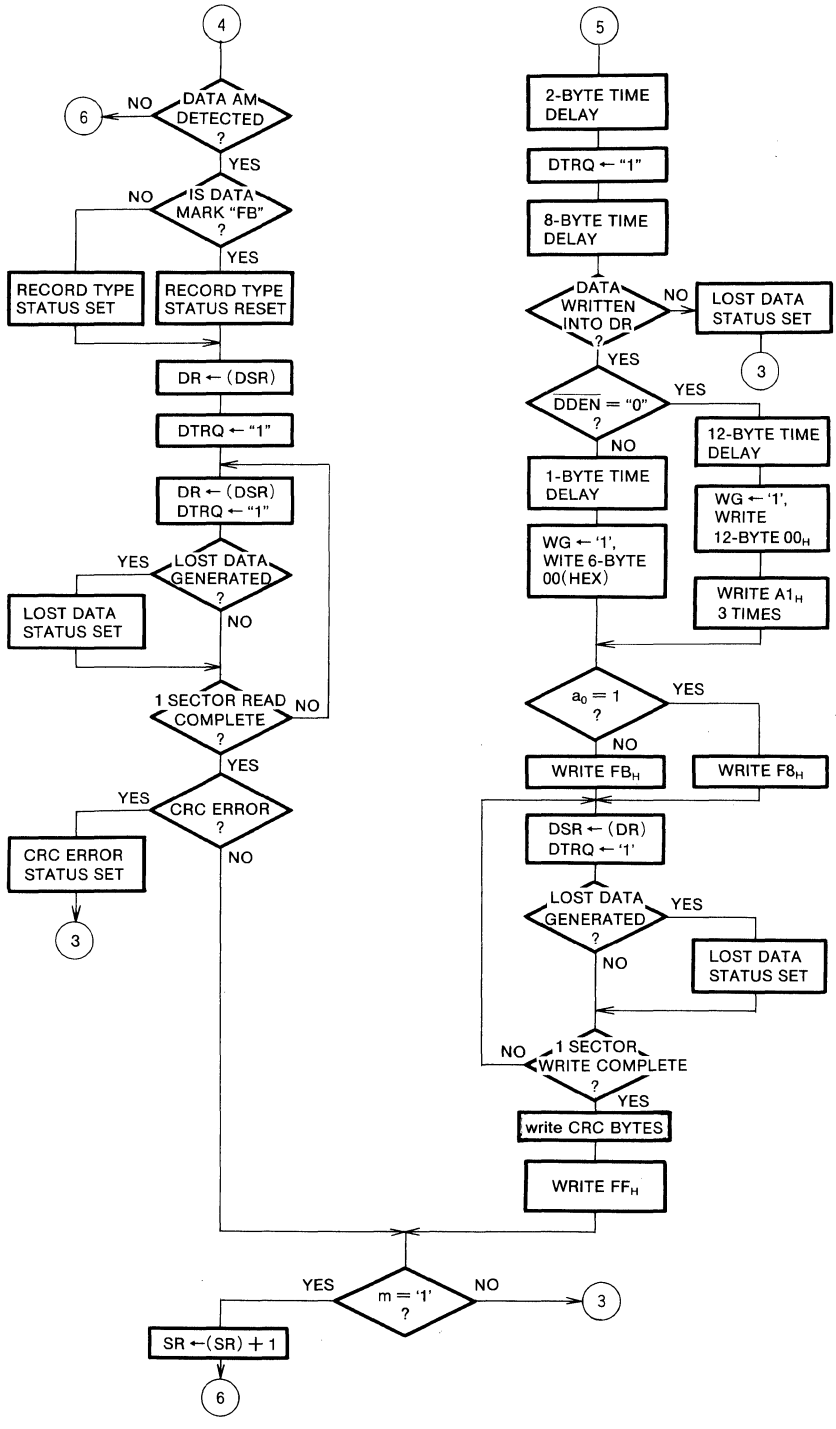

Note 1 : The track register, sector register, data register and data shift register are designated TR, SR, DR and DSR, respectively. Information in parentheses indicates the contents of the registers.
"H" denotes hexadecimal notation.

2 : The 15 ms delay is not applied when the test input $\overline{TEST}$ is "0". 15 ms is the delay time when clock input CLK is 2MHz.

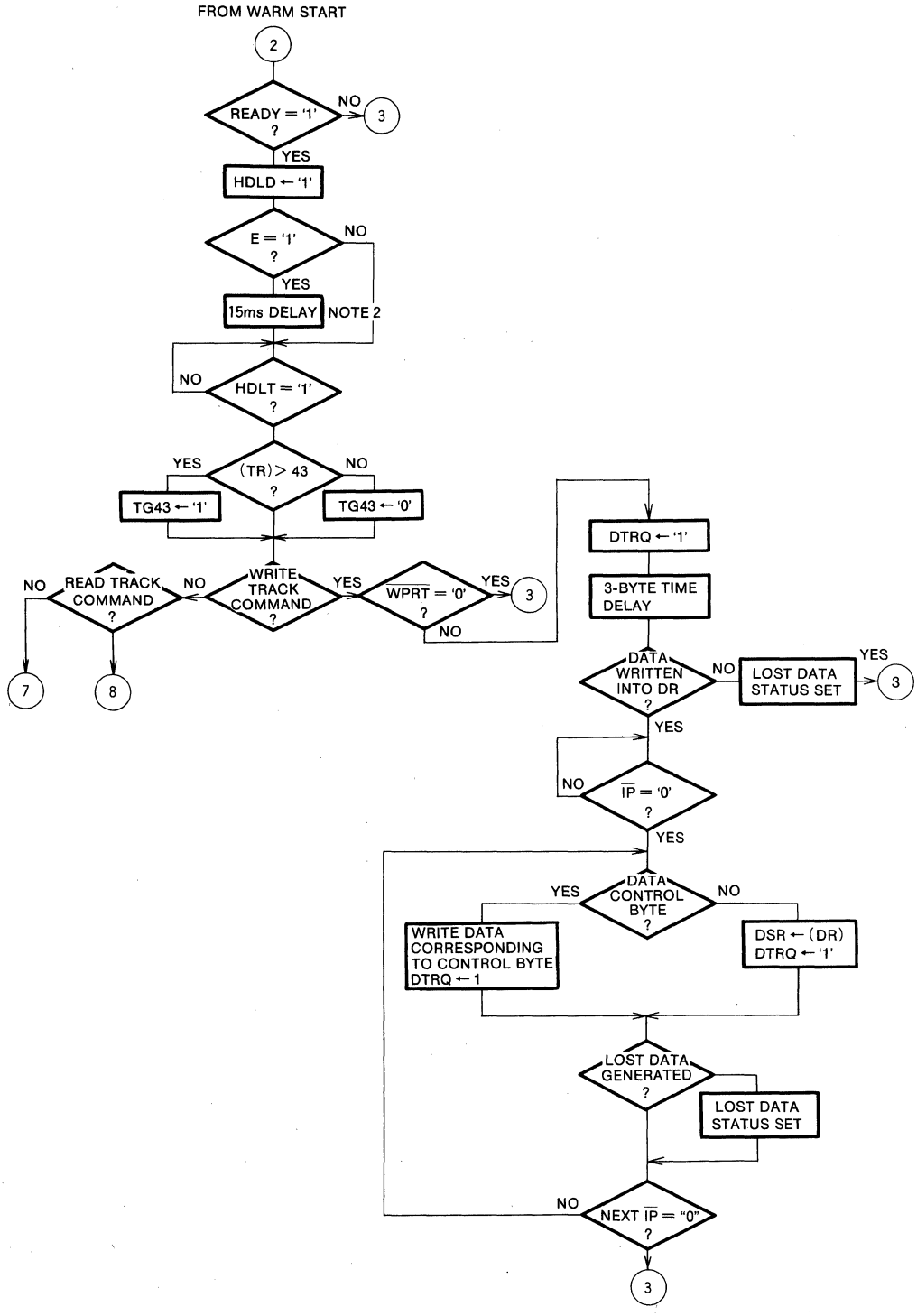
6

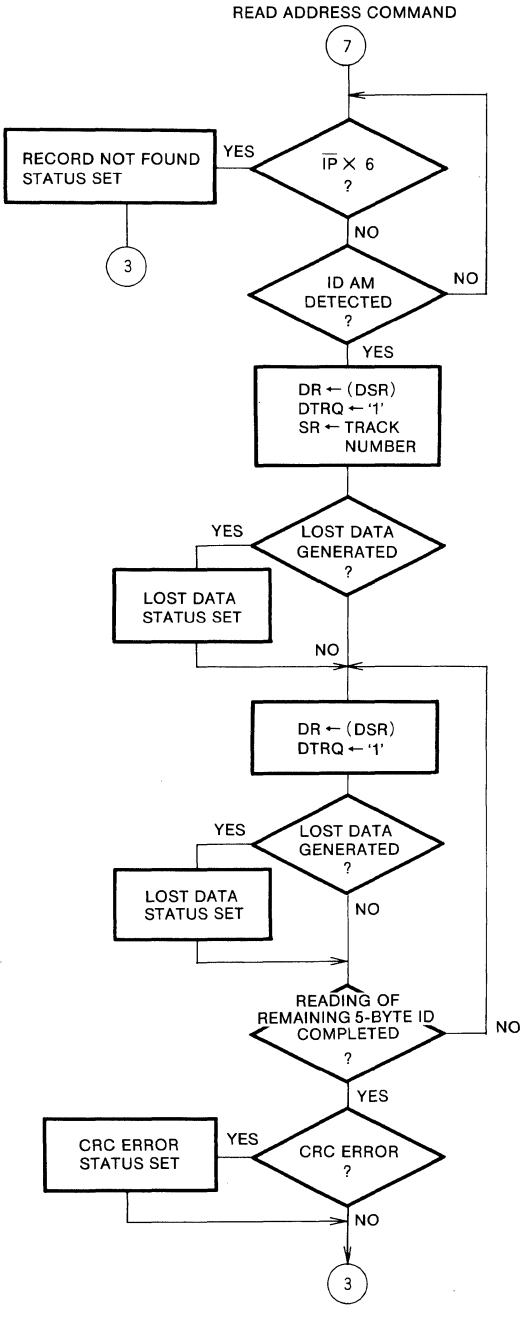
## TYPE 2 COMMAND

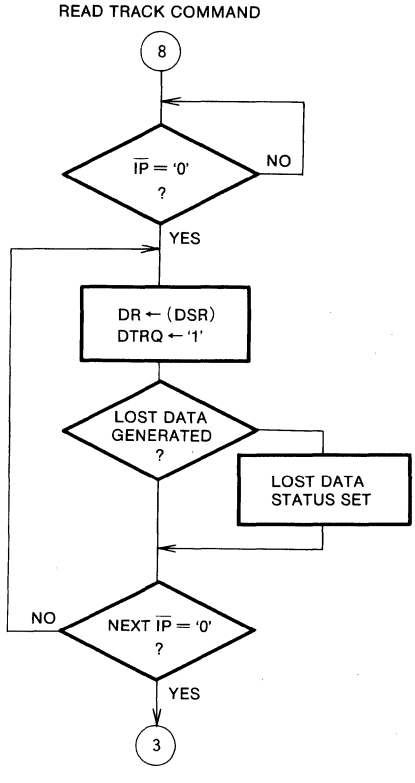



4
DATA AM DETECTED ?
NO
6
YES
IS DATA MARK "FB" ?
NO
YES
RECORD TYPE STATUS SET
RECORD TYPE STATUS RESET
DR ← (DSR)
DTRQ ← "1"
DR ← (DSR)
DTRQ ← "1"
LOST DATA GENERATED ?
YES
LOST DATA STATUS SET
NO
1 SECTOR READ COMPLETE ?
NO
YES
CRC ERROR ?
YES
CRC ERROR STATUS SET
NO
3
5
2-BYTE TIME DELAY
DTRQ ← "1"
8-BYTE TIME DELAY
DATA WRITTEN INTO DR ?
NO
LOST DATA STATUS SET
3
YES
DDEN = "0" ?
YES
NO
12-BYTE TIME DELAY
1-BYTE TIME DELAY
WG ← '1', WRITE 12-BYTE 00H
WG ← '1', WITE 6-BYTE 00(HEX)
WRITE A1H 3 TIMES
a0 = 1 ?
YES
NO
WRITE FBH
WRITE F8H
DSR ← (DR)
DTRQ ← '1'
LOST DATA GENERATED ?
YES
NO
LOST DATA STATUS SET
NO
1 SECTOR WRITE COMPLETE ?
YES
write CRC BYTES
WRITE FFH
YES
m = '1' ?
NO
3
SR ← (SR) + 1
6

## TYPE 3 COMMAND




READ ADDRESS COMMAND
7
RECORD NOT FOUND
STATUS SET
YES
IP × 6
?
NO
3
ID AM
DETECTED
?
NO
YES
DR ← (DSR)
DTRQ ← '1'
SR ← TRACK
NUMBER
YES
LOST DATA
GENERATED
?
LOST DATA
STATUS SET
NO
DR ← (DSR)
DTRQ ← '1'
YES
LOST DATA
GENERATED
?
LOST DATA
STATUS SET
NO
READING OF
REMAINING 5-BYTE ID
COMPLETED
?
NO
YES
CRC ERROR
STATUS SET
YES
CRC ERROR
?
NO
3


READ TRACK COMMAND
8
IP = '0'
?
NO
YES
DR ← (DSR)
DTRQ ← '1'
LOST DATA
GENERATED
?
LOST DATA
STATUS SET
NO
NEXT IP = '0'
?
YES
3

6

## 12. STATUS

The significance of the bits in the status register differs according to the command. The bit 0 of the status register is set during type 1, 2 and 3 commands to indicate the busy status. When this bit is set, the other status bits may be reset or updated. When the type 4 command has been executed, the busy status bit is reset, but whether the remaining status bits are reset or not depends on whether the previous command is being performed or not when the type 4 command is issued. When M5W1791-02P is in standby, the remaining status bits are reset or updates according to the same status bit configuration as the type 1 command. When the type 4 command has been issued during the execution of the pervious command, the remaining status bits show the status of the previous command.

Tables 12.1 and 12.2 show the significance of each status bit.

Tabl 12.1 Status Composition

| Command \ Status bit | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Type 1 command | | Not ready | Write protect | Head loaded | Seek error | CRC error | Track 00 | Index | Busy |
| Type 2 command | Read sector | Not ready | 0 | Record type | Record not found | CRC error | Lost data | Data request | Busy |
| | Write sector | Not ready | Write protect | Write fault | Record not found | CRC error | Lost data | Data request | Busy |
| Type 3 command | Read address | Not ready | 0 | 0 | Record not found | CRC error | Lost data | Data request | Busy |
| | Read track | Not ready | 0 | 0 | 0 | 0 | Lost data | Data request | Busy |
| | Write track | Not ready | write protect | Write fault | 0 | 0 | 0 | Data request | Busy |
| Type 4 command | No preceding Command | Not ready | Write protect | Head loaded | 0 | 0 | Track 00 | Index | 0 |
| | Preceding command | Same as definition of status bit based on preceding command. | | | | | | | 0 |

Tabe 12.2 Status Register Contents

| Command | Status bit | Status | Status Significance |
|---|---|---|---|
| Type 1 | 7 | Not ready | "1" denotes that the disk is not ready. This status is provided by the OR relationship between the READY input inverted signal and the $\overline{\text{RESET}}$ input inverted signal. |
| | 6 | Write protect | "1" denotes that the disk is in the write protect status. This status is the inverted signal of the write protect input $\overline{\text{WPRT}}$. |
| | 5 | Head loaded | "1" denotes that the head has been loaded onto the disk and stabilized. This status is provided by the AND relationship between the head load output HDLD and head load timing input HDLT. |
| | 4 | Seek error | "1" denotes that the verify opration was not successful. This status is reset at the beginning of the following command execution. |
| | 3 | CRC error | "1" denotes that there is a CRC error in the ID field. This status is reset at the beginning of the next command execution. (Note 1) |
| | 2 | Track 00 | "1" denotes that the head is on track 00. This status is the inverted signal of the track 00 input $\overline{\text{TR00}}$. |
| | 1 | Index | "1" denotes that the index pulse input $\overline{\text{IP}}$ is active. This status is the inverted signal of $\overline{\text{IP}}$. |
| | 0 | Busy | "1" denotes that the type 1 command is being executed. After the CPU has written the command, a maximum of 24 clocks for single density and 12 clocks for double-denisty are required for the busy status flag to be set. |
| Type 2/ Type 3 | 7 | Write protect | "1" denotes that the disk is not ready. This status is produced by the OR relationship between the READY input inverted signal and the $\overline{\text{RESET}}$ input inverted signal. |
| | 6 | Write protect | "1" denotes that the disk is in the write protect status. This status is the write protect input $\overline{\text{WPRT}}$ inverted signal. |
| | 5 | Record type<br>Write fault | The record type is set during read. "1" denotes that the address mark of the data field was the deleted data mark. "0" denotes that it was the data mark.<br>During write operations, "1" denotes that the command has been suspended by the write fault input.<br>This status is reset when the next command execution begins (Note 1) |
| | 4 | Record not found | "1" denotes that the designated ID has not been properly detected. This status is reset when the next command execution begins. (Note 1) |
| | 3 | CRC error | "1" denotes that a CRC error is detected in the ID field or data field.<br>This status is reset when the following command execution begins. (Note 1) |
| | 2 | Lost data | "1" denotes that lost data have arisen. This status is reset when the following command execution begins. (Note 1) |
| | 1 | Data request | "1" denotes that reading data from writing data to the data register is requested. This status is the same as the data request output DTRQ. |
| | 0 | Busy | "1" denotes that the command is being executed. After the CPU system has written the command, a maximum of 24 clocks for single-density and 12 clocks for double-denisty are required until the busy status flag is set. |

Note 1 : Refer to Table 12.1 for details when the type 4 command is executed.

6

## 13. DISK FORMATTING

Disk formatting is performed by the write track command. Formatting examples are giben below for both single-density 128 bytes/sector based on the IBM 3740 format and double-density 256 bytes/sector based on the IBM system 34 format.

Table 13.1 Disk IBM 3740 Format

| Transfer byte number | Transfer data (HEX) | Significance of transfer bytes |
|---|---|---|
| 40 | FF | Gap 4 |
| 6 | 00 | Sync pattern |
| 1 | FC | index mark |
| 26 | FF | Gap 1 |
| (Note 1) 6 | 00 | Sync Pattern |
| 1 | FE | ID address mark |
| 1 | 00~4C | Track number |
| 1 | 00 or 01 | Side number |
| 1 | 01~1A | Sector number |
| 1 | 00 | Data length |
| 1 | F7 | 2-byte CRC write |
| 11 | FF | Gap 2 |
| 6 | 00 | Sync pattern |
| 1 | FB | Data mark |
| 128 | E5 | Data |
| 1 | F7 | 2-byte CRC write |
| 27 | FF | Gap 3 |
| (Note 2) 247 | FF | Gap |

Note 1 : This sequence is repeated 26 times while the sector number is updated. The formatting of one track is then completed.
2 : This is the standard value which keeps sending the FF data until the interrupt request output INTRQ is set.

Table 13.2 Disk IBM System 34 Format

| Transfer byte number | Transfer data (HEX) | Significance of transfer bytes |
|---|---|---|
| 80 | 4E | Gap 4 |
| 12 | 00 | Sync pattern |
| 3 | F6 | index mark |
| 1 | FC | index mark |
| 50 | 4E | Gap 1 |
| (Note 1) 12 | 00 | Sync Pattern |
| 3 | F5 | ID address mark |
| 1 | FE | ID address mark |
| 1 | 00~4C | Track number |
| 1 | 00 or 01 | Side number |
| 1 | 01~1A | Sector number |
| 1 | 01 | Data length |
| 1 | F7 | 2-byte CRC write |
| 22 | 4E | Gap 2 |
| 12 | 00 | Sync pattern |
| 3 | F5 | Data address mark |
| 1 | FB | Data mark |
| 256 | 40 | Data |
| 1 | F7 | 2-byte CRC write |
| 54 | 4E | Gap 3 |
| (Note 2) 598 | 4E | Gap 4 |

Note 1 : This sequence is repeated 26 times while the sector number is updated. The formatting of one track is then completed.
2 : This is the standard value which keeps sending the 4E data until the interrupt request output INTRQ is set.

## 14. TRACK FORMAT

Track format is given in Fig. 14.

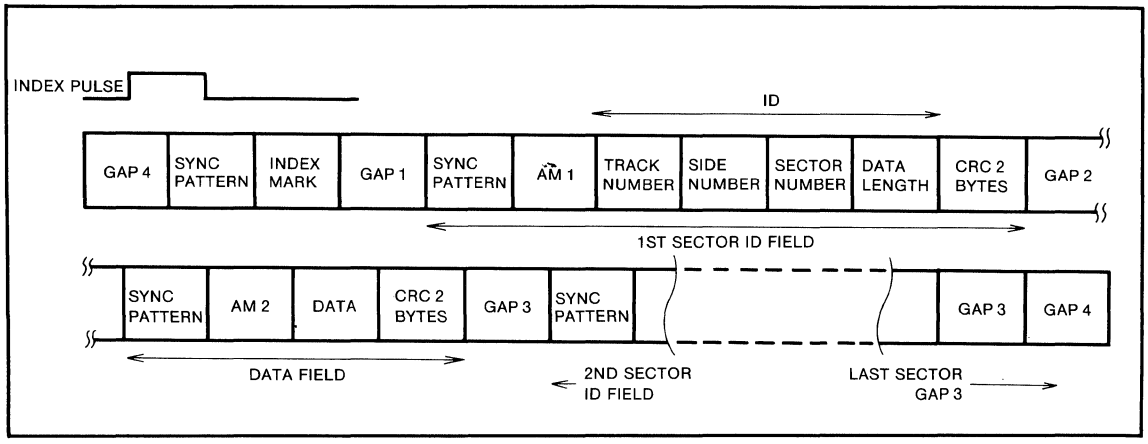



Fig. 14 Track format

## 15. TYPICAL EXTERNAL READ CLOCK GENERATOR CIRCUIT

A read clock must be applied from an external oscillator with the M5W1791-02P. Described below is an example of an external read clock generator circuit used for an 8-inch floppy disk and employing a PLL circuit.

The circuit itself is an analog PLL circuit containing a voltage-controlled oscilator (VCO) with a center frequency of 8MHz. It is applicable to both single- and double-density modes, and is composed of a phase comparator, filter and VCO. Fig. 15.1 shows the phase coimparator and Fig. 15.2 shows the filter and VCO.

In Fig. 15.1 the phase of the raw data read from the floppy disk is compared with the phase fo the signal produced by dividing the VCO CLOCK. If, as a result, the phases do not match, the VCO frequency is tracked by the $\overline{UP}$ or DOWN signal. When $\overline{VFOE}$ is not active, the reference clock is input.

The filter in Fig. 15.2 acquires the required frequency gain characteristics by means of the NF loop RC elements. $C_1$ is for tracking the VCO with respect to the relatively low frequency fluctuations in the form of flutter during floppy disk rotation, etc. In contrast, $C_2$ is for reducing the VCO gain in the event for relatively high frequency fluctuatiions.

A 74S124 is required for the VCO TTL, since the 74LS124 is not sufficient as the 8MHz voltage-controlled oscillation. $R_1$, $R_2$ and $R_3$ determine the gain. $R_1$ and $R_2$ are resistances from 500 ohms to 3.3 kohms. $R_3$ has a resistance from 2.2 to 4.7 kohms.

$C_1$ has a capacitance of 0.047$\mu$F to 0.3$\mu$F while $C_2$ has a value of 0.001$\mu$F to 0.0033$\mu$F.

$C_3$ has a capacitance of 47pF for generating an 8MHz frequency when VR is set to its center position and the CONT input is made $1/2V_{CC}$, $R_4$ is for setting the operating point of $TR_1$ and it is provided with a resistance of 50 kohms to 1 Mohm.

Care should be taken with parts layout and writing of the VCO circuit, especially for the power supply and ground line of the 74S124. $V_{CC}$ instability causes a marked deterioration in PLL response.

In the above example there is no filter or gain switching by read gate output RG.

Note: The circuit in the example given above has low sensitivity to elements value, and works stably. However, the actual circuit used should be determined with regard to the whole system, including the floppy disk system.

6

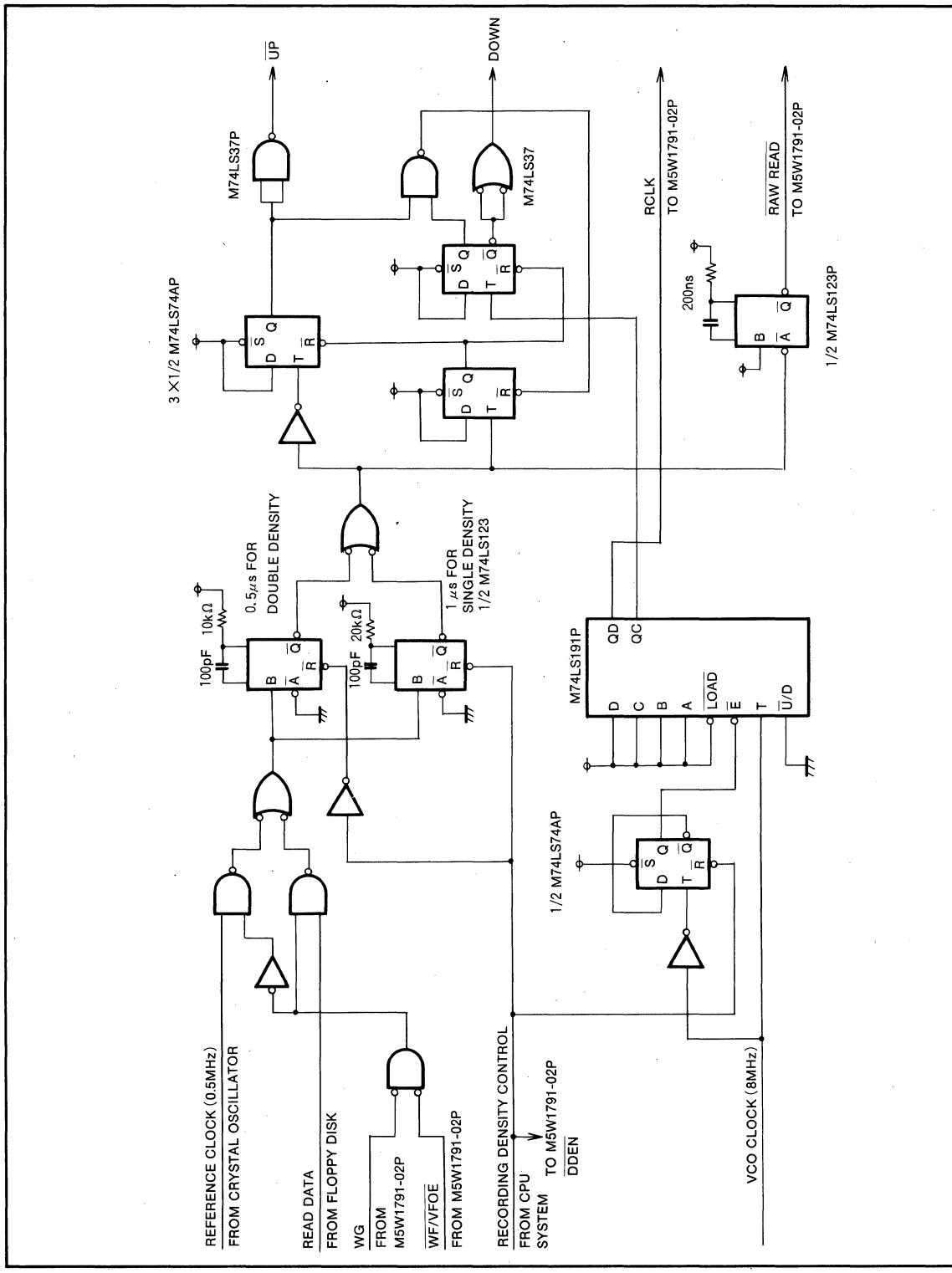



Fig. 15.1 Phase comparator



MITSUBISHI ELECTRIC

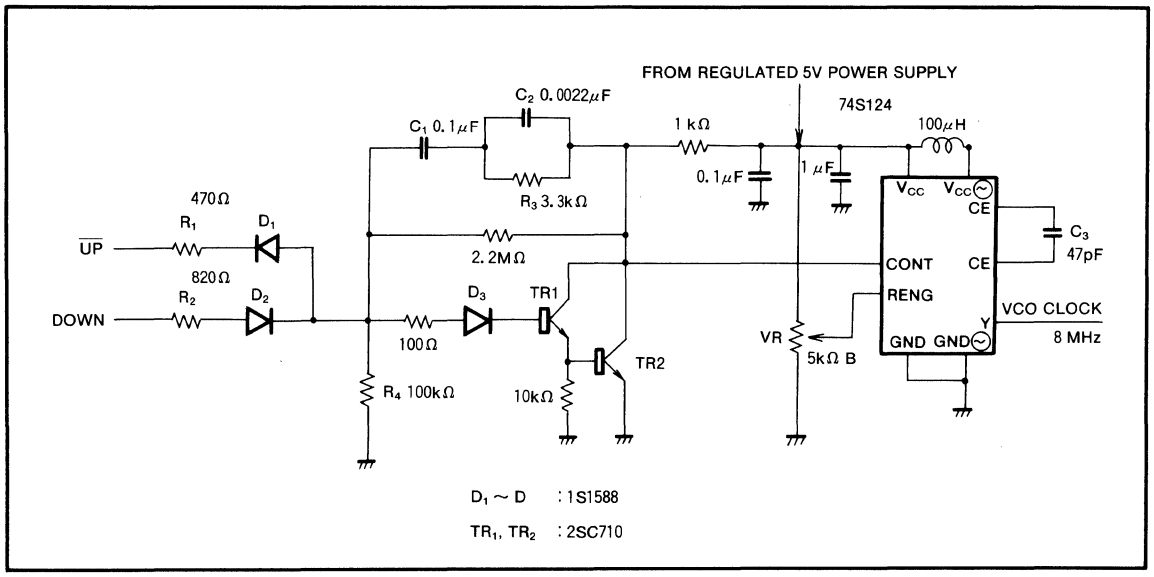



Fig. 15.2 Filter and VCO

## 16. TYPICAL WRITE PRECOMPENSATION CIRCUIT

Fig. 16 gives an example of a write precompensation circuit. The amount of compensation must be set to a value which regulated for the floppy disk system. Clock generator 74S124, for the VCO of the external read clock generator cirucit in Section 15, has 2-channel VCO's so the extra one can be used also. In this case, the write data pulse width of the M74LS153 in Fig. 16 is determined by the clock and if required, it should be converted to the write data pulse width demanded by the floppy disk system using a one-shot multi-vibrator, etc.

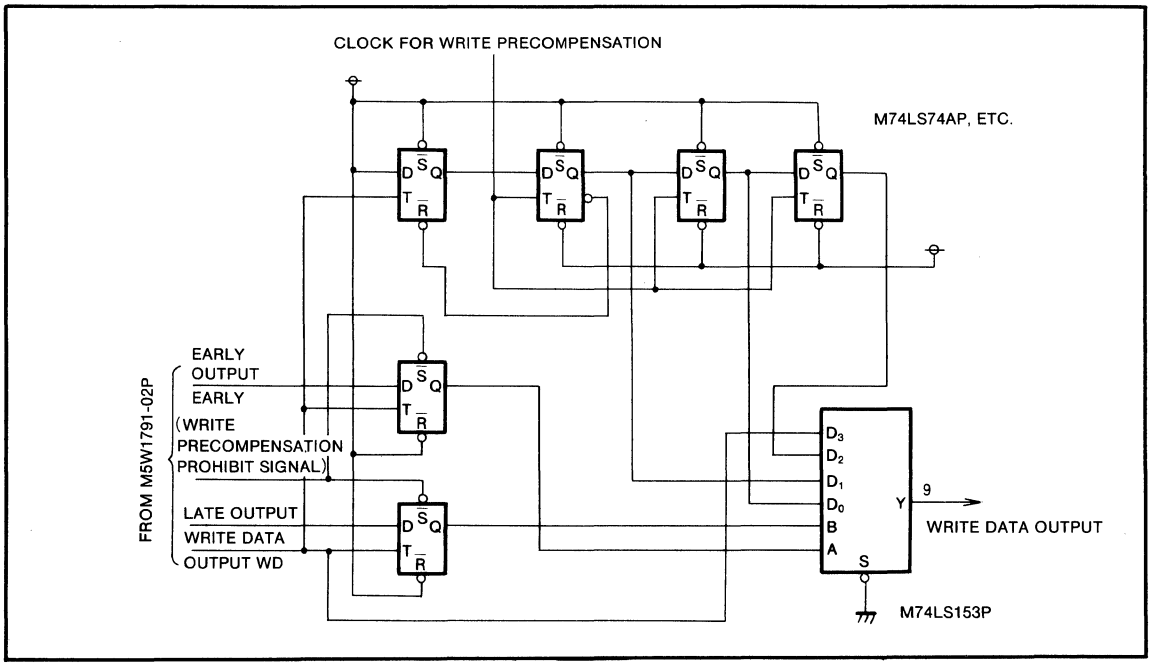



Fig. 16 Write precompensation circuit

## 17. EXAMPLE OF A WRITE GATE OUTPUT AND WRITE FAULT/VFO ENABLE CIRCUIT

The $\overline{WF}/\overline{VFOE}$ serves as the write fault input or VFO enable output, depending on the WG output.

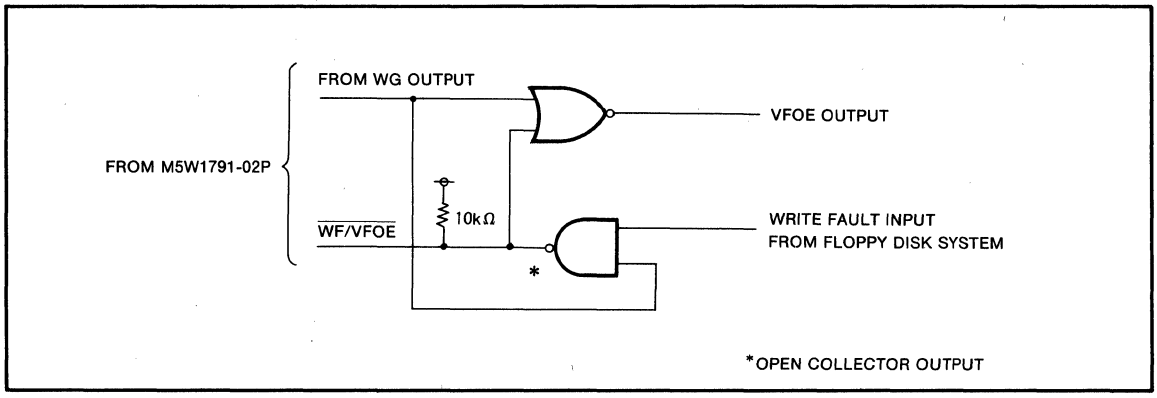
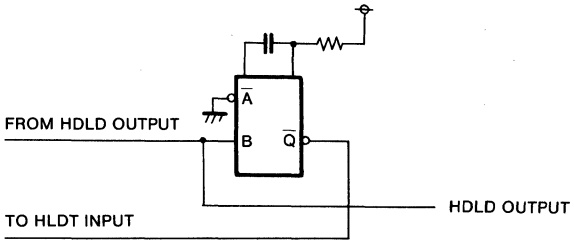



**Fig. 17 Write fault/VFOE control circuit**

## 18. AN EXAMPLE OF THE HEAD LOAD OUTPU AND HEAD LOAD TIMING CIRCUIT

The head load timing input is made available after the settling time has elapsed from the head load output.



# 19 ELECTRICAL CHARACTERISTICS

## 19.1 ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −0.5～7 | V |
| $V_I$ | Input voltage | | −0.5～7 | V |
| $V_O$ | Output voltage | | −0.5～7 | V |
| $P_d$ | Power dissipation | $T_a$=25℃ | 350 | mW |
| $T_{opr}$ | Operating free-air temperature range | | 0～70 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65～150 | ℃ |

## 19.2 RECOMMENDED OPERATING CONDITIONS ($T_a$=0～70℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | $V_{SS}$−0.5 | | 0.8 | V |

## 19.3 ELECTRICAL CHARACTERISTICS ($T_a$=0～70℃, $V_{CC}$=5V±5%, unless otherwise noted)

| Symbol | Parameter | Test condition | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$=−200μA | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$=1.8mA | | | 0.4 | V |
| $I_{CC}$ | Supply current | | | | 70 | mA |
| $I_I$ | Input current.(HDLT, $\overline{TEST}$, $\overline{WF/VFOE}$, $\overline{WPRT}$, $\overline{DDEN}$) | $V_I$=$V_{CC}$～0V | −100 | | 10 | μA |
| | Input current other inputs | $V_I$=$V_{CC}$～0V | −10 | | 10 | μA |
| $I_{OZ}$ | Off-state output current | $V_I$=$V_{CC}$～0V | −10 | | 10 | μA |

6

## 19.4 TIMING REQUIREMENTS ($T_a$=0~70℃, $V_{CC}$=5V±5%, $V_{SS}$=0V, unlese otherwise noted)

| Symbol | Parameter | Alternative symbol | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{su(A-R)}$ $t_{su(CS-R)}$ | Address setup time before read and chip select | TSET | | 50 | | | ns |
| $t_{h(R-A)}$ $t_{h(R-CS)}$ | Address hold time after read and chip select | THLD | | 10 | | | ns |
| $t_{W(R)}$ | Read pulse width | TRE | $C_L$=50pF | 280 | | | ns |
| $t_{su(A-W)}$ $t_{su(CS-W)}$ | Address setup time before write and chip select | TSET | | 50 | | | ns |
| $t_{h(W-A)}$ $t_{h(W-CS)}$ | Address hold time after write and chip select | THLD | | 10 | | | ns |
| $t_{W(W)}$ | Write pulse width | TWE | | 200 | | | ns |
| $t_{su(DQ-W)}$ | Data setup time before write | TDS | | 250 | | | ns |
| $t_{h(W-DQ)}$ | Data hold time after write | TDH | | 20 | | | ns |
| $t_{W(RR)}$ | Raw read pulse width | $T_{PW}$ | (Note1. 2) | 100 | | 250 | ns |
| $t_{C(RR)}$ | Raw read cycle time | Tbc | (Note 3) | 1600 | 2000 | | ns |
| $t_{W(RCLK)}$ | Read clock high-level width | Ta | (Note 4) | 800 | | | ns |
| $t_{W(\overline{RCLK})}$ | Read clock low-level width | Tb | (Note 4) | 800 | | | ns |
| $t_{C(RCLK)}$ | Read clock cycle time | Tc | | 1600 | | | ns |
| $t_{h(RCLK-RR)}$ | Read clock hold time before raw read | $T_{x1}$ | | 40 | | | ns |
| $t_{h(RR-RCLK)}$ | Read clock hold time after raw read | $T_{x2}$ | FM | 40 | | | ns |
| | | | MFM | 40 | | | ns |
| $t_{W(WD)}$ | Write data pulse width | Twp | FM | 450 | 500 | 550 | ns |
| | | | MFM | 150 | 200 | 250 | ns |
| $t_{C(WD)}$ | Write data cycle time | Tbc | | | 2, 3, 4 | | μs |
| $t_{W(\phi)}$ | Clock high-level pulse width | $TCD_1$ | | 230 | 250 | 20000 | ns |
| $t_{W(\overline{\phi})}$ | Clock low-level pulse width | $TCD_2$ | | 200 | 250 | 20000 | ns |
| $t_{W(RESET)}$ | Reset pulse width | TMR | | 50 | | | μs |
| $t_{W(IP)}$ | Index pulse width | TIP | (Note 5) | 10 | | | μs |
| $t_{W(WF)}$ | Write fault pulse width | TWF | (Note 5) | 10 | | | μs |

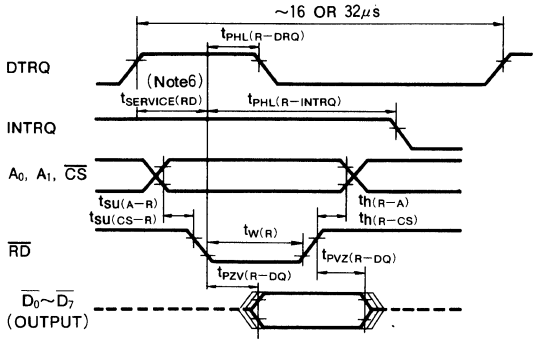
## 19.5 SWITCHING CHARACTERISTICS ($T_a$=0~70℃, $V_{CC}$=5V±5%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Alternative symbol | Test conditidns | Limrts | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| $t_{PLH(WG-WD)}$ | Propagation time from write gate to write data | Twg | FM (Note 5) | | 2 | | μs |
| | | | MFM (Note 5) | | 1 | | μs |
| $t_{PLH(E-WD)}$ $t_{PLH(L-WD)}$ | Propagation time from early or late to write data | Ts | MFM (Note 5) | 125 | | | ns |
| $t_{PHL(WD-E)}$ $t_{PHL(WD-L)}$ | Propagation time from write data to early or late | Th | MFM (Note 5) | 125 | | | ns |
| $t_{PHL(WD-WG)}$ | Propagation time from write data to write gate | Twt | FM (Note 5) | | 2 | | μs |
| | | | MFM (Note 5) | | 1 | | μs |
| $t_{PZV(R-DQ)}$ | Output enable time after read | TDACC | $C_L$=50pF | | | 250 | ns |
| $t_{PVZ(R-DQ)}$ | Output disable time after read | TDOH | $C_L$=50pF | 50 | | 150 | ns |
| $t_{PHL(R-DRQ)}$ | Propagation time from read to DRQ | TDRR(RD) | | | | 250 | ns |
| $t_{PHL(R-INTRQ)}$ | Propagation time from read to INTRQ | TIRR(RD) | (Note 5) | | | 500 | ns |
| $t_{PHL(W-DRQ)}$ | Propagation time from write to DRQ | TDRR(WR) | | | | 250 | ns |
| $t_{PHL(W-INTRQ)}$ | Propagation time from write to INTRQ | TIRR(WR) | (Note 5) | | | 500 | ns |
| $t_{W(STP)}$ | Step pulse width | TSTP | (Note 5) | 2or4 | | | μs |
| $t_{PLH(DIR-STP)}$ | Propagation time from direction to step | TDIR | (Note 5) | 12 | | | μs |
| $t_{V(WD-CLK)}$ | Write data valid time before clock | $Twd_1$ | CLK=1MHz MFM | 200 | | | ns |
| | | | CLK=2MHz MFM | 30 | | | ns |
| $t_{V(CLK-WD)}$ | Write data valid time after clock | $Twd_2$ | CLK=1MHz MFM | 50 | | | ns |
| | | | CLK=2MHz MFM | 50 | | | ns |

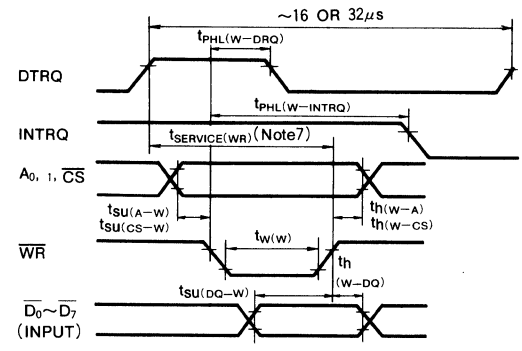
Note 1 : The pulse of $\overline{\text{RAW READ}}$ may be any width if pulse is entirely within RCLK. When the pulse occurs in the RCLK window, $\overline{\text{RAW READ}}$ pulse width must be less than 300 ns for MFM mode and 600 ns for FM mode at CLK=2MHz. Times double for 1MHz.
2 : 100 ns pulse width is recommended for the $\overline{\text{RAW READ}}$ pulse in 8 MFM mode.
3 : $\overline{\text{RAW READ}}$ cycle time $T_{C(RR)}$ and WD cycle time $T_{C(WD)}$ is normally 2μs in MFM and 4μs in FM. Times double when CLK=1MHz.
4 : The polarity of RCLK during $\overline{\text{RAW READ}}$ is not important.
5 : Times double when CLK=1MHz.

## 19.6 TIMING DIAGRAM

### Read

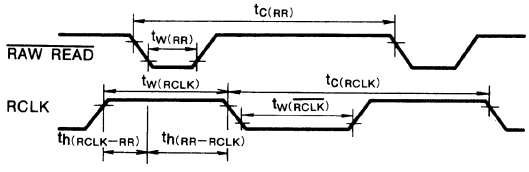



### Write

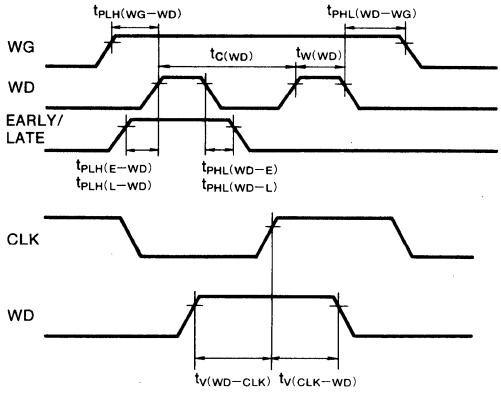



Note 6 : $t_{SERVICE(RD)}$ maximum value, FM: 27.5μs, MFN: 13.5μs
7 : $t_{SERVICE(WR)}$ maximum value; FM: 23.5μs, MFM: 11.5μs

### Input data




### Write data




### Others