

M61531FP

6ch Electronic Volume with 10 Input Selectors

REJ03F0050-0110Z

Rev.1.1

Jun.01.2004

Features

Functions	Features
Electric volume	6 channel independent electric volume with high voltage transistor (0 to -99 dB/1 dB step, -∞ dB)
Input selector	L/R channel 10 input selector
Multi channel input	All channel 2 input selector
Tone Control	(1) Bass: -16 to +16 dB (2 dB step), Treble: -10 to +10 dB (2 dB step) (2) Tone block position is selectable (3) Tone input ATT (0/-6/-12/-18 dB)
Loudness	Built-in loudness circuit of center tap type in L/Rch
REC output	4 Lines REC output (Both L and R channels)
Input ATT	Input ATT (for ADC: 0/-6/-12/-18 dB)
Input gain control	Input gain control (0/+6/+12/+18 dB)
Output gain control	Output gain control (0/+6/+12/+18 dB)
Balance out	Built-in balance out (for ADC)
Bus control	3 wire control, 3 to 5V I/F support

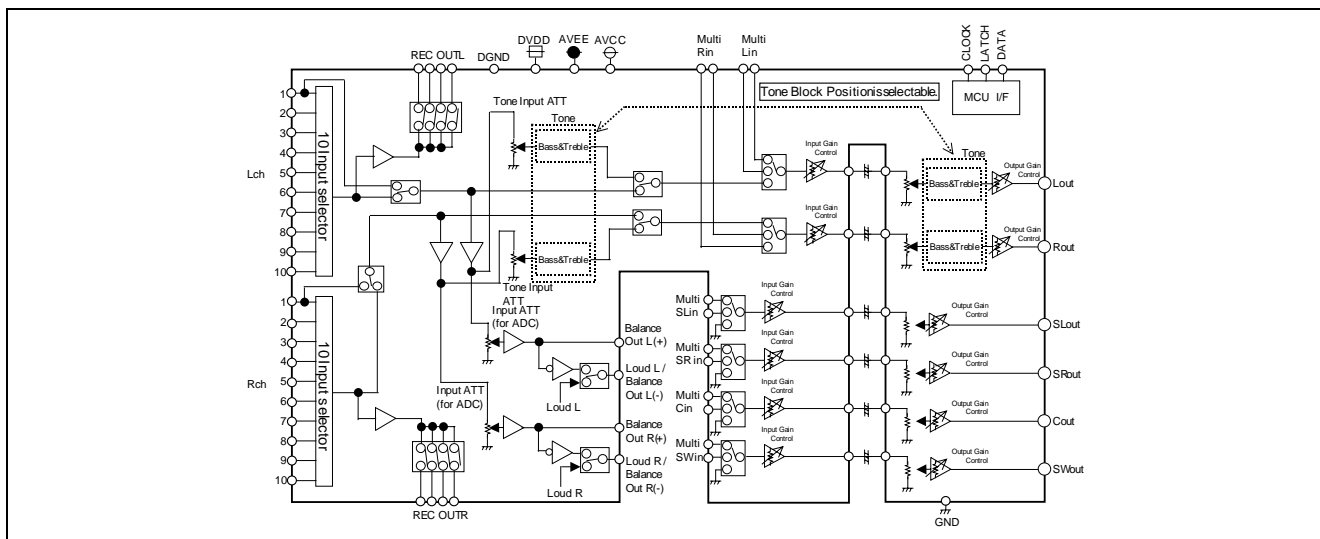
Application

- Receiver, AV Amp, Mini Stereo etc.

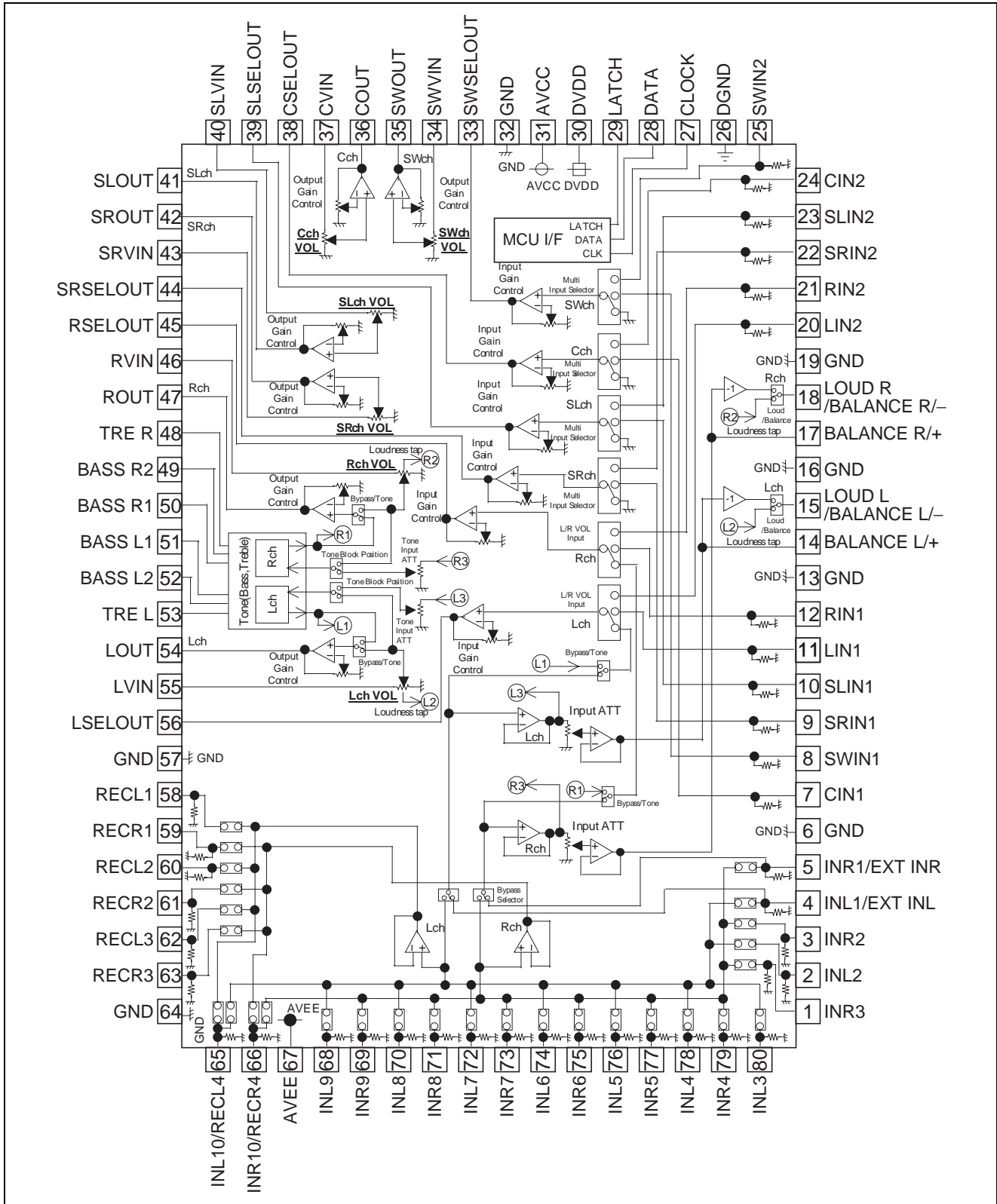
Recommended Operating Condition

- Supply voltage range: AVCC = 7.0 V (Typ.), AVEE = -7.0 V (Typ.), DVDD = 2.7 to 5.5 V

System Block Diagram



Block Diagram and Pin Configuration (Top View)

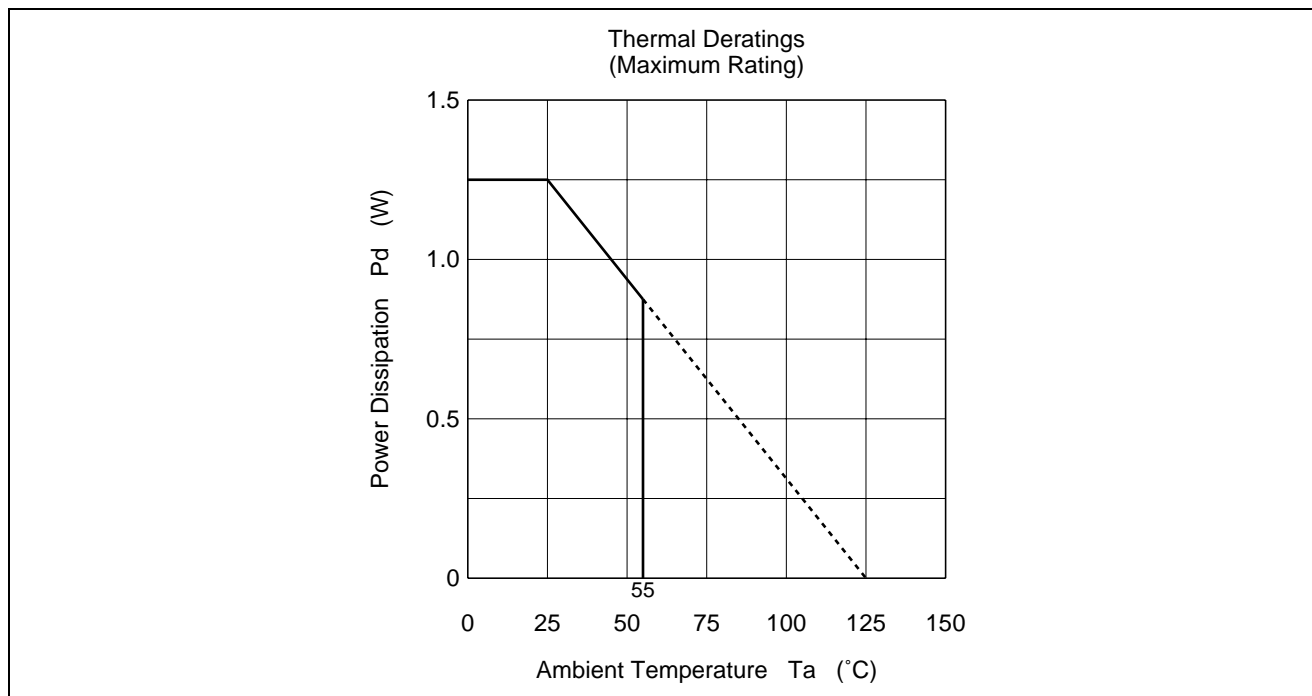


Pin Description

Pin No.	Pin Name	Function
3, 1, 79, 77, 75, 73, 71, 69	INR2, 3, 4, 5, 6, 7, 8, 9	Input pin of R channel (Input Selector)
2, 80, 78, 76, 74, 72, 70, 68	INL2, 3, 4, 5, 6, 7, 8, 9	Input pin of L channel (Input Selector)
4	INL1/EXT INL	Input pin of L channel (Input Selector)/External Input pin(Lch)
5	INR1/EXT INR	Input pin of L channel (Input Selector)/External Input pin(Rch)
6, 13, 16, 19, 32, 57, 64	GND	Analog Ground
7, 24	CIN1/CIN2	Input pin of C channel (2 Input Selector)
8, 25	SWIN1/SWIN2	Input pin of SW channel (2 Input Selector)
9, 22	SRIN1/SRIN2	Input pin of SR channel (2 Input Selector)
10, 23	SLIN1/SLIN2	Input pin of SL channel (2 Input Selector)
11, 20	LIN1/LIN2	Input pin of L channel (2 Input Selector)
12, 21	RIN1/RIN2	Input pin of R channel (2 Input Selector)
14, 17	BALANCE L/+, R/+	Output pin of L/R channel Balance Output(+)
15, 18	LOUD L/BALANCE L/–, LOUD R/BALANCE R/–	Frequency characteristic setting pin of Loudness /Output pin of L/R channel Balance Output(–)
26	DGND	Ground of internal logic circuit
27, 28, 29	CLOCK, DATA, LATCH	Input pin of control clock /data/ trigger
30	DVDD	Power supply to internal logic circuit
31	AVCC	Positive power supply to internal analog circuit
33	SWSELOUT	Output pin of SW channel volume input selector
34	SWVIN	Input pin of SW channel volume
35	SWOUT	Output pin of SW channel
36	COUT	Output pin of C channel
37	CVIN	Input pin of C channel volume
38	CSELOUT	Output pin of C channel volume input selector
39	SLSELOUT	Output pin of SL channel volume input selector
40	SLVIN	Input pin of SL channel volume
41	SLOUT	Output pin of SL channel
42	SROUT	Output pin of SR channel
43	SRVIN	Input pin of SR channel volume
44	SRSELOUT	Output pin of SR channel volume input selector
45	RSELOUT	Output pin of R channel volume input selector
46	RVIN	Input pin of R channel volume
47	ROUT	Output pin of R channel
51, 52, 50, 49	BASS L1, L2/BASS R1, R2	Frequency characteristic setting pin of tone control (BASS)
53, 48	TRE L/TRE R	Frequency characteristic setting pin of tone control (TREBLE)
54	LOUT	Output pin of L channel
55	LVIN	Input pin of L channel volume
56	LSELOUT	Output pin of L channel volume input selector
58, 60, 62/59, 61, 63	REC L1, L2, L3 /REC R1, R2, R3	Output pin of REC (Lch and Rch)
65	INL10/REC L4	Input pin of L channel (Input Selector)/Output pin of REC (Lch)
66	INR10/REC R4	Input pin of R channel (Input Selector)/Output pin of REC (Rch)
67	AVEE	Negative power supply to internal analog circuit

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Condition
Power supply	Supply voltage	± 8.0	V	AVCC-AVEE
		6.0		DVDD-GND
Power dissipation	P_d	1250	mW	$T_a \leq 25^\circ\text{C}$
Thermal derating	$K\theta$	12.5	mW/ $^\circ\text{C}$	$T_a > 25^\circ\text{C}$
Operating temperature	T_{opr}	-20 to +55	$^\circ\text{C}$	
Storage temperature	T_{stg}	-40 to +125	$^\circ\text{C}$	



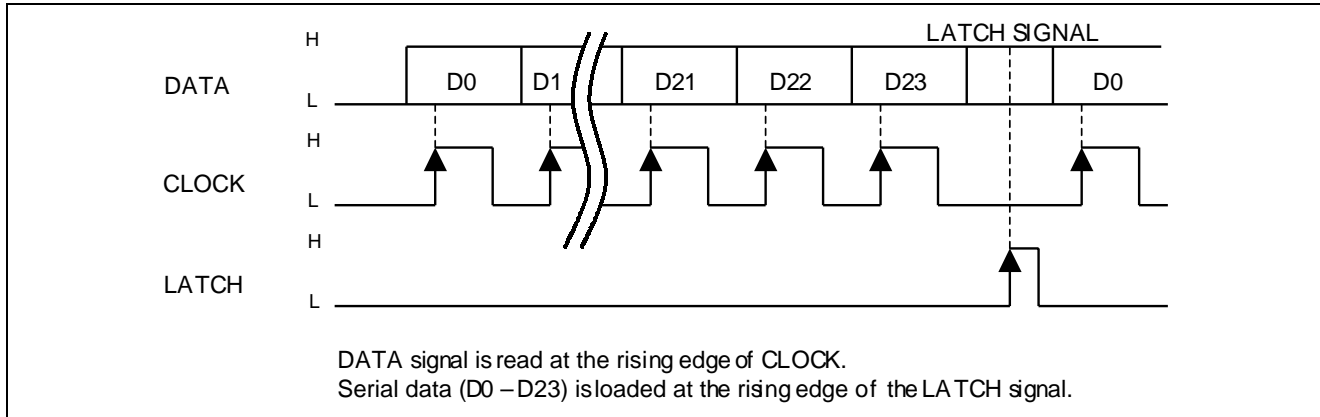
Recommended Operating Conditions

($T_a = 25^\circ\text{C}$, unless otherwise noted)

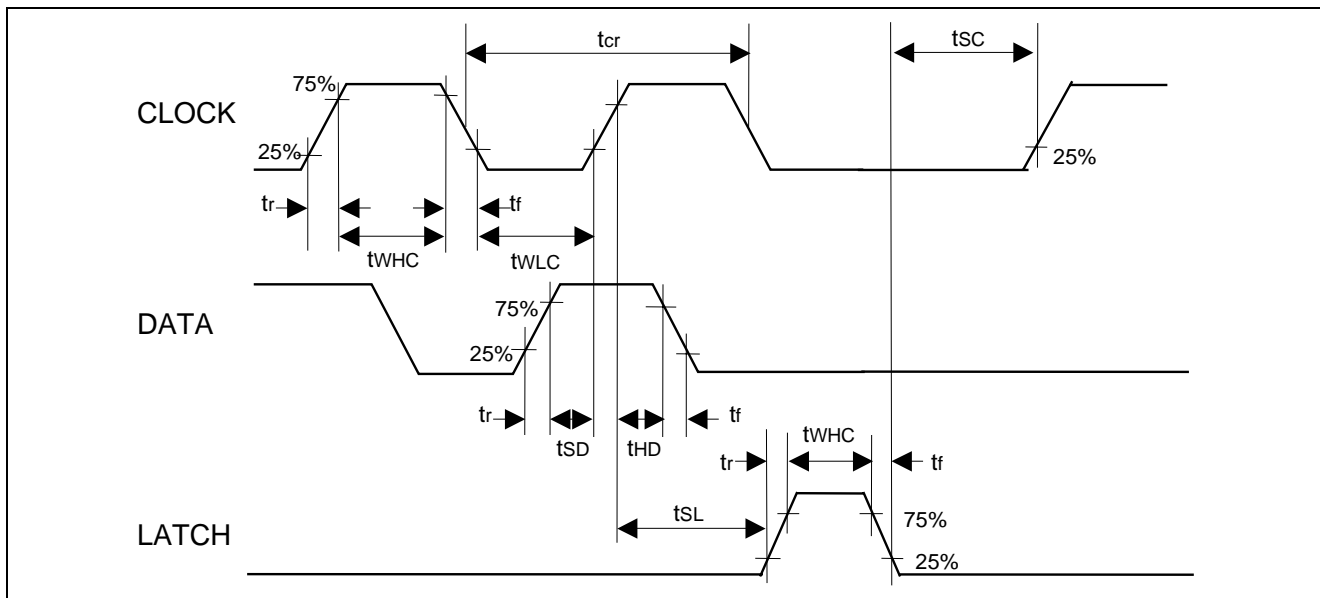
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Analog supply voltage (Positive)	AVCC	4.5	7.0	7.5	V	
Analog supply voltage (Negative)	AVEE	-7.5	-7.0	-4.5	V	
Digital supply voltage	DVDD	2.7	3.3	5.5	V	
Logic "H" level input voltage	V_{IH}	$DVDD \times 0.7$	—	DVDD	V	DGND reference
Logic "L" level input voltage	V_{IL}	DGND	—	$DVDD \times 0.2$	V	DGND reference

Note: $AVEE \leq DGND < DVDD \leq AVCC$

Relationship between Data and Clock



Clock and Data Timings



Timing Definition of Digital Block

Item	Symbol	Min.	Typ.	Max.	Unit
Clock cycle time	t_{cr}	4	—	—	μs
Clock pulse width ("H" level)	t_{whc}	1.6	—	—	μs
Clock pulse width ("L" level)	t_{wlc}	1.6	—	—	μs
Rising time of clock,data and latch	t_r	—	—	0.4	μs
Falling time of clock,data and latch	t_f	—	—	0.4	μs
Data setup time	t_{SD}	0.8	—	—	μs
Data hold time	t_{HD}	0.8	—	—	μs
Latch setup time	t_{SL}	1	—	—	μs
Latch pulse width	t_{whl}	1.6	—	—	μs
Clock setup time	t_{SC}	4	—	—	μs

Data Control Specification

Initialize all data of the 4 formats when digital power supply (DVDD) turn on.
 Prohibit using except specified data code as follows.

D0a	D1a	D2a	D3a	D4a	D5a	D6a	D7a	D8a	D9a	D10a	D11a	D12a	D13a	D14a	D15a	D16a	D17a	D18a	D19a	D20a	D21a	D22	D23						
(1)Input Selector																													
(2)Input ATT				(3) REC Output 1		(3) REC Output 2		(3) REC Output 3		(3) REC Output 4		(4) Multi Input Selector		(5) L/R VOL Input		(6) Input Gain Control		(7) Output Gain Control		(8) INS10 /REC4 Selector		(9) All Ch Output Mute		(10) Multi Input Mute		(5) L/R VOL Input			
				(19)Lch Volume																									
				(19)Rch Volume																									
				(19)Cch Volume																									
D0b	D1b	D2b	D3b	D4b	D5b	D6b	D7b	D8b	D9b	D10b	D11b	D12b	D13b	D14b	D15b	D16b	D17b	D18b	D19b	D20b	D21b	D22	D23						
(19)SLch Volume																													
(19)SRch Volume																													
(19)SWch Volume																													
D0d	D1d	D2d	D3d	D4d	D5d	D6d	D7d	D8d	D9d	D10d	D11d	D12d	D13d	D14d	D15d	D16d	D17d	D18d	D19d	D20d	D21d	D22	D23						
(11)Tone Bass				(12) Tone Input ATT														(13) Bypass /Tone		(14) Tone Block Position		(15) Loudness		(16) Loudness Balance Out		(17) L/R Bypass		(11)Tone Treble	
				(19)SLch Volume																									
				(19)SRch Volume																									
				(19)Cch Volume																									

Setting Code

(1) Input Selector

Setting	D0a	D1a	D2a	D3a
All off	0	0	0	0
IN1	0	0	0	1
IN2	0	0	1	0
IN3	0	0	1	1
IN4	0	1	0	0
IN5	0	1	0	1
IN6	0	1	1	0
IN7	0	1	1	1
IN8	1	0	0	0
IN9	1	0	0	1
IN10	1	0	1	0

(2) Input ATT

Setting	D4a	D5a
0 dB	0	0
-6 dB	0	1
-12 dB	1	0
-18 dB	1	1

(3) REC Output

REC Output	REC1	REC2	REC3	REC4
Setting	D6a	D7a	D8a	D9a
Off	0	0	0	0
On	1	1	1	1

(4) Multi Input Selector (Except for L/R)

Setting	D10a
Multi IN1	0
Multi IN2	1

(5) L/R VOL Input

Setting	D11a	D19a
Bypass	0	*
Multi IN1	1	0
Multi IN2	1	1

(6) Input Gain Control

Setting	D12a	D13a
0 dB	0	0
+6 dB	0	1
+12 dB	1	0
+18 dB	1	1

(7) Output Gain Control

Setting	D14a	D15a
0 dB	0	0
+6 dB	0	1
+12 dB	1	0
+18 dB	1	1

(8) IN10/REC4 Selector

Setting	D16a
IN10	0
REC4	1

(9) All Ch Output Mute

Setting	D17a
Mute off	0
Mute on	1

(10) Multi Input Mute (Except for L/R)

Setting	D18a
Mute off Depend on (4) Multi Input	0
Mute on	1

(12) Tone Input ATT

Setting	D9d	D10d
0 dB	0	0
-6 dB	0	1
-12 dB	1	0
-18 dB	1	1

(13) Bypass/Tone

Setting	D11d
Bypass	0
Tone	1

Note: (//////) It's initial setting when power is turned on.

Setting Code (cont.)

(11)Tone Control (Bass/Treble)

ATT Setting	Bass	D0d	D1d	D2d	D3d	D4d
	Treble	—	D5d	D6d	D7d	D8d
+16 dB*		1	0	0	0	0
+14 dB*		0	1	1	1	1
+12 dB*		0	1	1	1	0
+10 dB		0	1	1	0	1
+8 dB		0	1	1	0	0
+6 dB		0	1	0	1	1
+4 dB		0	1	0	1	0
+2 dB		0	1	0	0	1
0		0	0	0	0	0
-2 dB		0	0	0	0	1
-4 dB		0	0	0	1	0
-6 dB		0	0	0	1	1
-8 dB		0	0	1	0	0
-10 dB		0	0	1	0	1
-12 dB*		0	0	1	1	0
-14 dB*		0	0	1	1	1
-16 dB*		0	1	0	0	0

Note: (//////) It's initial setting when power is turned on.

* Only bypass setting

(14)Tone Block Position

Setting	D12d
Before VOL	0
After VOL	1

(15)Loudness

Setting	D13d
Off	0
On	1

(16)Loud/Balance

Setting	D14d
Balance output	0
Loudness	1

(17)L/R Bypass

Setting	D15d
Selector	0
External IN	1

(18)6 channel Volume

ATT	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b	ATT	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c									
0 dB		0	0	0	0	0	0	0	-16 dB		0	0	1	0	0	0	0
-1 dB		0	0	0	0	0	0	1	-17 dB		0	0	1	0	0	0	1
-2 dB		0	0	0	0	0	1	0	-18 dB		0	0	1	0	0	1	0
-3 dB		0	0	0	0	0	1	1	-19 dB		0	0	1	0	0	1	1
-4 dB		0	0	0	0	1	0	0	-20 dB		0	0	1	0	1	0	0
-5 dB		0	0	0	0	1	0	1	-21 dB		0	0	1	0	1	0	1
-6 dB		0	0	0	0	1	1	0	-22 dB		0	0	1	0	1	1	0
-7 dB		0	0	0	0	1	1	1	-23 dB		0	0	1	0	1	1	1
-8 dB		0	0	0	1	0	0	0	-24 dB		0	0	1	1	0	0	0
-9 dB		0	0	0	1	0	0	1	-25 dB		0	0	1	1	0	0	1
-10 dB		0	0	0	1	0	1	0	-26 dB		0	0	1	1	0	1	0
-11 dB		0	0	0	1	0	1	1	-27 dB		0	0	1	1	0	1	1
-12 dB		0	0	0	1	1	0	0	-28 dB		0	0	1	1	1	0	0
-13 dB		0	0	0	1	1	0	1	-29 dB		0	0	1	1	1	0	1
-14 dB		0	0	0	1	1	1	0	-30 dB		0	0	1	1	1	1	0
-15 dB		0	0	0	1	1	1	1	-31 dB		0	0	1	1	1	1	1

Setting Code (cont.)

(18)6 channel Volume (cont.)

	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
ATT	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
-32 dB	0	1	0	0	0	0	0	0
-33 dB	0	1	0	0	0	0	0	1
-34 dB	0	1	0	0	0	0	1	0
-35 dB	0	1	0	0	0	0	1	1
-36 dB	0	1	0	0	0	1	0	0
-37 dB	0	1	0	0	0	1	0	1
-38 dB	0	1	0	0	0	1	1	0
-39 dB	0	1	0	0	0	1	1	1
-40 dB	0	1	0	1	0	0	0	0
-41 dB	0	1	0	1	0	0	0	1
-42 dB	0	1	0	1	0	0	1	0
-43 dB	0	1	0	1	0	0	1	1
-44 dB	0	1	0	1	1	0	0	0
-45 dB	0	1	0	1	1	0	0	1
-46 dB	0	1	0	1	1	1	0	0
-47 dB	0	1	0	1	1	1	1	1
-48 dB	0	1	1	0	0	0	0	0
-49 dB	0	1	1	0	0	0	0	1
-50 dB	0	1	1	0	0	0	1	0
-51 dB	0	1	1	0	0	0	1	1
-52 dB	0	1	1	0	1	0	0	0
-53 dB	0	1	1	0	1	0	0	1
-54 dB	0	1	1	0	1	1	0	0
-55 dB	0	1	1	0	1	1	1	1
-56 dB	0	1	1	1	0	0	0	0
-57 dB	0	1	1	1	0	0	0	1
-58 dB	0	1	1	1	0	0	1	0
-59 dB	0	1	1	1	0	0	1	1
-60 dB	0	1	1	1	1	0	0	0
-61 dB	0	1	1	1	1	0	0	1
-62 dB	0	1	1	1	1	1	0	0
-63 dB	0	1	1	1	1	1	1	1
-64 dB	1	0	0	0	0	0	0	0
-65 dB	1	0	0	0	0	0	0	1
-66 dB	1	0	0	0	0	0	1	0

Note: (//////) It's initial setting when power is turned on.

	Lch	D0b	D1b	D2b	D3b	D4b	D5b	D6b
	SLch	D0c	D1c	D2c	D3c	D4c	D5c	D6c
	Rch	D7b	D8b	D9b	D10b	D11b	D12b	D13b
	SRch	D7c	D8c	D9c	D10c	D11c	D12c	D13c
	Cch	D14b	D15b	D16b	D17b	D18b	D19b	D20b
ATT	SWch	D14c	D15c	D16c	D17c	D18c	D19c	D20c
-67 dB		1	0	0	0	0	1	1
-68 dB		1	0	0	0	1	0	0
-69 dB		1	0	0	0	1	0	1
-70 dB		1	0	0	0	1	1	0
-71 dB		1	0	0	0	1	1	1
-72 dB		1	0	0	1	0	0	0
-73 dB		1	0	0	1	0	0	1
-74 dB		1	0	0	1	0	1	0
-75 dB		1	0	0	1	0	1	1
-76 dB		1	0	0	1	1	0	0
-77 dB		1	0	0	1	1	0	1
-78 dB		1	0	0	1	1	1	0
-79 dB		1	0	0	1	1	1	1
-80 dB		1	0	1	0	0	0	0
-81 dB		1	0	1	0	0	0	1
-82 dB		1	0	1	0	0	1	0
-83 dB		1	0	1	0	0	1	1
-84 dB		1	0	1	0	1	0	0
-85 dB		1	0	1	0	1	0	1
-86 dB		1	0	1	0	1	1	0
-87 dB		1	0	1	0	1	1	1
-88 dB		1	0	1	1	0	0	0
-89 dB		1	0	1	1	0	0	1
-90 dB		1	0	1	1	0	1	0
-91 dB		1	0	1	1	0	1	1
-92 dB		1	0	1	1	1	0	0
-93 dB		1	0	1	1	1	0	1
-94 dB		1	0	1	1	1	1	0
-95 dB		1	0	1	1	1	1	1
-96 dB		1	1	0	0	0	0	0
-97 dB		1	1	0	0	0	0	1
-98 dB		1	1	0	0	0	1	0
-99 dB		1	1	0	0	0	1	1
-∞ dB		1	1	1	1	0	0	0

Electrical Characteristics

Unless otherwise noted, $T_a = 25^\circ\text{C}$, $AVCC = 7\text{ V}$, $AVEE = -7\text{ V}$, $DVDD = 3.3\text{ V}$, $f = 1\text{ kHz}$, $\text{Volume} = 0\text{ dB}$, $\text{Input Selector} = \text{IN1}$, $\text{Input ATT} = 0\text{ dB}$, $\text{Input Gain Control} = 0\text{ dB}$, $\text{Output Gain Control} = 0\text{ dB}$, $\text{L/R Volume Input} = \text{Bypass}$, $\text{Multi Input Selector} = \text{Multi IN1}$, $\text{Tone} = 0\text{ dB}$, $\text{Tone Input ATT} = 0\text{ dB}$, $\text{Bypass/Tone} = \text{Bypass}$, $\text{Tone Position} = \text{Before Vol}$, $\text{Loudness} = \text{OFF}$, $\text{Loud/Balance} = \text{Balance}$, $\text{L/R Bypass} = \text{Selector}$

(1) Power supply characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Analog positive power circuit current	Alcc	—	50	70	mA	With $AVCC = 7\text{ V}$ and $AVEE = -7\text{ V}$, Pin31 pin current, when no signal is provided
Analog negative power circuit current	Alee	-70	-50	—	mA	With $AVCC = 7\text{ V}$ and $AVEE = -7\text{ V}$, Pin67 pin current, when no signal is provided
Digital power circuit current	Dldd	—	3	6	mA	With $DVDD = 3.3\text{ V}$, Pin30 pin current, when no signal is provided

(2) Input/Output characteristics (Over all)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input resistance	Rin	35	47	65	k Ω	1 to 5, 65, 66, 68 to 80pin When each selector chooses a terminal concerned.
Maximum output voltage	VOM	3.6	4.2	—	Vrms	(4, 5, 7, 8, 9, 10)pin input, (54, 47, 36, 35, 42, 41) pin output, THD = 1%, $R_L = 10\text{ k}\Omega$, Output Gain Control = +12 dB setting
Pass gain	Gv	-2.0	0	2.0	dB	(4, 5, 7, 8, 9, 10) pin input, (54, 47, 36, 35, 42, 41) pin output, $V_i = 0.3\text{ Vrms}$, FLAT
Total harmonic distortion	THD1	—	0.005	0.05	%	(4, 5, 7, 8, 9, 10) pin input, (54, 47, 36, 35, 42, 41) pin output, BW:400 Hz to 30 kHz, $f = 1\text{ kHz}$, $V_o = 0.3\text{ Vrms}$, $R_L = 10\text{ k}\Omega$
	THD2	—	0.03	0.1		(4, 5, 7, 8, 9, 10) pin input, (54, 47, 36, 35, 42, 41) pin output, BW: 400 Hz to 30 kHz, $f = 1\text{ kHz}$, $V_o = 2\text{ Vrms}$, $R_L = 10\text{ k}\Omega$
Balance of mutual channels	CBAL	-0.5	0	0.5	dB	(4, 5) pin input, (54, 47) pin output, $V_i = 0.3\text{ Vrms}$, JIS-A
Output noise voltage	Vono (VOL = $-\infty\text{ dB}$)	—	1.5	6	μVrms	JIS-A, (4, 5, 7, 8, 9, 10) pin: $R_g = 0\ \Omega$, (54, 47, 36, 35, 42, 41) pin output, Output gain control = 0 dB
		—	9	20		Volume = $-\infty\text{ dB}$ setting Output gain control = +12 dB
	Vono (VOL = 0 dB)	—	2.5	8		JIS-A, (4, 5, 7, 8, 9, 10) pin: $R_g = 0\ \Omega$, (54, 47, 36, 35, 42, 41) pin output, Output gain control = 0 dB
		—	12	25		Volume = 0 dB setting Output gain control = +12 dB
Vonobal (Balance out)	—	5	10		JIS-A, (4, 5) pin: $R_g = 0\ \Omega$, (14, 15, 17, 18) pin output	
Input/Multi selector channel separation	CS1	—	-90	-70	dB	<Input Selector> (54, 47) pin output, $V_o = 1\text{ Vrms}$, $R_g = 0\ \Omega$, $R_L = 10\text{ k}\Omega$, JIS-A
	CS2	—	-90	-70		<Multi Input Selector> (35, 36, 41, 42, 47, 54) pin output, $V_o = 1\text{ Vrms}$, $R_g = 0\ \Omega$, $R_L = 10\text{ k}\Omega$, JIS-A, L/R VOL Input = Multi input
Cross talk of mutual channels	CT1 (L/R)	—	-90	-70	dB	(4, 5) pin input, (47, 54) pin output, $V_o = 1\text{ Vrms}$, $R_g = 0\ \Omega$, $R_L = 10\text{ k}\Omega$, JIS-A
	CT2 (Multi Input)	—	-90	-70		(7, 8, 9, 10, 11, 12) pin input, (35, 36, 41, 42, 47, 54) pin output, $V_o = 1\text{ Vrms}$, $R_g = 0\ \Omega$, $R_L = 10\text{ k}\Omega$, JIS-A, L/R VOL Input = Multi input

(3) 6 channel Volume characteristics

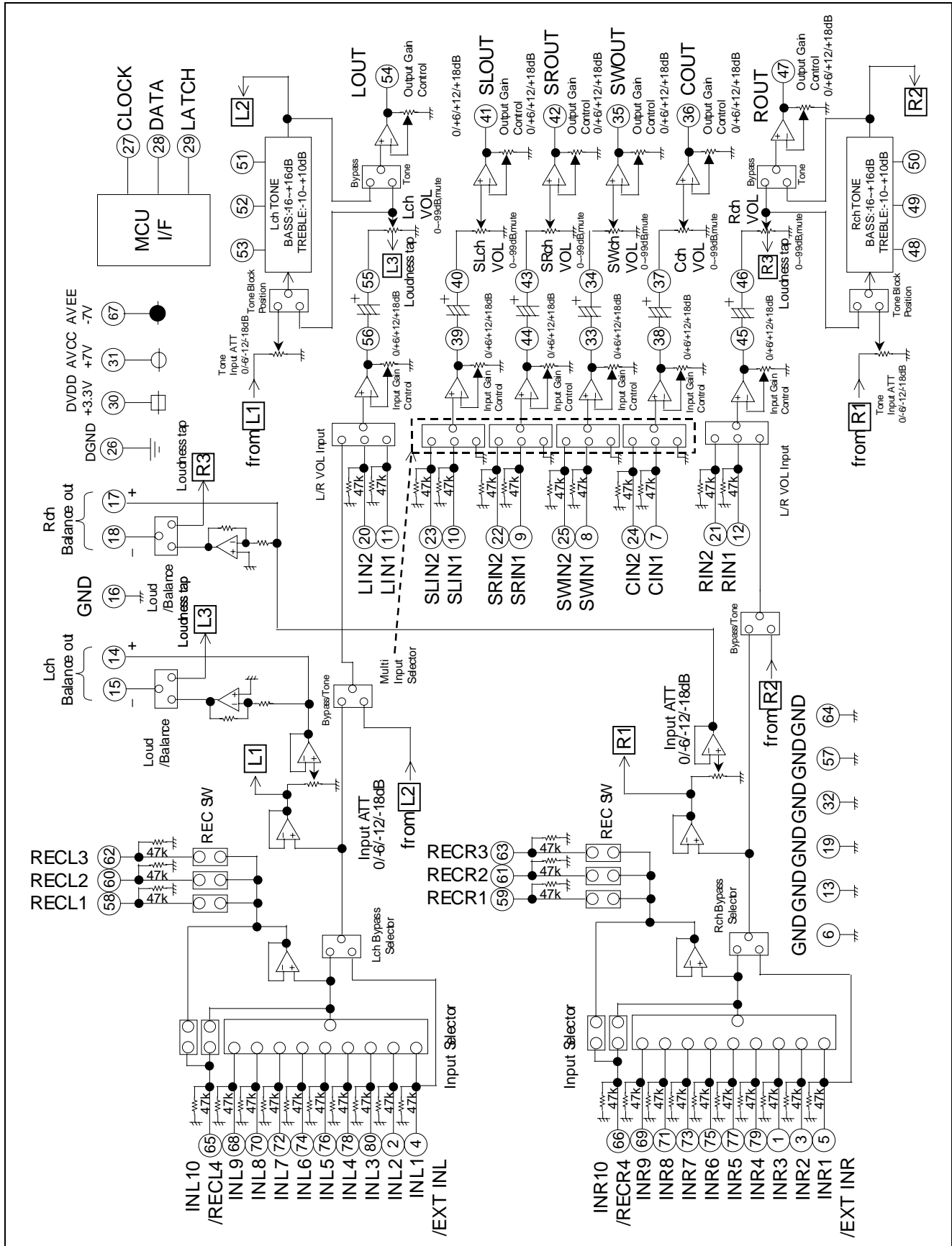
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Maximum attenuation	ATTmax	—	-100	-95	dB	(35, 36, 41, 42, 47, 54) pin output, $V_i = 2 V_{rms}$, JIS-A, VOL = $-\infty$
Volume gain gang error of mutual channels	Dvol	-0.5	0	+0.5	dB	(35, 36, 41, 42, 47, 54) pin output, Volume = 0 dB setting

(4) Tone control characteristics

Unless otherwise noted, Bypass/Tone = Tone, (1, 2) PIN Input, (56, 45) PIN Output

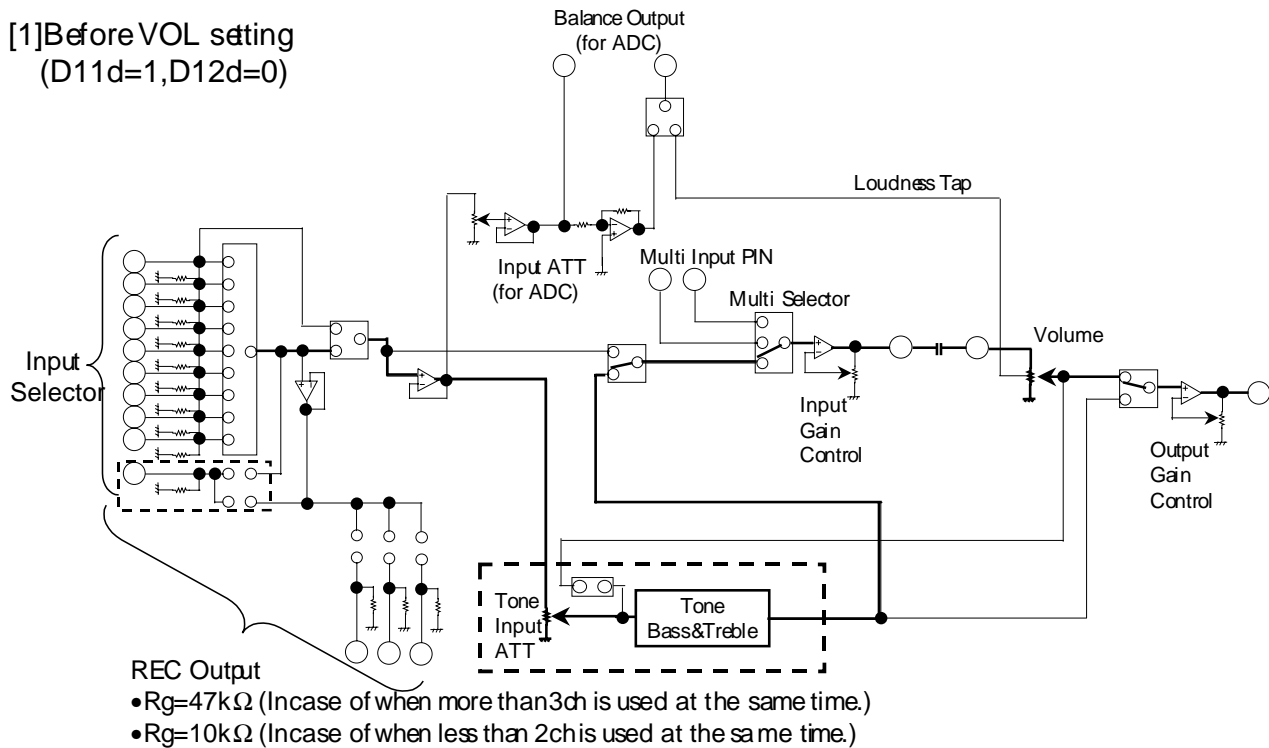
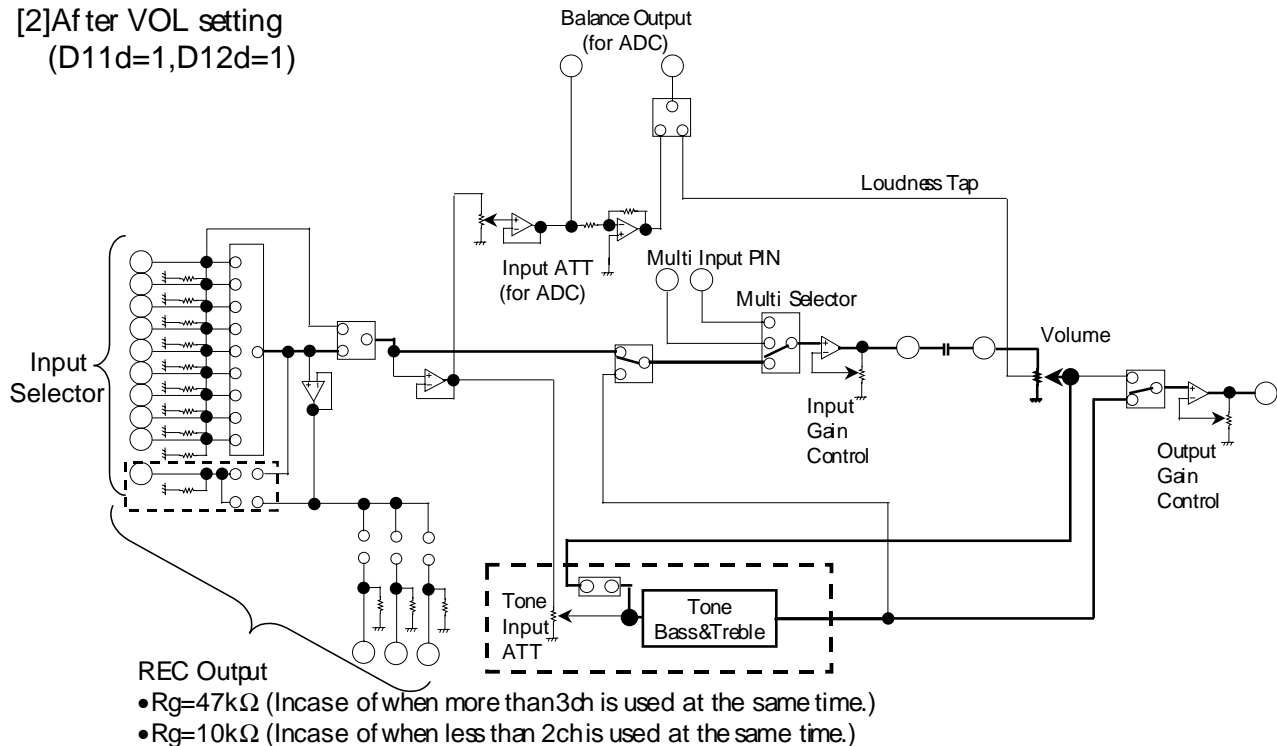
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Tone control voltage gain (Boost/Bass)	G(BASS)B	+14	+16	+18	dB	f = 100 Hz, Bass +16 dB setting
Tone control voltage gain (Cut/Bass)	G(BASS)C	-18	-16	-14	dB	f = 100 Hz, Bass -16 dB setting
Tone control voltage gain (Boost/Treble)	G(TRE)B	+8	+10	+12	dB	f = 10 kHz, Treble +10 dB setting
Tone control voltage gain (Cut/Treble)	G(TRE)C	-12	-10	-8	dB	f = 10 kHz, Treble -10 dB setting
Balance of mutual channels	BALT	-2	0	+2	dB	Bass setting +16, -16 dB, Treble setting +10, -10 dB

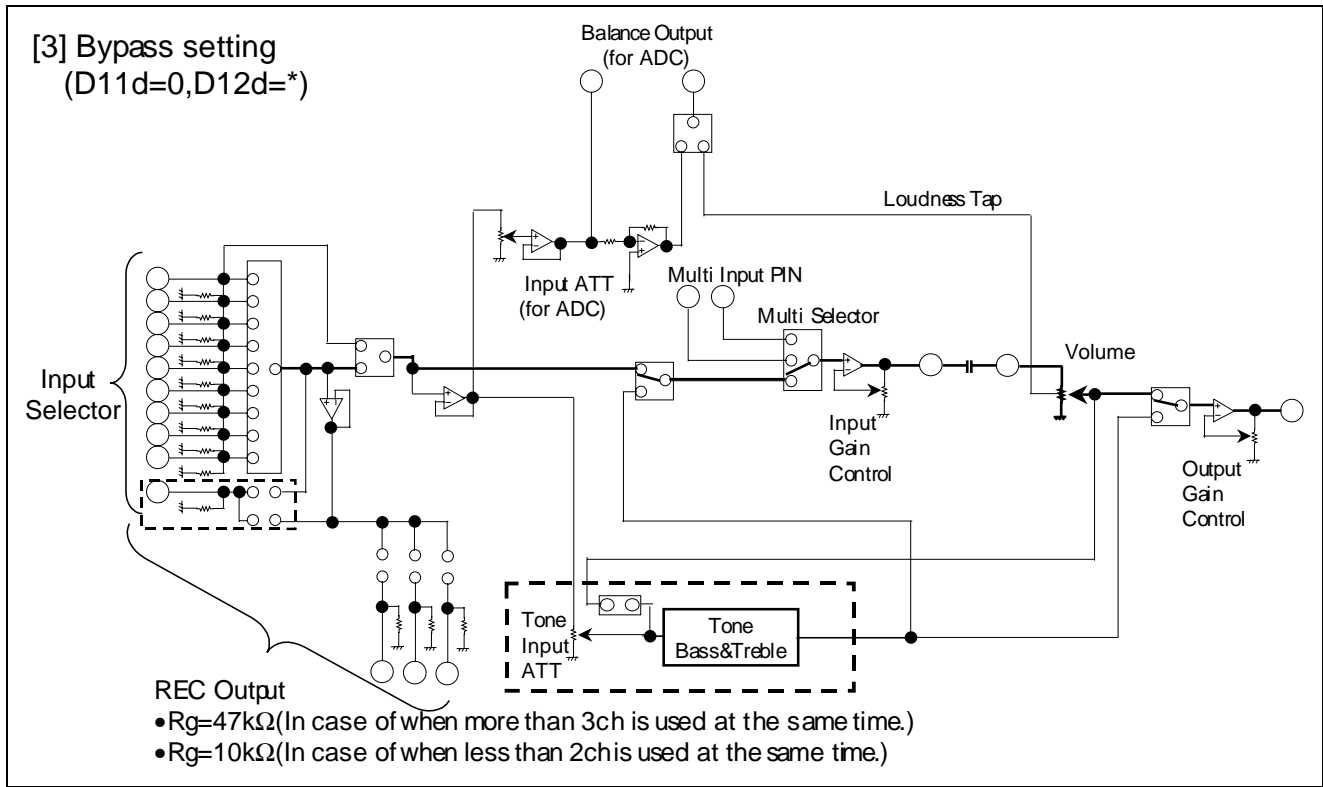
Internal Block Diagram



Application Block Diagram

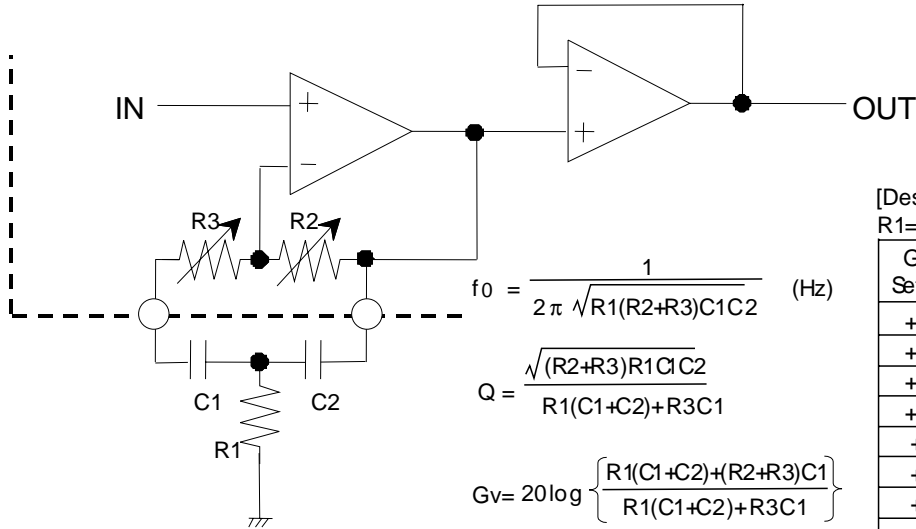
<TONE CONTROL> ToneBlock Position is selectable.

[1] Before VOL setting
(D11d=1, D12d=0)[2] After VOL setting
(D11d=1, D12d=1)



(1) Bass

<Boost>



[Designed Parameter]
 R1=4.7 kΩ, C1=0.22μF, C2=0.047μF

Gain Setting	Designed Parameter	
	R3(kΩ)	R2(kΩ)
+16dB	3.5	48.7
+14dB	5.8	46.3
+12dB	8.8	43.3
+10dB	12.6	39.5
+8dB	17.3	34.8
+6dB	23.3	28.8
+4dB	30.8	21.3
+2dB	40.2	11.9

$$f_0 = \frac{1}{2\pi \sqrt{R1(R2+R3)C1C2}} \text{ (Hz)}$$

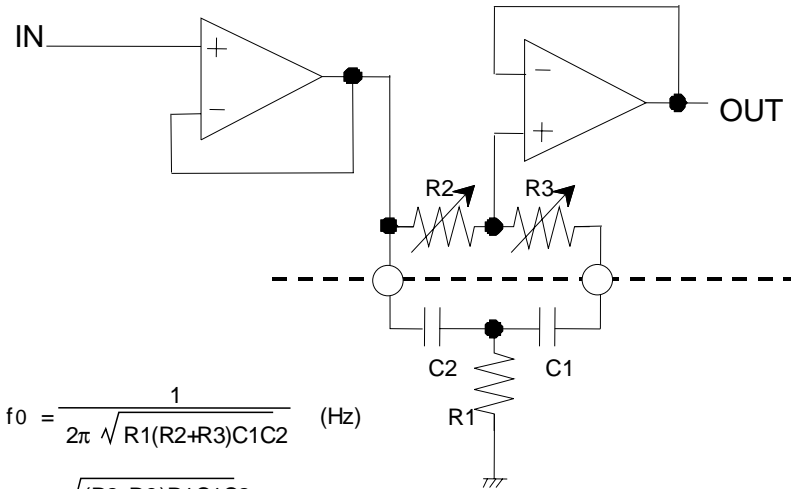
$$Q = \frac{\sqrt{(R2+R3)R1C1C2}}{R1(C1+C2)+R3C1}$$

$$Gv = 20 \log \left\{ \frac{R1(C1+C2)+(R2+R3)C1}{R1(C1+C2)+R3C1} \right\} \text{ (dB)}$$

<Cut>

[Designed Parameter]
 R1=4.7 kΩ, C1=0.22μF, C2=0.047μF

Gain Setting	Designed Parameter	
	R3(kΩ)	R2(kΩ)
-16dB	3.5	48.7
-14dB	5.8	46.3
-12dB	8.8	43.3
-10dB	12.6	39.5
-8dB	17.3	34.8
-6dB	23.3	28.8
-4dB	30.8	21.3
-2dB	40.2	11.9



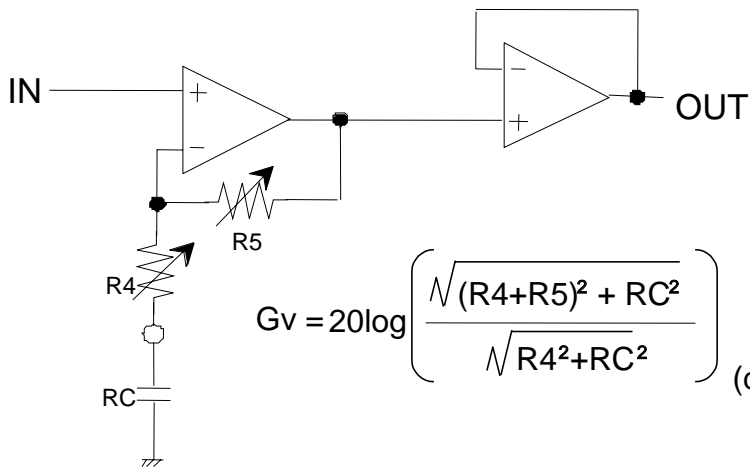
$$f_0 = \frac{1}{2\pi \sqrt{R1(R2+R3)C1C2}} \text{ (Hz)}$$

$$Q = \frac{\sqrt{(R2+R3)R1C1C2}}{R1(C1+C2)+R3C1}$$

$$Gv = 20 \log \left\{ \frac{R1(C1+C2)+R3C1}{R1(C1+C2)+(R2+R3)C1} \right\} \text{ (dB)}$$

(2)Treble

<Boost>



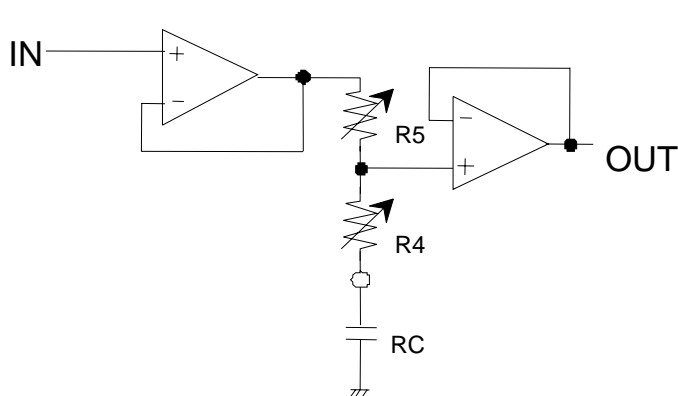
$$G_v = 20 \log \left(\frac{\sqrt{(R_4 + R_5)^2 + RC^2}}{\sqrt{R_4^2 + RC^2}} \right) \text{ (dB)}$$

[Desig ned Parameter]

RC=2200pF

Gain Setting	Desi gned Parameter	
	R4(kΩ)	R5(kΩ)
+10dB	7.6	24.7
+8dB	11.0	21.3
+6dB	14.9	17.4
+4dB	19.6	12.7
+2dB	25.3	7.0

<Cut>



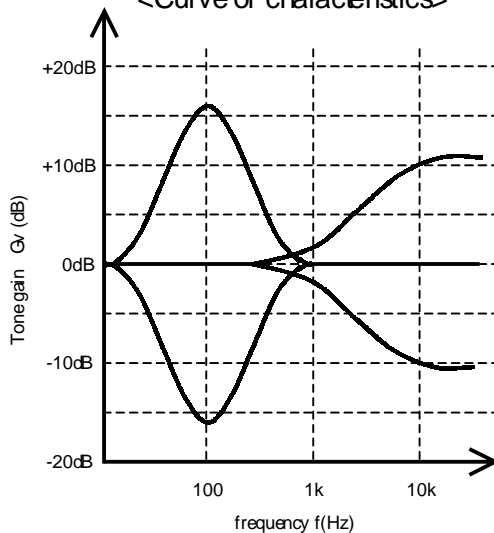
$$G_v = 20 \log \left(\frac{\sqrt{R_4^2 + RC^2}}{\sqrt{(R_4 + R_5)^2 + RC^2}} \right) \text{ (dB)}$$

[Desig ned Parameter]

RC=2200pF

Gain Setting	Desi gned Parameter	
	R4(kΩ)	R5(kΩ)
-10dB	7.6	24.7
-8dB	11.0	21.3
-6dB	14.9	17.4
-4dB	19.6	12.7
-2dB	25.3	7.0

<Curve of characteristics>

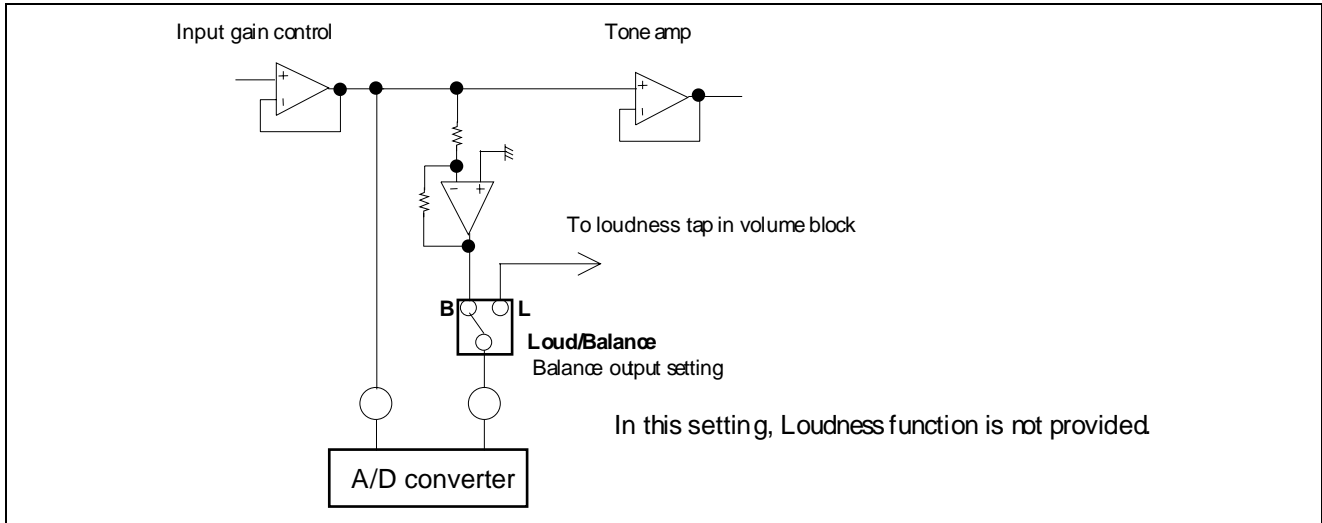


Balance Output/Loudness

Can be chose “Balance output” for external A/D converter or “Loudness” function by MCU command.
 “Balance output” and “Loudness” function can not be used at the same time.

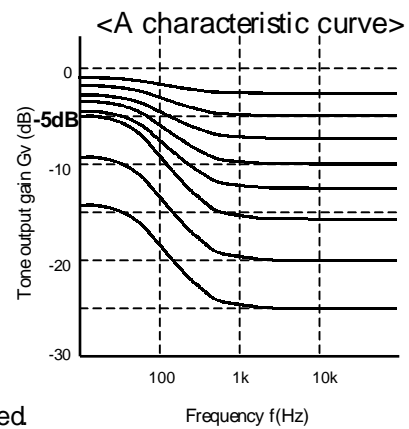
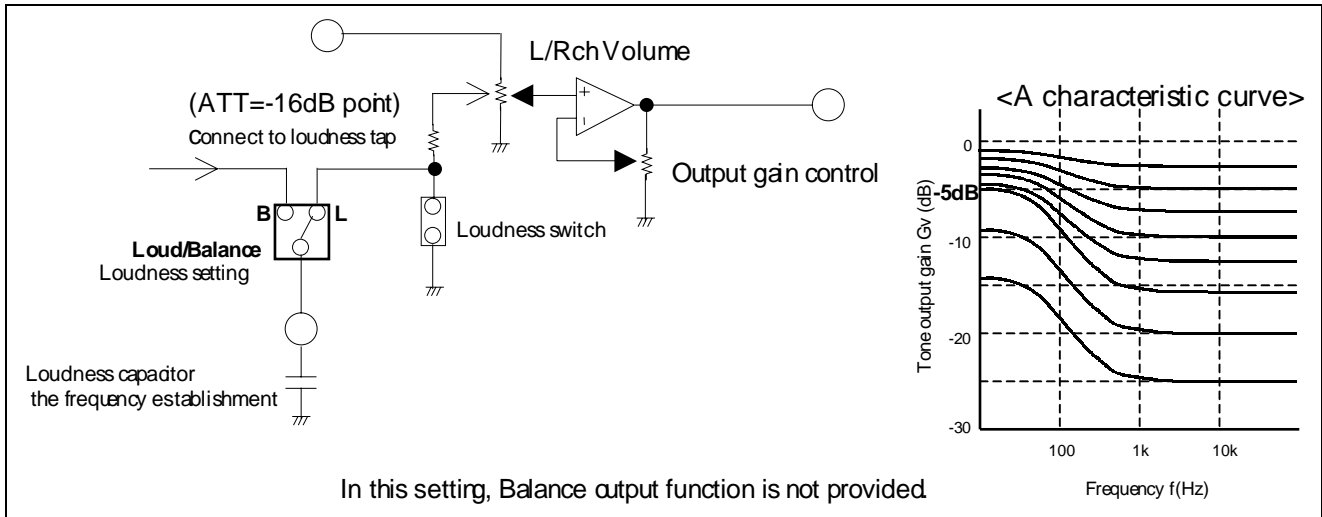
(1) Balance output

The M61531FP has Balance output (L/R channel) for external A/D converter.
 Loud/Balance = Balance Output setting

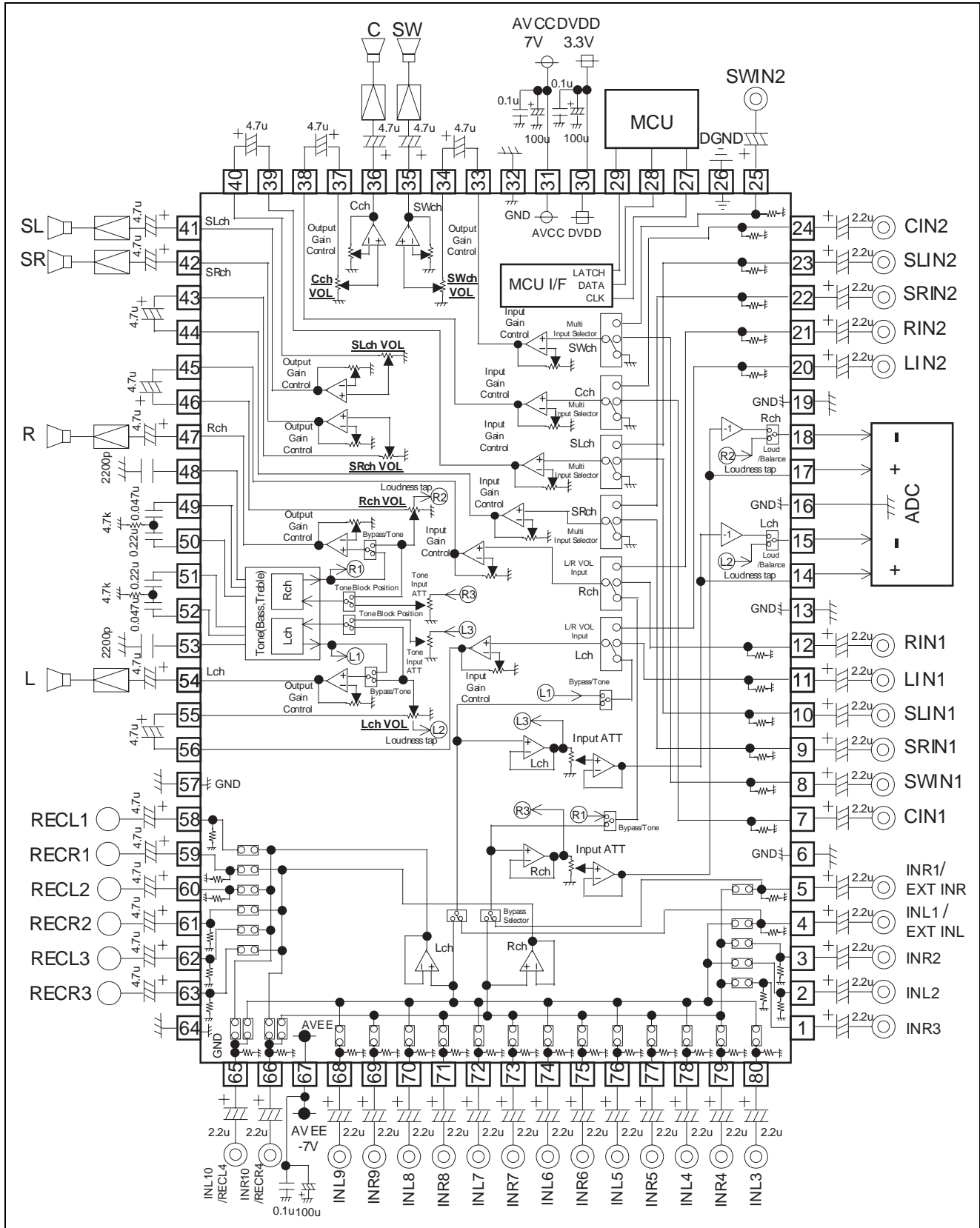


(2) Loudness

The M61531FP has center tap type Loudness circuit in L/Rch volume block.
 Loud/Balance = Loudness setting



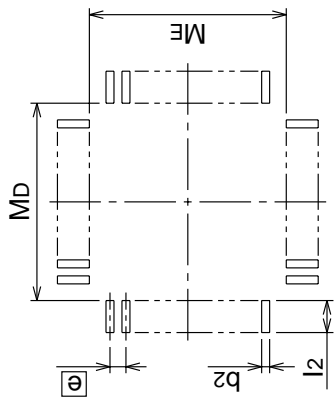
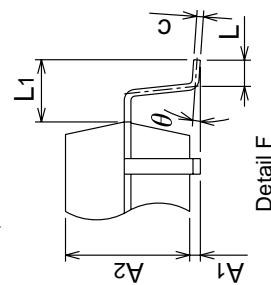
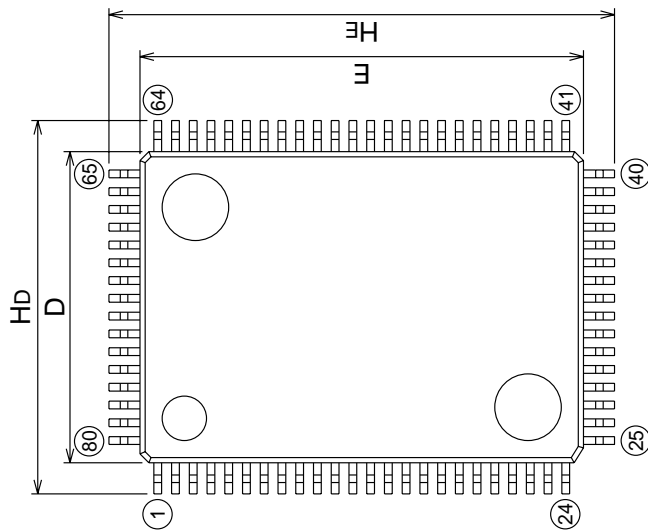
Application Example



Package Dimensions

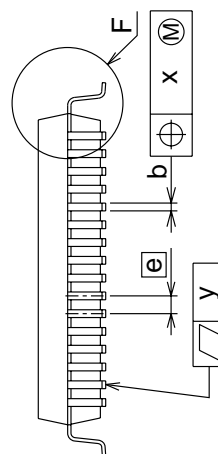
80P6N-A (MMP) Plastic 80pin 14 × 20mm body QFP

EIAJ Package Code QFP80-P-1420-0.80	JEDEC Code —	Weight(g) 1.58	Lead Material Alloy 42
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Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Norm	Max
A	—	—	3.05
A1	0	0.1	0.2
A2	—	2.8	—
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	—	0.8	—
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	—	1.4	—
x	—	—	0.2
y	—	—	0.1
θ	0°	—	10°
b2	—	0.5	—
l2	1.3	—	—
MD	—	14.6	—
ME	—	20.6	—



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