



# M616Z08

## 128 Kbit (8 Kbit x 16) SRAM WITH OUTPUT ENABLE

### FEATURES SUMMARY

- OPERATION VOLTAGE: 2.34V to 3.6V
- 8 Kbit x 16 SRAM
- EQUAL CYCLE and ACCESS TIMES: AS FAST AS 20ns
- TRI-STATE COMMON I/O
- TWO WRITE ENABLE PINS ALLOW WRITING TO UPPER AND LOWER BYTES

Figure 1. 44-pin, Hatless SOIC Package

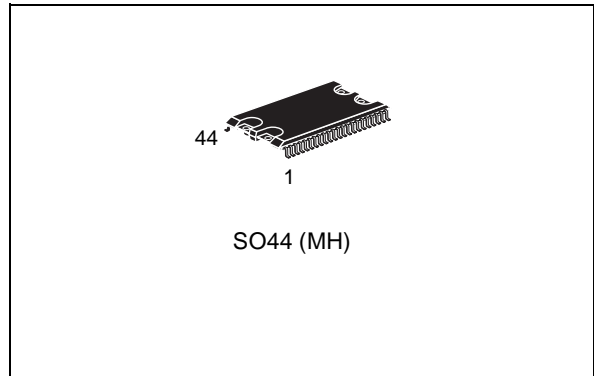


Figure 2. Logic Diagram

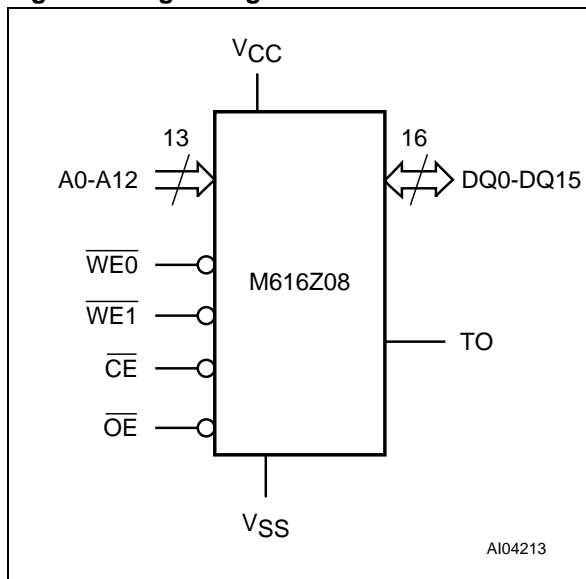


Table 1. Signal Names

A0-A12	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE0}$	WRITE Enable DQ 0-7
$\overline{WE1}$	WRITE Enable DQ 8-15
V <sub>CC</sub>	Supply Voltage
V <sub>SS</sub>	Ground
TO	Time-Out Pin

Note: TO Pin should be connected to V<sub>CC</sub>.

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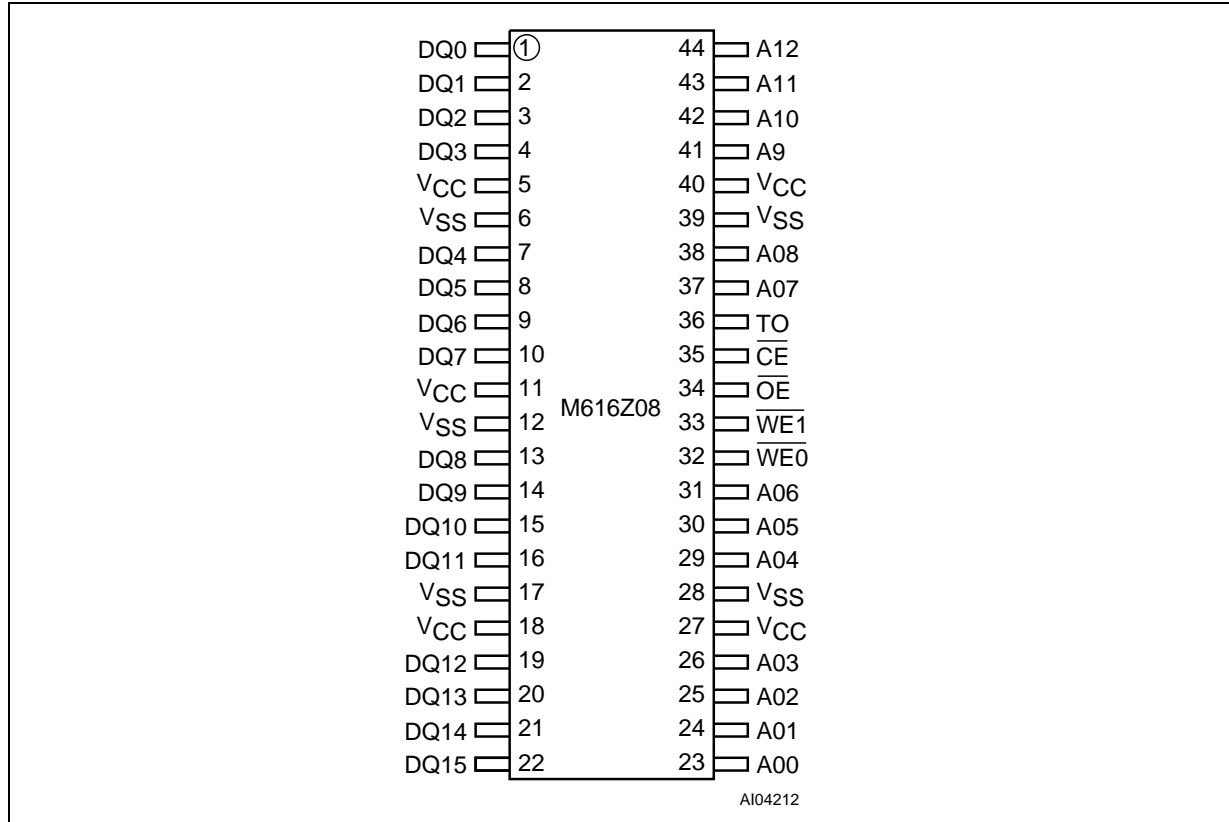
**DESCRIPTION**

The M616Z08 is a 128 Kbit (131,072 bit) CMOS SRAM, organized by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.6V ± 10% or

3.3V ± 10% supply, and all inputs and outputs are TTL compatible.

The M616Z08 is available in a 44-lead SOIC package.

**Figure 3. 44-pin Connections**



Note: TO Pin should be connected to VCC.

**MAXIMUM RATING**

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is

not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$T_A$	Ambient Operating Temperature	-40 to 125	°C
$T_{STG}^{(1)}$	Storage Temperature	-65 to 150	°C
$V_{IO}^{(2,3)}$	Input or Output Voltage	-0.3 to $V_{CC} + 0.3$	V
$V_{CC}$	Supply Voltage	-0.3 to 4.0	V
$I_O^{(4)}$	Output Current	10	mA
$P_D$	Power Dissipation	270	mW

Note: 1. Reflow at peak temperature of 215°C to 225°C for < 60 seconds (total thermal budget not to exceed 180°C for between 90 and 120 seconds).

2. Up to a maximum operating  $V_{CC}$  of 3.6V only.

3.  $V_{IL}(\min) = V_{SS} - 2.0V$  AC (pulse width  $\leq 10\% t_{AVAV}(\min)$ )  
 $V_{IH}(\max) = V_{CC} + 2.0V$  AC (pulse width  $\leq 10\% t_{AVAV}(\min)$ )

4. One output at a time, not to exceed 1 second duration.

## DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measure-

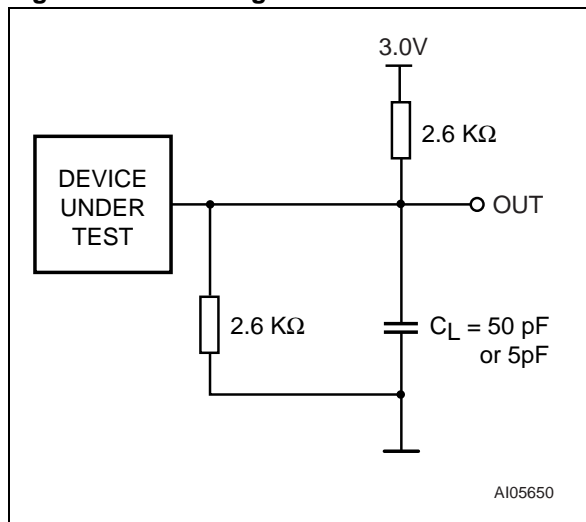
ment Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

**Table 3. DC and AC Measurement Conditions**

Parameter	M616Z08
V <sub>CC</sub> Supply Voltage	2.34 to 3.0V or 3.0 to 3.6V
Ambient Operating Temperature	−40 to 125°C
Load Capacitance (C <sub>L</sub> )	50pF
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output High Z is defined as the point where data is no longer driven.

**Figure 4. AC Testing Load Circuit**



**Table 4. Capacitance**

Symbol	Parameter <sup>(1,2)</sup>	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance on all pins (except DQ)		10	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance		10	pF

Note: 1. Effective capacitance measured with power supply at 3.3V; sampled only, not 100% tested.  
 2. At 25°C; f = 1MHz.  
 3. Outputs deselected.

Table 5. DC Characteristics

Sym	Parameter	Test Condition <sup>(1)</sup>	Min	Typ	Max	Unit	
I <sub>LI</sub>	Input Leakage Current	0V ≤ VIN ≤ VCC	TO Pin <sup>(2)</sup>		65	125	μA
			All other inputs			±1	μA
I <sub>LO</sub>	Output Leakage Current	0V ≤ VOUT ≤ VCC			±1	μA	
I <sub>CC1</sub> <sup>(3)</sup>	Supply Current	VCC = 3.6V			75	mA	
I <sub>CC3</sub> <sup>(4)</sup>	Supply Current (Standby) CMOS	VCC = 3.6V, CE ≥ VCC - 0.2V, f = 0			1	mA	
V <sub>IL</sub>	Input Low Voltage		-0.3		0.3VCC	V	
V <sub>IH</sub>	Input High Voltage		0.7VCC		VCC + 0.3	V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1mA			0.2	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -1mA	2.34 to 3.0V	VCC-0.2V			
			3.0 to 3.6V	VCC-0.3V			V

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = -40 to 125°C; VCC = 3.0 to 3.6V or 2.34 to 3.0V (except where noted).  
 2. Input leakage on TO Pin due to internal pull-down to VSS.  
 3. Average AC current, Outputs open, cycling at t<sub>AVAV</sub> minimum.  
 4. All other Inputs at V<sub>IL</sub> ≤ 0.2V or V<sub>IH</sub> ≥ VCC - 0.2V.

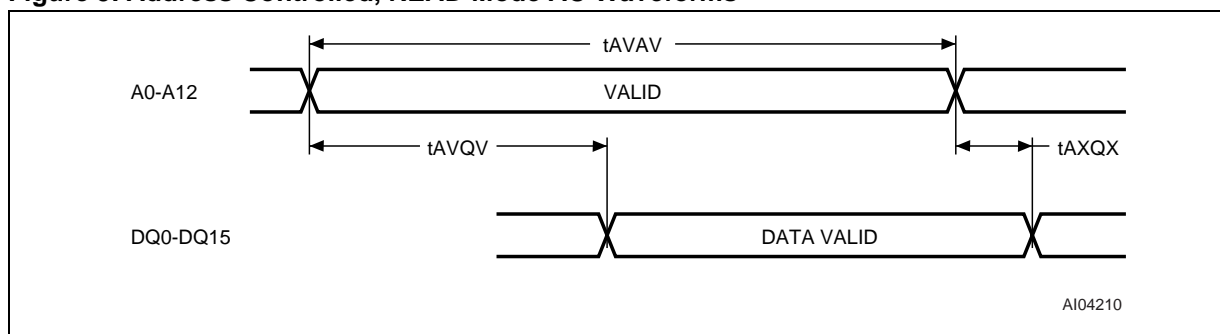
**OPERATION**

**READ Mode**

The M616Z08 is in the READ Mode whenever WRITE Enable ( $\overline{WE0}$  or  $\overline{WE1}$ ) is High with Output Enable ( $\overline{OE}$ ) Low, and Chip Enable ( $\overline{CE}$ ) is asserted. This provides access to data from sixteen of the 131,072 locations in the static memory array, specified by the 13 address inputs. Valid data will be available at the sixteen output pins within t<sub>AVQV</sub>

after the last stable address, providing  $\overline{OE}$  is Low and  $\overline{CE}$  is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t<sub>ELQV</sub> or t<sub>GLQV</sub>) rather than the address. Data out may be indeterminate at t<sub>ELQX</sub> and t<sub>GLQX</sub>, but data lines will always be valid at t<sub>AVQV</sub>.

Figure 5. Address Controlled, READ Mode AC Waveforms



Note:  $\overline{CE}$  = Low,  $\overline{OE}$  = Low,  $\overline{WE(0,1)}$  = High.

Figure 6. Chip Enable or Output Enable Controlled, READ Mode AC Waveforms

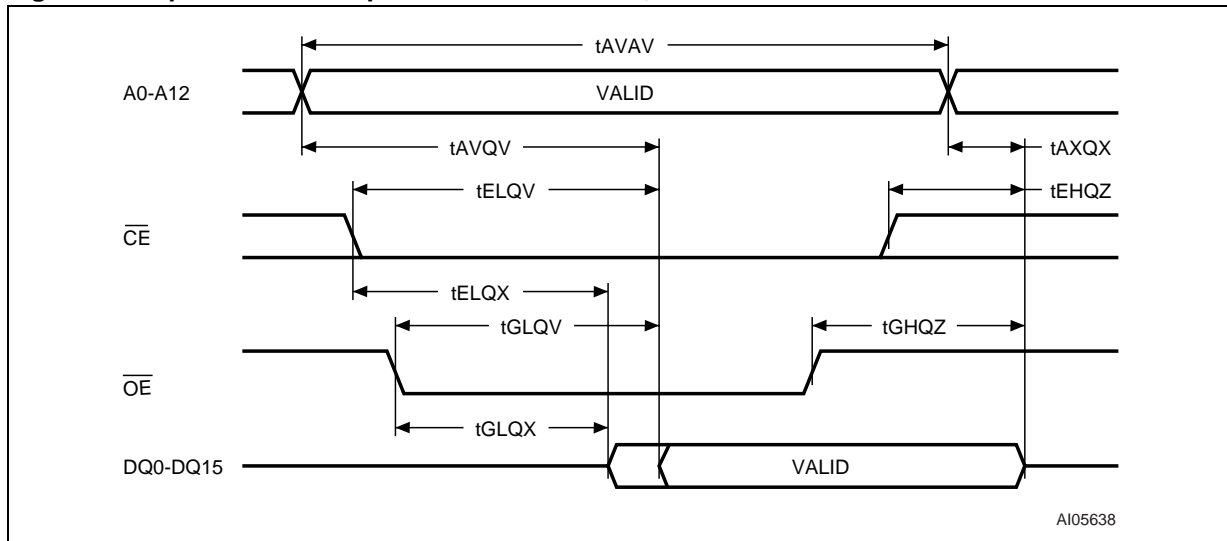


Table 6. READ Mode AC Characteristics

Symbol	Parameter <sup>(1)</sup>	M616Z08				Unit
		-20				
		2.34 to 3.0V		3.0 to 3.6V		
		Min	Max	Min	Max	
$t_{AVAV}$	READ Cycle Time	36		20		ns
$t_{AVQV}$	Address Valid to Output Valid		36		20	ns
$t_{ELQV}$	Chip Enable Low to Output Valid		36		20	ns
$t_{GLQV}$	Output Enable Low to Output Valid		20		10	ns
$t_{ELQX}$	Chip Enable Low to Output Transition	0		0		ns
$t_{GLQX}$	Output Enable Low to Output Transition	0		0		ns
$t_{EHQZ}^{(2)}$	Chip Enable High to Output Hi-Z		10		10	ns
$t_{GHQZ}^{(2)}$	Output Enable High to Output Hi-Z		10		10	ns
$t_{AXQX}$	Address Transition to Output Transition	0		0		ns

Note: 1. Valid for Ambient Operating Temperature:  $T_A = -40$  to  $125^\circ\text{C}$  (except where noted).

2.  $C_L = 5\text{pF}$ .

**WRITE Mode**

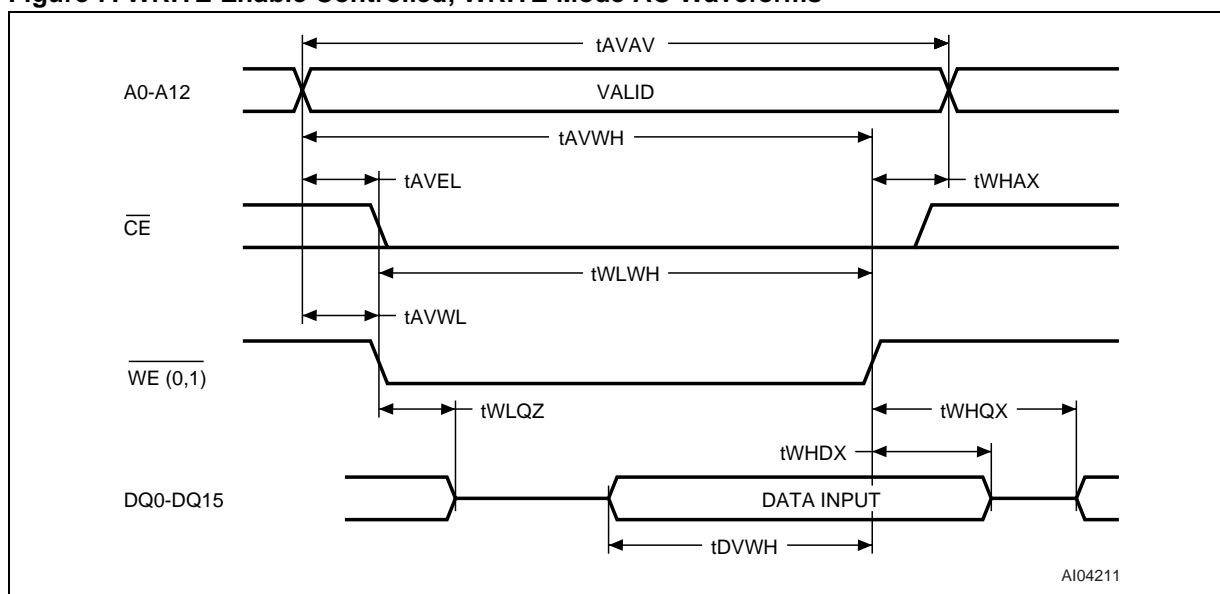
The M616Z08 is in the WRITE mode whenever the WE0 (low memory addresses) or WE1 (high memory addresses) and CE pins are low (see Table 8, page 10). Either the Chip Enable input ( $\overline{CE}$ ) or the WRITE Enable input ( $\overline{WE0}$  or  $\overline{WE1}$ ) must be deasserted during Address transitions for subsequent WRITE cycles. WRITE begins with the concurrence of Chip Enable being active with  $\overline{WE0}$  or  $\overline{WE1}$  low. Therefore, address setup time is referenced to WRITE Enable and Chip Enable as  $t_{AVWL}$  and  $t_{AVEH}$  respectively, and is determined by the latter occurring edge.

The WRITE cycle can be terminated by the earlier rising edge of CE, or  $\overline{WE0/WE1}$ .

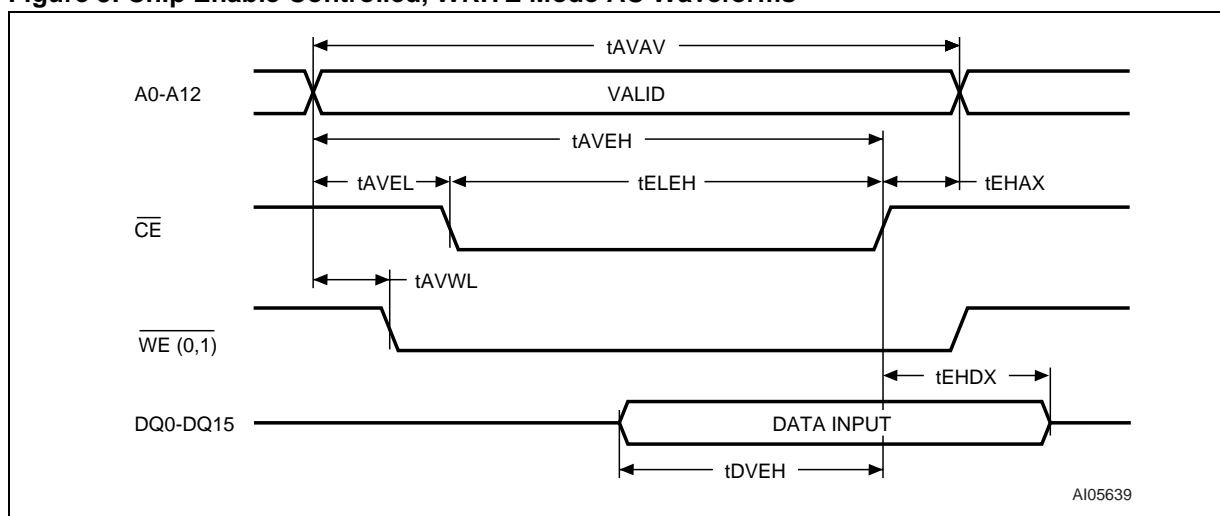
if the Output is enabled ( $\overline{CE} = \text{Low}$  and  $\overline{OE} = \text{Low}$ ), then  $\overline{WE0}$  or  $\overline{WE1}$  will return the outputs to high impedance within  $t_{WLQZ}$  of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for  $t_{DVWH}$  before the rising edge of WRITE Enable, or for  $t_{DVEH}$  before the rising edge of CE, whichever occurs first, and remain valid for  $t_{WHDX}$  or  $t_{EHDX}$ .

**Note:** When using MCP555 with TO Pin high, relaxed WRITE timing (CSNT = 1 in the chip select configuration register) should be selected.

**Figure 7. WRITE Enable Controlled, WRITE Mode AC Waveforms**



**Figure 8. Chip Enable Controlled, WRITE Mode AC Waveforms**



Note: 1. Output Enable ( $\overline{OE}$ ) = High.  
 2. If  $\overline{CE}$  goes High with  $\overline{WE0}$  or  $\overline{WE1}$  high, the output remains in a high-impedance state.



Table 7. WRITE Mode AC Characteristics

Symbol	Parameter <sup>(1)</sup>	M616Z08				Unit
		-20				
		2.34 to 3.0V		3.0 to 3.6V		
		Min	Max	Min	Max	
t <sub>AVAV</sub>	WRITE Cycle Time	36		20		ns
t <sub>AVWL</sub>	Address Valid to WRITE Enable Low	2		2		ns
t <sub>AVWH</sub>	Address Valid to WRITE Enable High	34		18		ns
t <sub>AVEH</sub>	Address Valid to Chip Enable High	34		18		ns
t <sub>WLWH</sub>	WRITE Enable Pulse Width	25		11		ns
t <sub>WHAX</sub>	WRITE Enable High to Address Transition	2		2		ns
t <sub>WHDX</sub>	WRITE Enable High to Input Transition	2		2		ns
t <sub>WHQX</sub> <sup>(3)</sup>	WRITE Enable High to Output Transition	0		0		ns
t <sub>WLQZ</sub> <sup>(2,3)</sup>	WRITE Enable Low to Output Hi-Z		10		10	ns
t <sub>AVEL</sub>	Address Valid to Chip Enable Low	2		2		ns
t <sub>ELEH</sub>	Chip Enable Low to Chip Enable High	25		11		ns
t <sub>EHAX</sub>	Chip Enable High to Address Transition	2		2		ns
t <sub>EHDX</sub>	Chip Enable High to Input Transition	2		2		ns
t <sub>DVWH</sub>	Input Valid to WRITE Enable High	20		8		ns
t <sub>DVEH</sub>	Input Valid to Chip Enable High	20		8		ns

Note: 1. Valid for Ambient Operating Temperature: T<sub>A</sub> = -40 to 125°C (except where noted).

2. C<sub>L</sub> = 5pF

3. At any given temperature and voltage condition, t<sub>WLQZ</sub> is less than t<sub>WHQX</sub> for any given device.

**“Operational” Mode**

The M616Z08 has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted (CE = High). An Output Enable ( $\overline{OE}$ ) signal provides a high speed tri-state control, allowing fast READ/WRITE cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs  $\overline{WE0}$  or  $\overline{WE1}$  and CE as summarized in “Operating Modes” (see Table 8 and Table 9).

**Noise Immunity**

When designing with high speed memory, proper power trace layout and capacitive decoupling must be maintained to ensure proper system operation. Power and ground line inductance should be reduced by providing separate power planes. The impedance of the decoupling path from the power pin through the decoupling capacitor should also be kept to a minimum. Small decoupling capacitors (10nF) should be located as close to the device pins as possible to limit the high frequency noise. Larger capacitor values (10uF and 1uF) are recommended to reduce low frequency noise and should be placed next to the power entry point of the board. Proper line termination should also be employed to minimize signal reflection.

See Motorola Semiconductor Application Note AN2127/D for additional Electromagnetic Compatibility (EMC) system design guidelines.

**Table 8.  $\overline{WE(0,1)}$  States during Access**

WRITE Enable	Used during 16-bit Port Access
$\overline{WE0}$	WRITE Enable for DQ (0-7)
$\overline{WE1}$	WRITE Enable for DQ (8-15)

**Table 9. Operating Modes**

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE0}$	$\overline{WE1}$	DQ0–DQ7	DQ8–15
Deselect	$V_{IH}$	X <sup>(1)</sup>	X <sup>(1)</sup>	X <sup>(1)</sup>	Hi-Z	Hi-Z
Word WRITE	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$	Hi-Z	Hi-Z
Byte 0 WRITE	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	Hi-Z	Hi-Z
Byte 1 WRITE	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	Hi-Z	Hi-Z
Byte 0 WRITE, Byte 1 READ	$V_{IL}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	Hi-Z	Data
Byte 1 WRITE, Byte 0 READ	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	Data	Hi-Z
Word READ	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	Data	Data

Note: 1. X = '1' or '0'



## PART NUMBERING

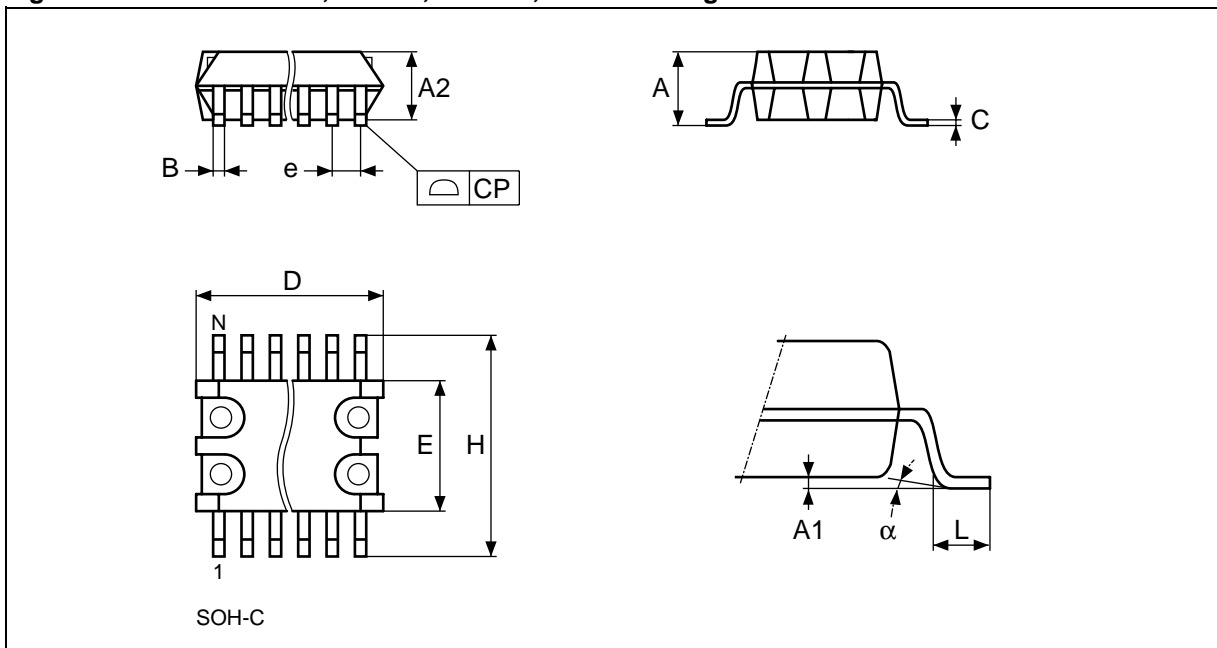
Table 10. Ordering Information Example

Example:	M6	16Z08	-20	MH	3	TR
<b>Device Type</b>	M6					
<b>Device Function</b>		16Z08 = 128Kbit (8 x16)				
<b>Speed</b>			-20 = 20ns (3.0 to 3.6V)			
<b>Package</b>				MH = 44-lead, Hatless SOIC		
<b>Temperature Range</b>					3 = -40 to 125°C	
<b>Shipping Method for SOIC</b>						blank = Tubes TR = Tape & Reel

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

PACKAGE MECHANICAL INFORMATION

Figure 9. SO44 – 44-Lead, Plastic, Hatless, Small Package Outline



Note: Drawing is not to scale.

Table 11. SO44 – 44-lead, Plastic, Hatless, Small Package Mechanical Data

Symb	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.46		0.014	0.018
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	0.81	–	–	0.032	–	–
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	44			44		
CP			0.10			0.004

**REVISION HISTORY****Table 12. Document Revision History**

<b>Date</b>	<b>Rev. #</b>	<b>Revision Details</b>
September 2001	1.0	First Issue
11/19/01	2.0	Correction of Operating Modes text (Table 9); document status changed to "Data Sheet;" add text for Noise Immunity (page 10)
02/12/02	2.1	Add TO Pin (Figure 2, 3, Table 1); change WRITE Mode AC Characteristics (Table 7)
02/21/02	2.2	Changes for TO Pin (Table 5) and change characteristics (Table 6, 7)
05/13/02	2.3	Add reflow time and temperature footnote (Table 2)
07/22/02	2.4	Add "Hatless" to package description (Figure 1, 9 and Table 10, 11)

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