

M62001L,FP/M62002L,FP/M62003L,FP/M62004L,FP/ M62005L,FP/M62006L,FP/M62007L,FP/M62008L,FP

LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

DESCRIPTION

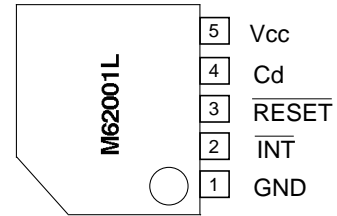
The M62001~8 are semiconductor integrated circuits whose optimum use is for the detection of the rise and fall in the power supply to a microcomputer system in order to reset or release the microcomputer system.

The M62001~8 carry out voltage detection in 2 steps and have 2 output pins. As Bi-CMOS process and low power dissipating circuits are employed, they output optimum signals through each output pin to a system that requires RAM backup. As output signals, interruption (INT) and compulsive reset (RESET) signals are available. The interruption signal (INT) is used to alter the microcomputer from normal mode to backup mode and vice versa. These output signals are classified into pulse type (M62001~M62004) and hold type (M62005~M62008).

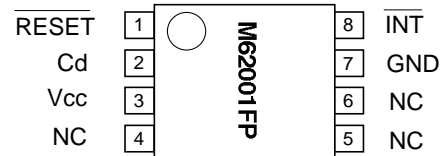
FEATURES

- Bi-CMOS process realizes a configuration of low current dissipating circuits.
 - Circuit current
 - $I_{CC}=5\mu A$ (Typ., normal mode, $V_{CC}=5.0V$)
 - $I_{CC}=1\mu A$ (Typ., backup mode, $V_{CC}=2.5V$)
- Two-step detection of supply voltage
 - Detection voltage in normal mode (21types)
 - $V_S=4.45V/4.25V$ (Typ.)
 - Detection voltage in backup mode
 - $V_{BATT}=2.15V$ (Typ.)
- Two outputs
 - Reset output (RESET): Output of compulsive reset signal
 - Interruption output (INT): Output of interruption signal
- Two types of output forms: CMOS and open drain
- Two types of interruption output (INT) signals
 - Pulse type (M62001~M62004)
 - Hold type (M62005~M62008)
- Two types of outline packages
 - 5-pin plastic SIP (single in-line package)
 - 8-pin plastic SOP (mini flat package)
- Output based on RAM backup mode (See the timing chart.)

PIN CONFIGURATION (TOP VIEW)



Outline 5P5T(M62001L~8L)



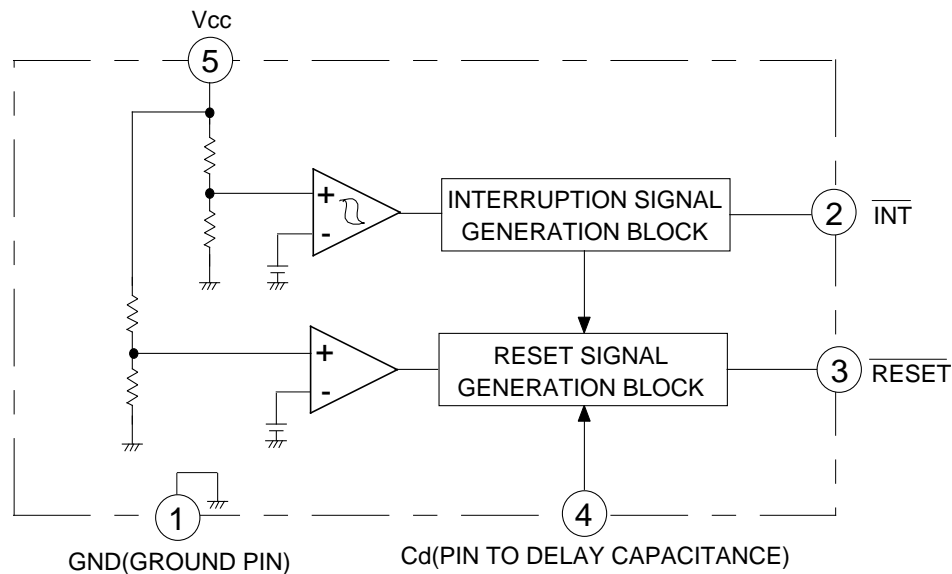
Outline 8P2S-A(M62001FP~8FP)

NC:NO CONNECTION

APPLICATION

Prevention of malfunction of microcomputer systems in electronic equipment such as OA equipment, industrial equipment, and home-use electronic appliances.

BLOCK DIAGRAM



NOTE: This is an example showing pin Nos. of M62001L~8L. (See PIN CONFIGURATION.)

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ABSOLUTE MAXIMUM RATINGS

(Ta=25°C, unless otherwise noted, These ratings commonly apply to the M62001L/FP~M62008L/FP.)



Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage		8	V
I _{SINK}	Output sink current		5	mA
P _d	Power dissipation		440	mW
K _θ	Thermal derating	(Ta 25°C)	4.4	mW/°C
T _{opr}	Operating temperature		-20 ~ +75	°C
T _{stg}	Storage temperature		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

(Ta=25°C, unless otherwise noted, These ratings commonly apply to the M62001L/8L.)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V _s	Supply voltage	Interruption level during V _{cc} drop (Equivalent to V _{SL})	(M62001,M62002, M62005,M62006)	4.30	4.45	4.60	V
			(M62003,M62004, M62007,M62008)	4.05	4.25	4.45	
V _{BATT}	Battery voltage	Reset level at backup	2.00	2.15	2.30	V	
V _s	Hysteresis voltage	V _S =V _{SH} -V _{SL}		100		mV	
I _{CC}	Circuit current	V _{cc} =5.0V:In normal mode		5.0	20	μA	
		V _{cc} =2.5V:In backup mode		1.0	4		
V _{sat1}	Sink ability	V _{cc} =4V, I _o =4mA (Output saturation voltage of N-ch transistor)		0.2	0.4	V	
V _{sat2}	Source ability	V _{cc} =4V, I _o =1mA (Output saturation voltage of P-ch transistor: [CMOS output] M62001, M62003, M62005, M62007)		0.2	0.4	V	
t _d	Delay time	External capacitance C _d =0.33μF		50		ms	
t _{pw}	Pulse width	Output pulse width (M62001, M62002, M62003, M62004)		7	10	μS	
t _{RESET}	Reset output response time	Time between V _{cc} (when falling)=V _{BATT} and output of RESET signal		30		μS	
t _{INT}	Interruption output reset time	Time between V _{cc} (when falling)=V _s and output of INT signal		100		μS	

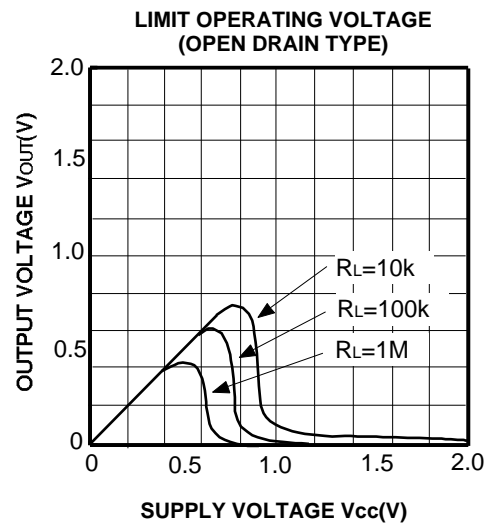
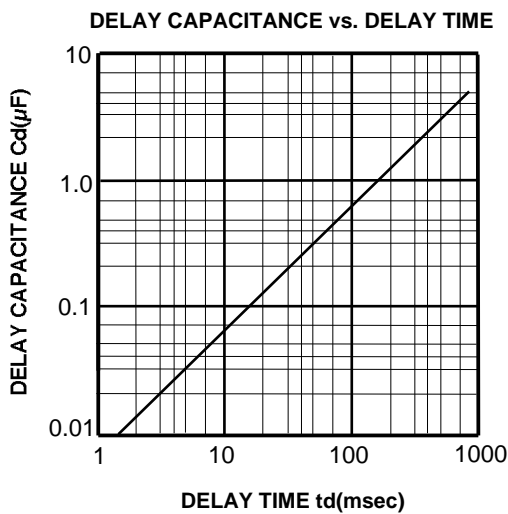
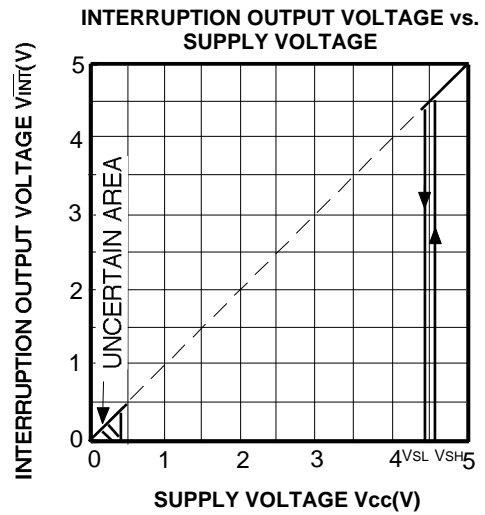
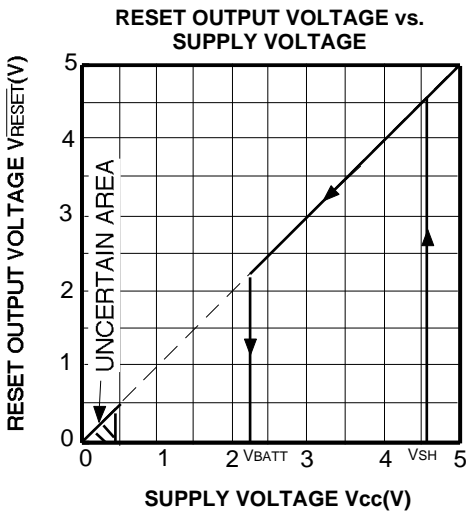
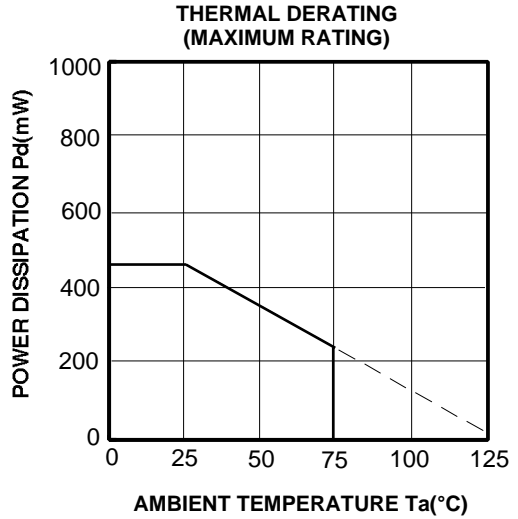
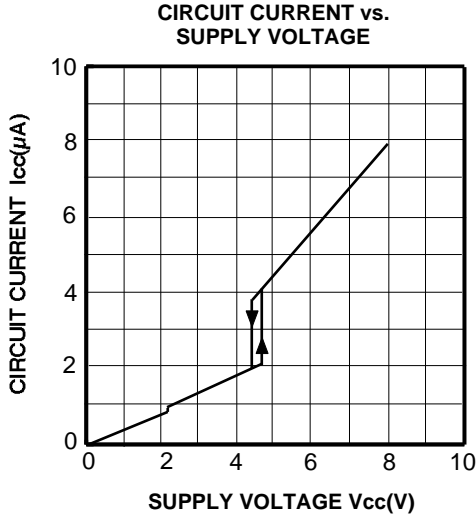
SUMMARY OF M62001L/FP~M62008L/FP

Type	Supply voltage detection level V _s (V)	Battery voltage detection level V _{BATT} (V)	Output form	Interruption signal output mode
M62001	4.45	2.15	CMOS	Pulse output 
M62002			Open drain	
M62003	CMOS			
M62004	Open drain			
M62005	4.45		CMOS	Hold output 
M62006			Open drain	
M62007	4.25		CMOS	
M62008			Open drain	

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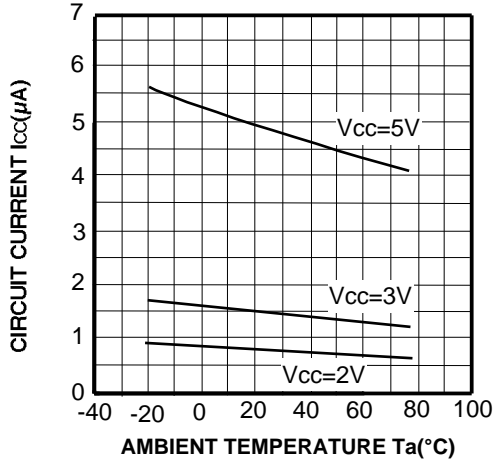
TYPICAL CHARACTERISTICS



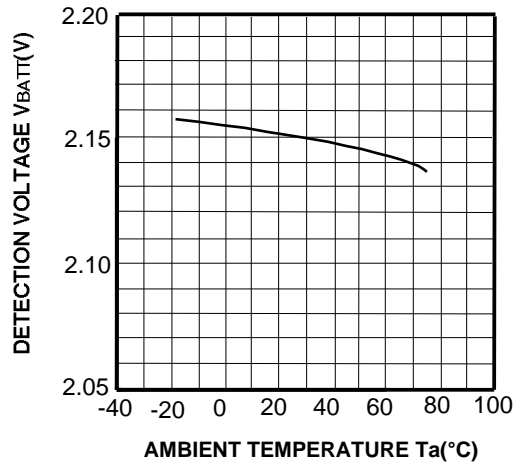
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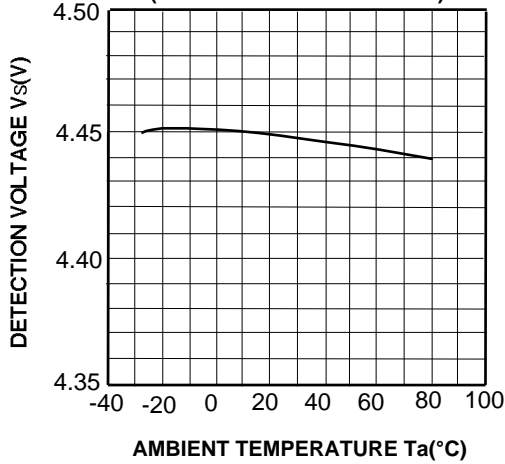
CIRCUIT CURRENT vs.
AMBIENT TEMPERATURE



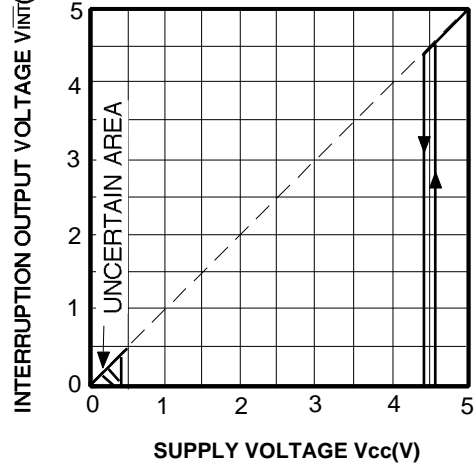
DETECTION VOLTAGE vs.
AMBIENT TEMPERATURE



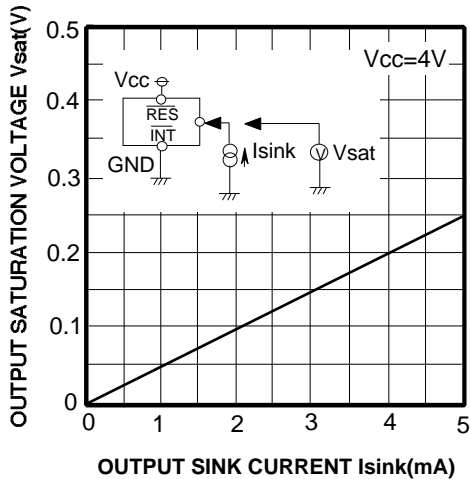
DETECTION VOLTAGE vs.
AMBIENT TEMPERATURE
(DETECTION AT 4.45V TYPE)



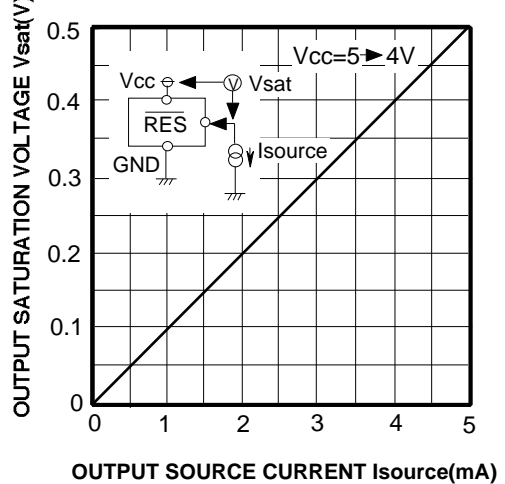
INTERRUPTION OUTPUT VOLTAGE vs.
SUPPLY VOLTAGE



Nch OUTPUT SATURATION VOLTAGE vs.
OUTPUT SINK CURRENT



Pch OUTPUT SATURATION VOLTAGE vs.
OUTPUT SOURCE CURRENT



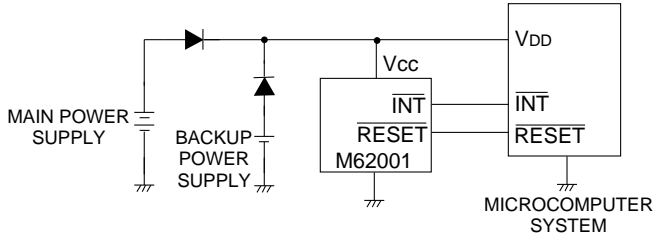
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LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

OPERATION PRINCIPLE

DESCRIPTION

In general, the memory backup function of a microcomputer, as shown in figure, uses two diodes to switch between main power supply and backup power supply. The M62001~M62008 are ICs that, in such memory backup operation, monitor in 2 steps each voltage on the V_{DD} line.



The ICs have an intelligent sequence such as substantial hysteresis action of RESET toward normal state at restoration of supply voltage, as well as 2-step detection in low power dissipation mode.

OPERATION IN DETAIL

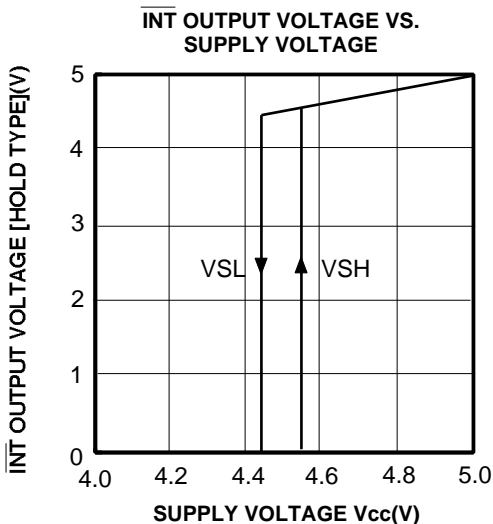
1. Two Step Detection

The ICs perform 2-step detection of supply voltage and have 2 output pins (INT and RESET). Although they have 2 comparators for 2-step detection, they differ significantly from such that are simply provided with independent detectors, because the RESET output signal is dependent at power-up and the like upon the INT output signal.

2. INT output (Detection of 4.45V and 4.25V)

The INT output at the power-up of supply voltage detects V_{SH} (4.45V/4.25V) to inform the microcomputer system of the fact that the supply voltage has reached its normal level. When the supply voltage drops from its normal level to V_{SL} (4.45V/4.25V) an interruption signal is output to alter the microcomputer system into RAM backup mode. The microcomputer at this point enters sleep state and secures memory by a stop command issued by the interruption signal. These detection voltage, V_{SH} the rise, and V_{SL} the fall, of supply voltage, have a 100-mV hysteresis voltage between themselves.

$$V_{SH} - V_{SL} \approx 100(\text{mV})$$



3. RESET Output (Detection of 2.15V)

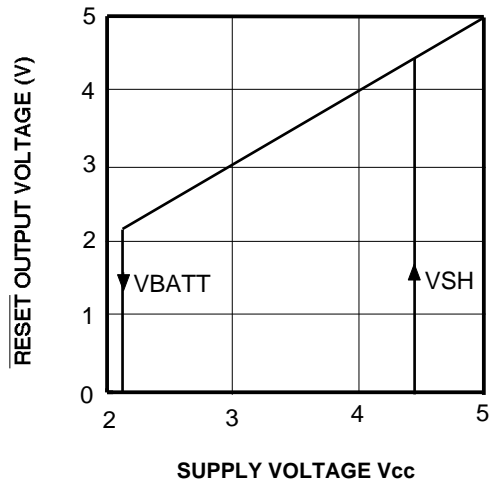
The RESET outputs a signal to prevent the microcomputer from malfunctioning due to a drop in supply voltage. When powering up, RESET is kept at low level until the supply voltage reaches V_{SH}. If the supply voltage rises to V_{SH}, RESET is set to high level. By inserting a capacitor between the Cd pin and GND, it is possible to produce a desired delay time (td). To set a delay time, equation below is used.

$$t_d \approx 1.52 \times 10^5 \times X_C d (\text{sec})$$

Once the supply voltage has exceeded V_{SH} and the RESET output is set to high level, RESET maintains the high level until the supply voltage drops to V_{BATT}. When the supply voltage drops to V_{BATT}, RESET goes low thereby resetting and initializing the microcomputer.

The RESET output has a large hysteresis voltage of approximately 2V between the rise in supply voltage at power-up and its fall.

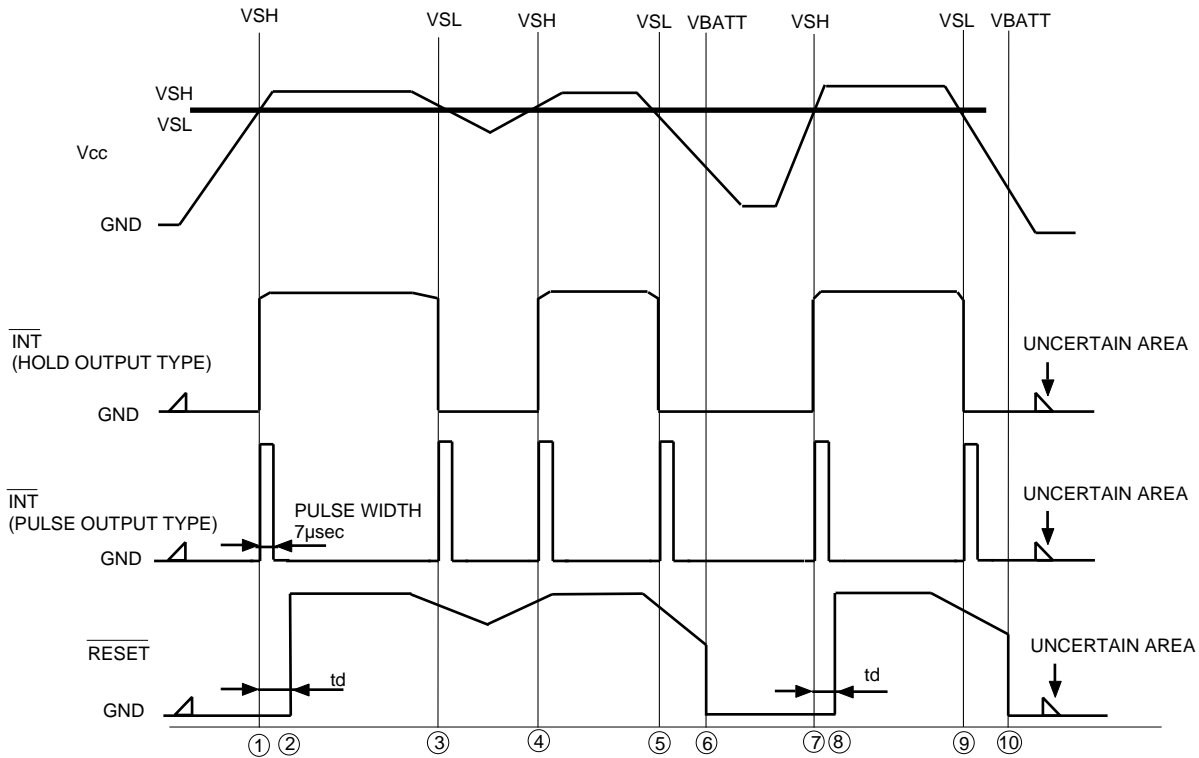
RESET OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



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LOW POWER 2 OUTPUT SYSTEM RESET IC SERIES

OPERATION DESCRIPTION



- ① If V_{cc} rises to $V_{SH}(4.55V/4.35V)$, the \overline{INT} output is set to high level.
*1. A pulse is output if \overline{INT} is of pulse output type.
- ② \overline{RESET} goes high t_d (s) after V_{SH}
* $t_d=1.52 \times 105XC$ (sec)
- ③ If V_{cc} drops to $V_{SH}(4.55V/4.25V)$, \overline{INT} goes low.
*1. A pulse is output if \overline{INT} is of pulse output type.
*2. The \overline{RESET} output continues to be held high.
- ④ If V_{cc} returns to V_{SH} , the \overline{INT} output is set to high level.
- ⑤ Same as ③.
- ⑥ If V_{cc} becomes lower than $V_{BATT}(2.15V)$, the \overline{RESET} output is set to low thereby resetting the microcomputer and initializing system.
- ⑦ Same as ①.
- ⑧ Same as ②.
- ⑨ Same as ③ and ⑤.
- ⑩ Same as ⑥.

APPLICATION EXAMPLE

