M62301SP,FP

10~12-BIT 4CH INTEGRATING A-D CONVERTER

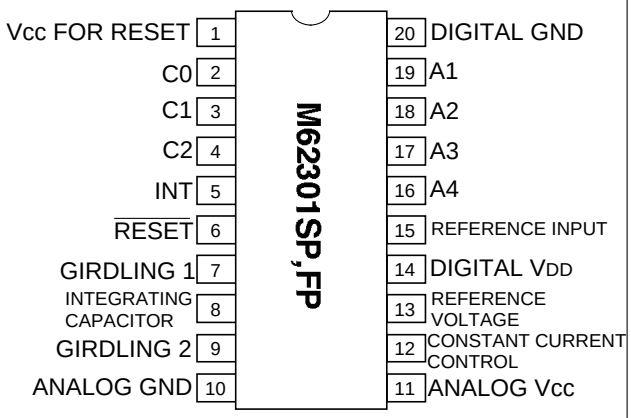
DESCRIPTION

M62301 semiconductor integrated circuit forms an integrating A-D converter,being connected to a microcomputer unit.By using selection signals and counter clock signals from the unit,a 10~12-bit A-D converter can be created at a low cost.

The integration time and resolution can be set at the user's option by changing external parameters.In addition,the built-in circuit offset,delay time and temperature fluctuation are adjustable,enabling a wide range of applications.

M62301 has a 3 input decoder circuit,high-precision reference voltage(1.22V)generator,current supply and comparator for integration,and voltage-monitoring reset circuit for a 5V power supply.It is also equipped with girdling to prevent current leak from integration capacitor.

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B(SP)
20P2N-A(FP)

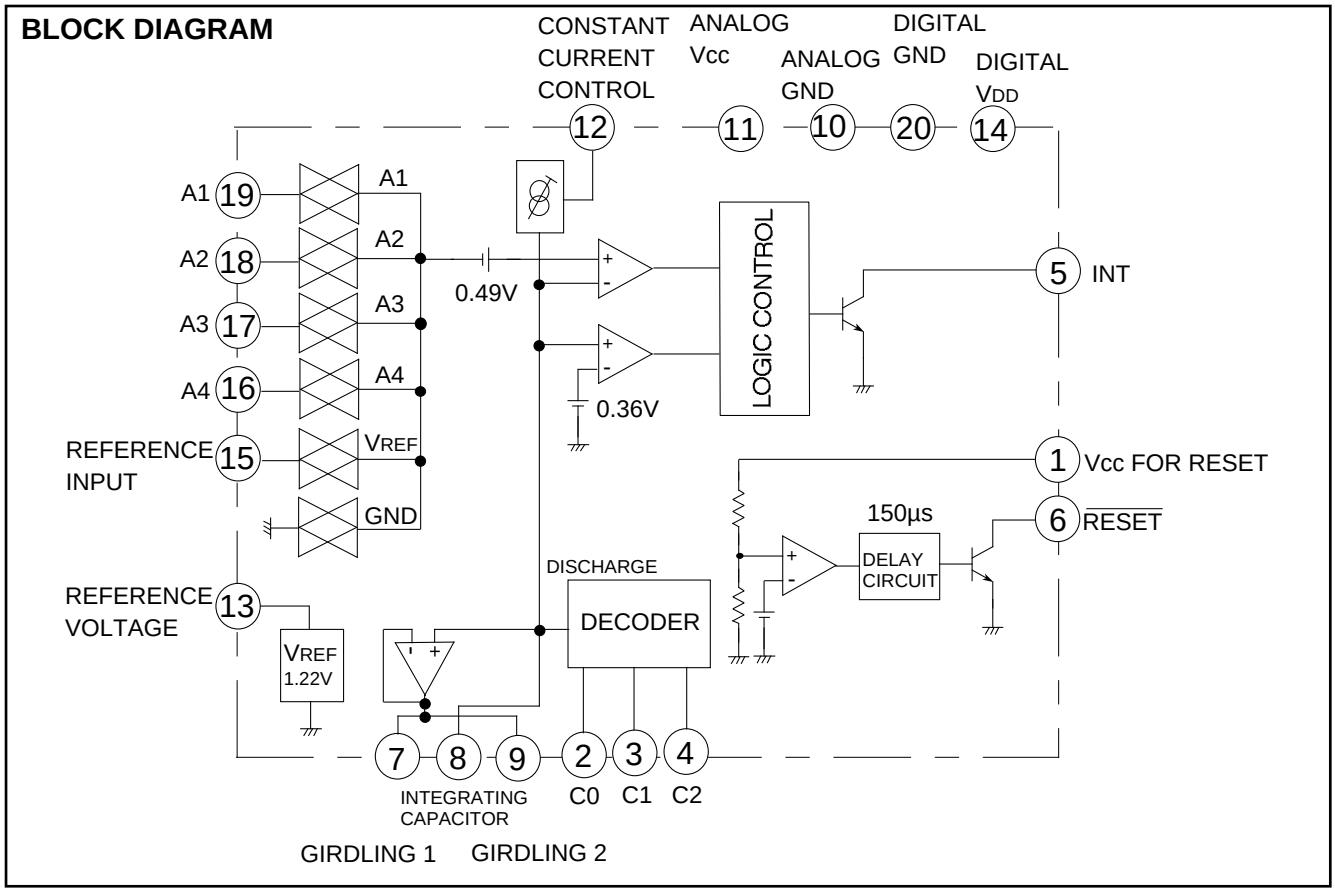
FEATURES

- Separate power supplies for analog section and digital section.
- Low power dissipation.....2mA(typ)
  (1mA for A-D conversion and the other 1mA for reset)
- Linear error.....±0.02%(typ)
- Conversion time.....526µs/ch(typ)
- Built-in system reset.....4.45V(typ)

APPLICATION

High-precision control systems such as temperature control and speed control

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Analog section supply voltage		15	V
V_{DD}	Digital section supply voltage		8	V
V_{ID}	Digital input voltage		-0.3~VDD+0.3	V
V_{IA}	Analog input voltage		-0.3~VDD+0.3	V
I_{OINT}	INT output current		6	mA
I_{ORE}	Reset output current		6	mA
V_{INT}	INT output withstand voltage		15	V
V_{RESET}	Reset output withstand voltage		15	V
V_{RE}	Reset supply voltage		6	V
Pd	Power dissipation		990(DIP)/660(FP)	mW
K_Θ	Thermal derating		9.9(DIP)/6.6(FP)	mW/°C
T_{opr}	Operating temperature		-20 ~ +75	°C
T_{stg}	Storage temperature		-55 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Analog section supply voltage	4.5	8.0	12.0	V
V_{DD}	Digital section supply voltage	4.5	5.0	5.5	V
V_{IA}	Analog input voltage range (I_I=50μA)	0		No more than(Vcc-2.5V) and V_{DD}(Note 1)	V
V_{IR}	Reference input voltage(I_I=50μA)	1	—	No more than(Vcc-2.5V) and V_{DD}(Note 1)	V
C_I	Integration capacity	300	—	22000	pF
R_I	Resistance to determine charge current	6	—	60	kΩ
I_O	Output current		—	4	mA

Note 1.Maximum analog input voltage is less than the difference between Vcc-2.5V as well as V_{DD}.

*Charging current $I_I = \frac{V_{REF}}{R1}$

ELECTRICAL CHARACTERISTICS(Vcc=5.0V,V_{DD}=5.0V,Ta=25°C, unless otherwise noted)

	Symbol	Parameter	Test conditions	Limits			Unit
				Min.	Typ.	Max.	
A-D converter	Icc	Supply current		—	1.0	2.0	mA
	V_{IA}	Analog input voltage range	I_I=100µA	0		2.5	V
			I_I=200µA			2.2	
	V_{REF}	Reference input voltage	I_{REF}=±5µA C_{REF}=4700pF	1.17	1.22	1.27	V
	I_{REF} ⊕	Permissible current inflow at reference voltage				50	µA
	I_{REF} ⊖					-10	
	Ec	Conversion error	(Note 1)R_I=24kΩ		0.05	0.1	%/FSR
	E_L	Linear error	(Note 2)R_I=24kΩ		0.02	0.09	%/FSR
	T_T	Conversion time	V_{IA}=2.5V,C_I=0.01µF R_I=24kΩ		526		µs
	Tdi	Discharge time	V 8=3V→ 0.3V C_I=4700pF		3	17	µs
	I_B	Analog input current			-0.35	-3.5	µA
	V_{IH}	Digital input “H“ level		3.5			V
	V_{IL}	Digital input “L“ level				0.8	V
	V_{LINT}	INT output “L“ level	I_{OL}=1mA		0.1	0.4	V
	I_{OHINT}	INT output leak current	V 5=15V	—	—	1	µA
Reset section	V_{DET}	Detection voltage		4.30	4.45	4.60	V
	ΔVDET	Hysteresis voltage		30	50	80	mV
	T_{DE}	Delay time		75	150	300	µs
	V_{LRE}	Reset output “L“ level	I_{OL}=1mA		0.1	0.4	V
	I_{OHRE}	Reset output leak current	V 5=15V	—	—	1	µA
	I_{RE}	Supply current	VRE=5V		1.0	2.0	mA
	V_{OPL}	Limit operating voltage	R_L=2.2kΩ,$V_{L\overline{RE}}$≤0.4V		0.75	1.0	V
			R_L=100kΩ,$V_{L\overline{RE}}$≤0.4V		0.6	0.8	

Note 1.Conversion error;Deviation from the line that links the “0“ scale point (mode 0) and reference scale point (mode 3. V_{FSR}=2.5V).Associated with all channels.

Note 2.Linear error;Deviation from the line that links the 0-V input point and 2.5V input point on a given channel.

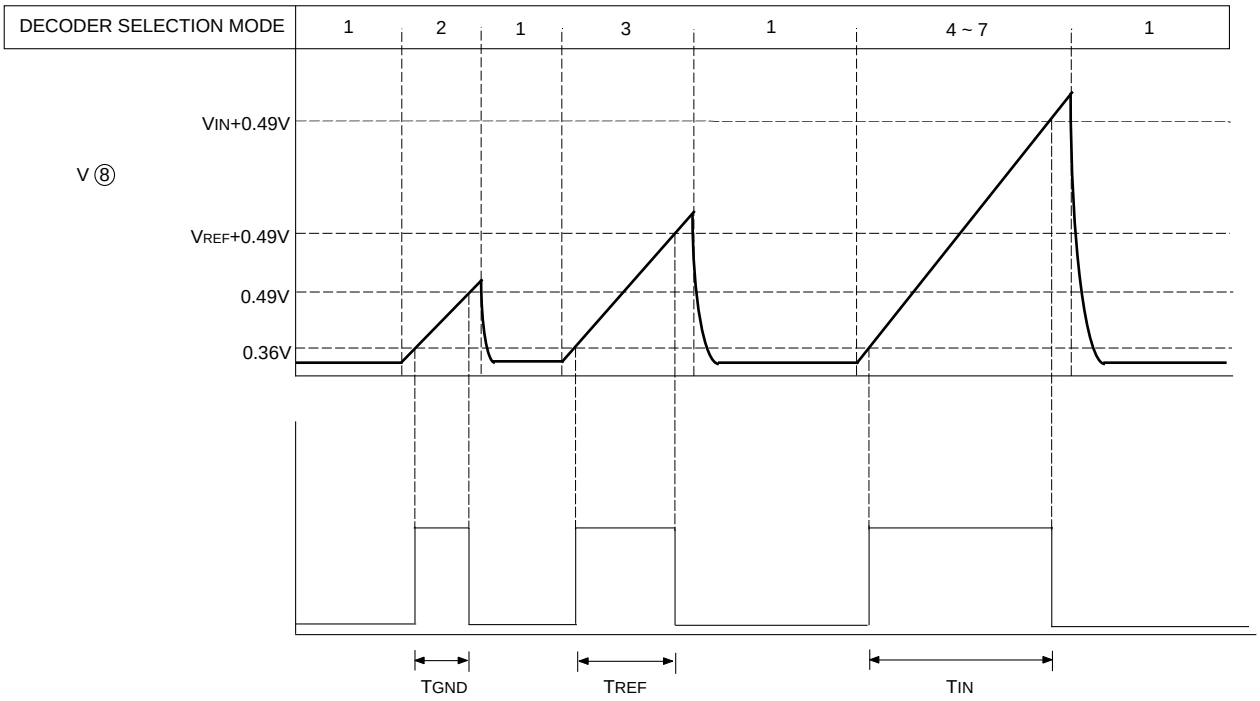
OPERATING DESCRIPTION

(1)Decoder

Based on digital inputs to C0,C1,C2,the analog switch is set to on,and the input of "0" scale (GND input),input of reference scale (reference voltage input),input to A1~A4,or discharge from integration capacitor (C_I) is performed.None of these operations is performed when the "mode 8" input is given:

Mode	1	2	3	4	5	6	7	8
C0	0	1	0	1	0	1	0	1
C1	0	0	1	1	0	0	1	1
C2	0	0	0	0	1	1	1	1
	Discharge	GND	V_{REF}	A1	A2	A3	A4	—

(2)A-D conversion



Multiplexer first selects V_{GND},obtaining minimum pulse T_{GND}.It then selects V_{REF},obtaining reference pulse T_{REF}.Input is selected next,obtaining input pulse T_{IN}.V_{IN} is obtained by deducting T_{GND},as the offset,from T_{REF} and T_{IN}.

$$V_{IN}=V_{REF} \bullet \frac{T_{IN}-T_G}{T_{REF}-T_G}$$

By measuring voltage at the maximum input for approximately 500µs under the counter clock of 8MHz,resolution of approximately 12bits can be obtained;

$$\frac{500\mu s}{125ns} \fallingdotseq 2^{12}$$

Note. To ensure discharge from capacitor C_I,the decoder input as in the above diagram should stay in mode 1 at least for the period calculated above:$Tdi=(C_I \times \frac{V_{IA}max+0.49}{1mA})$

It is not necessary to measure T_{GND},and T_{REF} for each channel.

(3)Constant current control

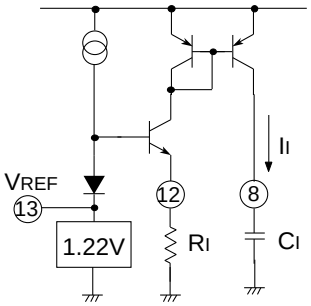
Integrating current I_I can be obtained based on the reference voltage(1.22V)by the built-in high-precision generator and resistance R_I.

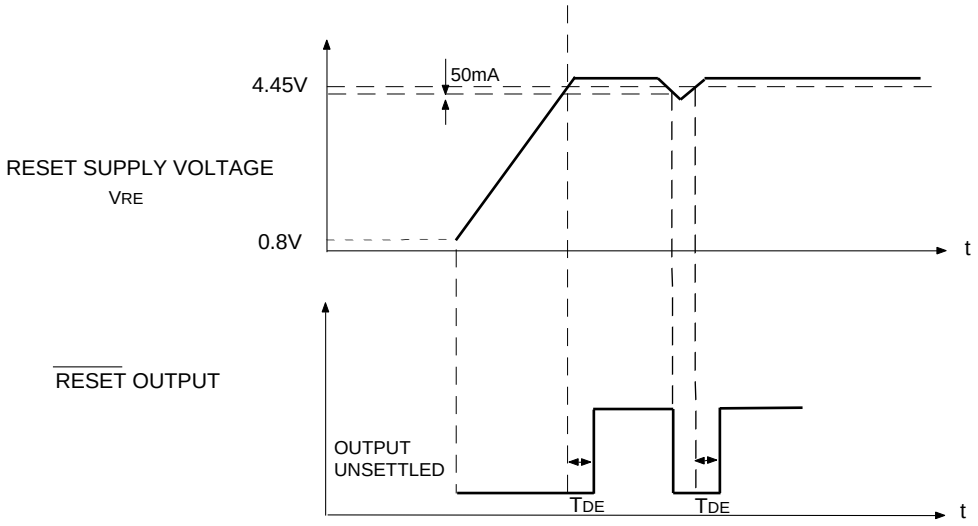
$$I_I = \frac{1.22}{R_I} \text{ (A)} \quad \text{.....(1)}$$

Integration time T_I can be calculated as follows;

$$T_I = (V_{IN} + 0.49) \frac{CI}{I_I} \quad \text{.....(2)}$$

(However,parameters such as built-in comparator offset voltage,analog switch offset,voltage leak current and delay time are not counted.)

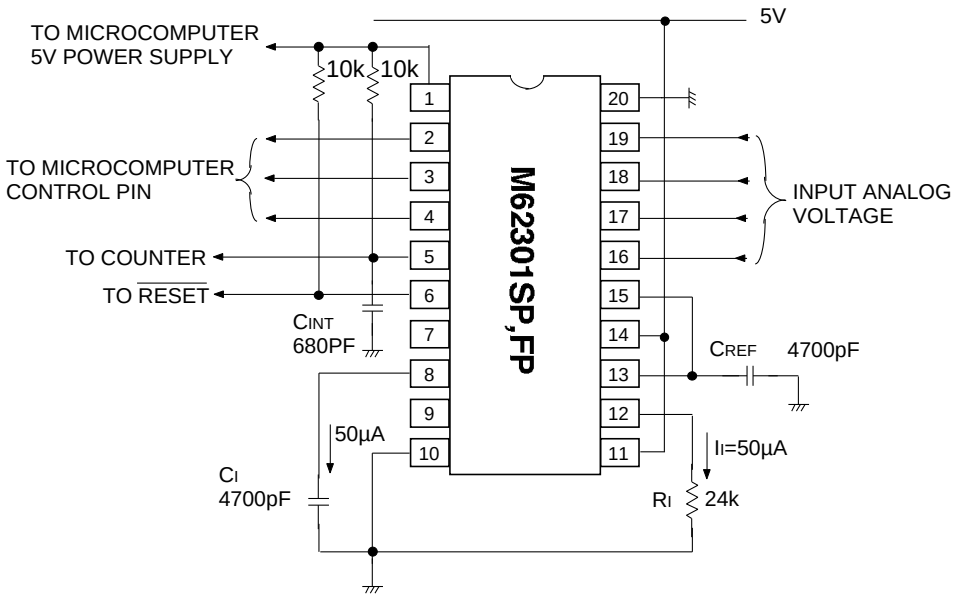




When voltage applied to pin V_{RE} becomes less than 4.45V,the $\overline{\text{RESET}}$ output status becomes "L".If voltage increases over 4.50V,the $\overline{\text{RESET}}$ status becomes "H" within 150µsec.

APPLICATION SUGGESTION

1.4-channel 11-bit A-D converter system



CREF:To stabilize reference voltage, be sure to connect capacitance of approximately 4700pF.

CINT:We suggest that this capacitance be connected to prevent malfunction due to noise.

Use CI that leaks as slight current as possible.To prevent leak to the circuit board,we recommend providing girdling ⑦ , ⑨

Charge current $I_I = \frac{1.22V}{24k\Omega} \fallingdotseq 50\mu A$

Resolution depends on the number of microcomputer counter clock pulses that are generated while the INT output status is "high" at the maximum input voltage 2.5V (vcc-2.5V).

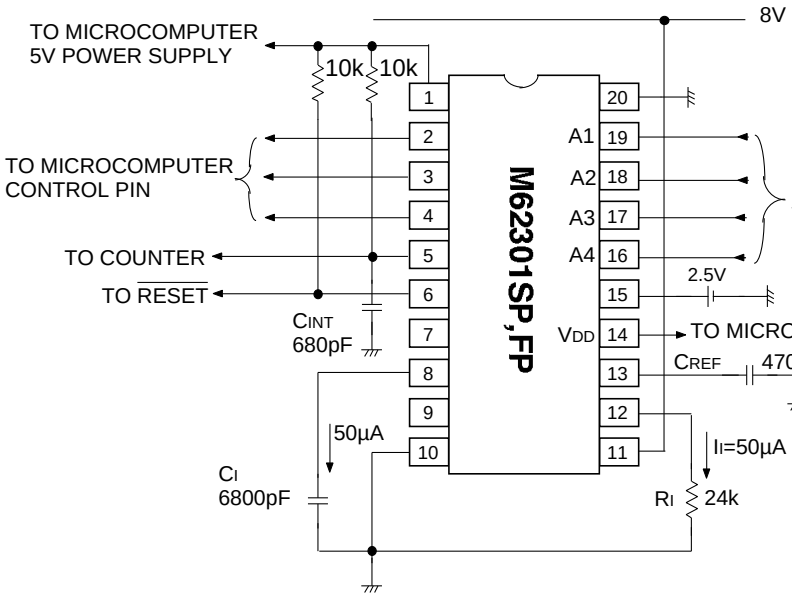
When the microcomputer counter clock frequency is 8MHz,the resolution can be calculated by using the constant calculated above,as follows;

$$\frac{4700pF \times \frac{(2.5+0.13)}{50\mu A}}{\frac{1}{8M}} \fallingdotseq 2^{11}$$

Therefore,the resolution of this system is approximately 11 bits.

2.4-channel 12-bit A-D converter system

Separate power supplies to analog section and digital section, analog input voltage range mode wider up to V_{DD},external reference voltage for integration.



C_{REF}:To stabilize reference voltage, be sure to connect capacitance of approximately 4700pF.

C_{INT}:We suggest that this capacitance be connected to prevent malfunction due to noise.

Use CI that leaks as slight current as possible.To prevent leak to the circuit board,we recommend providing girdling ⑦ , ⑨

Because separate power supplies are provided for the analog are digital sections,the M62301 has two supply voltage Vcc and V_{DD},enabling a wide analog input voltage range V_{IA}.The upper limit of the range is required to be no more than the difference between Vcc-2.5V as well as V_{DD},therefore,the analog input voltage range in this application is 0V to 5V.

When the counter clock frequency is 8MHz,resolution is:

$$\frac{6800pF \times \frac{(5 + 0.13)}{50\mu A}}{\frac{1}{8M}} \fallingdotseq 2^{12}$$

An A-D converter system with resolution of approximately 12 bits can be formed.

Recommended operational settings according to clock frequency,resolution,and time required for discharge(decoder mode 1)

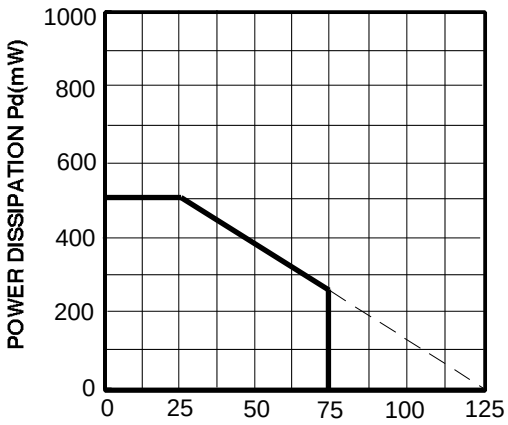
Counter clock	Resolution	Change current I_I(μA)	Resistance to determine constant current R_I(kΩ)	Integration capacitance C_I	Discharge time Tdi(μs)
8MHz	10-bit	50	24	1400pF	7.7
		100	12	2800pF	15.4
	11-bit	50	24	2800pF	15.4
		100	12	5600pF	30.7
	12-bit	50	24	5600pF	30.7
		100	12	12000pF	65.9
16MHz	10-bit	50	24	700pF	3.9
		100	12	1400pF	7.7
	11-bit	50	24	1400pF	7.7
		100	12	2800pF	15.4
	12-bit	50	24	2800pF	15.4
		100	12	5600pF	30.7

Note 1.Discharge time $Tdi=(C_I \times \frac{V_{IA}max+0.49}{1mA})$

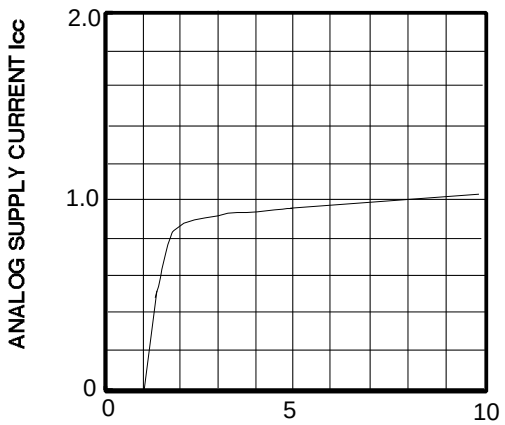
The values in this table apply when V_{IA}max is 5V.

TYPICAL CHARACTERISTICS

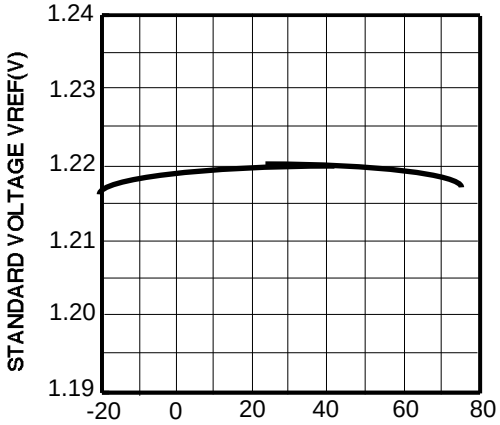
THERMAL DERATING



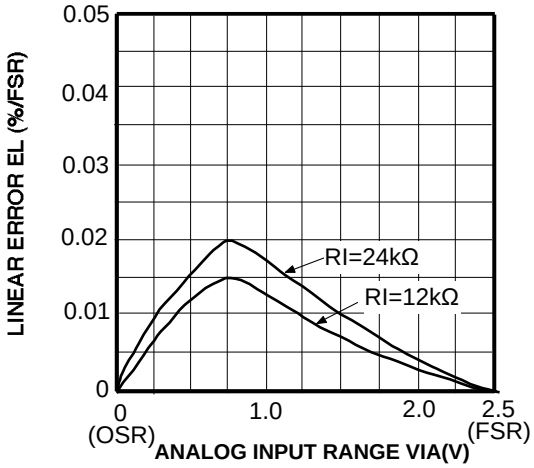
ANALOG PART SUPPLY CURRENT VS.SUPPLY VOLTAGE



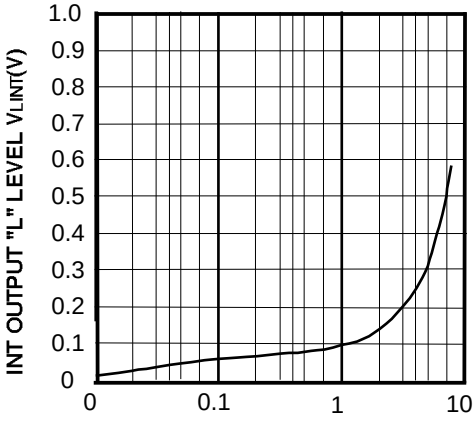
STANDARD VOLTAGE VS. AMBIENT TEMPERATURE



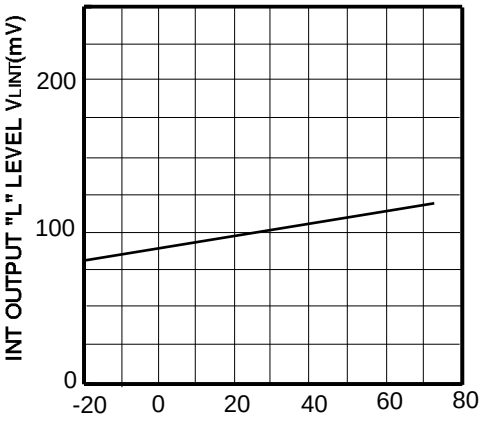
LINEAR ERROR



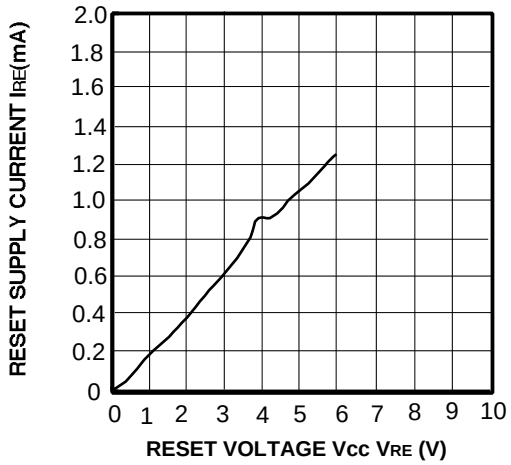
INT OUTPUT "L" LEVEL VS.OUTPUT CURRENT



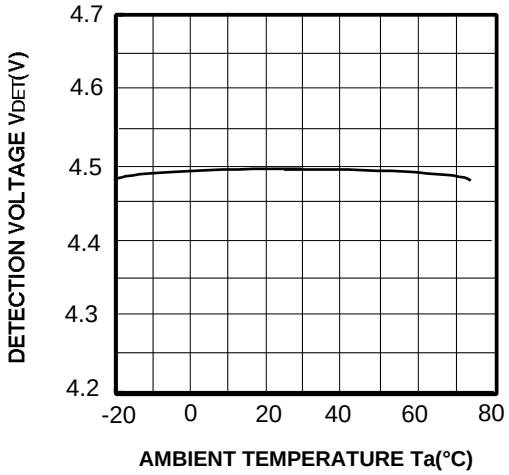
INT OUTPUT VS.AMBIENT TEMPERATURE



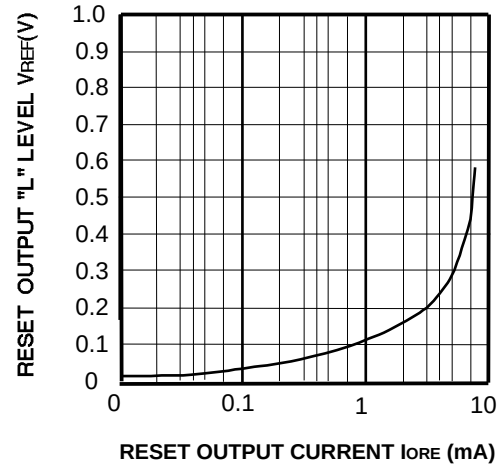
RESET SUPPLY CURRENT VS. SUPPLY VOLTAGE



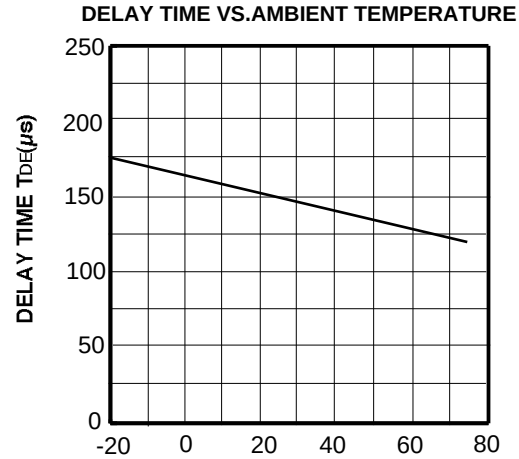
DETECTION VOLTAGE vs. AMBIENT TEMPERATURE



RESET OUTPUT "L" LEVEL VS.OUTPUT CURRENT



DELAY TIME VS.AMBIENT TEMPERATURE



LIMIT RESET VOLTAGE