

M62332P/FP, M62337P/FP

R03DS0037EJ0500 Rev.5.00 Jun 03, 2011

8-bit 2ch I²C BUS D/A Converter with Buffer Amplifiers

Description

The M62332/M62337 is an integrated circuit semiconductor of CMOS structure with 2 channels of built in D/A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from $V_{\rm CC}$ to ground.

The M62332 and the M62337 differ only in their slave address.

Features

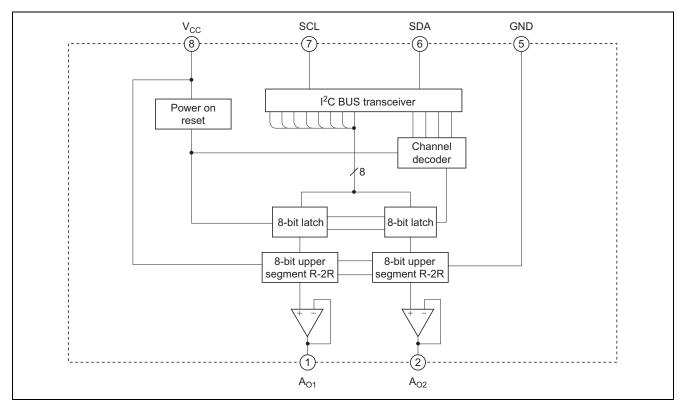
- Digital data transfer format: I²C BUS serial data method
- Output buffer operational amplifier: It operates in the whole voltage range from V_{CC} to ground.
- High output current drive capacity: ±1.0 mA over

Application

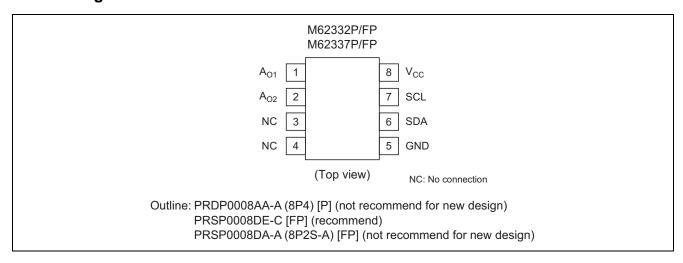
Conversion from digital data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of display-monitor or CTV.

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
6	SDA	Serial data input terminal
7	SCL	Serial clock input terminal
1	A _{O1}	8-bit resolution D/A converter output terminal
2	A _{O2}	
8	Vcc	Power supply terminal
5	GND	GND terminal

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{in}	-0.3 to V_{CC} + 0.3	V
Output voltage	Vo	-0.3 to V_{CC} + 0.3	V
Power dissipation	Pd	417 (P) / 272 (FP)	mW
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-40 to +125	°C

Electrical Characteristics

(V_{CC} = +5 V ± 10%, GND = 0 V, Ta = -20 to +85°C unless otherwise noted)

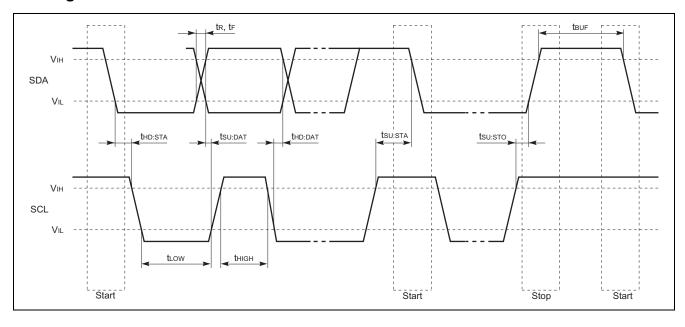
			Limits			
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Supply voltage	V _{CC}	2.7	5.0	5.5	V	
Supply current	I _{CC}	0	0.6	2.5	mA	CLK = 500 kHz operation, $I_{AO} = 0 \mu A$ Data: 6Ah (at maximum current)
		0	0.4	1.6	mA	SDA = SCL = GND, $I_{AO} = 0 \mu A$
Output low voltage (SDA)	V _{OL}	_	_	0.4	V	Isink = 3 mA
Input leak current	I _{ILK}	-10	_	10	μΑ	$V_{IN} = 0$ to V_{CC}
Input low voltage	V_{IL}	1	_	0.2 V _{CC}	V	
Input high voltage	V _{IH}	0.8 V _{CC}	_	_	V	
Buffer amplifier output	V_{AO}	0.1	_	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100 \mu A$
voltage range		0.2	_	$V_{CC} - 0.2$	V	$I_{AO} = \pm 500 \mu A$
Buffer amplifier output	I _{AO}	-1.0	_	1.0	mA	Upper side saturation voltage = 0.3 V
drive range						Lower side saturation voltage = 0.2 V
Differential nonlinearity	S _{DL}	-1.0	_	1.0	LSB	V _{CC} = 5.12 V (20 mV/LSB)
Nonlinearity	SL	-1.5	_	1.5	LSB	without load $(I_{AO} = 0)$
Zero code error	Szero	-2.0	_	2.0	LSB	
Full scale error	S _{FULL}	-2.0	_	2.0	LSB	
Output capacitate load	Co	_	_	0.1	μF	
Buffer amplifier output impedance	R _O	_	5.0	_	Ω	

I²C BUS Line Characteristics

Item	Symbol	Min	Max	Unit
SCL clock frequency	f _{SCL}	0	100	kHz
Time the bus must be free before a new transmission can	t _{BUF}	4.7	_	μS
start				
Hold time START condition	t _{HD:STA}	4.0	_	μS
(After this period, the first clock pulse is generated)				
Low period of the clock	t _{LOW}	4.7	_	μS
High period of the clock	t _{HIGH}	4.0	_	μS
Set-up time for START condition	t _{SU:STA}	4.7	_	μS
(Only relevant for a repeated START condition)				
Hold time DATA	t _{HD:DAT}	0	_	μS
Set-up time DATA	t _{SU:DAT}	250	_	μS
Rise time of both SDA and SCL lines	t _R	_	1000	ns
Fall time of both SDA and SCL lines	t _F	_	300	ns
Set-up time for STOP condition	t _{SU:STO}	4.0	_	μS

Note: Transmitter must internal provide at least a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

Timing Chart



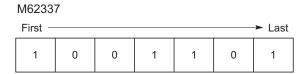
I²C BUS Format

	STA	Slave address	W	Α	Sub address	Α	DAC data	Α	STP
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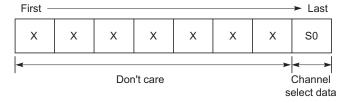
Note: STA: start condition, A: affirmation bit, W: write (SDA = Low), STP: stop condition

• Slave address





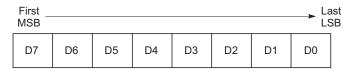
• Sub address



Channel select data

S0	Channel Selection
0	ch1 selection
1	ch2 selection

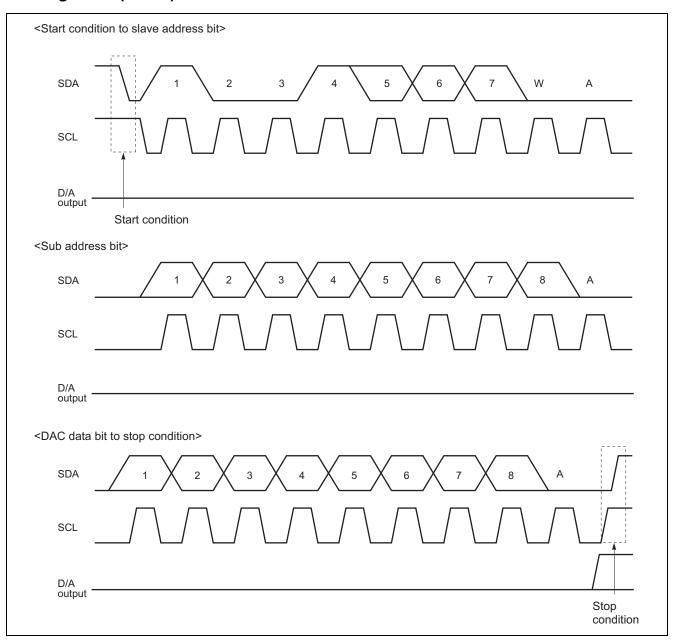
• DAC data





D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	V _{CC} / 256 × 1
0	0	0	0	0	0	0	1	V _{CC} / 256 × 2
0	0	0	0	0	0	1	0	V _{CC} / 256 × 3
0	0	0	0	0	0	1	1	V _{CC} / 256 × 4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	V _{CC} / 256 × 255
1	1	1	1	1	1	1	1	V _{CC}

Timing Chart (Model)



Start condition With SCL at High, SDA line goes from High to Low
 Stop condition With SCL at High, SDA line goes from Low to High (Under normal circumstances, SDA is changed when SCL is Low)

• Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data. (The transmitting IC releases the SDA line just then transmit 8-bit data.)

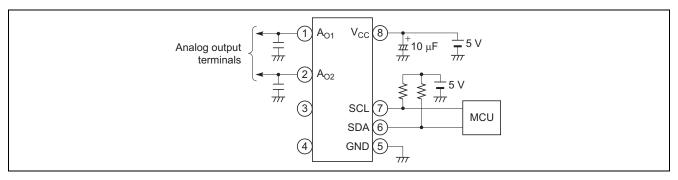
Digital Data Formats

STA	Slave	addre	SS	W	Α	Sub	address 1	А	DA	C data 1	А	

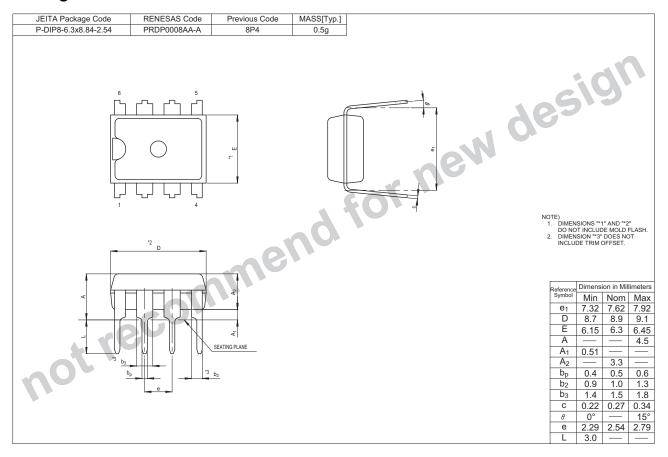
Precaution for Use

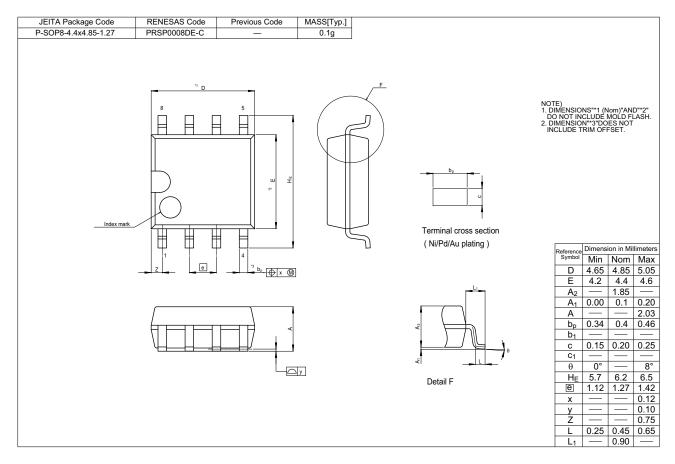
- Supply voltage terminal (V_{CC}) is also used for D/A converter upper reference voltage setting. If ripple or spike is input this terminal, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among V_{CC} to GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor (0.1 μ F Max) among output to GND for every noise eliminate.
- Purchase of Renesas's I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to I²C Standard Specification as defined by Philips.

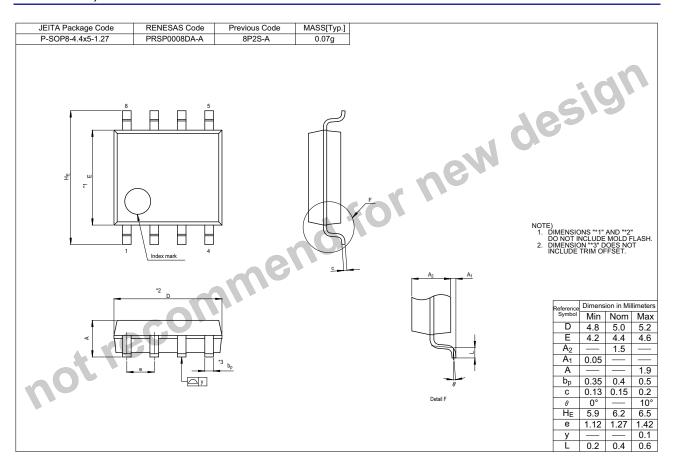
Application Example



Package Dimensions







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