

M62352P/FP/GP

R03DS0041EJ0400 Rev.4.00 Jun 03, 2011

Description

The M62352 is an integrated circuit semiconductor of CMOS structure with 12 channels of built-in D/A converters with output buffer operational amplifiers.

The 3-wire serial interface method is used for the transfer format of digital data to allow connection with microcomputer with minimum wiring.

It is able to cascading serial use with DO terminal.

The output buffer operational amplifier operates in the whole voltage range from power supply to ground for both input/output.

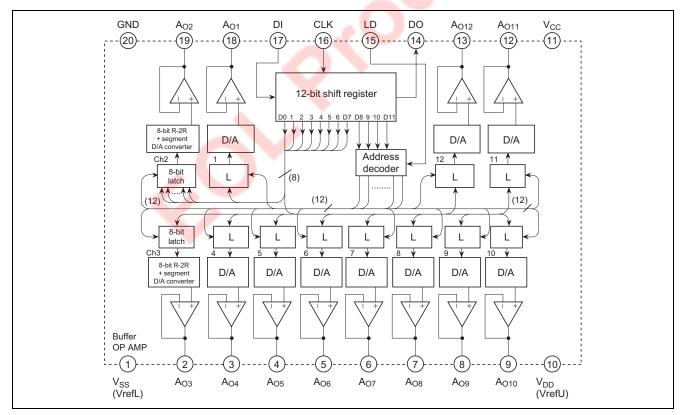
Features

- 12-bit serial data input (3-wire serial data transfer method)
- Highly stable output buffer operational amplifier allow operation in the all voltage range from power supply to ground.

Application

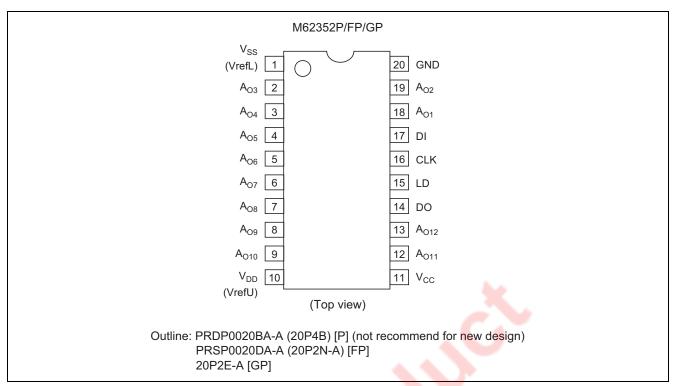
Adjustment/control of industrial or home-use electronic equipment, such as VTR camera, VTR set, TV, and CRT display.

Block Diagram





Pin Arrangement

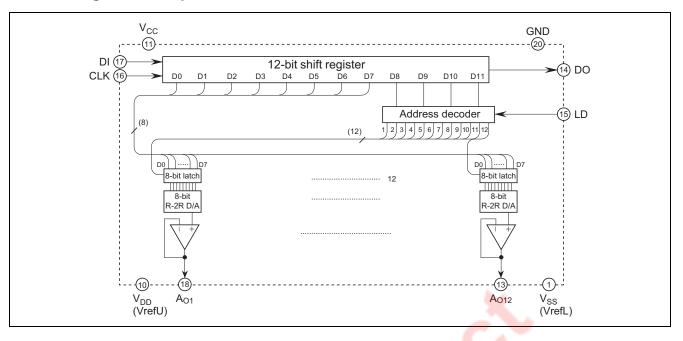


Pin Description

Pin No.	Pin Name	Function
17	DI	Serial data input terminal
14	DO	Serial data output terminal
16	CLK	Serial clock input terminal
15	LD	LD terminal input high level then latch circuit data load
18	A _{O1}	8-bit D/A converter output terminal
19	A _{O2}	
2	A _{O3}	
3	A _{O4}	
4	A ₀₅	
5	A _{O6}	
6	A ₀₇	
7	A _{O8}	
8	A _{O9}	
9	A _{O10}	
12	A ₀₁₁	
13	A ₀₁₂	
11	V _{CC}	Power supply terminal
20	GND	Digital and analog common GND
10	V _{DD}	D/A converter upper reference voltage input terminal
1	V _{SS}	D/A converter lower reference voltage input terminal



Block Diagram for Explanation of Terminals



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{cc}	-0.3 to +7.0	V
D/A converter upper reference voltage	V _{DD}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to V _{CC} + 0.3	V
Output voltage	Vo	-0.3 to V _{CC} + 0.3	V
Power dissipation	Pd	350 (P) / 300 (FP) / 150 (GP)	mW
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-40 to +125	°C

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Electrical Characteristics

Digital Part

 $(V_{CC}, VrefU = +5 V \pm 10\%, V_{CC} \ge VrefU, GND, VrefL = 0 V, Ta = -20^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted})$

			Limits			
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Supply voltage	Vcc	4.5	5.0	5.5	V	
Circuit current	Icc		1.6	3.2	mA	CLK = 1 MHz operation
						$I_{OA} = 0 \ \mu A$
Input leak current	I _{ILK}	-10		10	μA	$V_{IN} = 0$ to V_{CC}
Input low voltage	VIL			0.2 V _{CC}	V	
Input high voltage	VIH	0.8 V _{CC}			V	
Output low voltage	V _{OL}		—	0.4	V	I _{OL} = 2.5 mA
Output high voltage	V _{OH}	$V_{CC} - 0.4$	_	_	V	I _{OH} = -400 μA

Analog Part

(V_{CC}, VrefU = +5 V \pm 10%, V_{CC} \geq VrefU, Ta = -20°C to +85°C, unless otherwise noted)

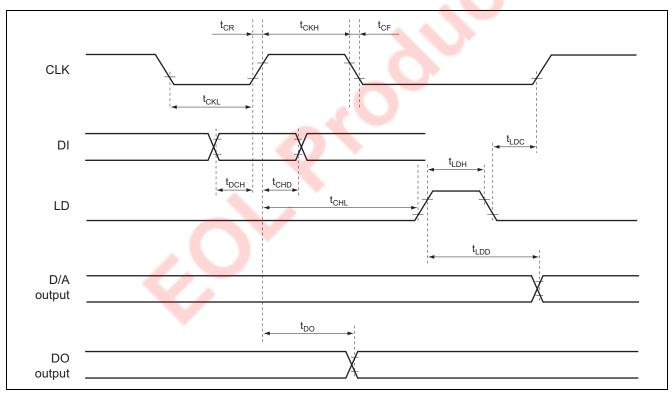
			Limits			
ltem	Symbol	Min	Тур	Max	Unit	Test Conditions
Current dissipation	I _{DD}	—	1.5	3.5	mA	$VrefU = 5 V$, $VrefL = 0 V$, $I_{AO} = 0 \mu A$
						Data condition; at maximum current
D/A converter upper	V _{DD}	3.5		V _{cc}	V	The output dose not necessarily be
reference voltage range						the value within the reference voltage
D/A converter lower	V _{SS}	GND	—	V _{CC} – 3.5	V	setting range. The output value is
reference voltage range						determined by the buffer amplifier
						output voltage range (V _{AO})
Buffer amplifier output	V _{AO}	0.1		V _{CC} – 0.1	V	$I_{OA} = \pm 100 \ \mu A$
voltage range		0.2		$V_{CC} - 0.2$		I _{OA} = ±500 μA
Buffer amplifier output	I _{AO}	-1		1	mA	Upper side saturation voltage = 0.3 V
drive range						Lower side saturation voltage = 0.2 V
Differential nonlinearity	SDL	-1.0		1.0	LSB	VrefU = 4.79 V
error						VrefL = 0.95 V
Nonlinearity error	SL	-1.5	—	1.5	LSB	V _{CC} = 5.5 V (15 mV/LSB)
Zero code error	SZERO	-2	_	2	LSB	Without load ($I_{OA} = \pm 0 \ \mu A$)
Full scale error	SFULL	-2		2	LSB	
Output capacitive load	Co	—	—	0.1	μF	
Buffer amplifier output	Ro	_	5		Ω	
impedance						

AC Characteristics

(V_{CC}, VrefU = +5 V \pm 10%, V_{CC} \geq VrefU, GND, VrefL = 0 V, Ta = -20 to +85°C, unless otherwise noted)

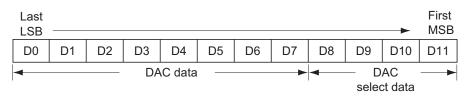
			Limits			
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Clock "L" pulse width	t _{CKL}	200	—	—	ns	
Clock "H" pulse width	t _{скн}	200	—	_	ns	
Clock rise time	t _{CR}	—	—	200	ns	
Clock fall time	t _{CF}	—	—	200	ns	
Data setup time	t _{DCH}	30	—	_	ns	
Data hold time	t _{CHD}	60	—	_	ns	
LD setup time	t _{CHL}	200	—	_	ns	
LD hold time	t _{LDC}	100	—	—	ns	
LD "H" pulse width	t _{LDH}	100	—	—	ns	
Data output delay time	t _{DO}	70	—	350	ns	$C_L \le 100 \text{ pF}$
D/A output setting time	t _{LDD}	—	—	300	μS	$C_L \leq 100 \text{ pF V}_{AO}\text{: } 0.5 \leftrightarrow 4.5 \text{ V}$
						The time until the output becomes
						t <mark>he fi</mark> nal value of 1/2 LSB

Timing Chart





Digital Data Format



DAC Data

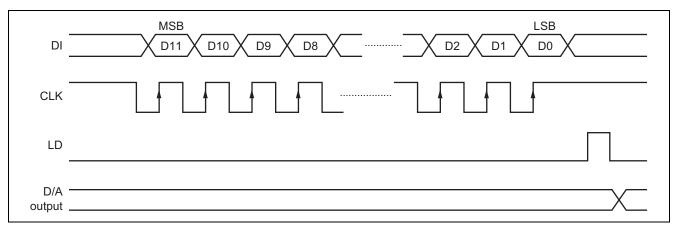
D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL
1	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 2 + VrefL
0	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 3 + VrefL
1	1	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 4 + VrefL
:	:	:	:	:	-	:	:	:
0	1	1	1	1	1	1	1	(VrefU – VrefL) / 256 × 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

Note: $VrefU = V_{DD}$, $VrefL = V_{SS}$

DAC Select Data

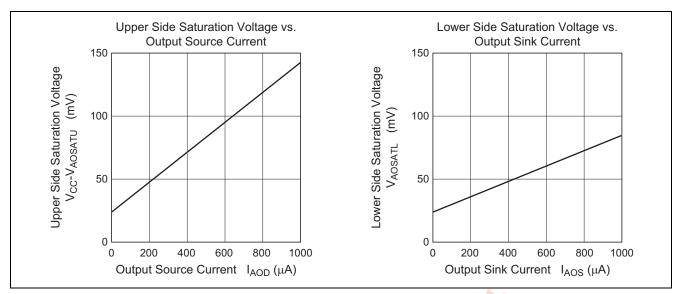
D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	A ₀₁ select
0	0	1	0	A ₀₂ select
0	0	1	1	A ₀₃ select
0	1	0	0	A ₀₄ select
0	1	0	1	A ₀₅ select
0	1	1	0	A ₀₆ select
0	1	1	1	A ₀₇ select
1	0	0	0	A ₀₈ select
1	0	0	1	A ₀₉ select
1	0	1	0	A ₀₁₀ select
1	0	1	1	A ₀₁₁ select
1	1	0	0	A ₀₁₂ select
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



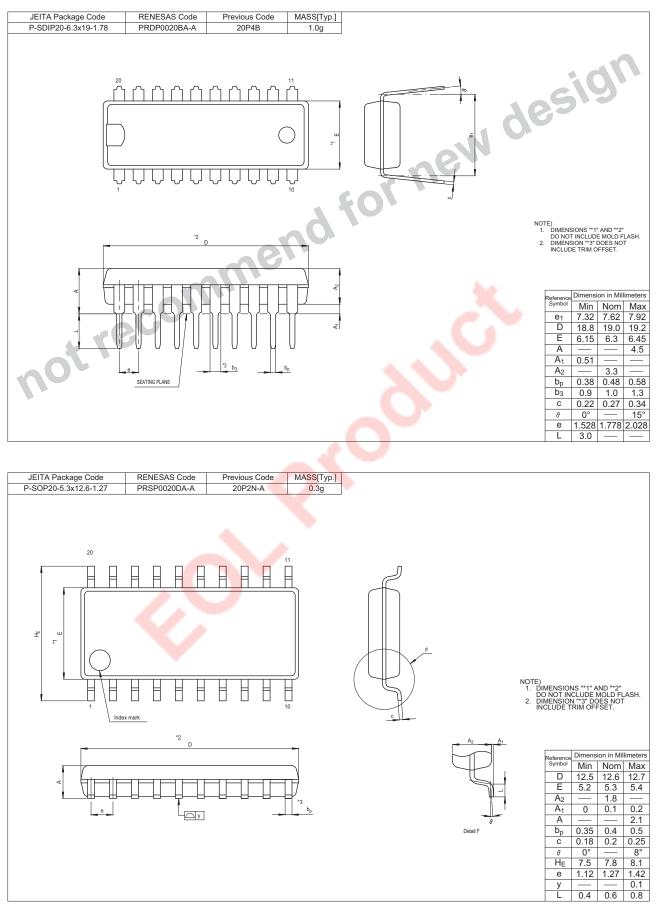


Typical Characteristics

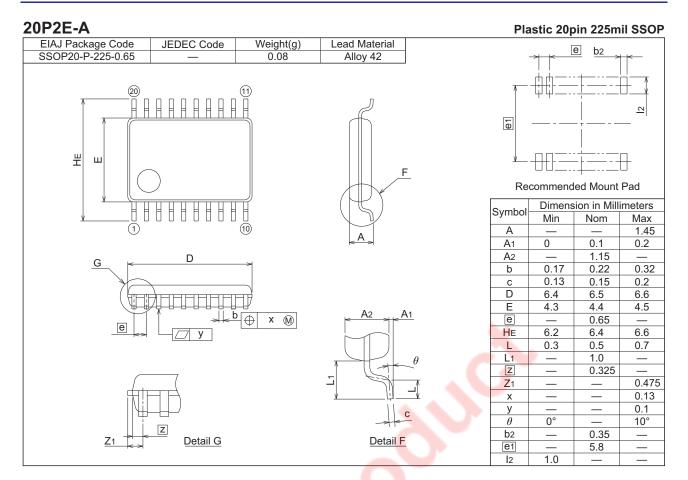




Package Dimensions









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