M62361FP

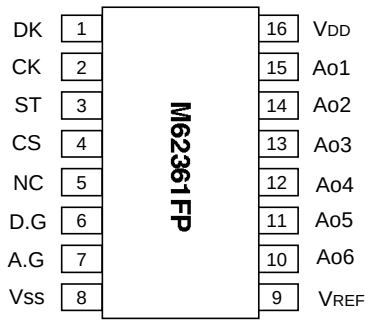
8-BIT 6CH D-A CONVERTER WITH BUFFER AMPLIFIERS

DESCRIPTION

The M62361FP is a Bi-CMOS semiconductor IC,containing 6 channels of 8-bit D-A converters(DAC),with a buffer operational amplifier provided in the output of each channel.It is easy to use due to serial data input, and three-pin(DT,CK,ST)connection with microcomputer.

This IC is designed to be operable when chip select data contained in the 15-bit data conforms to the state of the CS terminal.Accordingly,the IC can process data by strobe signals common with other devices connected to the bus of microcomputer, and does not involve an microcomputer port to drive the IC.The inputs are connected to a level shift circuit so that the input threshold level does not depend on supply voltage.The IC also contains an initialization function to reset output(0 scale)when power is turned ON or drops.

PIN CONFIGURATION (TOP VIEW)



Outline 16P2N-A

NC:NO CONNECTION

FEATURES

- Output buffer operational amplifier provided in each channel
- 15-bit serial data input
- 6 channels of R-2R and segment type 8-bit DAC
- Chip select terminal
- Power-on reset function

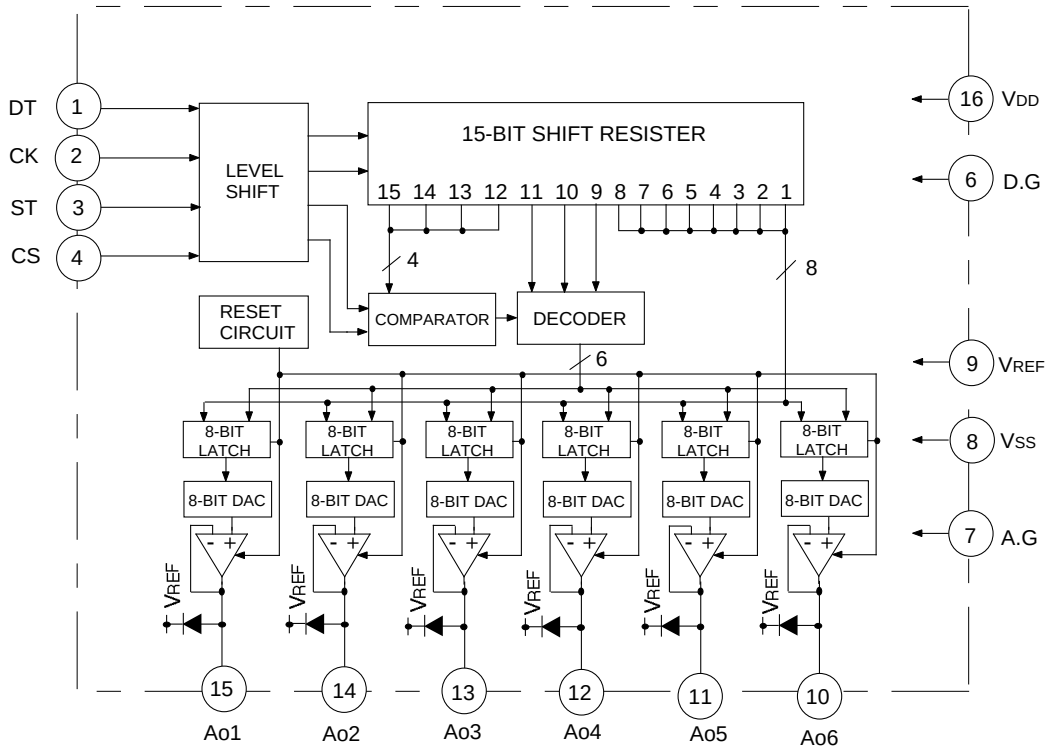
APPLICATION

Digital-analog conversion in industrial or home-use electric equipment.

Automatic control in combination with EEROM and microcomputer(Substitute for conventional semi-fixed resistor)

Signal gain setting of display monitor and CTV.

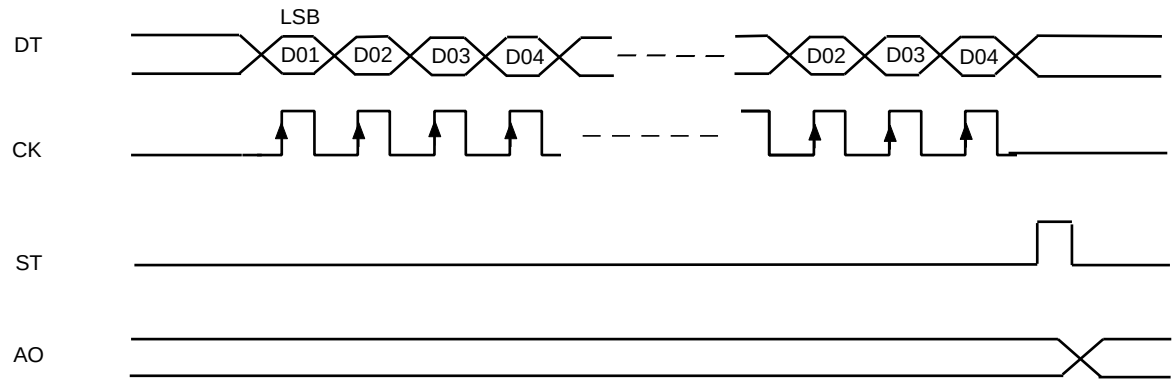
BLOCK DIAGRAM



EXPLANATION OF TERMINALS

Pin No.	Symbol	Function
①	DT	Serial data input terminal
②	CK	Shift clock input terminal to input data at rise of clock pulse
③	ST	Strobe input terminal to latch data in the register when H-level signal is input
④	CS	Chip select terminal
⑯	V_{DD}	Power supply terminal for input level shift circuit and buffer amplifier
⑥	D•G	GND terminal for digital line
⑦	A•G	GND terminal for analog line
⑨	V_{REF}	8-bit D-A converter power supply terminal
⑧	Vss	8-bit D-A converter minimum power supply terminal
⑮	Ao1	8-bit D-A converter output terminal
⑭	Ao2	
⑬	Ao3	
⑫	Ao4	
⑪	Ao5	
⑩	Ao6	
⑤	NC	Not used

TIMING CHART (MODEL)



ABSOLUTE MAXIMUM RATINGS(Ta=25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{DD}	Supply voltage		-0.3~+15	V
V_{REF}	Reference voltage		-0.3~+8	V
V_{IN}	Input voltage		-0.3~V_{DD}	V
Ao	Output voltage		-0.3~V_{DD}	V
Pd	Power dissipation		550	mW
K_θ	Thermal derating		5.5	mW/°C
T_{opr}	Operating temperature		-20~+85	°C
T_{stg}	Storage temperature		-55~+125	°C

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS(Ta=25°C,V_{DD}=8.0V,V_{REF}=5.0V,Vss=0V,R_L=2kΩ unless otherwise noted)

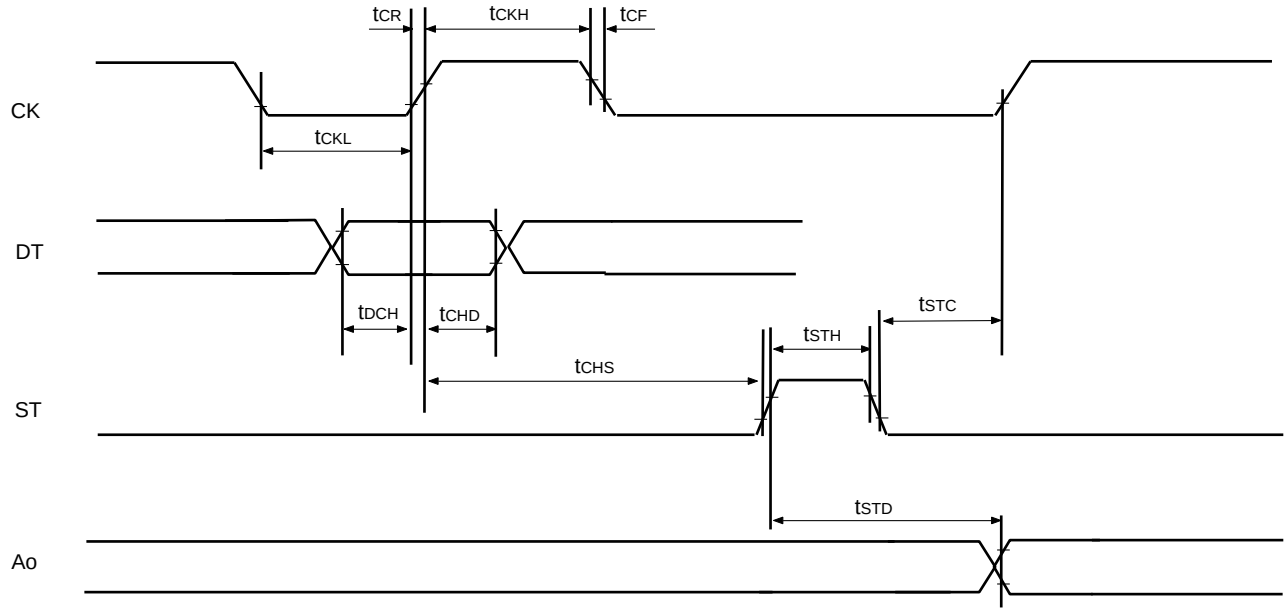
Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Operating supply voltage		Ta=-25 ~ +85°C	6.0	8.0	14.0	V
I_{DD}	Current dissipation		Set at $\frac{128}{256}$ for all channels. RL=∞		5	10	mA
V_{REF}	Voltage range at V_{REF}		V_{REF}=V_{DD}-2V	4.0		7.5	V
Vss	Voltage range at V_{ss}			-0.2	0.0	1.0	V
I_{REF}	Maximum sink current at V_{REF}		Set at $\frac{107}{256}$ for all channels.		1.5	3	mA
RSL	Resolution					8	bit
E_{ZR}	Zero point error		Vss≥0.3V	-1.5		1.5	LSB
E_{FS}	Full scale error			-1.5		1.5	LSB
DNL	Differential nonlinearity error		Monotony assured	-1.0		1	LSB
E_{CH}	Error between channels			-3		3	LSB
V_{IH}	Input voltage	H-level	V_{DD}=6.0 ~ 10V	3.5		V_{DD}	V
V_{IL}		L-level	V_{DD}=6.0 ~ 10V	0		1.0	V
I_{IH}	Input current	H-level	V_{DD}=6.0 ~ 10V		0	10	µA
I_{IL}		L-level	V_{DD}=6.0 ~ 10V		-1.5	10	µA
V_{AO}	Output voltage range			0.3		V_{REF} -2LSB	V
Isink	Output sink current		Set at $\frac{15}{256}$ min. for all channels.	0		100	µA
Isource	Output source current		For FSR*,Ao≥FSR-2LSB	-5		0	mA
SR	Output through rate			0.3			V/µs
VS1	Reset detection voltage 1		Detection of V_{DD} power	4.25	4.45	4.65	V
ΔVS1	Hysteresis voltage 1		Detection of V_{DD} power	0.05	0.1	0.2	V
VS2	Reset detection voltage 2		Detection of V_{REF} power	2.85	3.0	3.15	V
ΔVS2	Hysteresis voltage 2		Detection of V_{REF} power	0.03	0.06	0.15	V

(*Full scale range = maximum output voltage setting)

AC CHARACTERISTICS(Ta=25°C,V_{DD}=8.0V,V_{REF}=5.0V,Vss=0V,R_L=2kΩ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{CKL}	Clock "L"pulse width		200			ns
t_{CKH}	Clock "H"pulse width		200			ns
t_{CR}	Clock rise time				200	ns
t_{CF}	Clock fall time				200	ns
t_{DCH}	Data set up time		300			ns
t_{CHD}	Data hold time		200			ns
t_{CHS}	ST set up time		500			ns
t_{STC}	ST hold time		500			ns
t_{STH}	ST "H" pulse width		500			ns
t_{STD}	Ao output setting time	0→FSR FSR→0			20	µs

TIMING CHART



DESCRIPTION OF OPERATION

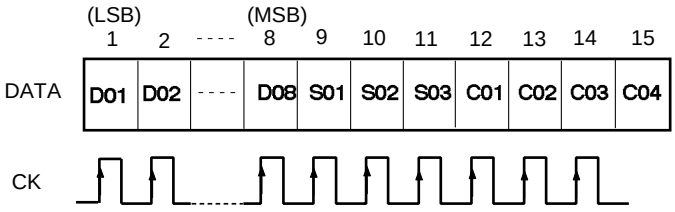
1.Level shift circuit

The logical operation in the IC is controlled by V_{REF} voltage. Therefore,the logical level of input is shifted to DG(Low)or V_{REF}(High),regardless of fluctuating V_{DD}.

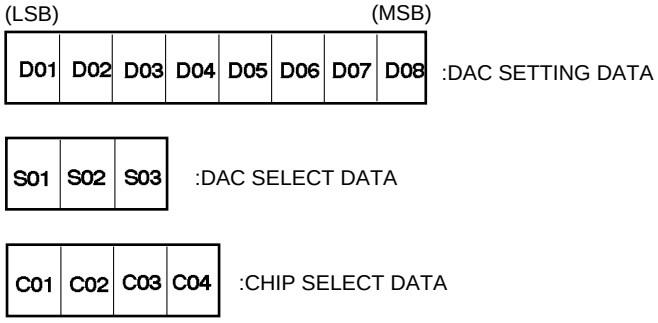
2.15-bit shift register

Data necessary for setting DAC is serially input.The data is input at positive edge of CK signal.The register is capable of retaining 15-bit data consisting of 3 blocks:DAC data.DAC select data and chip select data.

(1)15 bit serial data



(2)Data allocation



3.Decoder(DAC select decoder)

Appropriate one of the 6 DAC channels is selected by the 3-bit DAC select data:S01,S02,S03.

S01	S02	S03	V_{OUT}
0	0	0	1
1	0	0	2
0	1	0	3
1	1	0	4
0	0	1	5
1	0	1	6
0	1	1	not select
1	1	1	not select

4.Comparator(Chip select data)

Whether DAC data is effective or not is determined by the 4-bit data(C01 ~ C04)and the logic at CS terminal.Either of the following data combination is required.

C01	C02	C03	C04	CS
0	0	1	1	0
0	0	1	0	1

5.8-bit latch circuit

When the data input to shift register meets the above requirement for comparator,D01~D08 data are latched in the channel selected by decoder.This data latching takes place when input at ST terminal is HIGH.

6.8-bit DAC + buffer amplifier

Potential difference between V_{REF} and Vss is output with 8-bit resolution,using the R-2R system.No resolution is obtained for bit data lower than the output saturated voltage of the buffer amplifiers data lower than the output saturated voltage of the buffer amplifiers of analog output A01 to A06.The minimum value of 300mA,given for the electrical characteristic concerning output voltage range(V_{AO}),indicates that no resolution is secured for output lower than 300mV.
For all bit data,resolution is secured when Vss is operated with 300mV or higher voltage.

$$Ao = \frac{2^0 X\ D01 + 2^1 X\ D02 + 2^2 X\ D03 + 2^3 X\ D04 + 2^4 X\ D05 + 2^5 X\ D06 + 2^6 X\ D07 + 2^7 X\ D08}{256} \bullet (V_{REF} - Vss) + Vss$$

DAC SETTING DATA(V_{REF}=5.0V,Vss=0V)

(LSB) (MSB)

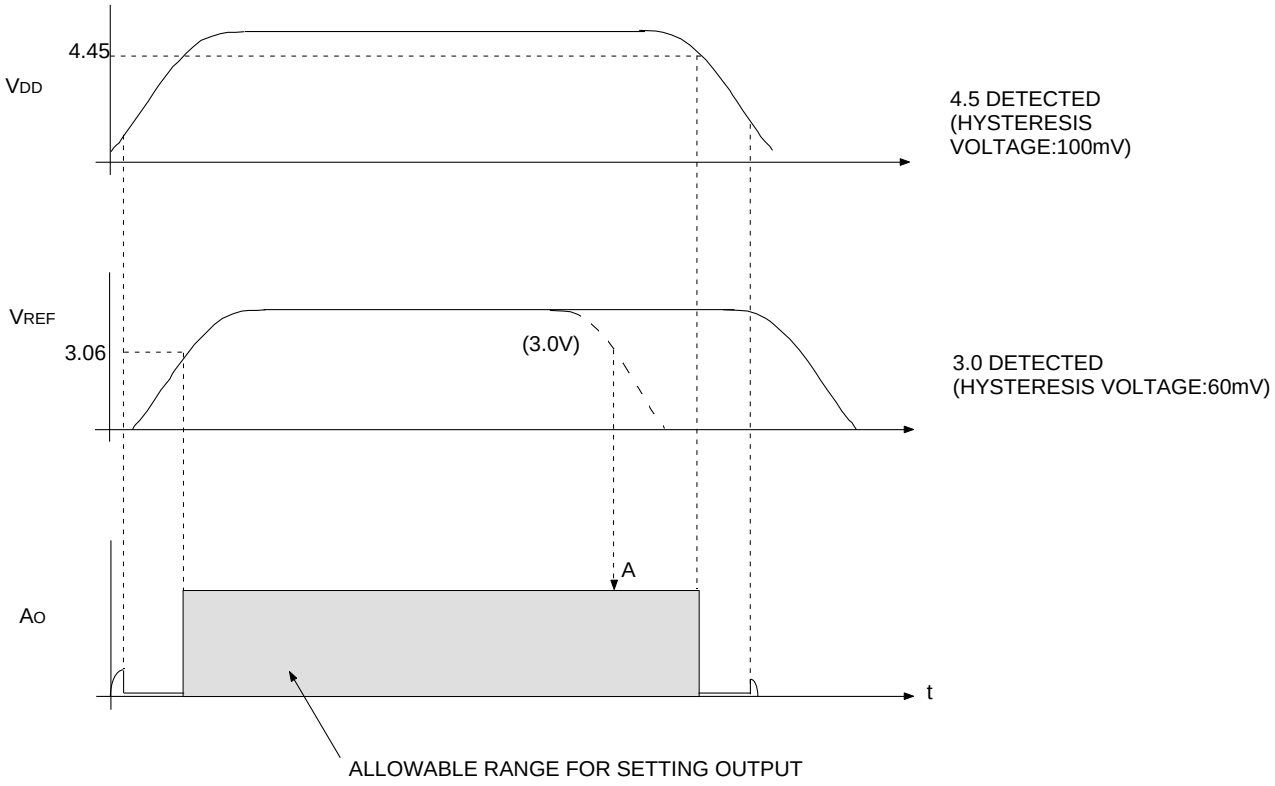
C01	C02	C03	C04	C05	C06	C07	C08	A01~A06		
0	0	0	0	0	0	0	0	Vsat		0
↓	↓	↓	↓	↓	↓	↓	↓	↓		⋮
1	1	1	1	1	1	1	1			(15/256)
0	0	0	0	0	0	0	0	V_{REF}	X	(16/256)
1	0	0	0	0	0	0	0	V_{REF}	X	(17/256)
										⋮
0	1	1	1	1	1	1	1	V_{REF}	X	(254/256)
1	1	1	1	1	1	1	1	V_{REF}	X	(255/256)

7.Reset circuit

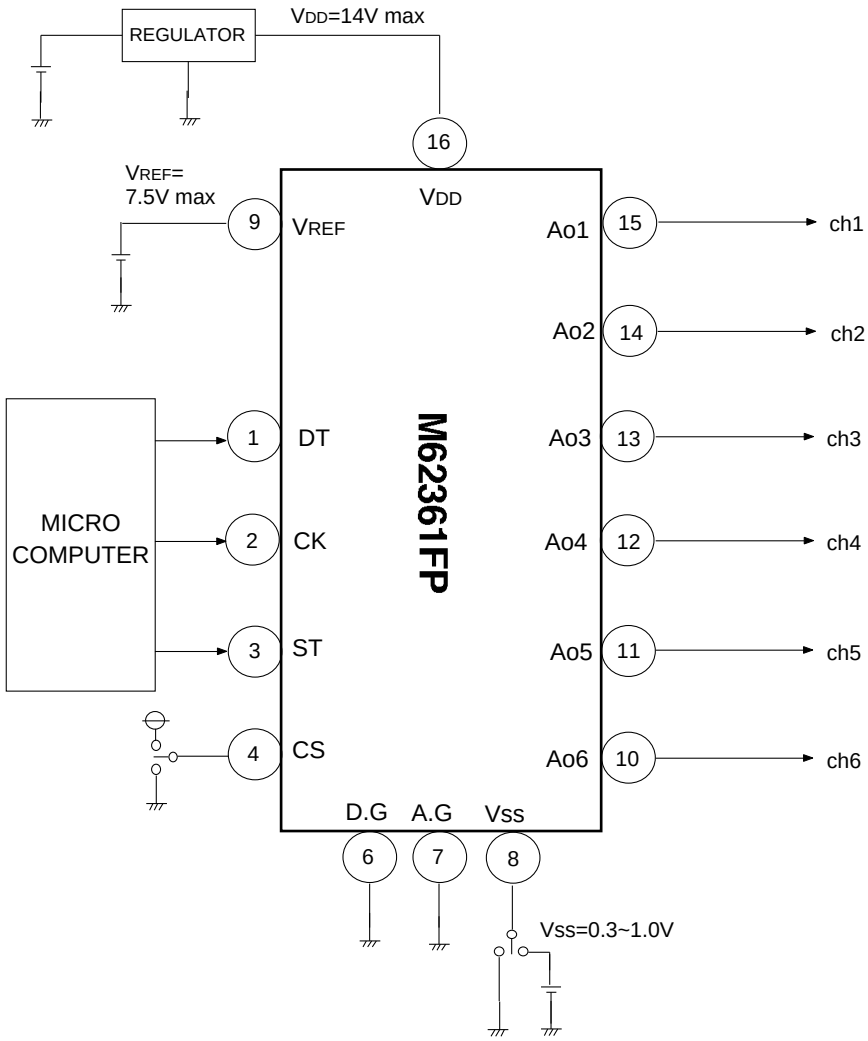
This circuit monitors V_{DD} and V_{REF},ensuring stable analog output when power is turned ON or OFF.If either input is abnormal,the reset circuit causes output buffer amplifiers to stop operation to retain the output in Vsat state,as well as resetting DAC data(0 scale)of all channels.

If V_{REF} drops earlier than V_{DD},the analog output reset operation starts at point A.

RESET TIMING CHART



APPLICATION EXAMPLE

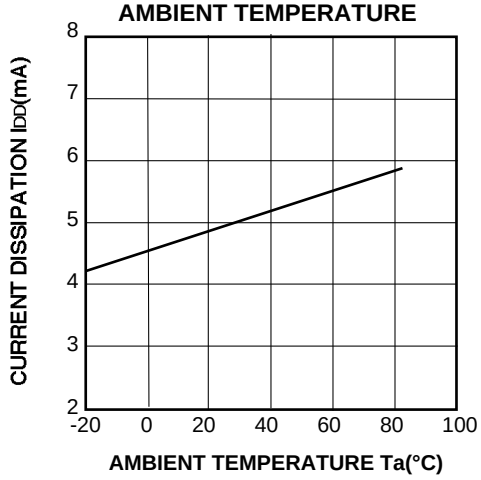


When ⑧ pin is GND,Ao output is 0.3~VREF-1 LSB

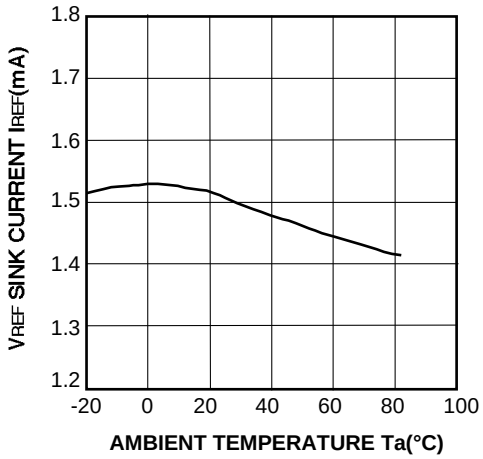
When ⑧ pin is Vss,Ao output is Vss~VREF-1 LSB

TYPICAL CHARACTERISTICS(T_a=25°C, V_{DD}=8.0V, V_{REF}=5.0V, R_L=2kΩ, unless otherwise noted)

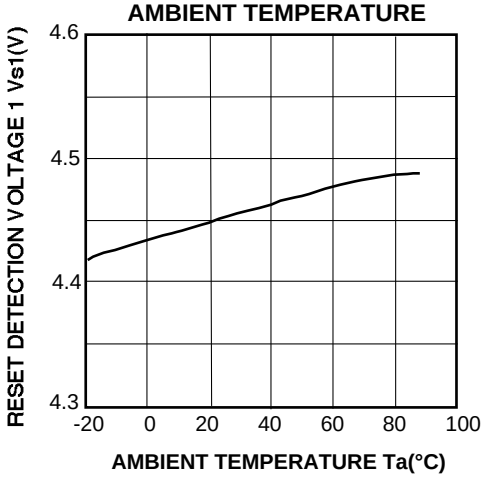
CURRENT DISSIPATION VS. AMBIENT TEMPERATURE



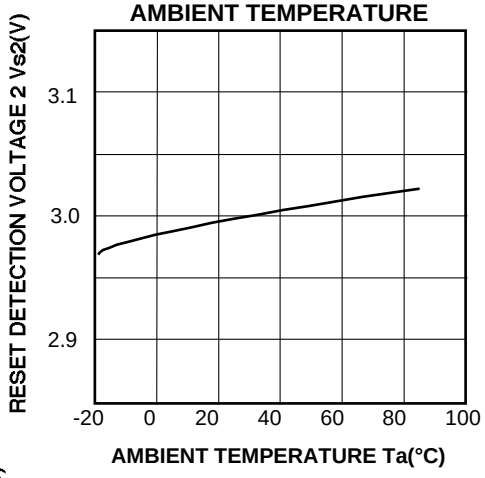
VREF SINK CURRENT VS. AMBIENT TEMPERATURE



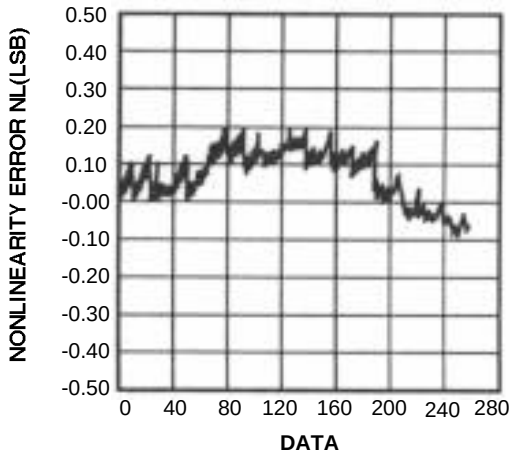
RESET DETECTION VOLTAGE 1 VS. AMBIENT TEMPERATURE



RESET DETECTION VOLTAGE 2 VS. AMBIENT TEMPERATURE



NONLINEARITY ERROR



DIFFERENTIAL NONLINEARITY ERROR