# M62425FP

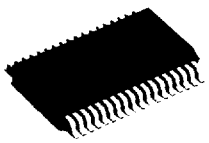
## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

## DESCRIPTION

The M62425FP is a VCA (Voltage Controlled Amplifier) IC developed for electronic volume of AV equipment. Two built-in DAC channels for the VCA control in channels are capable of controlling each channel independently. In addition, 6 built-in output ports is capable of achieving free applications.

## FEATURES

- Built-in VCA circuit for volume control
- Independent control of each channel
- 2 built-in DAC channels for the VAC control in each channel
- Available with ± power supply or single power supply
- Volume variable range from -90 to 0 dB
- Built-in output buffer amplifier capable of setting gain with external installation
- 6 built-in open collector type output ports (NPN transistor)
- Built-in microcomputer interface circuit controlled with 10-bit serial data
- 2-wire system of clock and data for transmitting data from microcomputer

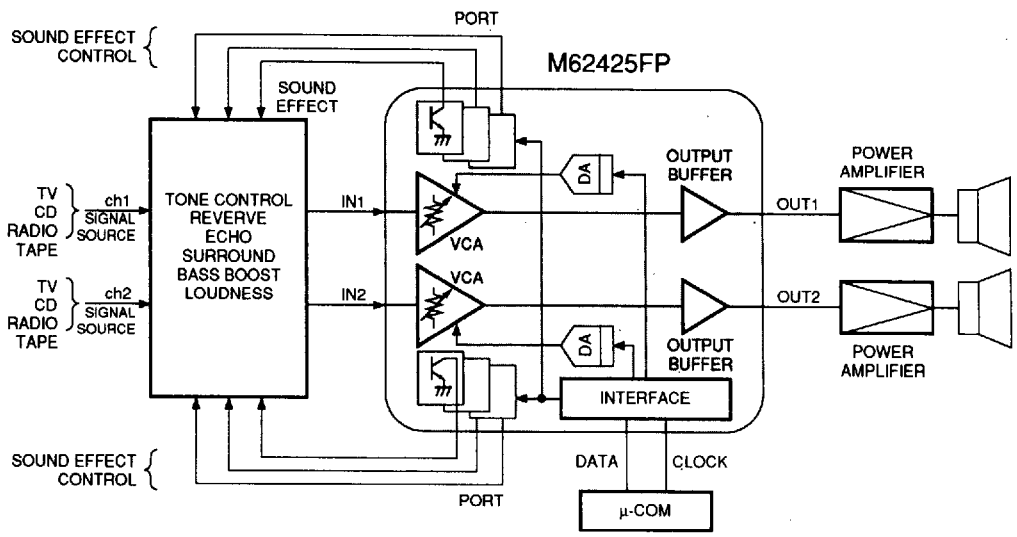


Outline 36P2R-A
0.8 mm pitch 450 mil SSOP
(8.4 mm X 15.0mm X 2.0 mm)

## RECOMMENDED OPERATING CONDITIONS

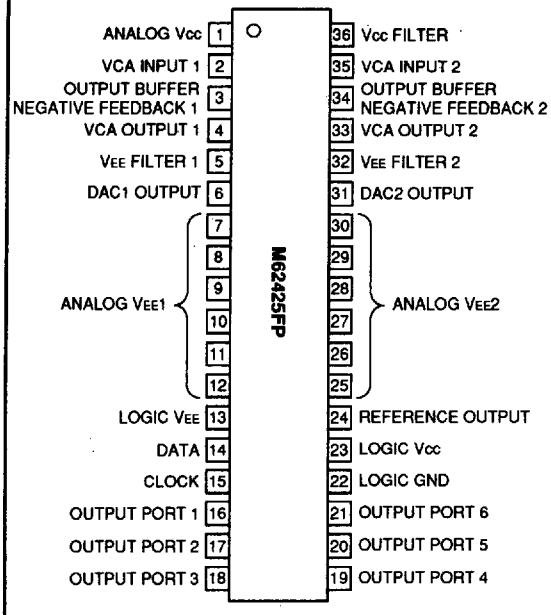
Supply voltage range..... Vcc=±4 to ±7.5V(Single power supply:8 to 15V)
Rated supply voltage..... Vcc=±7V (Single power supply:14V)

## SYSTEM CONFIGURATION



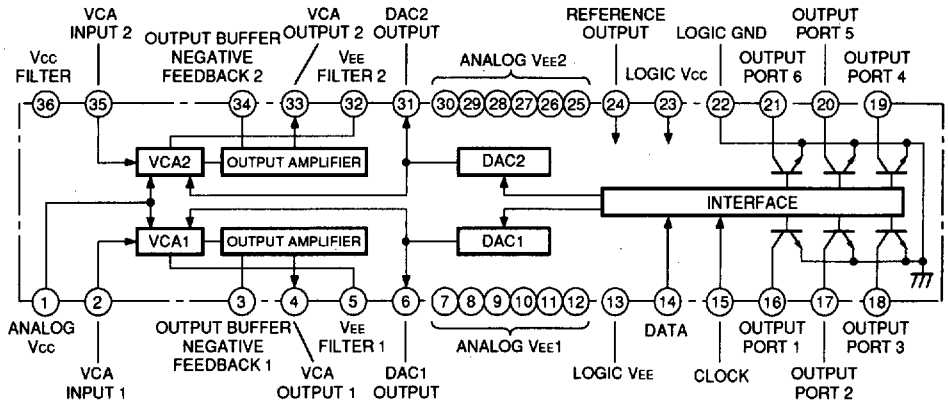
## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### PIN CONFIGURATION (TOP VIEW)




Outline 36P2R-A

### IC INTERNAL BLOCK DIAGRAM



## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### PIN DESCRIPTION

| Pin No. | Symbol | Function description |
|---|---|---|
| ① | Analog Vcc | 2 power supplies:Applies 4 to 7.5V (rating:7V), Single power supply:Applies 8 to 15V (rating:14V) |
| ② (㉟) | VCA input 1 (2) | Signal input pin at CH1 (2) side |
| ③ (㉞) | Output buffer negative feedback 1(2) | Output buffer inverted input pin |
| ④ (㉝) | VCA output 1 (2) | Signal output pin at CH1 (2) side |
| ⑤ (㉜) | VEE filter 1 (2) | For removal of analog VEE power supply ripple, grounds with single power supply |
| ⑥ (㉛) | DAC1 (2) output | Voltage output pin for VCA1 (2) control |
| ⑦ – ⑫ | Analog VEE1 | 2 power supplies:Applies -4 to -7.5V (rating:-7V), single power supply:grounds |
| ⑬ | Logic VEE | 2 power supplies:Applies -4 to -7.5V (rating:-7V), single power supply:grounds |
| ⑭ | DATA | Transfer of serial data from microcomputer to IC (LSB first) |
| ⑮ | CLOCK | Clock for transfer of serial data from microcomputer to IC |
| ⑯ | Output port 1 | Open collector output pin ① |
| ⑰ | Output port 2 | Open collector output pin ② |
| ⑱ | Output port 3 | Open collector output pin ③ |
| ⑲ | Output port 4 | Open collector output pin ④ |
| ⑳ | Output port 5 | Open collector output pin ⑤ |
| ㉑ | Output port 6 | Open collector output pin ⑥ |
| ㉒ | Logic GND | Grounds |
| ㉓ | Logic Vcc | 2 power supplies: Applies -4 to -7.5V (rating:7V), single power supply: Supplies 8 to 15V (rating:14V) |
| ㉔ | Reference output | Reference voltage output pin (2 power supplies:-2V typ, single power supply:5V typ) |
| ㉕ – ㉚ | Analog VEE2 | 2 power supplies:Applies -4 to -7.5V (rating:-7V), single power supply:grounds |
| ㊱ | Vcc filter | For removal of Vcc power supply ripple |

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### ABSOLUTE MAXIMUM RATINGS (Ta=25°C, unless otherwise noted)

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Maximum supply voltage | | +8 | V |
| $V_{EE}$ | | | -8 | V |
| $P_d$ | Power dissipation | | 1.2 | W |
| $K_\theta$ | Thermal derating | Ta≥25°C | 12 | mW/°C |
| $T_{opr}$ | Operating temperature | | -20 to +75 | °C |
| $T_{stg}$ | Storage temperature | | -40 to +125 | °C |

### ELECTRICAL CHARACTERISTICS

($V_{CC}$=±7V, f=1kHz, Rg=10kΩ $R_L$=1kΩ, Vin=1Vrms, output buffer set to 6 dB, unless otherwise noted)

| Block name | Symbol | Parameter | | Test conditions | DAC data 1/2 | PORT data 3 | | | | | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | D0 | D1 | D2 | D3 | D4 | D5 | Min. | Typ. | Max. | |
| Power supply | $I_{CC}$ | Circuit current | | No signal | FFH | 0 | 0 | 0 | 0 | 0 | 0 | – | +33 | +45 | mA |
| | $I_{EE}$ | Circuit current | | No signal | FFH | 0 | 0 | 0 | 0 | 0 | 0 | -45 | -33 | – | mA |
| Electronic volume | $ATT_{min}$ | Min. attenuation | | | FFH | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 6 | 8 | dB |
| | $ATT_{total}$ | Max. attenuation (total) | | Vin=1.25Vrms, JIS-A $ATT_{total}=ATT_{max}-ATT_{min}$ When a capacitor of 100μF is connected between $V_{EE}$ filter and GND | 00H | 0 | 0 | 0 | 0 | 0 | 0 | – | -84 | -74 | dB |
| | CB | Channel balance | | | FFH | 0 | 0 | 0 | 0 | 0 | 0 | -2 | 0 | +2 | dB |
| | THD | Total harmonic distortion ratio | | 15kHz LPF | FFH | 0 | 0 | 0 | 0 | 0 | 0 | – | 0.01 | 0.1 | % |
| | $R_I$ | Input resistance | | | FFH | 0 | 0 | 0 | 0 | 0 | 0 | 50 | 150 | – | kΩ |
| | $N_{O(min)}$ | Output noise power (min) | | Rg=10kΩ, no signal, JIS-A | FFH | 0 | 0 | 0 | 0 | 0 | 0 | – | 18 | 40 | μVrms |
| | $N_{O(max)}$ | Output noise power (max) | | Rg=10kΩ, no signal, JIS-A | 00H | 0 | 0 | 0 | 0 | 0 | 0 | – | 10 | 20 | μVrms |
| | $V_{Imax}$ | Allowable input voltage | | THD=1% | FFH | 0 | 0 | 0 | 0 | 0 | 0 | 1.25 | 2.0 | – | Vrms |
| | $V_{Omax}$ | Maximum output voltage | | THD=1% | FFH | 0 | 0 | 0 | 0 | 0 | 0 | 2.5 | 4.0 | – | Vrms |
| | CT | Crosstalk | | Rg=0Ω Vin=1.25Vrms, JIS-A | FFH | 0 | 0 | 0 | 0 | 0 | 0 | – | -94 | -80 | dB |
| PORT 1 to 6 | $I_{OH}$ | Output port High level current | | $V_{OH}$=7V | FFH | 0 | 0 | 0 | 0 | 0 | 0 | -1 | 0 | 10 | μA |
| | $V_{OL}$ | Output port Low level voltage | | $I_{OL}$=5mA | FFH | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0.15 | 0.5 | V |
| Logic input | ICH | Clock input current | | VCH=5V | | | | | | | | -1.3 | -1.0 | 0.3 | μA |
| | ICL | | | VCL=0V | | | | | | | | -3.0 | -1.3 | 0.3 | μA |
| | IDH | Data input current | | VDH=5V | | | | | | | | -1.3 | -1.0 | 0.3 | μA |
| | IDL | | | VDL=0V | | | | | | | | -3.0 | -1.3 | 0.3 | μA |
| | VCH | CLOCK | "H" level voltage | Recommended condition | | | | | | | | 3.5 | – | 5.5 | V |
| | VCL | | "L" level voltage | Recommended condition | | | | | | | | 0.0 | – | 1.5 | V |
| | VDH | DATA | "H" level voltage | Recommended condition | | | | | | | | 3.5 | – | 5.5 | V |
| | VDL | | "L" level voltage | Recommended condition | | | | | | | | 0.0 | – | 1.5 | V |

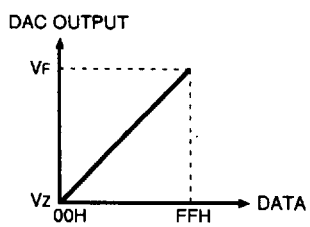
Note 1: DAC data 1/2 is given in hexadecimal.
2: The maximum attenuation (total) is influenced by residual signal components in the $V_{EE}$ filter when two power supplies are used. Addition of a capacitor between the $V_{EE}$ filter and the GND can reduce the influence.
3: Allowable input voltage (reference value)
With Gv=0dB, standard:4.0Vrms, minimum:2.0Vrms (THD=1%)

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### DIGITAL CONTROL SPECIFICATIONS

DATA FORMAT

| | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DATA 1 (MSB) | MODE SELECT "1" | MODE SELECT "1" | | | | DAC1 DATA (8bit) | | | | | (LSB) |
| DATA 2 (MSB) | MODE SELECT "1" | MODE SELECT "0" | | | | DAC2 DATA (8bit) | | | | | (LSB) |
| DATA 3 (MSB) | MODE SELECT "0" | MODE SELECT "1" | "0" | "0" | PORT OUT6 | PORT OUT5 | PORT OUT4 | PORT OUT3 | PORT OUT2 | PORT OUT1 | (LSB) |

| | Signal name | Function |
|---|---|---|
| D0 | DAC | DAC data (8 bits)<br>For output of VCA control voltage<br>00H to FFH<br>  |
| D1 | | |
| D2 | | |
| D3 | | |
| D4 | | |
| D5 | | |
| D6 | | |
| D7 | | |
| D8 | Mode select | "1" "1" } Selects data 1<br>"0" "1" } Selects data 2 |
| D9 | | |

| | Signal name | Function |
|---|---|---|
| D0 | OUT1 | For control of output port 1<br>High impedance with "0"<br>Current pull-in with "1" |
| D1 | OUT2 | For control of output port 2<br>High impedance with "0"<br>Current pull-in with "1" |
| D2 | OUT3 | For control of output port 3<br>High impedance with "0"<br>Current pull-in with "1" |
| D3 | OUT4 | For control of output port 4<br>High impedance with "0"<br>Current pull-in with "1" |
| D4 | OUT5 | For control of output port 5<br>High impedance with "0"<br>Current pull-in current with "1" |
| D5 | OUT6 | For control of output port 6<br>High impedance with "0"<br>Current pull-in with "1" |
| D6 | Not defined | D6 is set to "0"<br>D7 is set to "0" |
| D7 | | |
| D8 | Mode select | "1" "0" } Selects data 3 |
| D9 | | |

### DATA SETTING LIST

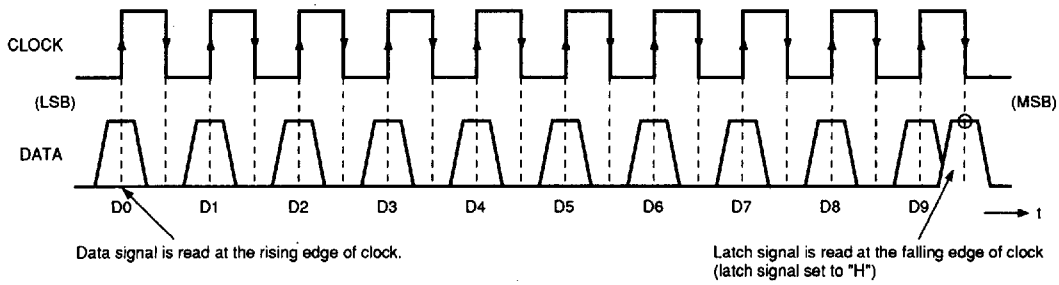
| D/A converter for VCA | Data | 00H | 01H | ---------- | FEH | FEH |
|---|---|---|---|---|---|---|
| | Setting | Vz | $\frac{255Vz+VF}{256}$ | ---------- | $\frac{2Vz+254VF}{256}$ | $\frac{Vz+255VF}{256}$ |

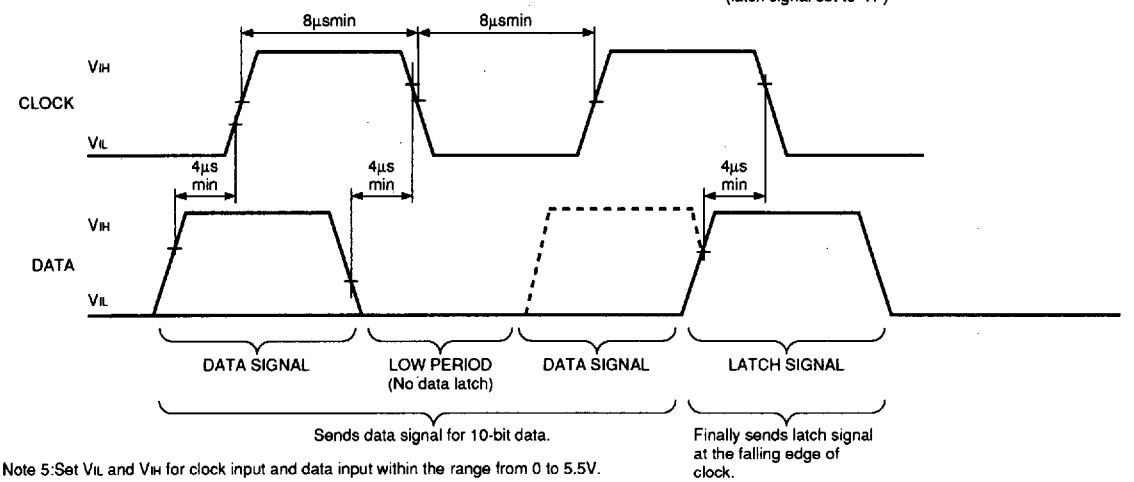
Note 4: Vz and VF put their references on the VEE voltage and reference output (pin (24)), respectively.

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### DATATIMING (RECOMMENDED CONDITIONS)

* Data communication is provided with SB first.




Note 5: Set $V_{IL}$ and $V_{IH}$ for clock input and data input within the range from 0 to 5.5V.

### VCA ATTENUATION (REFERENCE EXAMPLE)

| Gv=+6dB | |
|---|---|
| Control data (D/A converter) | VCA attenuation (dB) |
| 14H | Maximum attenuation |
| 1FH | -68 |
| 2FH | -54 |
| 3FH | -40 |
| 4FH | -29 |
| 5FH | -20 |
| 6FH | -13 |
| 7FH | -6.9 |
| 8FH | -2.5 |
| 9FH | +0.5 |
| AFH | +2.6 |
| BFH | +4.0 |
| CFH | +5.0 |
| DFH | +5.5 |
| EFH | +6.0 |
| FFH | +6.0 |

Note 6: Errors in DAC increase at the following data switching points: 0FH to 10H, 1FH to 20H, 2FH to 30H, 3FH to 40H, 4FH to 50H, 5FH to 60H, 6FH to 70H, 7FH to 80H, 8FH to 90H, 9FH to A0H, AFH to B0H, BFH to C0H, CFH to D0H, DFH to E0H, and EFH to F0H. Care must be taken for the consecutive usage over the above switching points.

### RECOMMENDED VOLUME DATA (2dB/step)

Example <relative value with Gv=6dB>

| Attenuation set value (dB) | Control data | Attenuation set value (dB) | Control data |
|---|---|---|---|
| 0 | FFH | -42 | 43H |
| -2 | BFH | -44 | 41H |
| -4 | A7H | -46 | 3FH |
| -6 | 9BH | -48 | 3CH |
| -8 | 8FH | -50 | 3AH |
| -10 | 87H | -52 | 38H |
| -12 | 7FH | -54 | 34H |
| -14 | 7BH | -56 | 32H |
| -16 | 77H | -58 | 31H |
| -18 | 72H | -60 | 2FH |
| -20 | 6EH | -62 | 2DH |
| -22 | 67H | -64 | 2BH |
| -24 | 62H | -66 | 29H |
| -26 | 5EH | -68 | 28H |
| -28 | 5AH | -70 | 26H |
| -30 | 57H | -72 | 24H |
| -32 | 53H | -74 | 22H |
| -34 | 50H | -76 | 20H |
| -36 | 4CH | -78 | 1EH |
| -38 | 49H | -80 | 1CH |
| -40 | 45H | -82 | 18H |

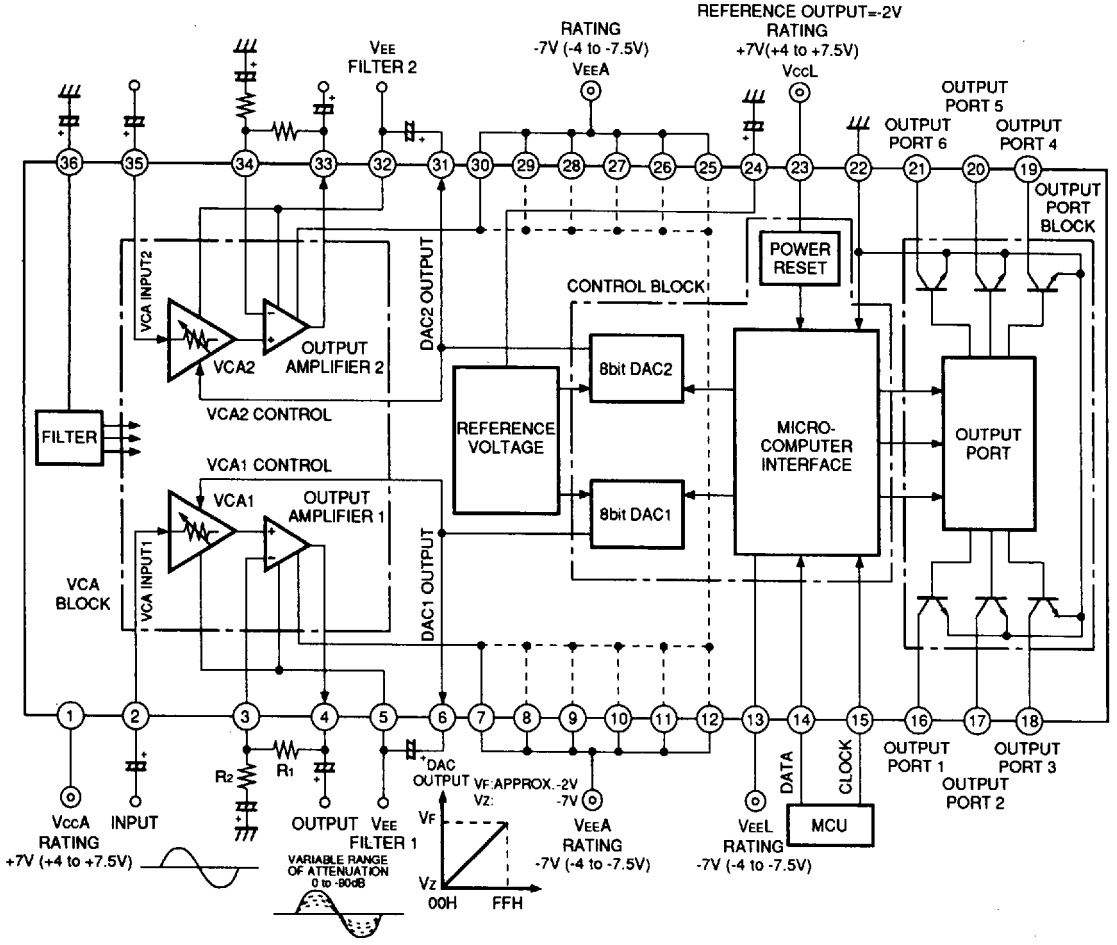
*The above set values are taken when a capacitance of 100µF is connected to the $V_{EE}$ filter.



*Since attenuation set values are target values, actual values may be a little smaller or larger than them.

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### DESCRIPTIVE DIAGRAM OF BLOCK OPERATION (With two power supplies used)




Note 7. Pins ⑦ to ⑫ and ㉕ to ㉚ are electrically connected in the inside of the package. (For radiation)

### BASIC OPERATION

(1) VCA block: Handles main analog signal and consists of the VCA circuit and an an output amplifier.

① Input signal is attenuated through the VCA circuit and is then output.

② The VCA circuit is controlled with the DC voltage output from the 8-bit D/A converter.

③ Total gain can be changed with the output amplifier.
Use the following formula to set the gain.

$$Gv\ (total) = 20\log \frac{R_1+R_2}{R_2}\ (dB)$$

(2) Control block: Controls functions with blocks that process data sent from the microcomputer.

① When power is turned on, reset signal is output from the reset circuit to forcibly place the internal logic in the following status: sets the DAC control data to 00H (maximum attenuation status) and puts the output port in high impedance status.
The reset is not released until the supply voltage is ±2.5V (single power supply: 5V) or more. Therefore, send data after ② the supply voltage is put in the recommended operating range.

For the control from the microcomputer, 10-bit serial data is used.

To control DAC1, select the data 1 (mode select "1", "1") side.

To control DAC2, select the data 2 (mode select "1", "0") side.

To set port output, select the mode data 3 (mode select "0", "1") side.



For data setting, see the digital control specification in page 5 of this data.

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

(3) Output port block:Six output ports are built in.

① Output ports adopt current pull-in type and open collector type (NPNTr) output type.

② After power is turned on, high impedance status is kept until the first data is accepted.

③ Six output ports can be set individually with control data.

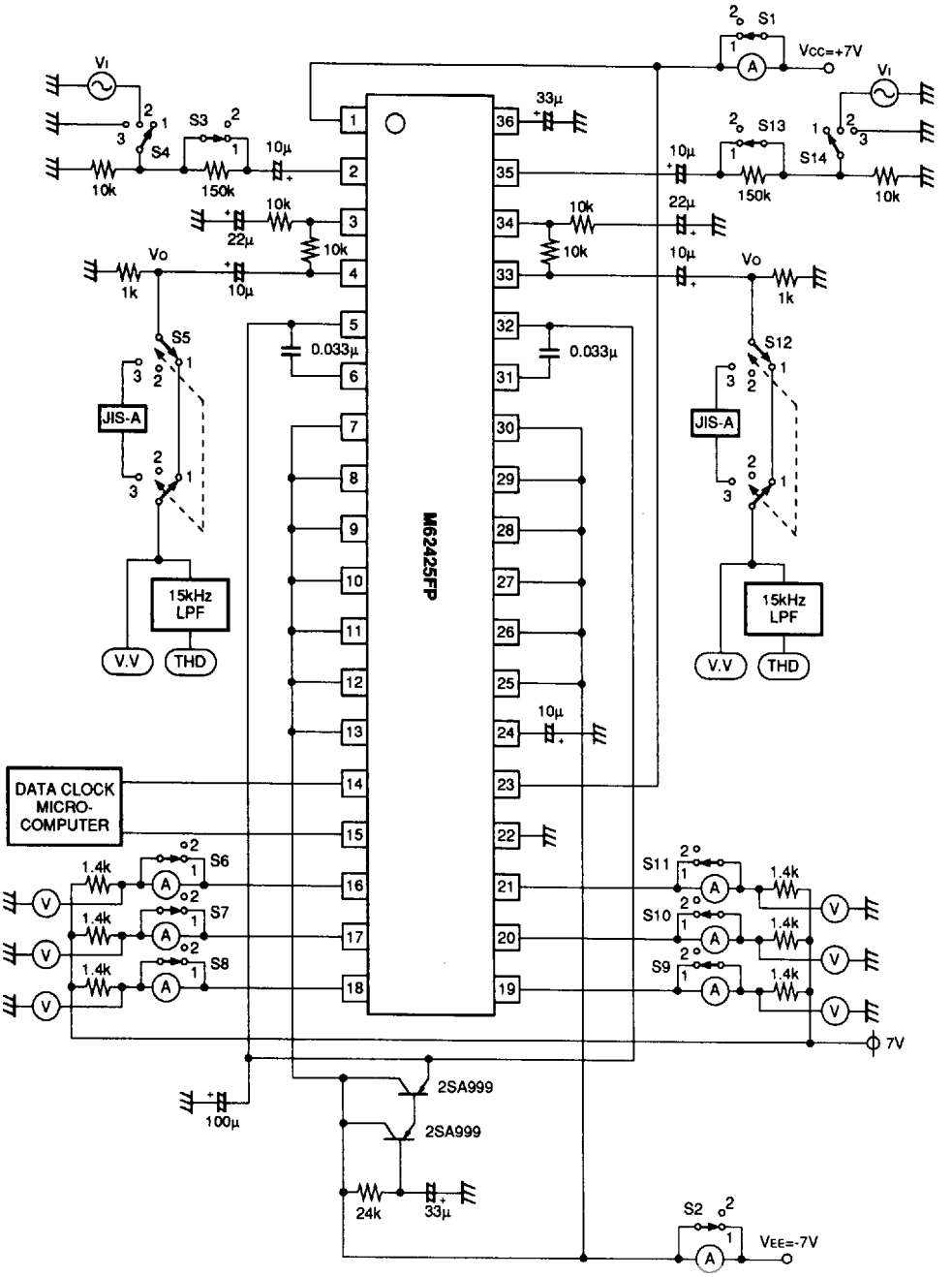
### SWITCHING CONDITIONS AND MEASUREMENT

| Symbol | Parameter | | Switch | | | | | | | | | | | | | Test method |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | |
| $I_{CC}$ | Circuit current | | 2 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | Tests current flowing to pins ① and ㉓ when no signal is given |
| $I_{EE}$ | Circuit current | | 1 | 2 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | Measures current flowing to pins ⑧ to ⑫, ㉕ to ㉚, and ⑬ when no signal is given |
| $ATT_{min}$ | Minimum attenuation | | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | Finds the attenuation with ATT (dB)=20log (Vo/Vi) |
| $ATT_{total}$ | Maximum attenuation (total) | | 1 | 1 | 1 | 2 | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | 1 | 2 | $ATT_{total}=ATT_{max}$ (00H) $-ATT_{min}$ (FFH) $ATT_{max}$ means JIS-Ain |
| CB | Channel balance | | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | CB (dB)=ATTch1-ATTch2 |
| THD | Total harmonic distortion | | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 15kHz LPF in |
| $R_I$ | Input resistance | | 1 | 1 | 1→2 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1→2 | 2 | Vo1 with S3, S13 to 1<br>Vo2 with S3, S13 to 2<br>$R_I$ (kΩ)=150/(Vo1/Vo2-1) |
| $N_{O\ (min)}$ | Output noise power (min) | | 1 | 1 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | 1 | 1 | No signal, JIS-A |
| $N_{O\ (max)}$ | Output noise power (max) | | 1 | 1 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 3 | 1 | 1 | No signal, JIS-A |
| $V_{Imax}$ | Allowable input voltage | | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | Input signal voltage when the output distortion is 1% |
| $V_{Omax}$ | Maximum output voltage | | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | Output signal voltage when the output distortion is 1% |
| CT | Crosstalk | | 1 | 1 | 1 | 3 | 3 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 2 | CT=20log Vo2/Vo1 (dB) JIS-A in when the ch output is Vo1 with Vi=1.25Vrms entered and the output at no-input side is Vo2 |
| | | | | | | 2 | 2 | | | | | | | 3 | | 3 | |
| $I_{OH}$ | Output port High level current | | 1 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 1 | 1 | Tests the current supplied to pins ⑯ to ㉑ when the output port is put in high impedance |
| $V_{OL}$ | Output port Low level current | | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | Tests the voltage at pins ⑯ to ㉑ when current is pulled in the output port. |
| ICH | Clock input current | | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | Tests the current flowing to pin ⑮ |
| ICL | | | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |
| IDH | Data input current | | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | Tests the current flowing to pin ⑭ |
| IDL | | | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |
| VCH | CLOCK | "H" level voltage | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |
| VCL | | "L" level voltage | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |
| VDH | DATA | "H" level voltage | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |
| VDL | | "L" level voltage | 1 | 1 | 1 | 1 | 2 | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 1 | 1 | |

Note 8. When switching conditions in an item are divided into two stages (upper and lower), tests are taken with the two conditions:all switching conditions at the upper stage are applied and all switching conditions at the lower stage are applied.

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### TEST CIRCUIT



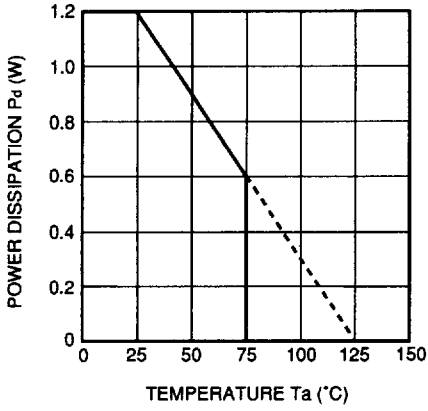



Units Resistance :Ω
Capacitance :F

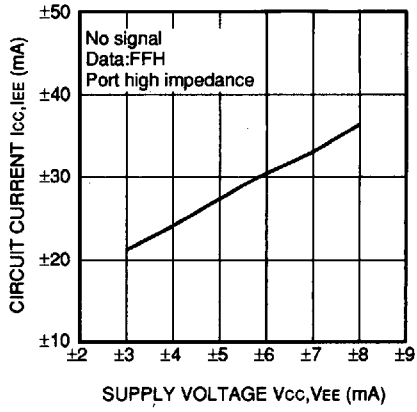
## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### TYPICAL CHARACTERISTICS

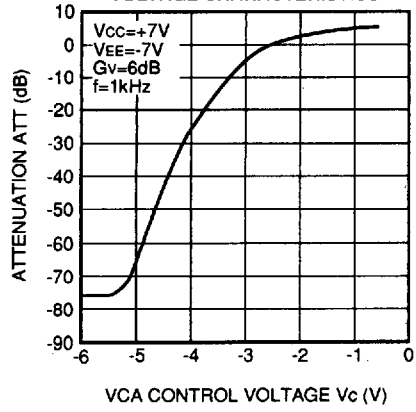
THERMAL DERATING (MAXIMUM RATING)



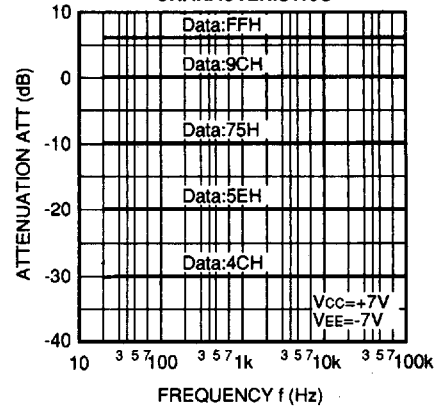

CIRCUIT CURRENT VS. SUPPLY VOLTAGE CHARACTERISTICS



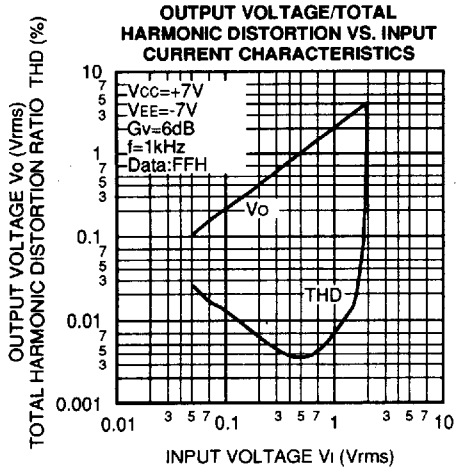

ATTENUATION VS. VCA CONTROL VOLTAGE CHARACTERISTICS



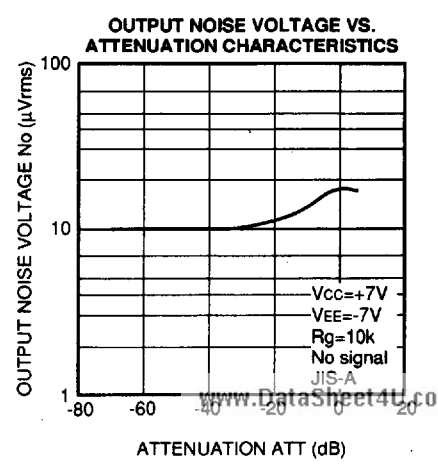

ATTENUATION VS. FREQUENCY CHARACTERISTICS




OUTPUT VOLTAGE/TOTAL HARMONIC DISTORTION VS. INPUT CURRENT CHARACTERISTICS



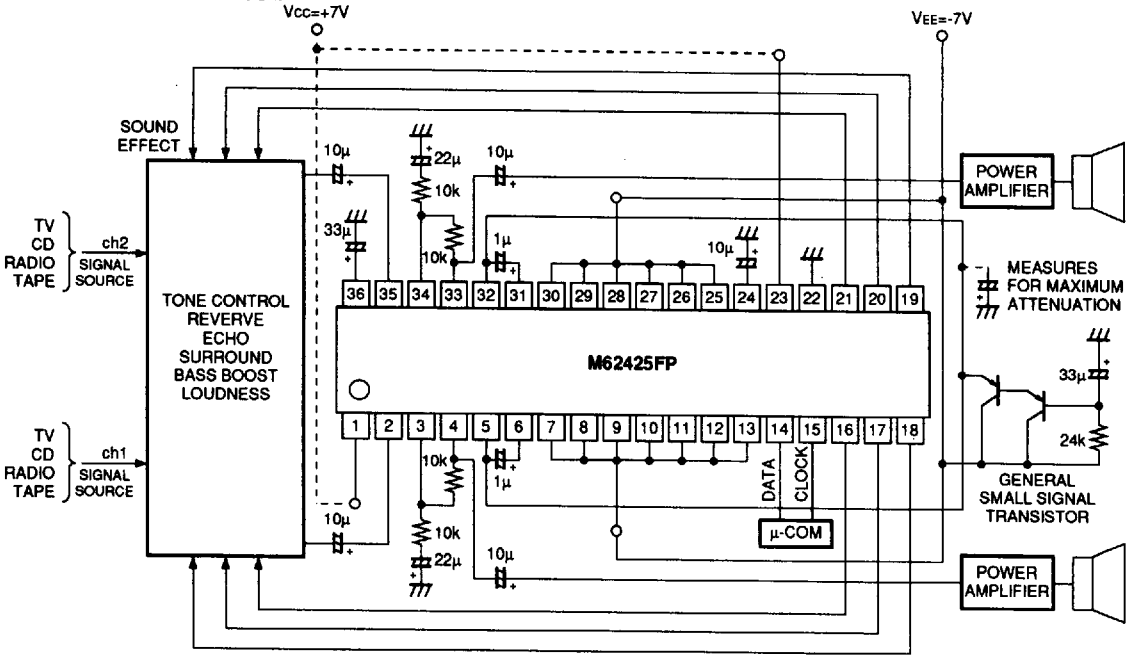

OUTPUT NOISE VOLTAGE VS. ATTENUATION CHARACTERISTICS



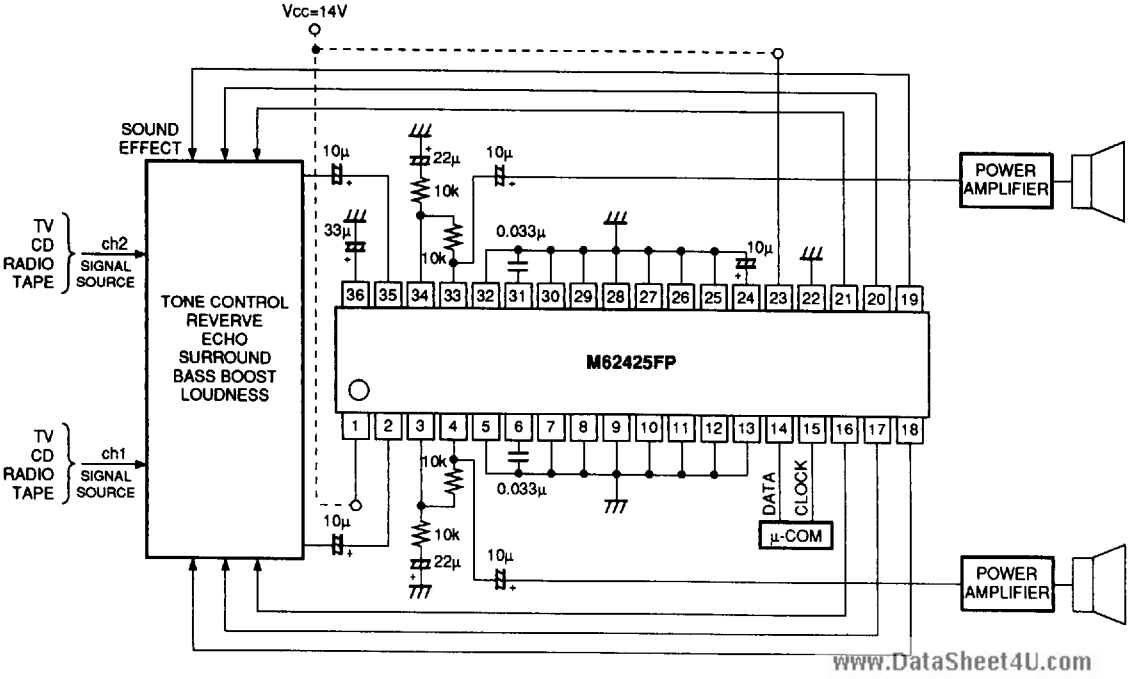
## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### APPLICATION EXAMPLES

#### 2 POWER SUPPLIES IN USE




#### SINGLE POWER SUPPLY IN USE



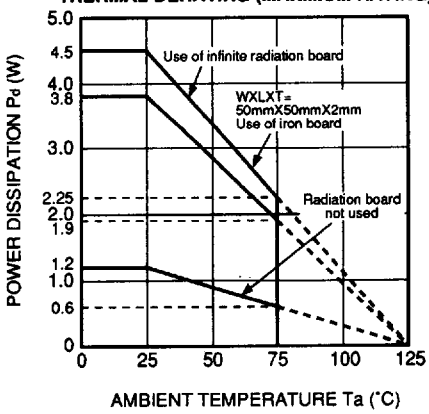



Units Resistance :Ω
Capacitance :F

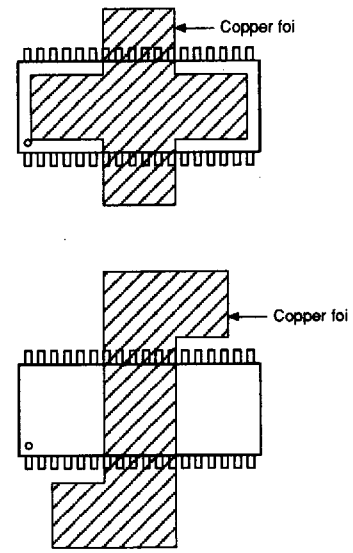
## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

### PRECAUTIONS FOR USE

THERMAL DERATING (MAXIMUM RATING)




Layout example of printed circuit board




(1) Since the M62425FP contains two channels of VCA circuits and two channels of DAC circuits, a large circuit current flows (standard current=±30mA). Since larger power consumption is required, a layout of the board must take into account the thermal derating characteristics.

- To increase heat radiation (heat diffusion) effect, spread copper foil as widely as possible around the foot of the analog $V_{EEpn}$. (See the example.)
- If a measure for heat radiation effect cannot be taken, calculate the maximum power by $\pm V_{CC} \times I_{CCmax}$ and then use the IC within the above rated $P_d$,taking into account the operating temperature, Vcc applied voltage, etc.

(2) This IC has an analog block and a digital block. When making a layout of the board, carefully take measures for prevention against entry of digital noise.

(3) Internal reset circuit operates in a status of low supply voltage. Set the operating status when the supply voltage is within the recommended operating range.

(4) Always apply almost equal voltage to analog Vcc pin ① and logic Vcc pin ㉘.

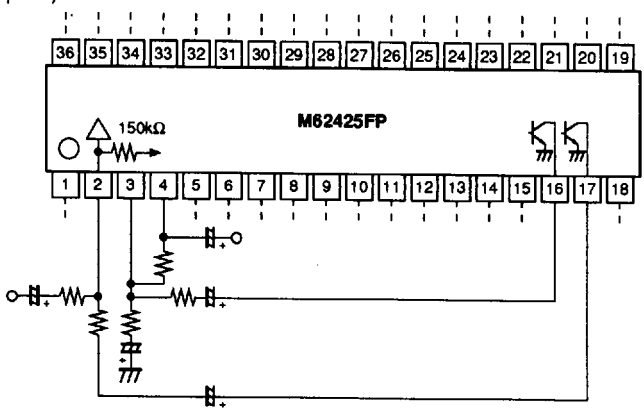
(5) Use negative resistance of 1kΩ or more.

## 2CH ELECTRONIC VOLUME, BALANCE AND 6 OUTPUT PORTS WITH MICROCOMPUTER INTERFACE

(6) The peak inverse voltage of the output port is approximately 4V. Special care must be taken for the use of two power supplies. In example 1 given below, the signal amplitude to be handled may be smaller than that in example 2. Notice that parasitic diode operates at the negative side from VEE. (It is recommended to apply a voltage between VEE and Vcc.)

**[Example of switching frequency characteristics of output amplifier with output port]**

(Example 1)




(Example 2)