

M64898GP

PLL Frequency Synthesizer with DC/DC Converter for PC

REJ03F0168-0201

Rev.2.01

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Description

The M64898GP is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR /PC. It contains the prescaler with operating up to 1.3 GHz, 4 band drivers and DC/DC converter for Tuning voltage.

Features

- Built-in DC/DC converter for Tuning voltage
- 4 integrated PNP band drivers ($I_O = 30 \text{ mA}$, $V_{\text{sat}} = 0.2 \text{ V Typ @ } V_{\text{CC1}} \text{ to } 10 \text{ V}$)
- Built-in prescaler with input amplifier (max = 1.3 GHz)
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X'tal 4 MHz is used to realize 3 type of tuning steps (Divider ratio 1/512, 1/640, 1/1024)
- Software compatible with M64892/M64893
- Automatic switching of tuning step according to the number of data bits (62.5 kHz at 18 bits, 32.25 kHz at 19 bits)
- Built-in Power on reset system
- Small package (SSOP)

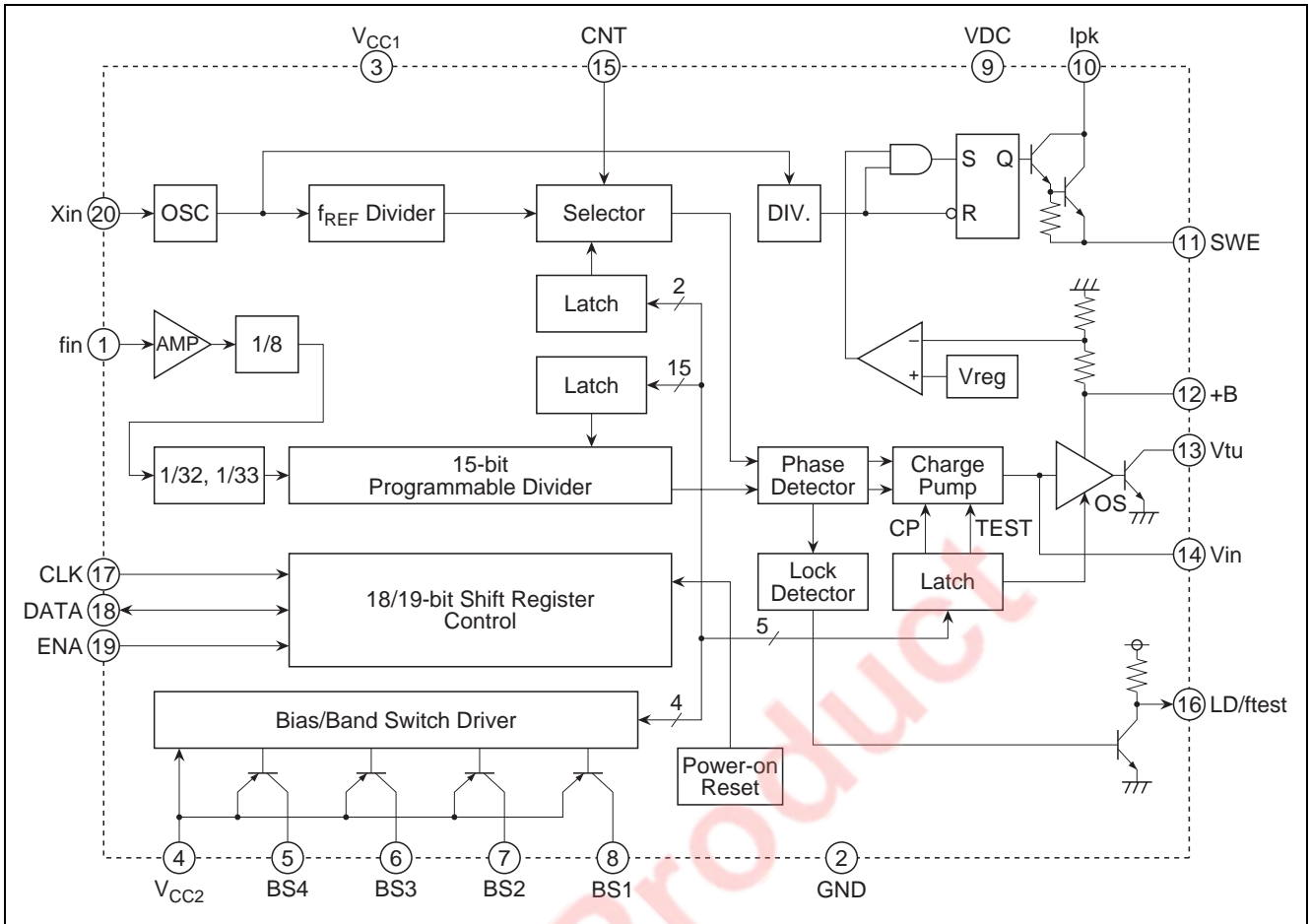
Application

PC, TV, VCR tuners

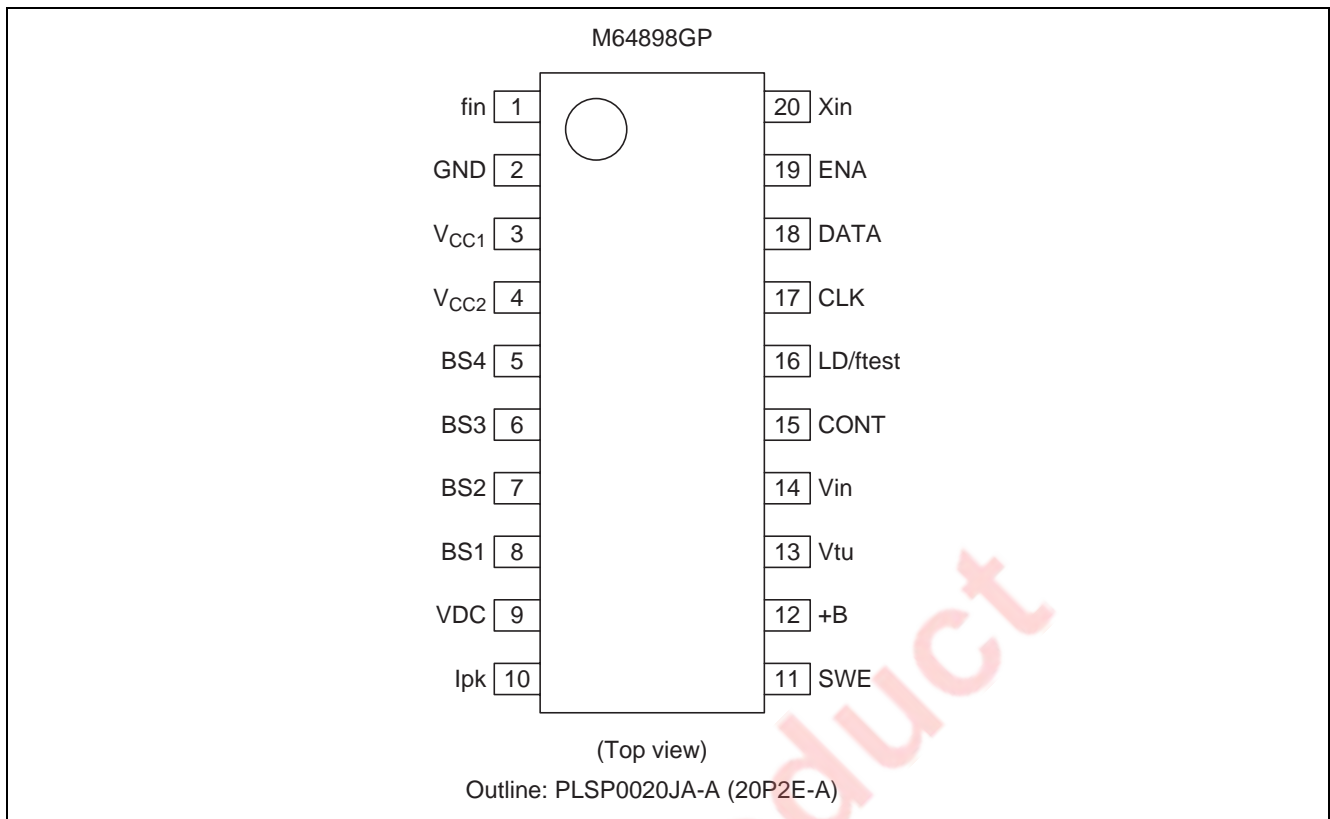
Recommended Operating Condition

- Supply voltage range
 - $V_{\text{CC1}} = 4.5 \text{ to } 5.5 \text{ V}$
 - $V_{\text{CC2}} = V_{\text{CC1}} \text{ to } 10 \text{ V}$
- Rated supply voltage
 - $V_{\text{CC1}} = 5 \text{ V}$
 - $V_{\text{CC2}} = V_{\text{CC1}}$

Block Diagram



Pin Arrangement



EOL Product

Pin Description

Pin No.	Symbol	Pin Name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0 V.
3	V _{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0 V ± 0.5 V
4	V _{CC2}	Power supply voltage 2	Power supply for band switching, V _{CC1} to 10 V
5	BS4	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
6	BS3		
7	BS2		
8	BS1		
9	VDC	DC/DC power supply voltage	DC/DC power supply voltage terminal. 5.0 V ± 0.5V
10	l _{pk}	Peak current detect	When potential difference with VDC terminal becomes more than 0.33 V by current limiting detector of DC/DC converter, the listing rises with off.
11	SWE	Switching output	DC/DC converter oscillator output.
12	+B	Power supply voltage	Power supply voltage for tuning voltage.
13	V _{tu}	Tuning output	This supplies the tuning voltage.
14	V _{in}	Filter input (charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f 1/N) is ahead compared to the reference frequency (f _{REF}), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
15	LD/ftest	Lock detect/Test port	Lock detector output. When loop of phase locked loop locked it, it rise with "H" level in "L" level or unlock. In control byte data input, the programmable freq. divider output and reference freq. output is selected by the test mode.
16	CONT	f _{REF} switch	Set up reference frequency divider ratio. In "L" level, set it up in 1/640 (19 bit) in setting "opening" in 1/1024 (19 bit) or 1/512 (18 bit).
17	CLOCK	Clock input	Data is read into the shift register when the clock signal falls.
18	DATA	Data input	Input for band SW and programmable freq. divider set up.
19	ENABLE	Enable input	This normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
20	Xin	This is connected to the crystal oscillator.	4.0 MHz crystal oscillator is connected.

Absolute Maximum Ratings

(Ta = -20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage 1	V _{CC1}	6.0	V	Pin 3
Supply voltage 2	V _{CC2}	10.8	V	Pin 4
Input voltage	V _I	6.0	V	Not to exceed V _{CC1}
Output voltage	V _O	6.0	V	f _{REF} output
Voltage applied when the band output is OFF	V _{B_{SOFF}}	10.8	V	
Band output current	I _{B_{SON}}	40.0	mA	per 1 band output circuit
ON the time when the band output is ON	t _{B_{SON}}	10	s	40 mA per 1 band output circuit 3 circuits are pn at same time.
Power dissipation	P _d	255	mW	Ta = 75°C
Operating temperature	T _{opr}	-20 to +75	°C	
Storage temperature	T _{stg}	-40 to +125	°C	

Recommended Operating Conditions

(Ta = -20°C to +75°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage 1	V _{CC1}	4.5 to 5.5	V	Pin 3
Supply voltage 2	V _{CC2}	V _{CC1} to 10.0	V	Pin 4
Operating frequency (1)	f _{opr1}	4.0	V	Crystal oscillation circuit
Operating frequency (2)	f _{opr2}	80 to 1300	MHz	
Band output current 5 to 8	I _{BDL}	0 to 30	mA	Normally 1 circuit is on. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.

Electrical Characteristics

(Ta = -20°C to +75°C, unless otherwise noted, V_{CC1} = 5.0 V, V_{CC2} = 9.0 V)

Item	Symbol	Test Pin	Limits			Unit	Test Conditions	
			Min.	Typ.	Max.			
Input terminals	"H" input voltage	V _{IH}	17 to 19	3.0	—	V _{CC1} + 0.3	V	
	"L" input voltage	V _{IL1}	15	—	—	0.4	V	
	"L" input voltage	V _{IL2}	17 to 19	—	—	1.5	V	
	"H" input current	I _{IH}	17 to 19	—	—	10	μA	V _{CC1} = 5.5 V, V _i = 4.0 V
	"L" input current	I _{IL1}	15	—	-50	-80	μA	V _{CC1} = 5.5 V, V _i = 0 V
	"L" input current	I _{IL2}	17, 19	—	-6	-10	μA	V _{CC1} = 5.5 V, V _i = 0.5 V
	"L" input current	I _{IL3}	18	—	-18	-30	μA	V _{CC1} = 5.5 V, V _i = 0.5 V
Lock output	"H" output voltage	V _{OH}	16	5.0	—	—	V	V _{CC1} = 5.5 V
	"L" output voltage	V _{OL}	16	—	0.3	0.5	V	V _{CC1} = 5.5 V
Band SW	Output voltage	V _{BS}	5 to 8	11.6	11.8	—	V	V _{CC2} = 9 V, I _o = -30 mA
	Leak current	I _{OLK1}	5 to 8	—	—	-10	μA	V _{CC2} = 9 V, Band SW is OFF V _o = 0 V
Tuning output	Output voltage "H"	V _{toH}	13	30.5	—	—	V	+B = 31 V
	Output voltage "L"	V _{toL}	13	—	0.2	0.4	V	+B = 31 V
Charge pump	"H" output current	I _{cpo}	14	—	270	370	μA	V _{CC1} = 5.0 V, V _o = 2.5 V
	Leak current	I _{cpLK}	14	—	—	50	nA	V _{CC1} = 5.0 V, V _o = 2.5 V
Supply current 1		I _{CC1}	3	—	20	30	mA	V _{CC1} = 5.5 V
Supply current 2	4 circuits OFF	I _{CC2A}	4	—	—	0.3	mA	V _{CC2} = 9 V
	1 circuit ON, Output open	I _{CC2B}	4	—	4.0	6.0	mA	V _{CC2} = 9 V
	Output current 30 mA	I _{CC2C}	4	—	34.0	36.0	mA	V _{CC2} = 9 V, I _o = -30 mA
DC/DC Converter								
Supply current (action)		I _{CCdc}	9	—	1.3	3.0	mA	V _{CC1} = 5.5 V
Output voltage		V _{do}	12	28	31	35	V	V _{CC1} = 5.5 V
OSC frequency		f _{OSC}	11	—	571	—	kHz	V _{CC1} = 5.5 V
Current limit detect voltage		V _{ipk}	10	—	330	—	mV	V _{CC1} = 5.5 V

Note: The typical values are at V_{CC1} = 5.0 V, V_{CC2} = 9.0 V, Ta = +25°C.

Switching Characteristics

(Ta = -20°C to +75°C, unless otherwise noted, V_{CC1} = 5.0 V, V_{CC2} = 9.0 V)

Item	Symbol	Test Pin	Limits			Unit	Test Conditions	
			Min.	Typ.	Max.			
Prescaler operating frequency	f _{opr}	1	80	—	1300	MHz	V _{CC1} = 4.5 to 5.5 V Vin = Vinmin to Vinmax	
Operating input voltage	V _{in}	1	-24	—	4	dBm	V _{CC1} = 4.5 to 5.5 V	80 to 100 MHz
			-27	—	4			100 to 950 MHz
			-15	—	4			950 to 1300 MHz
Clock pulse width	t _{PWC}	17	1	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Data setup time	t _{SU (D)}	18	2	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Data hold time	t _{H (D)}	18	1	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Enable setup time	t _{SU (E)}	18	3	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Enable hold time	t _{H (E)}	18	3	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Enable data interval time	t _{INT}	19, 18	1	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Rise time	t _R	17, 18, 19	—	—	1	μs	V _{CC1} = 4.5 to 5.5 V	
Fall time	t _F	17, 18, 19	—	—	1	μs	V _{CC1} = 4.5 to 5.5 V	
Next enable prohibit time	t _{BT}	19	5	—	—	μs	V _{CC1} = 4.5 to 5.5 V	
Next clock prohibit time	t _{BCL}	17, 19	5	—	—	μs	V _{CC1} = 4.5 to 5.5 V	

Method of Setting Data

The programmable divider ratio uses 15 bits. Setting up the band switching output uses 4 bits.

The test mode data uses 8 bits. The total bits used are 27 bits. Data is read in when the enable signal is “H” and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal. The programmable counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of the 19th pulse of the clock signal. When the enable signal goes to “L” before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

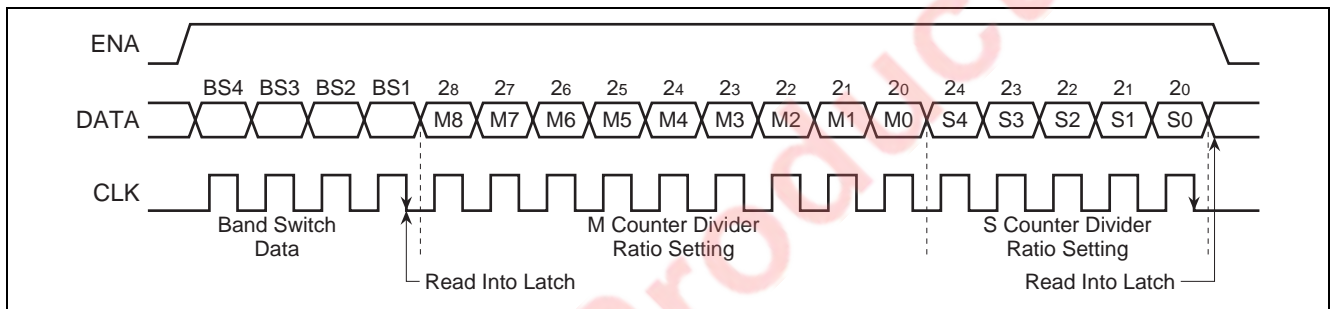
Automatic judgment facility comes being it, and, as for Shift register, CONT terminal rises by 18/19 bits at the time of “L”. At the time of data of 18 bits, M9 bit of Programmable divider is done reset of, and it is established in reference frequency divider ratio is established 1/512.

At the time of 19 bits, reference frequency divider ratio is established in 1/1024.

When reference frequency divider ratio was established in 1/640 by 19 bits at the time if “opening” CONT terminal, and it became “L” before 19 pulses enable signal, only band SW data are renewed, and other data are ignored.

1. Transfer of the 18th bit data (CONT terminal is “L”)

Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the divider of the 1/512 of the reference frequency is used.



2. Transfer of the 19th bit data (CONT terminal is “L” or “open”)

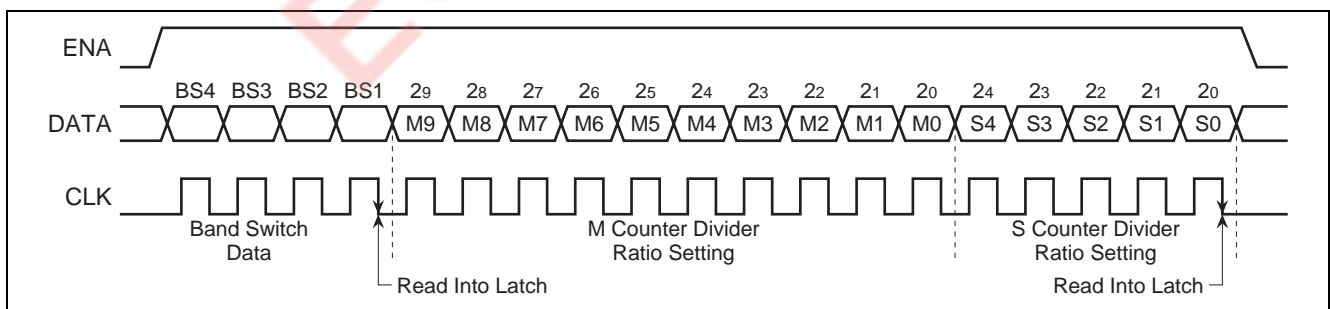
The data is latched at the 19th pulse of the clock signal.

Reference frequency divider ratio is established in 1/1024 in case of “L” CONT terminal at this time.

Reference frequency divider ratio is established in 1/640 in case of “opening” CONT terminal.

Invalid the clock signal after 19th pulse.

Note: When CONT terminal is “L”, to change reference frequency, set up as ENA in “L” after 19th pulse of clock signal by all means.



How to Set the Dividing Ratio of the Programmable Divider

1. Transfer of the 18th bit data (CONT terminal is “L”)

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32 M + S) \quad \begin{array}{l} \text{M: 9 bit main counter divider} \\ \text{S: 5 bit swallow counter divider} \end{array}$$

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \cdot M \cdot 511$$

$$0 \cdot S \cdot 31$$

Therefore, the range of divider N is 8,192 to 131,064.

The tuning frequency f_{VCO} is given in the following equations.

$$\begin{aligned} f_{VCO} &= f_{REF} \cdot N \\ &= 7.8125 \cdot 8 \cdot (32 M + S) \\ &= 62.5 \cdot (32 M + S) \text{ (kHz)} \end{aligned}$$

Therefore, the tuning frequency range is 64 MHz to 1023.9375 MHz.

2. Transfer of the 19th bit data (CONT terminal is “L”)

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32 M + S) \quad \begin{array}{l} \text{M: 10 bit main counter divider} \\ \text{S: 5 bit swallow counter divider} \end{array}$$

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \cdot M \cdot 1023$$

$$0 \cdot S \cdot 31$$

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

$$\begin{aligned} f_{VCO} &= f_{REF} \cdot N \\ &= 3.90625 \cdot 8 \cdot (32 M + S) \\ &= 31.25 \cdot (32 M + S) \text{ (kHz)} \end{aligned}$$

Therefore, the tuning frequency range is 32 MHz to 1023.96875 MHz.

3. Transfer of the 19th data (CONT terminal is “open”)

Total divider N is given by the following formulas in addition to the prescaler used in the previous stage.

$$N = 8 \cdot (32M + S) \quad \begin{array}{l} \text{M: 10 bit main counter divider} \\ \text{S: 5 bit swallow counter divider} \end{array}$$

The M and S counters are binary the possible ranges of divider are as follows.

$$32 \cdot M \cdot 1023$$

$$0 \cdot S \cdot 31$$

Therefore, the range of divider N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

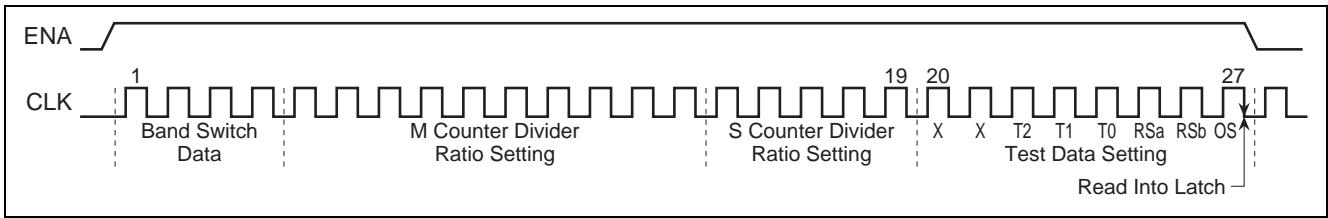
$$\begin{aligned} f_{VCO} &= f_{REF} \cdot N \\ &= 6.25 \cdot 8 \cdot (32 M + S) \\ &= 50.0 \cdot (32 M + S) \text{ (kHz)} \end{aligned}$$

But, the tuning frequency range is 51.2 MHz to 1300 MHz from the maximum prescaler operating frequency.

Test Mode Data Set up Method

The data for the test mode uses 20 to 27 bits. Data is latched when the 27th clock signal falls.

1. When transferring 3-wire 27 bit data



2. Test mode bit set up

- X : Random, 0 or 1 normal "0"
- T0, T1 & T2 : Set up test modes
- RSa, RSb : Set the frequency divider of the reference frequency
- OS : Set up the tuning amplifier

Setting up for the Test Mode

T2	T1	T0	Charge Pump	Pin 12 Output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f_{REF}	Test mode
1	0	1	High impedance	$f1/N$	Test mode

RSa, RSb: Set up for the Reference Frequency Divider Ratio

RSa	RSb	Divider Ratio
1	1	1/512
0	1	1/1024
X	0	1/640

OS: Set up the Tuning Amplifier

OS	Tuning Voltage Output	Mode
0	ON	Normal
1	OFF	Test

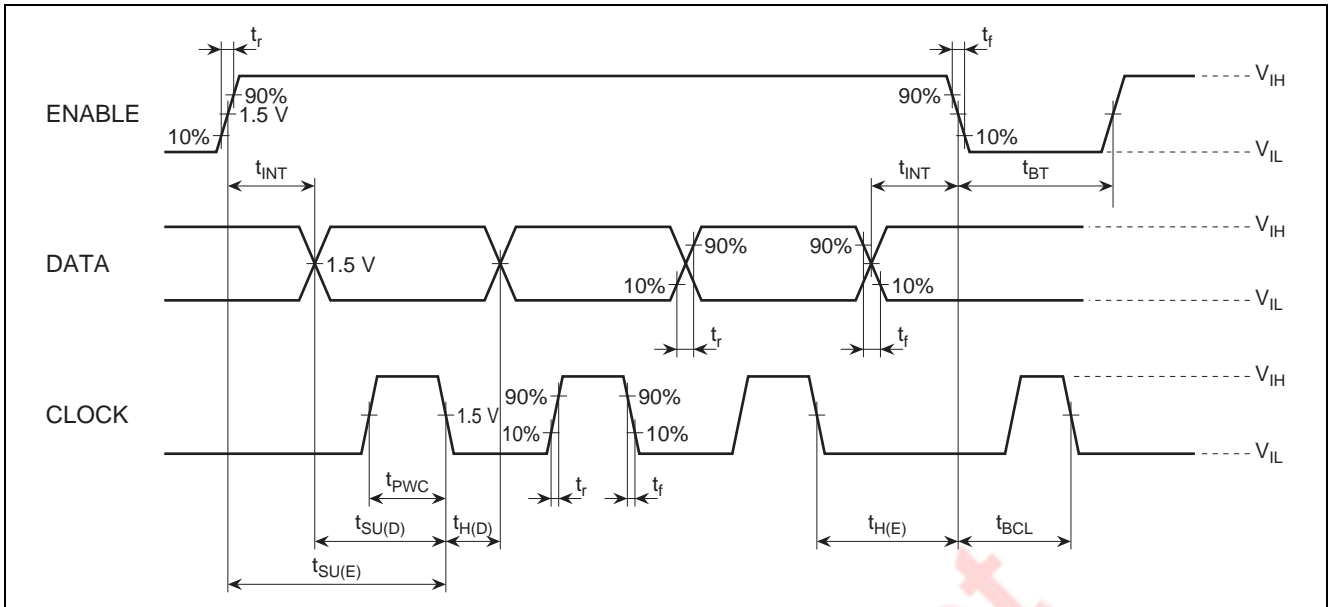
Power on Reset Operation

(Initial state the power is turned ON)

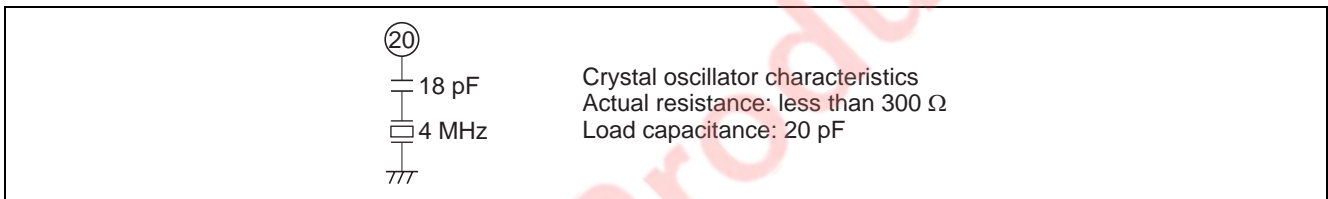
- BS4 to BS1 : OFF
- Charge pump : High impedance
- Tuning amplifier : OFF
- Charge pump current : 270 μ A
- Frequency divider ratio : 1/1024
- Lock detect : H

Charge pump current is replaced by 70 μ A when locks it by automatic change facility.

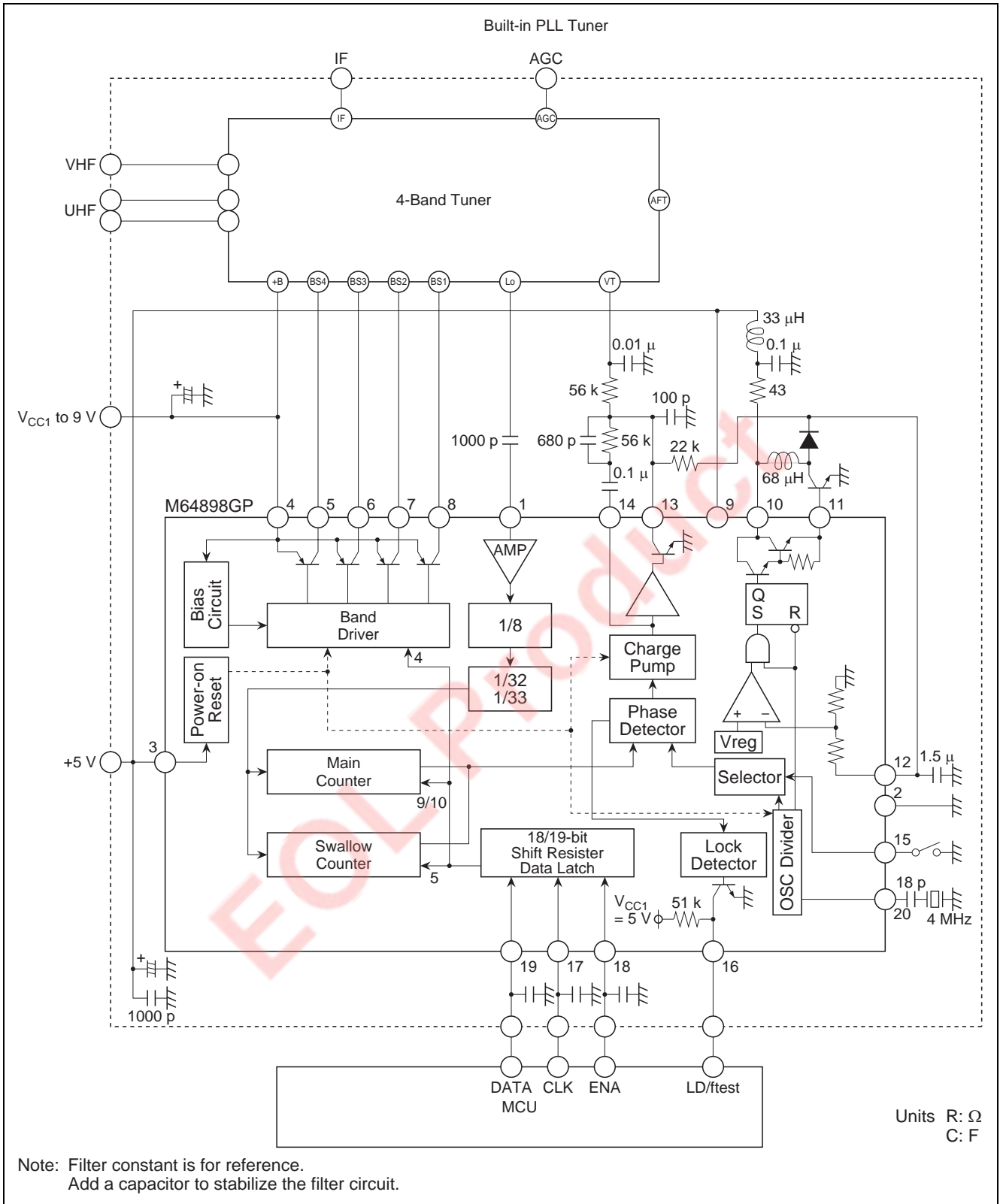
Timing Diagram



Crystal Oscillator Connection Diagram

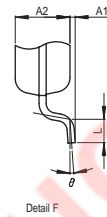
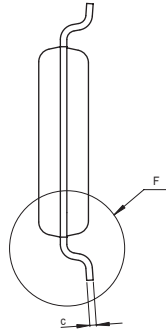
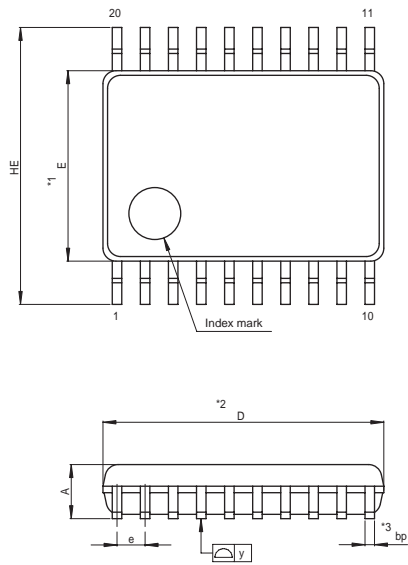


Application Example



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JA-A	20P2E-A	0.08g



NOTE)
 1. DIMENSIONS *1* AND *2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION *3* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A ₂	—	1.15	—
A	—	—	1.45
A ₁	0	0.1	0.2
b _p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H _E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

EOL Product

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