PRELIMINARY
Notice:This is not a final specification.
Some parametric limits are subject to change.

M65530FP

TRIPLE 10-BIT VIDEO D-A CONVERTER

DESCRIPTION

The M65530FP is a CMOS 10-bit digital-to-analog converter for video signal processing. The IC features an adjustment function of analog output amplitude, thereby controlling the amplitude by simply changing an adjustment resistor.

FEATURE

- Triple 10-bit video speed D-A converters
- Maximum conversion rate of 50 MSPS
- Adjustable analog output amplitude.....2.0V(Typ)
- Digital input.....TTL level
- Power down function for analog blocks
- Surface mounting package
  (68-pin quad flat package, 0.65mm line and space,
  14 x 10 mm body)

APPLICATIONS

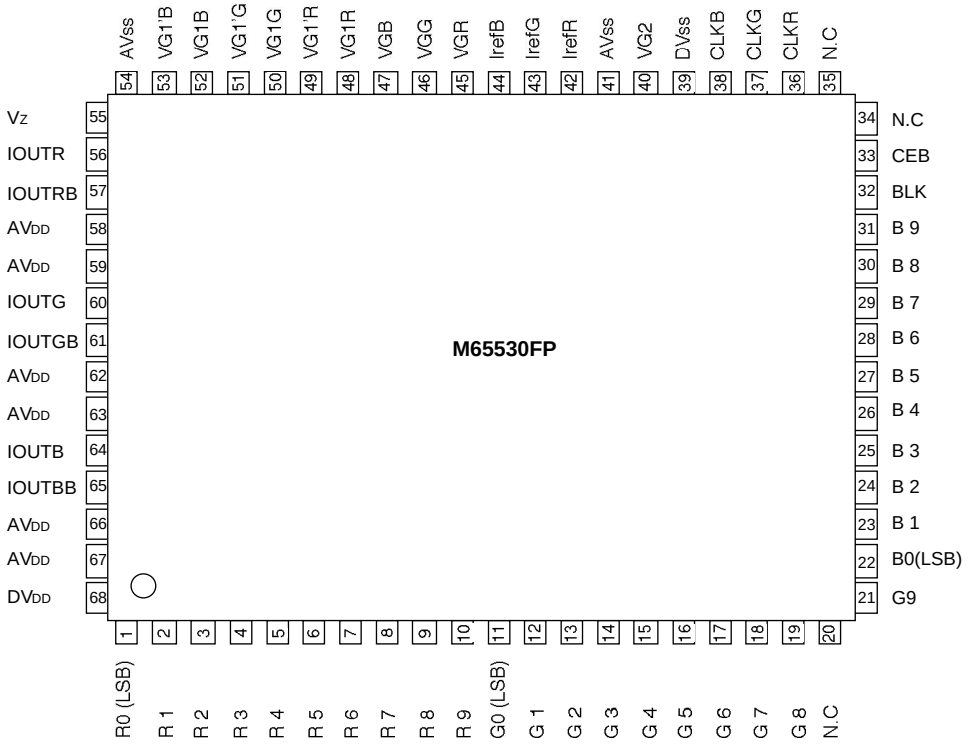
TV, VCR, etc.

RECOMMENDED OPERATING CONDITION

Supply voltage range.....4.75 to 5.25 V

Rated supply voltage.....5.0 V

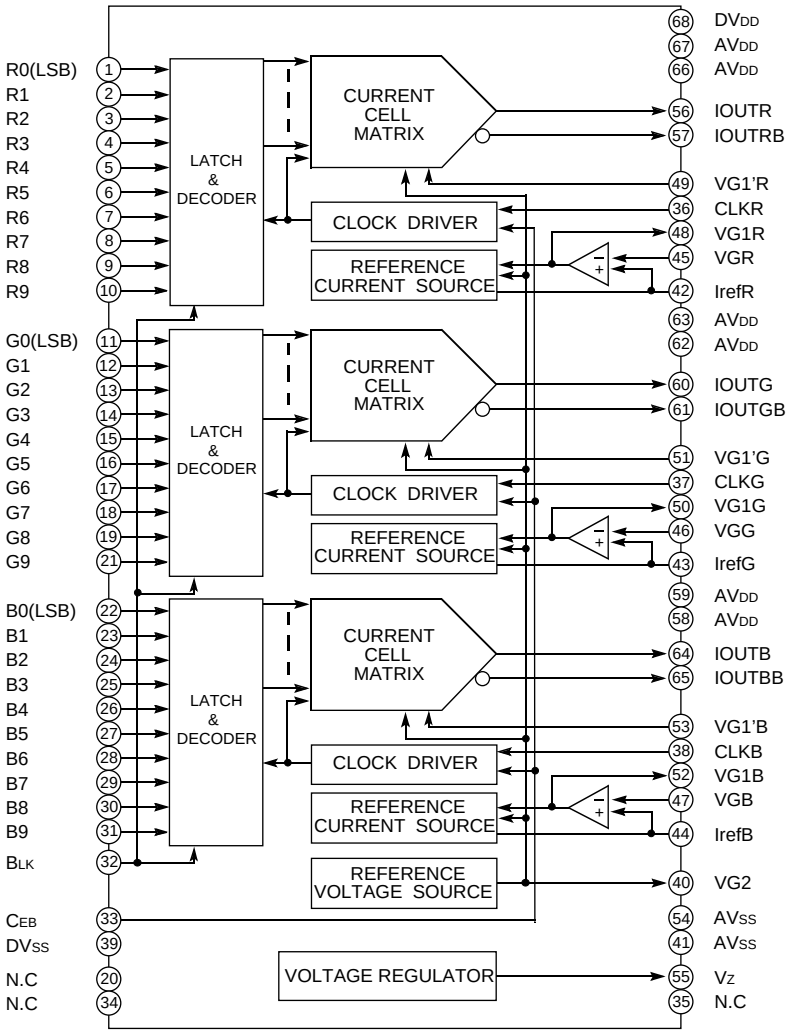
PIN CONFIGURATION (TOP VIEW)



Outline 68P6S-A

NC:NO CONNECTION

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C, unless otherwise noted.)

Symbol	Parameter	Conditions	Ratings	Unit
DV_{DD}	Digital supply voltage	Pin 68	0 to 7.0	V
AV_{DD}	Analog supply voltage	Pin 58, 59, 62, 63, 66, 67	0 to 7.0	V
V_{ID}	Digital input voltage	Pin 1 to 19, 21 to 33, 36 to 38	0 to 7.0	V
I_{OUT}	Analog output current	Pin 56, 57, 60, 61, 64, 65	-30 to 0	mA
P_d	Power dissipation		900	mW
T_{opr}	Operating temperature		0 to +70	°C
T_{stg}	Storage temperature		-20 to +125	°C

In current measurement, (+) and (-) is corresponding to an inflow and an outflow current, respectively.

ELECTRICAL CHARACTERISTICS (Ta = 25°C, AV_{DD} = DV_{DD} = 5.00V, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Res	Resolution			10		Bits
V_{DD}	Supply voltage		4.75	5.00	5.25	V
DI_{DD}	Digital supply current			8		mA
AI_{DD}	Analog supply current			100		mA
NL	Integral nonlinearity	R_L=75Ω, Rref=750Ω			± 2.0	LSB
DNL	Differential nonlinearity	R_L=75Ω, Rref=750Ω			± 0.5	LSB
V_{IH}	Digital input voltage "H"		2.15		V_{CC}	V
V_{IL}	Digital input voltage "L"		0		0.85	V
t_{su}	Data set-up time		5			ns
t_h	Data hold time		5			ns
t_s	Settling time	R_L=75Ω, Rref=750Ω, ±1%FS			25	ns
V_{FS}	Full-scale amplitude	R_L=75Ω, Rref=750Ω			2.0	V_{P-P}
V_Z	Regulated voltage source			1.28		V

In current measurement, (+) and (-) is corresponding to an inflow and an outflow current, respectively.

RECOMMENDED OPERATING CONDITIONS (Ta = 25°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{DD}	Supply voltage	4.75	5.00	5.25	V
V_{IH}	Digital input voltage (High)	2.15		V_{CC}	V
V_{IL}	Digital input voltage (Low)	0		0.85	V
t_{WH}	Clock pulse width (High)	10			ns
t_{WL}	Clock pulse width (Low)	10			ns
t_{su}	Set-up time	5			ns
t_h	Hold time	5			ns

DESCRIPTION OF PIN

Pin No.	Name	I/O	Function	It connects to ---
1 to 10	R0 to R9	I	Digital input pin for a DAC (Red channel).	DSP LSI
11 to 19, 21	G0 to G9	I	Digital input pin for a DAC (Green channel).	DSP LSI
20, 34, 35	N.C.	-	No connection. It is grounded during actual use.	GND
22 to 31	B0 to B9	I	Digital input pin for a DAC (Blue channel).	DSP LSI
32	BLK	I	Analog output setting during a blanking interval.	Control LSI
33	CEB	I	Power-down control during unused conditions.	Control LSI
36 to 38	CLKR,G,B	I	Clock input.	DSP LSI
39	DV_{SS}	-	Digital ground.	GND
40	VG2	O	Reference voltage for a current switch.	Bypass capacitor
41	AV_{SS}	-	Analog ground.	GND
42 to 44	IrefR,G,B	O	The resistor for a conversion between voltage and current is connected to this pin.	Current setting resistor
45 to 47	VGR,G,B	I	A voltage input for an analog output current control. It is connected to the VZ(pin 55) during an actual use.	Variable resistor
48, 50, 52	VG1R,G,B	O	Phase compensation for a reference current source.	Phase compen. capacitor
49, 51, 53	VG1'R,G,B	I	A reference voltage input for a current matrix. It is connected to VG1 according to the application.	Phase compen. capacitor
54	AV_{SS}	-	Analog ground.	GND
55	V_Z	O	Reference voltage output.	Bypass capacitor
56, 60, 64	I OUT R,G,B	O	Analog output.	Output terminal (filter)
57, 61, 65	I OUT RB,GB,BB	O	Inverse analog output.	GND
58, 59, 62 63, 66, 67	AV_{DD}	-	Analog supply voltage of 5.0V.	Power supply
68	DV_{DD}	-	Digital supply voltage of 5.0V.	Power supply

Table of an analog power-down function (pin 33)

Analog power-down signal	Power-down function
"H"	Power-down
"L"	Normal operation

Table of a blanking function (pin 32)

Blanking signal	Blanking function
"H"	Blanking
"L"	Normal operation

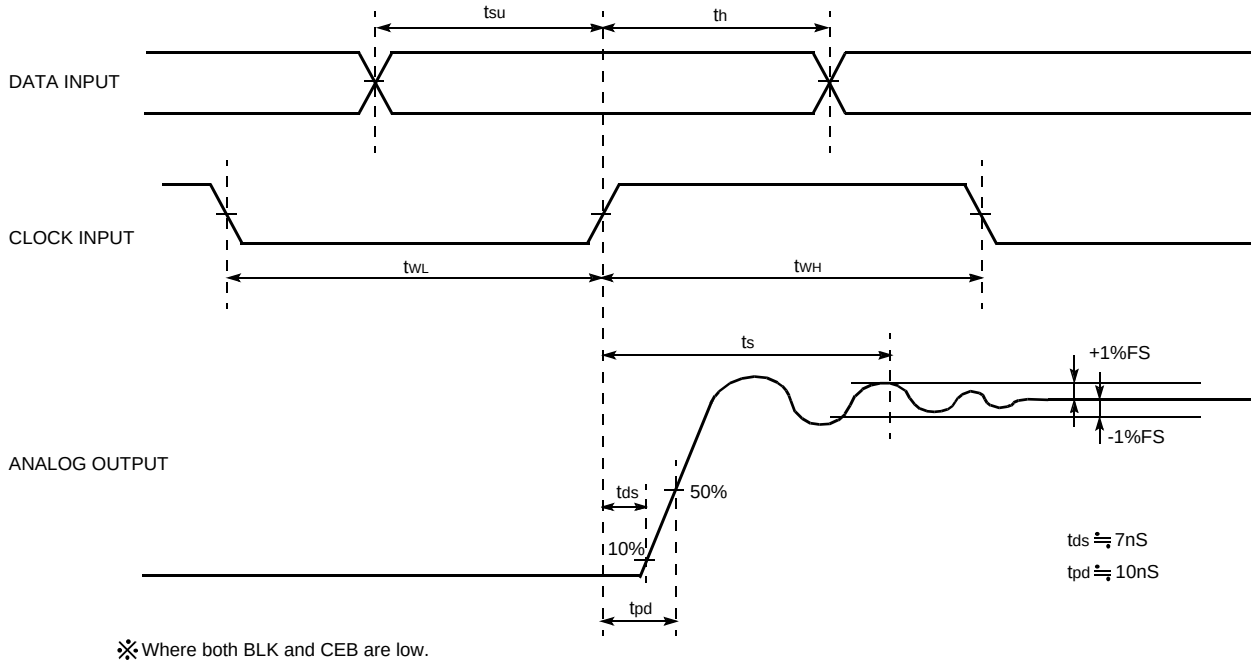
• A blanking operation sets an analog output to 0V on the first rising edge of the clock after a blanking signal has become "H" regardless of a digital input code.

Table of an analog output function (iout)

Digital input code										Analog output voltage
9 MSB	8	7	6	5	4	3	2	1	0 LSB	
1	1	1	1	1	1	1	1	1	1	2.0000V
1	1	1	1	1	1	1	1	1	0	1.9980V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	0	0	0	0	0	1.0000V
0	1	1	1	1	1	1	1	1	1	0.9980V
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	0	0	0	0	0	0	0	0	1	0.0020V
0	0	0	0	0	0	0	0	0	0	0.0000V

Note : The analog output voltage is a theoretical value in the condition of V_{DD} = 5.0V, V_Z = 1.28V, Rref = 768Ω and R_L = 75Ω.

INPUT / OUTPUT TIMING DIAGRAM



※Where both BLK and CEB are low.

CURRENT SETTING RESISTOR (Rref) AND OUTPUT LOAD RESISTOR (R_L) (external components)

Full-scale output amplitude (V_{FS}) of each D/A converter is ;

V_{FS} = (VG / Rref) x 16 x R_L (V_{P-P}).

where VG = 1.28 V, Rref = 768 Ω, R_L = 75 Ω and V_{DD} = 5.0V.

The full-scale output of about 2.0 V_{P-P} is available by setting R_L and Rref to 75 Ω and 768 Ω, respectively.
An output impedance of the analog output terminal is almost the same as the load resistor (R_L).

NOTES TO THE OPERATION

1. Both a ground and a supply planes in a PCB should be as wide as possible for reducing a parasitic inductance and resistance. Especially, for the better performance, the analog plane needs to be much wider.

2. A tantalum or electrolytic capacitor of 10µF or more and a ceramic capacitor of 0.01µF are tied together, which are connected between a digital supply and ground, also between a analog supply and ground.
   These capacitors should be placed as close as possible to the IC.
   They work as bypass capacitors for preventing a degradation in the performance by a supply voltage
   fluctuation caused by digital signals including a clock and digital inputs and so on.

3. The analog output should be isolated as much as possible from a clock and digital inputs, thus minimizing decoupling and interactive noise.

APPLICATION EXAMPLE