

DESCRIPTION

The M65677FP encodes CCIR601 or CCIR656 format Y/Cb/Cr data into analog NTSC and PAL video signals, including Digital Signal Processing functions such as Closed Caption encoding, Overlay OSD, Anti Video Copy Processing (Note1) e.t.c. It also includes peripheral processing function such as 10bit DAC e.t.c., so that low cost and compact system can be realized.

FEATURES

- Macrovision's video anti copy process Rev 7.01 supported (Note1)
- Overlay CGMS signal on line 20/283 for 525/60 (Note3)
- Generate CRCC for CGMS Signal
- Overlay WSS signal on line 23 for 625/50 (Note4)
- Color adjustment (TINT/color control)
- NTSC, B/G PAL or MPAL Video Outputs
- Component Y/C Video (S-Video) and CVBS or Y/U/V Outputs
- Supporting CCIR601 and CCIR656 format data
- Closed Caption Manager on line 21/284 for NTSC
- Generate ODD parity for Closed Caption Manager
- H/V Sync and Composite generating
- Overlay Digital OSD Supporting Y/Cb/Cr 4:4:4
- Over sampling Filter
- 2ch 10bit DAC and 3ch 6dB Amp (Note2)
- 3.3V I/O interface
- I²C Bus Interface for Controls
- Power down mode

Note

(Note1): This device is protected by U.S. patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. The use of Macrovision Corporation's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-par-view uses only, unless otherwise authorized in writing by Macrovision. Reverse engineering or disassembly is prohibited.

(Note2): 6dB Amp max. output is 1.0VP-P.

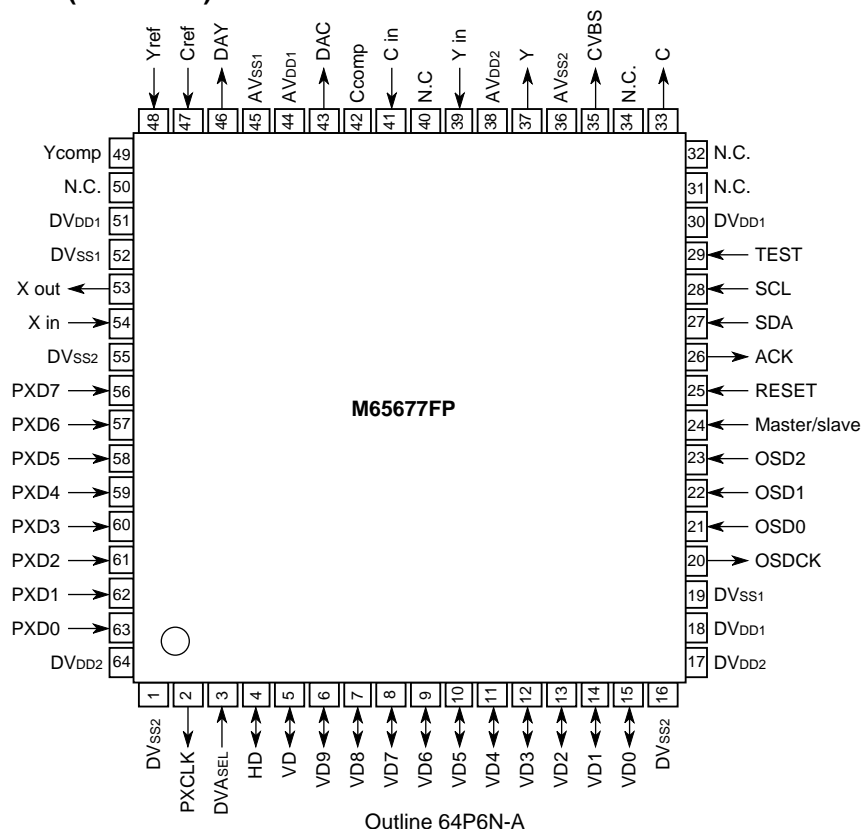
(Note3): Copy Generation Management System-A (IEC1880)

(Note4): Wide Screen Signaling (ETS300 294)

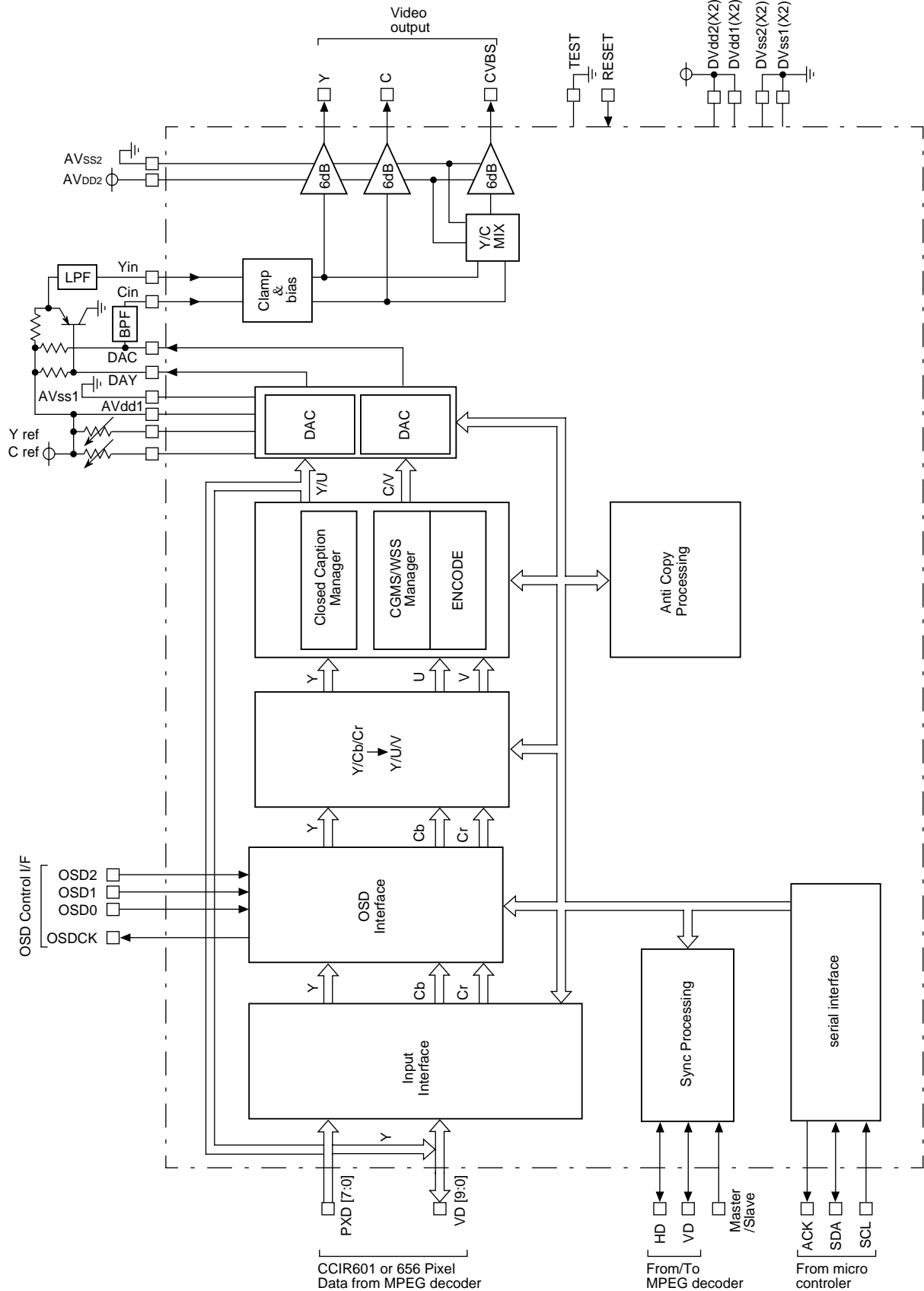
APPLICATION

DVB, DVD , Digital CATV, Video CD

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{DD}	Supply voltage	-0.3		4.5	V
V _I	Digital input voltage	-0.3		V _{DD} +0.3	V
V _O	Digital output voltage	-0.3		V _{DD} +0.3	V
T _a	Operating temperature	-20	+25	+75	°C
T _{stg}	Storage temperature	-40		+125	°C

RECOMMENDED OPERATING CONDITION (T_a=25°C, DV_{DD}=AV_{DD}=3.3V, DV_{SS}=AV_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Supply						
DV _{DDX}	Digital supply voltage		3.0	3.3	3.6	V
AV _{DDX}	Analog supply voltage		3.15	3.3	3.45	V
DI _{DD}	Digital current consumption		0		45	mA
AI _{DD}	Analog current consumption		0		55	mA
Digital input						
V _{IL}	Input voltage	DV _{DD} =3.0V	0		0.8	V
V _{IH}		DV _{DD} =3.6V	2.5		3.6	V
I _{IL} /I _{IH}	Input leakage current	DV _{DD} =3.0V, V _I =0V or V _I =3.6V			±15	μA
C _I	Input capacitance	f=1MHz, V _{DD} =0V		7	15	pF
Digital output						
V _{OL}	Output voltage	DV _{DD} =3.3V, I _o <1μA			0.05	V
V _{OH}			3.25			V
C _O	Output capacitance	f=1MHz, V _{DD} =0V		7	15	pF
I²C bus						
I _o	Output current	DV _{DD} =3.0V, V _{IL} =0.4V	4.0			mA
I _{oz}	Output leakage current (off)	DV _{DD} =3.6V, V _I =0V or V _I =3.6V			±15	μA
D/A converter						
Res	Resolution			10		Bit
INL	Integral non-linearity error				±2.0	LSB
DNL	Differential non-linearity error				±1.0	LSB
V _{fSMAX}	Maximum output amplitude		1.5			V _{P-P}
6-dB amplifier						
R _{bias}	Bias resistor		7.5	10.0	11.5	kΩ
G _{V_YC}	Output gain (Y/C)		5.50	6.00	6.50	dB
G _{V_CV}	Output gain (CVBS)		5.10	6.00	6.85	dB
DR _{in}	Input dynamic range		0.8			V _{P-P}
DR _{out}	Output dynamic range		1.6			V _{P-P}
I _{yich}	Yin clamp charge current		-12	-26	-50	μA
I _{yids}	Yin clamp discharge current		0.26	0.65	1.80	μA
R _{yicl}	Yin clamp discharge current	$R_{yicl} = -\frac{I_{yich}}{I_{yids}}$	20	0.65	70	-
V _{yicl}	Yin input clamp voltage		0.45	0.50	0.55	V
V _{yocl}	Y output clamp voltage		0.40	0.50	0.60	V
V _{cvcl}	CVBS output clamp voltage		0.30	0.50	0.70	V
V _{cin}	Cin input bias voltage		0.95	1.00	1.05	V
V _{cob}	C output bias voltage		0.90	1.00	1.10	V
I _{amp}	Output current		1.00			mA

DESCRIPTION OF PIN

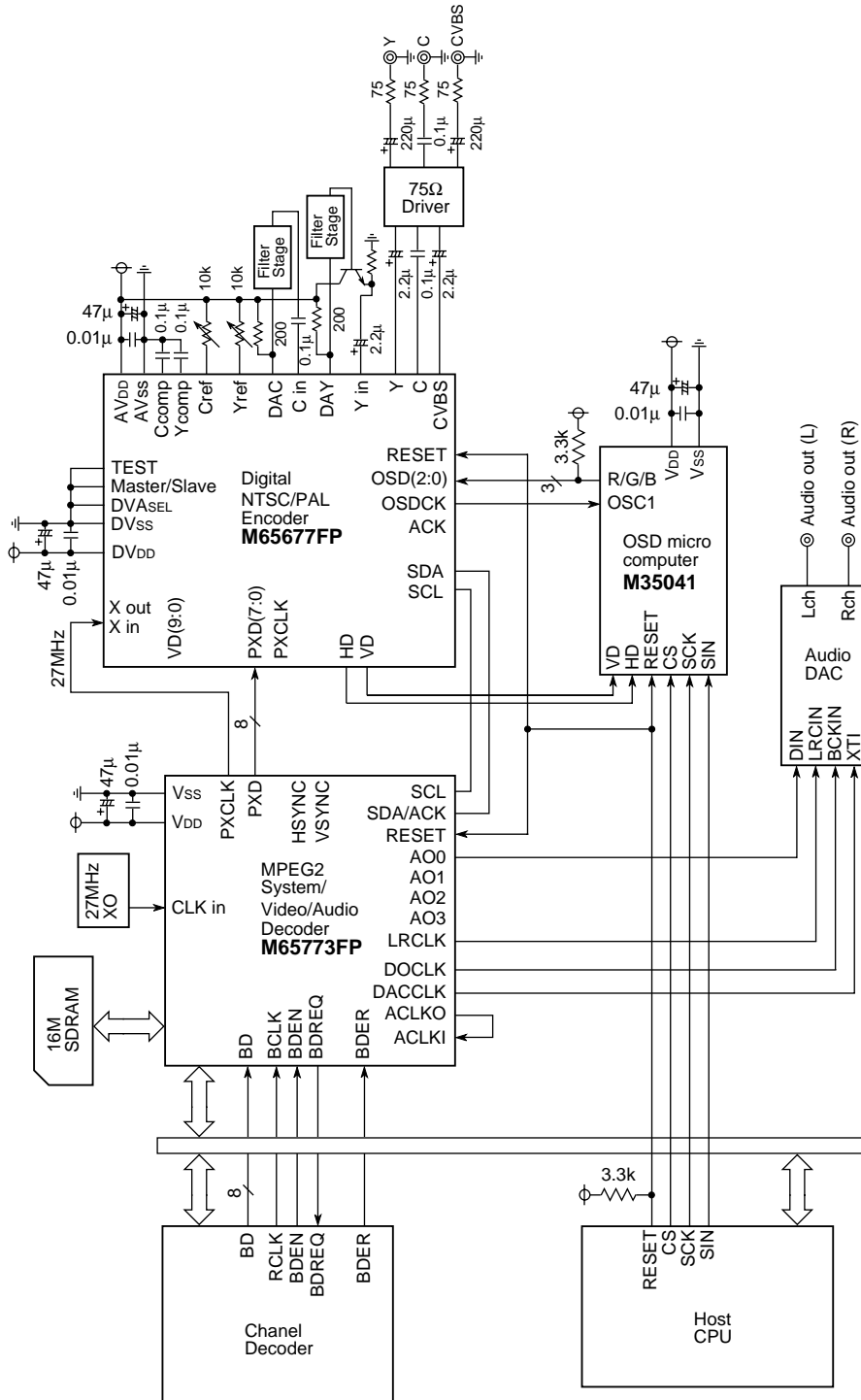
Pin No.	Pin name	Type	Function
1	DVSS2	Supply	Digital ground for the I/O.
2	PXCLK	O	Reference clock for input pixel data. The clock frequency is 27.0MHz.
3	DVASEL	I	I ² C slave address setting. "Low" is for the address of 40h, "High" is for the address of 42h.
4	HD	I/O	Horizontal sync signal input or output. It is an input and output in the slave and master mode, respectively.
5	VD	I/O	Vertical sync input or output. Or OddEven signal output. It is an input and output in the slave and master mode, respectively.
6	VD9	I/O	Video data outputs. In the Y/U/V output mode, the output is the 10-bit digital luma signal with a composite sync. VD9 is MSB and VD0 is LSB.
7	VD8		
8	VD7		
9	VD6		
10	VD5		
11	VD4		
12	VD3		
13	VD2		
14	VD1		
15	VD0		
16	DVSS2	Supply	Digital ground for the I/O.
17	DVDD2	Supply	Digital supply for the I/O.
18	DVDD1	Supply	Digital supply for the internal logic.
19	DVSS1	Supply	Digital ground for the internal logic.
20	OSDCK	O	The reference clock for an external OSD microcontroller. The frequency is 13.5MHz or 6.25MHz, alternated by the I ² C bus control.
21	OSD0	I	The color look-up table address input. MSB and LSB is OSD2 and OSD0, respectively.
22	OSD1		
23	OSD2		
24	Master/Slave	I	Synchronizing mode selection. "Low" is for the slave mode. "High" is for the master mode.
25	RESET	I	Initializing reset. "LOW" is active.
26	ACK	O	Acknowledge line (Open drain output).
27	SDA	I/O	Serial data line/Acknowledge line (Open drain output).
28	SCL	I	Serial clock line.
29	TEST	I	For testing. It should be grounded during an actual use.
30	DVDD1	Supply	Digital supply for the internal logic.
31	N.C.		No connection.
32	N.C.		No connection.
33	C	O	The analog chroma output from a 6dB amplifier. The output amplitude is 1.0V _{P-P} (typ.), while the input is 0.5V _{P-P} .
34	N.C.		No connection.
35	CVBS	O	The analog composite video signal from a 6dB amplifier. The output amplitude is 1.24V _{P-P} (typ.).
36	AVSS2	Supply	Analog ground for 6dB amplifiers.
37	Y	O	The analog luma output from a 6dB amplifier. The output amplitude is 1.2V _{P-P} (typ.), while input is 0.6V _{P-P} .
38	AVDD2	Supply	Analog supply for 6dB amplifiers.
39	Yin	I	The analog luma input from an external LPF. This input has bias circuit. The signal must input via a capacitor.
40	N.C.		No connection.
41	Cin	I	The analog chroma input from an external LPF. This input has bias circuit. The signal must input via a capacitor.



DESCRIPTION OF PIN (cont.)

Pin No.	Pin name	Type	Function
42	Ccomp	I	Phase compensation for chroma or V output DAC. It should be connected to the analog ground via a capacitor.
43	DAC	O	Chroma or V signal output. The DAC output should be connected to the analog supply via a load resistor (RL). The output amplitude is set up by reference resistor (Rref) and RL.
44	AVDD1	Supply	Analog supply for DACs.
45	AVSS1	Supply	Analog ground for DACs.
46	DAY	O	Luma or U signal output. It should be connected to the analog supply via a load resistor (RL). The output amplitude is set up by reference resistor (Rref) and RL.
47	Cref	I	A reference current source for chroma or V signal output DAC. It should be connected to the analog supply via a reference resistor (Rref).
48	Yref	I	A reference current source for Y or U DAC. It should be connected to the analog supply via a reference resistor (Rref).
49	Ycomp	I	Phase compensation for Y or U DAC. It should be connected to the analog ground via a capacitor.
50	N.C.		No connection.
51	DVDD1	Supply	Digital supply for the internal logic.
52	DVSS1	Supply	Digital ground for the internal logic.
53	Xout	O	System clock output. It must be in no connection except for a connection to a X'tal oscillator.
54	Xin	I	System clock input. The clock frequency is only 27.0MHz.
55	DVSS2	Supply	Digital ground for the I/O.
56	PXD7	I	Pixel data inputs. The acceptable video data are; • multiplexed video data (Y/Cb/Cr) including timing reference code of SAV and EAV, defined in CCIR Rec656 • multiplexed video data (Y/Cb/Cr) defined in CCIR Rec601 MSB and LSB is PXD7 and PXD0, respectively.
57	PXD6		
58	PXD5		
59	PXD4		
60	PXD3		
61	PXD2		
62	PXD1		
63	PXD0		
64	DVDD2	Supply	Digital supply for the I/O.

APPLICATION EXAMPLE

(CCIR656 I/F, Y/C/CVBS Output Mode)



-  : 3.3V Power Supply (for Digital/Analog)
-  : 5.0V Power Supply (for Analog)

Units Resistance : Ω
Capacitance : F