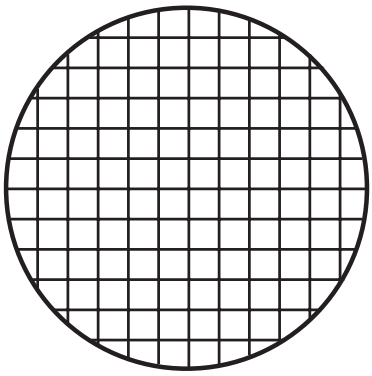
M65KA128AL

128Mbit (4 Banks x 2M x 16) 1.8V Supply, Low Power SDRAMs

Feature summary

- 128Mbit Synchronous Dynamic RAM
  - Organized as 4 Banks of 2 MWords, each 16 bits wide
- Supply Voltage
  - V_{DD} = 1.65V to 1.95V
  - V_{DDQ} = 1.65 to 1.95V for Input/Output
- Synchronous Burst Read and Write
  - Fixed Burst lengths: 1, 2, 4, 8 words or full Page
  - Burst Types: Sequential and Interleaved.
  - Maximum clock frequency: 104MHz
  - $\overline{CAS}$ Latency 2, 3
- Automatic Precharge
- Low Power features:
  - PASR (Partial Array Self Refresh),
  - Automatic TCSR (Temperature Compensated Self Refresh)
  - Driver Strength (DS)
  - Deep Power-Down Mode
- Delivery form: Unsawn Wafer
- Auto Refresh and Self Refresh
- LVCMOS Interface Compatible with Multiplexed Addressing
- Operating temperature
  - –25°C to +90°C



Wafer

The M65KA128AL is only available as part of a Multi-Chip Package Product.

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1 Summary description

The M65KA128AL is a 128 Mbit Low Power Synchronous DRAM (SDRAM) organized as 4 Banks of 2,097,152 Words of 16 bits each.

The Low Power SDRAM achieves low power consumption and high-speed data transfer using the pipeline architecture. It is well suited for handheld battery powered applications like PDAs, 2.5 and 3G mobile phones and handheld computers.

The device architecture is illustrated in *Figure 2: Functional Block Diagram*. The device uses Burst mode to read and write data. It is capable of one, two, four, eight-word and full page, sequential and interleaved Burst.

To minimize current consumption during self-refresh operations, the M65KA128AL includes three system-accessible mechanisms configured via the Extended Mode Register:

- Automatic Temperature Compensated Self Refresh (TCSR) is used to adapts the refresh rate according to the operating temperature.
- Partial Array Self Refresh (PASR) performs a limited refresh of a half bank, a quarter of bank, one bank, two banks or all banks.
- The Deep Power-Down (DPD) mode completely halts the refresh operation and achieves minimum current consumption by cutting off the supply voltage from the whole memory array.

The M65KA128AL is programmable through two registers, the Mode Register and the Extended Mode Register:

- The Mode Register is used to select the $\overline{\text{CAS}}$ Latency, the Burst Type (sequential or interleaved) and the Burst Length. For more details, refer to *Table 4: Mode Register Definition*, and to *Section 4.1: Mode Register Set command*.
- The Extended Mode Register is used to program the Low Power features (PASR and Driver Strength) to reduce the current consumption during the Self Refresh operations. For more details, refer to *Table 5: Extended Mode Register Definition*, and to *Section 4.2: Extended Mode Register Set command*.

The M65KA128AL is offered in unsawn wafer.

Figure 1. Logic Diagram

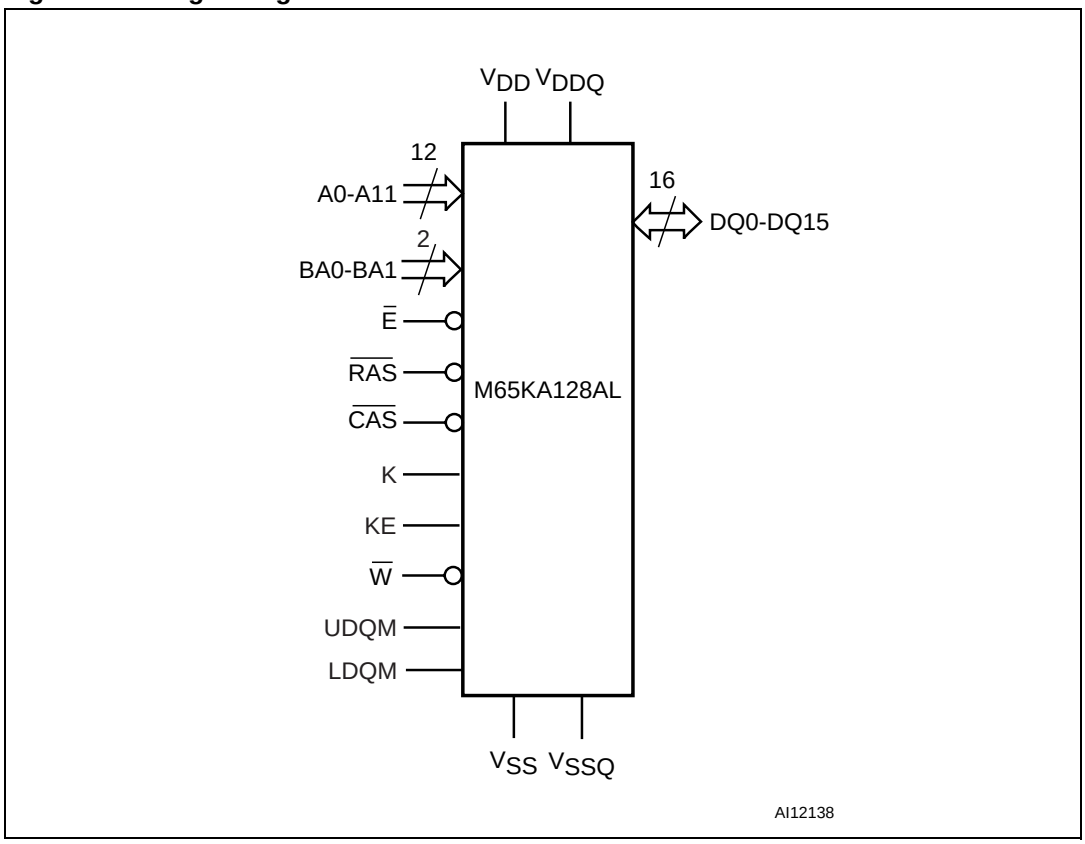
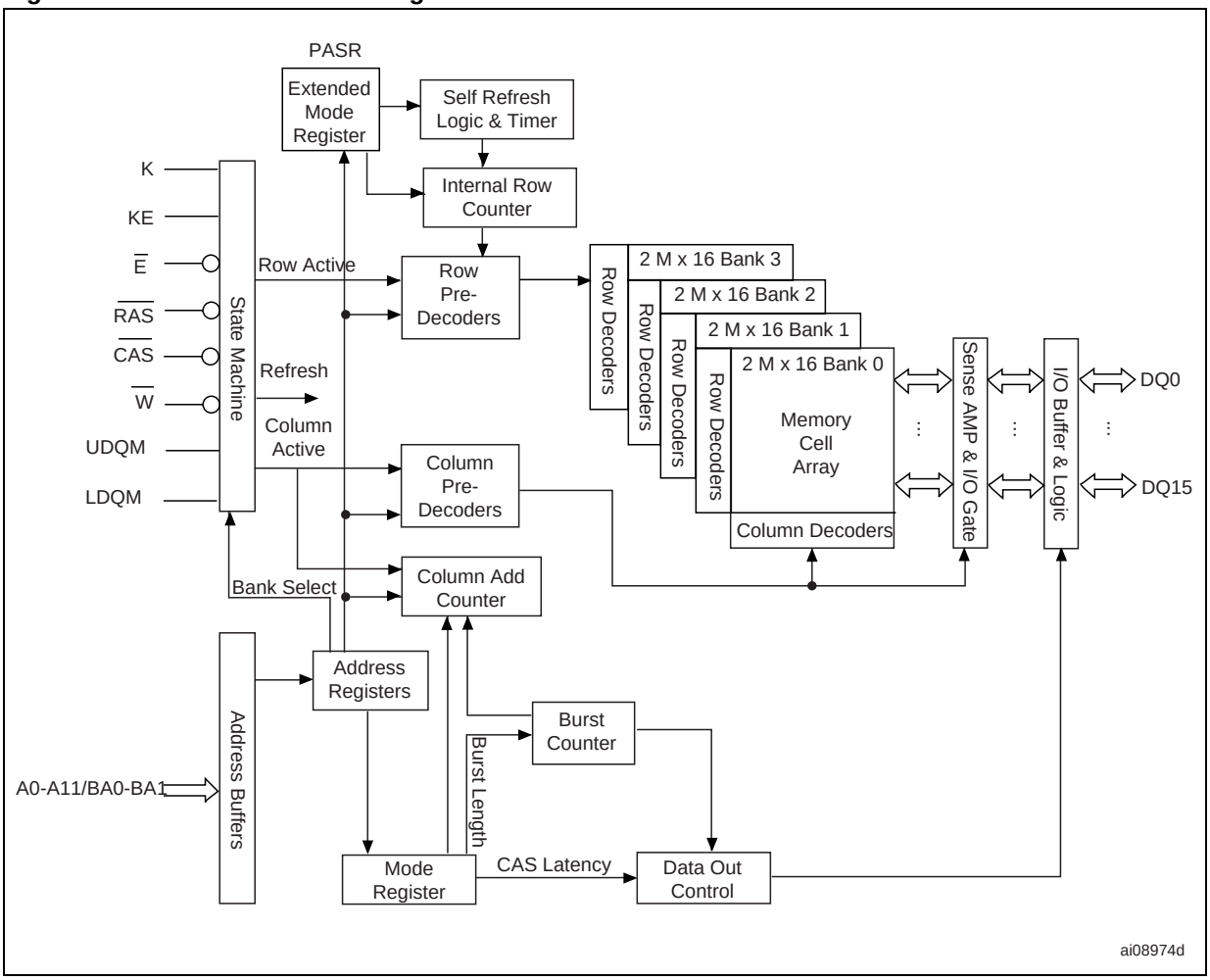


Table 1. Signal Names

A0-A11	Address Inputs
BA0-BA1	Bank Select Inputs
DQ0-DQ15	Data Inputs/Outputs
K	Clock Input
KE	Clock Enable Input
$\overline{E}$	Chip Select Input
$\overline{W}$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
UDQM	Upper Data Input/Output Mask
LDQM	Lower Data Input/Output Mask
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground

Figure 2. Functional Block Diagram



2 Signal descriptions

See *Figure 1: Logic Diagram*, and *Table 1: Signal Names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A11)

The A0-A11 Address Inputs are used to select the row or column to be made active. If a row is selected, all A0-A11 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used. If A10 is High (set to '1') during Read or Write, the Read or Write operation includes an Auto Precharge cycle. If A10 is Low (set to '0') during Read or Write, the Read or Write cycle does not include an Auto Precharge cycle.

2.2 Bank Select Inputs (BA0-BA1)

The BA0 and BA1 Banks Select Inputs are used to select the bank to be made active.

The device must be enabled, the Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}$, and $\overline{W}$ must be High, V_{IH}, when selecting the addresses. The address inputs are latched on the rising edge of the clock signal, K.

2.3 Data Inputs/Outputs (DQ0-DQ15)

The Data Inputs/Outputs output the data stored at the selected address during a Read operation, or are used to input the data during a write operation.

2.4 Chip Select ($\overline{E}$)

The Chip Select input $\overline{E}$ activates the memory state machine, address buffers and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.5 Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a Read or Write.

2.6 Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing.

2.8 Clock Input (K)

The Clock signal, K, is used to clock the Read and Write cycles. During normal operation, the Clock Enable pin, KE, is High, V_{IH}. The clock signal K can be suspended to switch the device to the Self Refresh, Power-Down or Deep Power-Down mode by driving KE Low, V_{IL}.

2.9 Clock Enable (KE)

The Clock Enable, KE, pin is used to control the synchronizing of the signals to Clock signal K. The signals are clocked when KE is High, V_{IH} When KE is Low, V_{IL}, the signals are no longer clocked and data Read and Write cycles are extended. KE is also involved in switching the device to the Self Refresh, Power-Down and Deep Power-Down modes.

2.10 Lower/Upper Data Input/Output Mask (LDQM/UDQM)

Lower Data Input/Output Mask and Upper Data Input/Output Mask pins are input signals used to control the Input and Output buffers, respectively.

During Read operations, LDQM and UDQM control the Output buffer. When both LDQM and UDQM are High, V_{IH}, the Output buffer is disabled. When held Low, V_{IL}, the Output buffer is enabled. LDQM and UDQM are used to mask the data read or written from or to the memory array. LDQM Low, V_{IL}, gates the data from or to the Lower Byte Data I/O (DQ0 to DQ7) while UDQM Low, gates the data from or to the Upper Byte Data I/Os (DQ8 to DQ15).

During read operations, the latency between LDQM/UDQM High or Low and data output disabled or enabled is two clock cycles. During write operations, there is no latency between LDQM/UDQM stable and data input valid.

2.11 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read and Write).

2.12 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid certain conditions that would result in data corruption.

2.13 V_{SS} Ground

Ground, $V_{SS,}$ is the reference for the core power supply. It must be connected to the system ground.

2.14 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package).

3 Operations

There are 7 operating modes that control the memory. Each of these is described in this section, see *Table 2: Operating Modes*, for a summary.

3.1 Power-Up

The Low Power SDRAM has to be powered up and initialized in a well determined manner:

1. Power must be applied to V_{DD} and V_{DDQ} simultaneously.
2. After applying V_{DD} and VD_{DQ}, a minimum pause of 200µs must be respected before the signals can be toggled.
3. The Precharge command must then be issued to all banks. The Clock Enable input, KE, and UDQM/LDQM must be held High until the Precharge command is issued to make sure that DQ0-DQ15 remain high impedance.
4. t_{RP} after precharging all the banks, the Mode Register and the Extended Mode Register must be set by issuing a Mode Register Set command and an Extended Mode Register Set command, respectively. A minimum pause of t_{MRD} must be respected after each register set command.
5. After configuring the registers, 2 or more Auto Refresh cycles must be executed before the device is ready for normal operation.

The fourth and fifth steps can be swapped.

3.2 Burst Read

The Read Command is used to switch the device to Burst Read mode (see *Section 4.4: Read command* for details). In Burst Read mode the data is output in bursts synchronized with the clock. A valid Burst Read operation is initiated by driving $\overline{E}$ and $\overline{CAS}$ Low, V_{IL}, and by driving $\overline{W}$ and $\overline{RAS}$ High, V_{IH}, at the positive edge of the clock signal, K.

Burst Read can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to ‘1’) when the Burst Read command is issued, the Burst Read operation will be followed by an Auto Precharge cycle.

During Burst Read operation, the memory reads data from the activated bank. Different Burst Types and Lengths can be programmed using the Mode Register bits (see *Section 5.1: Mode Register description*). The Burst Types available are Sequential and Interleaved, selected using Mode Register Bit A3. Possible Burst Lengths are 1-, 2-, 4-, 8-Word and Full Page, selected using Mode Register Bits A2 to A0.

3.3 Burst Write

The Write Command is used to switch the device to Burst Write mode (see *Section 4.5: Write command* for details). In Burst Write mode the data is input in bursts synchronized with the clock. A valid Burst Write is initiated by driving $\overline{E}$, $\overline{CAS}$ and $\overline{W}$ Low, V_{IL}, and by driving $\overline{RAS}$ High, V_{IH}, at the positive edge of the clock signal, K.

Burst Write can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to '1') when the Write command is issued, the Write operation will be followed by an Auto Precharge cycle.

During Burst Write operation, the memory writes data to the activated bank. As for Burst Read, different Burst Types and Lengths can be utilized, programmed in the same fashion.

3.4 Self Refresh

In Self Refresh mode, the data contained in the Low Power SDRAM memory array is retained and refreshed. The Low Power SDRAM refresh cycles are asynchronous.

The Self-Refresh mode is entered by driving KE Low (set to '0'), with $\overline{E}$, $\overline{RAS}$, and $\overline{CAS}$ Low, and $\overline{W}$ High (set to '1'). When in this mode, the device is not clocked any more.

The Self Refresh mode is exited by driving KE from Low to High, with $\overline{E}$ High, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

3.5 Auto Refresh

The Auto Refresh mode is used to refresh the Low Power SDRAM in normal operation mode whenever needed.

During an auto refresh operation, KE must be kept High, V_{IH} and the address bits are "Don't Care" because the specific address bits are generated by the internal refresh address counter.

3.6 Power-Down

In Power-Down mode, the current is reduced the Standby current.

For the memory to enter the Power-Down mode, KE must be held Low (set to '0'), after the Precharge Time t_{RP}, with $\overline{E}$ High (set to '1'), $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

The Power-Down mode is exited by driving KE High, with $\overline{E}$ High, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care, or with $\overline{E}$ Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

3.7 Deep Power-Down

The purpose of this mode is to achieve maximum power reduction by cutting the power supply to the whole memory array. Data is no longer retained when the device enters Deep Power-Down Mode.

The Low Power SDRAM is switched to Deep Power-Down mode by applying V_{IL} to $\overline{E}$ and $\overline{W}$, and V_{IH} to $\overline{RAS}$ and $\overline{CAS}$ on the rising edge of the clock, K, and by driving KE Low, V_{IL}. For more information, see *Figure 25: Deep Power-Down Entry AC Waveforms*.

The Low Power SDRAM is released from Deep Power-Down mode by applying V_{IH} to KE, with all other pins Don't Care. Then a special sequence, is required before the device can take any new command into account:

1. Maintain No Operation status conditions (see *Table 3* for a minimum time of 200µs,
2. Issue a Precharge command to all the banks of the device (see *Section 4.6: Precharge command* for details),
3. Issue 2 or more Auto-Refresh commands,
4. Issue a Mode Register Set command and an Extended Mode Register Set command to initialize the Mode Register and the Extended Mode Register, respectively.

The third and fourth steps can be swapped.

The Deep Power-Down mode exit sequence is illustrated in *Figure 26: Deep Power-Down Exit AC Waveforms*.

Table 2. Operating Modes (1)

Operating Mode	KEn-1	KEn	$\overline{E}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A10	A9, A11	A0-A7	BA0-BA1
Burst Read	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Valid	Start Column Address	Bank Select
Burst Write	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Valid	Start Column Address	Bank Select
Self Refresh	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X
Auto Refresh	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X
Power-Down	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X
			V_{IH}	X	X	X				
Deep Power-Down	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X
Device Deselect	V_{IH}	X	V_{IH}	X	X	X	X	X	X	X
No Operation	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			

1. X = Don't Care V_{IL} or V_{IH}.

4 Commands

There are 16 commands that control the memory. Refer to *Table 3: Commands*, in conjunction with the text descriptions below and to *Table 3: Commands*.

4.1 Mode Register Set command

The Mode Register Set command is issued by applying V_{IL} to $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ and by setting BA1 to '0', and BA0 to '0'.

The Mode Register Set command must be executed after the Power-Up sequence prior to issuing a Bank (Row) Active command.

The execution of a Mode Register Set command will re-program the Mode Register, modifying its contents.

4.2 Extended Mode Register Set command

The Extended Mode Register Set command is issued by applying V_{IL} to $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$, and then by setting BA1 to '1', and BA0 to '0'.

The Extended Mode Register Set command must be executed after the Power-Up sequence prior to issuing a Bank (Row) Active command.

The execution of an Extended Mode Register Set command will re-program the Extended Mode Register, modifying its contents.

4.3 Bank (Row) Activate command

The Bank (Row) Active command is used to activate a row in a specific bank of the device. This command is initiated by driving $\overline{E}$ and $\overline{RAS}$ Low, V_{IL}, and driving $\overline{CAS}$ and $\overline{W}$ High, V_{IH}, at the positive edge of the clock signal, K. The value on BA1 and BA0 selects the bank, and the value on A0-A11 selects the row. The selected row remains active for column access until a Precharge command is issued to the bank containing the row.

A minimum time of t_{RCD} is required after issuing the Bank (Row) Active command prior to initiating Read and Write operations from and to the activated bank.

4.4 Read command

The Read command is used to switch the Low Power SDRAM to Burst Read mode (see *Section 3.2: Burst Read*).

During Burst Read operation, the memory reads data from the activated bank. Inputs BA1 and BA0 are used to select a bank, Address inputs A8-A0 are used to select a starting column location. The value at input A10 determines whether Auto Precharge is activated. If Auto Precharge is selected, the row being accessed will be precharged at the end of the Burst Read operation. If Auto Precharge is not selected, the row will remain active for subsequent accesses. Different Burst Types and Lengths can be programmed using the Mode Register bits (see *Table 4: Mode Register Definition*):

- The Burst Types available are Sequential and Interleaved selected using Mode Register Bit MR3.
- Possible Burst Lengths are 1-, 2-, 4-, 8-Word and Full Page, selected using Mode Register Bits MR0 to MR2.

4.5 Write command

The Write command is used to switch the Low Power SDRAM to Burst Write mode (see *Section 3.3: Burst Write*).

During Burst Write operation, the memory writes data to the activated bank. Inputs BA1 and BA0 inputs are used to select a bank, the A8-A0 Address Inputs are used to select a starting column location. The value at the A10 input determines whether Auto Precharge is activated. If Auto Precharge is selected, the row being accessed will be precharged at the end of the Write burst. If Auto Precharge is not selected, the row will remain active for subsequent accesses.

Burst Types and Lengths apply to Burst Write operation in the same manner as they do to Burst Read operations.

4.6 Precharge command

The Precharge command is used to close the open row in a particular bank, or the open rows in all the banks, depending on the value on the A10 Address Input. If A10 is High, at V_{IH}, when the Precharge command is issued, the command will be applied to all the banks, closing all the open rows in these banks. If A10 is Low, at V_{IL}, when the Precharge command is issued, the command will be applied only to the selected bank, closing the open row of this bank.

The Precharge command can also be used to terminate a Burst. Issued during a Burst Read or Burst Write cycle, the Precharge command will interrupt the Burst operation and close the active bank.

The precharge command can be issued any time after t_{RAS} min. is satisfied. Soon after the precharge command is issued, the precharge operation performed and the synchronous DRAM enters the idle state after t_{RP} is satisfied. The t_{RP} parameter is the time required to perform the precharge. The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is CL-1 clock cycles before the reference clock that indicates the last data word is valid (see *Figure 5*)

In order to write all data to the memory cell correctly, the asynchronous parameter t_{DPL} must be satisfied. The t_{DPL} (min.) specification defines the earliest time that a precharge command can be issued.

After the Precharge command is issued, a minimum time of t_{RP} is required before the bank(s) are available.

4.7 Auto Precharge command

The Auto Precharge command is used to close the open row in a specific bank after a Read or Write cycle. Read or Write with Auto Precharge is initiated if the A10 Address Input is High, at V_{IH}, when a Read or Write command is issued.

4.8 Burst Terminate command

The Burst Terminate command is used to terminate a Burst operation. A Burst operation can be interrupted by using the Precharge command (see the *Section 4.6: Precharge command* for details), or by issuing the Burst Terminate command. Issuing the Burst Terminate command during a Burst Read or Write cycle will terminate the burst while leaving the bank open.

4.9 Data Mask command

The Data Mask command is used to mask the Read or Write data. A Data Mask command issued during a Read cycle will disable the data outputs, switching them to the high-impedance state after a delay of two clock cycles. A Data Mask command issued during a Write cycle will disable the data inputs with no delay.

4.10 Clock Suspend command

The Clock Suspend command is used to interrupt the internal clock of the Low Power SDRAM. The command is controlled by the Clock Enable input, KE, which is High, V_{IH}, in normal access mode. The Clock Suspend command is issued by driving KE Low, V_{IL} thus freezing the internal clock and extending data Read and Write cycles.

4.11 Power-Down command

The Power-Down command is used to put the device in Power-Down mode where the operating current is reduced to the Standby current.

All banks must be precharged and a minimum time of t_{RP} must elapse before issuing the Power-Down command.

4.12 Auto Refresh command

The Auto Refresh command is used to put the device in Auto refresh mode (see *Section 3.5: Auto Refresh*).

4.13 Self Refresh command

The purpose of the Self Refresh command is used to put the device in Self Refresh mode to retain and refresh the data contained in the Low Power SDRAM memory array. In Self Refresh mode, the Low Power SDRAM runs Refresh cycles asynchronously.

The Self Refresh cycle is performed according to the Extended Mode Register settings:

- EMR3 to EMR4 bits configure the Refresh rate at which the memory array is refreshed to perform a Temperature Compensated Self Refresh.
- EMR0 to EMR2 configure the part of the memory array being refresh (Partial Array Self Refresh).

4.14 Deep Power-Down command

The Deep Power-Down command is used to switch the Low Power SDRAM to Deep Power-Down Mode. This mode provides maximum power reduction as it cuts the power of the entire memory array of the device. For more information on how the command is issued and its exit sequence, see *Section 3.7: Deep Power-Down*, *Figure 25: Deep Power-Down Entry AC Waveforms*, and *Figure 26: Deep Power-Down Exit AC Waveforms*.

Table 3. Commands(1)

Command	KEn-1	KEn	$\overline{E}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	UDQM	LDQM	A10	A9, A11	A0-A7	BA0-BA1	DQ0-DQ7	DQ8-DQ15
Mode Register Set(2)	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	Op Code				X	X
Extended Mode Register Set(2)	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	Op Code				X	X
Bank (Row) Active	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	Start Row Address			Bank Select	X	X
Word Read/Read with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Output Valid	
Upper Byte Read/Read with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Hi-Z	Output Valid
Lower Byte Read/Read with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Output Valid	Hi-Z
Word Write/Write with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Input Valid	
Upper Byte Write/Write with Auto Precharge							V_{IL}	V_{IH}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Hi-Z	Input Valid
Lower Byte Write/Write with Auto Precharge							V_{IH}	V_{IL}	V_{IL}/V_{IH} (3)	X	Start Column Address	Bank Select	Input Valid	Hi-Z
Write with Auto Precharge	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}			V_{IH}	X	Start Column Address	Bank Select	X	X

Table 3. Commands(1) (continued)

Command	KEn-1	KEn	$\overline{E}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	UDQM	LDQM	A10	A9, A11	A0-A7	BA0-BA1	DQ0-DQ7	DQ8-DQ15
Precharge All Banks	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	V_{IH}	X		X	X	X
Precharge Selected Bank	V_{IH}	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	X	X	V_{IL}	X		V	X	X
Burst Terminate	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X			X	X	X
Auto Refresh	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X			X	X	X
Self Refresh Entry	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X			X	X	X
Self Refresh Exit(4)	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X	X			X	X	X
			V_{IL}	V_{IH}	V_{IH}	V_{IH}			X			X	X	X
Power-Down Entry(5)(6)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X			X	X	X
			V_{IH}	X	X	X								
Power-Down Exit(5)(6)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	X			X	X	X
			V_{IH}	X	X	X								
Deep Power-Down Entry	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X			X	X	X
Deep Power-Down Exit	V_{IL}	V_{IH}	X				X	X	X			X	X	X
Clock Suspend Entry	V_{IH}	V_{IL}	X	X	X	X	X	X	X			X	X	X
Clock Suspend Exit	V_{IL}	V_{IH}	X	X	X	X	X	X	X			X	X	X
Data Mask / Output Enable	V_{IH}	X	X	X	X	X	V_{IL}	V_{IL}	X			X	X	X
Data Mask / Output Disable	V_{IH}	X	X	X	X	X	V_{IH}	V_{IH}	X			X	Hi-Z	Hi-Z

1. X = Don't Care V_{IL} or V_{IH}. V = Valid.
2. BA1 and BA0 must both be driven Low, V_{IL}, to issue the Mode Register Set command. BA1 and BA0 must be driven High, V_{IH} and Low, V_{IL}, respectively, to issue the Extended Mode Register Set Command.
3. To perform Read or Write operations with Autoprecharge, A10 must be held High, V_{IH}.
4. The Self Refresh mode is exited by asynchronously driving KE from Low to High.
5. The Power-Down mode is exited by asynchronously driving KE from Low to High.
6. Banks must be precharged before issuing a Power-Down command.

5 Register descriptions

5.1 Mode Register description

The Mode Register is used to select the $\overline{CAS}$ Latency (1, 2 or 3), the Burst Type (sequential, interleaved), and the Burst Length (1-, 2-, 4-, 8-Word width or full page).

It is loaded by issuing a Mode Register Set command that programs A0 to A11 address bits. The values placed on the address lines are then latched into the Mode Register. BA0-BA1 must be set to '0'.

See *Table 4: Mode Register Definition*, for more details.

Table 4. Mode Register Definition

Address Bits	Mode Register Bit	Register Description	Value	Bit Description
A11-A7	-	-	00000	
A6-A4	MR6-MR4	$\overline{CAS}$ Latency Bits	010	2 Clock Cycles
			011	3 Clock Cycles
			Other configurations reserved	
A3	MR3	Burst Type	0	Sequential
			1	Interleaved
A2-A0	MR2-MR0	Burst Length Bit	000	1 Word (A3 is Don't Care)
			001	2 Words (A3 is Don't Care)
			010	4 Words (A3 is Don't Care)
			011	8 Words (A3 is Don't Care)
			111	Full Page if A3 Low Reserved if A3 High
			Other configurations reserved	
BA1-BA0	-	-	00	

5.2 Extended Mode Register description

The Extended Mode Register is used to program Low Power self-refresh operation of the device (PASR, DS, TCSR). It is used to select the area of the memory array refreshed during Partial Array Self Refresh operations, and the driver strength.

It is loaded by issuing a Extended Mode Register Set command that programs A0 to A11 address bits. The values placed on the address lines are then latched into the Extended Mode Register. BA0 and BA1 must be set to ‘0’ and ‘1’ respectively.

See *Table 5: Extended Mode Register Definition*, for more details.

Table 5. Extended Mode Register Definition

Address Bits	Mode Register Bit	Register Description	Value	Bit Description
A11-A10	-	-	00	
A9	EMR9	Auto Temperature Compensated Self Refresh (ATCSR)	0	Enabled
			1	Reserved
A8-A7	-	-	00	
A6-A5	EMR6-EMR5	Driver Strength Bits	00	Full Strength
			01	1/2 Strength
			10	1/4 Strength
			11	1/8 Strength
A4-A3	EMR4-EMR3		00	
A2-A0	EMR2-EMR0	Self Refresh Area Bits	000	All Banks
			001	Two Banks (BA1=0)
			010	One Banks (BA0 and BA1 =0)
			Other configurations reserved	
BA1-BA0	-	-	10	

6 Maximum rating

Stressing the device above the ratings listed in *Table 6: Absolute Maximum Ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_J	Junction Temperature	–25	90	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.5	2.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.5	2.6	V
I_{OS}	Short Circuit Output Current	50		mA
PD	Power Dissipation	1		W

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 7: Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter[1][2]	M65KA128AL			Units
	Min	Typ	Max	
Supply Voltage (V_{DD})	1.65	1.8	1.95	V
Input/Output Supply Voltage (V_{DDQ})[3]	1.65	1.8	1.95	V
Junction Temperature (T_J)	–25		90	°C
Load Capacitance (C_L)		30		pF
Output Impedance (Z_0)		50		Ω
Input Rise/Fall Time (t_R, t_F)		1		ns
Input High Voltage (V_{IH})		1.6		V
Input Low Voltage (V_{IL})		0.2		V
Input and Output Timing Ref. Voltages		$V_{DDQ}/2$		V
Output Transition Timing Reference Voltages	$0.3V_{DDQ}$		$0.7V_{DDQ}$	V

1. All voltages are referenced to V_{SS} = 0V.
2. T_J = –25 to 90°C, f = 1MHz
3. V_{DDQ} must not exceed the level of V_{DD}.

Figure 3. AC Measurement I/O Waveform

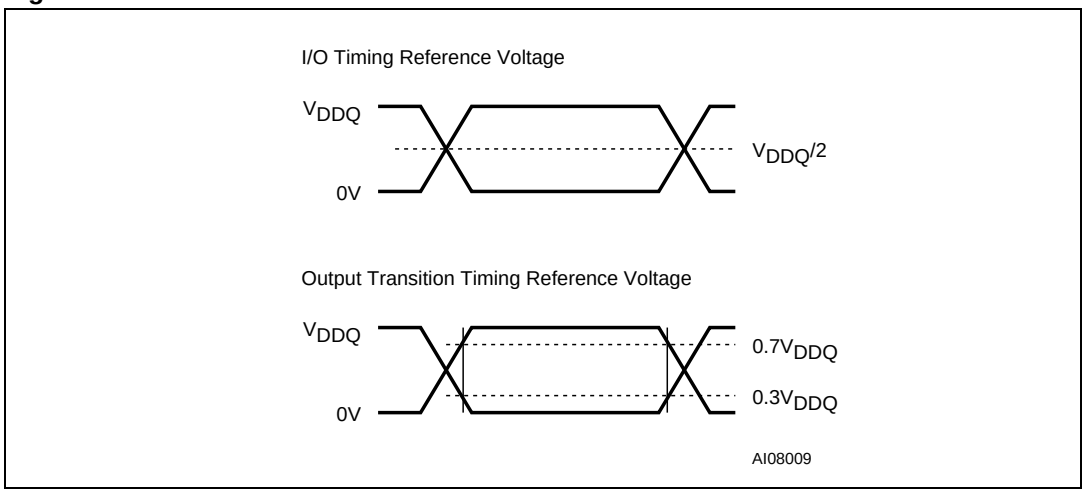
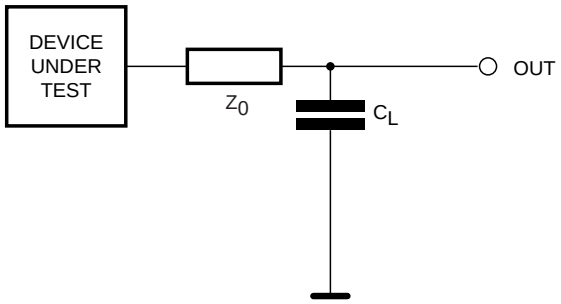


Table 8. AC Measurement Load Circuit



C_L includes probe capacitance

AI08008c

Table 9. Capacitance(1)(2)

Symbol	Parameter	Pin	M65KA128AL		Unit
			Min	Max	
C_{I1}	Input Capacitance	K	2.0	3.5	pF
C_{I2}		A0-A11, BA0, BA1, KE, $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, UDQM, LDQM	2.0	3.8	pF
C_{IO}	Data I/O Capacitance	DQ0-DQ15	6.0	7.5	pF

1. T_J = 25°C, f = 1MHz
2. Sampled only, not 100% tested.

Table 10. DC Characteristics 1

Symbol	Parameter	Test Condition(1)	M65KA128AL		Unit
			Min	Max	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le 1.8V$	–1	1	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le 1.8V$	–1.5	1.5	µA
V_{IL}	Input Low Voltage	V_{IN} = 0V	–0.3(3)	0.3	V
V_{IH}	Input High Voltage	V_{IN} = 0V	$0.8V_{DDQ}$	V_{DDQ} + 0.3(4)	V
V_{OL}	Output Low Voltage	I_{OUT} = 100µA, V_{IN} = 0V		0.2	V
V_{OH}	Output High Voltage	I_{OUT} = –100µA, V_{IN} = 0V	V_{DDQ} – 0.2		V

1. T_J = –25 to 90°C.
2. Data outputs are disabled.
3. V_{IL} may undershoot to -1.0V for less that 5ns.
4. V_{IH} may overshoot to 2.6V for less that 5ns.

Table 11. DC Characteristics 2

Symbol	Parameter	Test Condition(1)	Typ	Unit
I_{DD1}(2)	Operating Current	Burst length = 1, one bank active $t_{RC} \geq t_{RC}$(min), I_{OL} = 0mA	36	mA
I_{DD2P}	Standby Current in Power-Down Mode	KE ≤V_{IL}(max), t_{CK} = 15ns	0.6	mA
I_{DD2PS}		KE ≤V_{IL}(max), t_{CK} = ∞ Input signal stable	0.5	
I_{DD2N}	Standby Current in Non Power-Down Mode	KE ≥ V_{IH} (min), $\overline{E} \geq V_{IH}$ (min), t_{CK} = 15ns Input signals are changed once in 30ns	3	mA
I_{DD2NS}		KE ≥ V_{IH} (min), t_{CK} = ∞ Input signals are stable	1	
I_{DD3P}	Active Standby Current in Power-Down Mode	KE ≤V_{IL}(max), t_{CK} = 15ns	1	mA
I_{DD3PS}		KE ≤V_{IL}(max), t_{CK} = ∞	0.8	
I_{DD3N}	Active Standby Current in Non Power-Down Mode	KE ≥ V_{IH} (min), $\overline{E} \geq V_{IH}$ (min), t_{CK} = 15ns Input signals are changed once in 30ns	15	mA
I_{DD3NS}		KE ≥ V_{IH} (min), t_{CK} = ∞ Input signals are stable	5	
I_{DD4}(2)	Burst Mode Current, CL=2	$t_{CK} \geq t_{CK}$ (min), I_{OL} = 0mA All banks active	35	mA
	Burst Mode Current, CL=3		52	mA
I_{DD5}(3)(4)	Auto Refresh Current, CL=2	$t_{RC1} \geq t_{RC1}$(min)	65	mA
	Auto Refresh Current, CL=3			
I_{DD6}	Self Refresh Current	KE ≤0.2V	See *Table 12.*	µA
I_{DD7}	Standby Current in Deep Power-down Mode	See *Figure 25: Deep Power-Down Entry AC Waveforms*, and *Figure 26: Deep Power-Down Exit AC Waveforms*.	10	µA

1. T_J = –25 to 90°C.
2. I_{DD1} and I_{DD4} depend on the output loading and cycle rates. All measurements are made with the output open and on condition that the addresses are changed only once during t_{CK}(min.).
3. The minimum value of t_{RC} ($\overline{RAS}$ cycle time for Refresh operation) is shown in *Table 14: Asynchronous AC Characteristics*.
4. I_{DD5} is measured on condition that the addresses are changed only once during t_{CK} (min.).

Table 12. Self Refresh Current (I_{DD6}) Values in Normal Operating Mode(1)

Temperature	4 Banks		2 Banks		1 Bank		Unit
	Typ.	Max.	Typ.	Max.	Typ.	Max.	
T_J < 40°C		150		130		120	µA
40°C < T_J ≤70°C		200		170		150	µA
70°C ≤T_J ≤90°C		600		350		220	µA

1. V_{DD} = 1.8V, V_{DDQ} = 1.8V, V_{SS} = 0V, KE ≤0.2V.

Table 13. Synchronous AC Characteristics

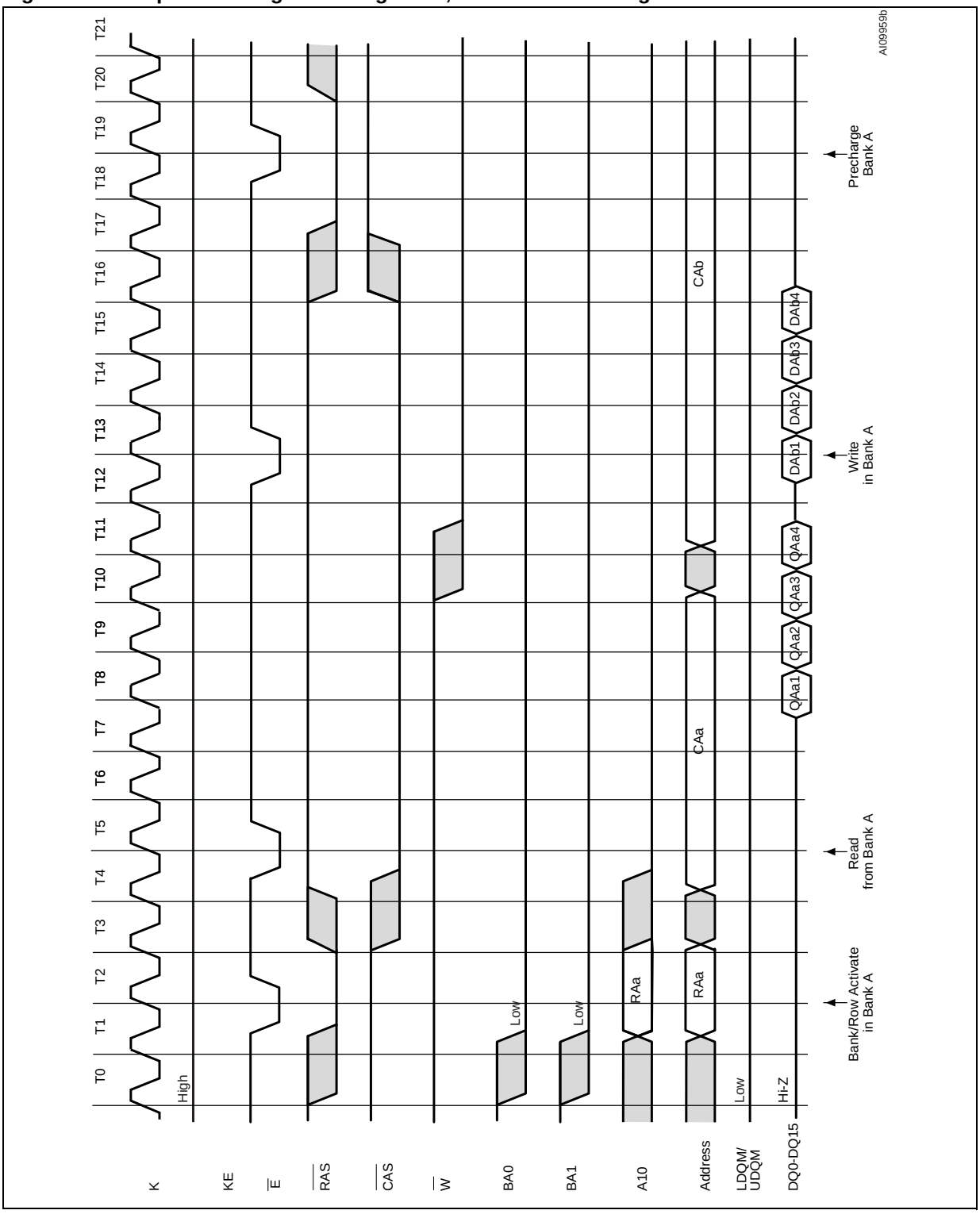
Symbol	Parameter	Test Condition	Min	Max	Unit
t_{AC}	Access Time From Clock	$\overline{CAS}$ Latency = 3		7	ns
		$\overline{CAS}$ Latency = 2		9	ns
t_{AS}	Address Setup Time		2		ns
t_{AH}	Address Hold Time		1		ns
t_{CK}	Clock Period	$\overline{CAS}$ Latency = 3	9.6		ns
		$\overline{CAS}$ Latency = 2	15		ns
t_{CS}	Command Setup Time		2		ns
t_{CH}	Command Hold Time		1		ns
t_{CHW}	Clock High Pulse Width		3		ns
t_{CLW}	Clock Low Pulse Width		3		ns
t_{CKS}	Clock Enable Setup Time		2		ns
t_{CKSP}	Clock Enable Setup Time (Power-Down Exit)		2		ns
t_{CKH}	Clock Enable Hold Time		1		ns
t_{DS}	Data Input Setup Time		2		ns
t_{DH}	Data Input Hold Time		1		ns
t_{OH}	Data Output Hold Time		3		ns
t_{OLZ}	Clock to Data Output Low-Z		0		ns
t_{OHZ}	Clock to Data Output High-Z	$\overline{CAS}$ Latency = 3	3	7	ns
		$\overline{CAS}$ Latency = 2	3	9	ns

Table 14. Asynchronous AC Characteristics

Symbol	Parameter		M65KA128AL		Unit(1)
			Min	Max	
t_{DPL}	Data Input Valid to Precharge Command		2		t_{CK}
t_{DAL}	Data Input Valid to Bank/Row Activate Command	$\overline{CAS}$ Latency = 3	2CLK + 28.5		ns
		$\overline{CAS}$ Latency = 2	2CLK + 30		ns
t_{DQZ}	UDQM or LDQM High to Data Output Hi-Z		2		t_{CK}
t_{DQM}	UDQM or LDQM High to Data Input Masked		0		t_{CK}
t_{MRD}	Mode Register Set Cycle Time		2		t_{CK}
t_{RC}	$\overline{RAS}$ Cycle Time		86		ns
t_{RCD}	Delay Time, $\overline{RAS}$ Active to $\overline{CAS}$ Active		28.5		ns
t_{RAS}	$\overline{RAS}$ Active Time		57	120,000	ns
t_{RP}	$\overline{RAS}$ Precharge Time		28.5		ns
t_{RRD}	Delay Time, $\overline{RAS}$ Active to $\overline{RAS}$ Bank Active		2		t_{CK}
t_{RC1}	Auto Refresh Exit Time		105		ns
t_{RC2}(2)	Self Refresh Exit Time		105		ns
t_{REF}	Refresh Time			64	ms
t_{τ}	Transition Time		1	30	ns
t_{WTL}	Delay Time, Write Command to Data Input		0		t_{CK}

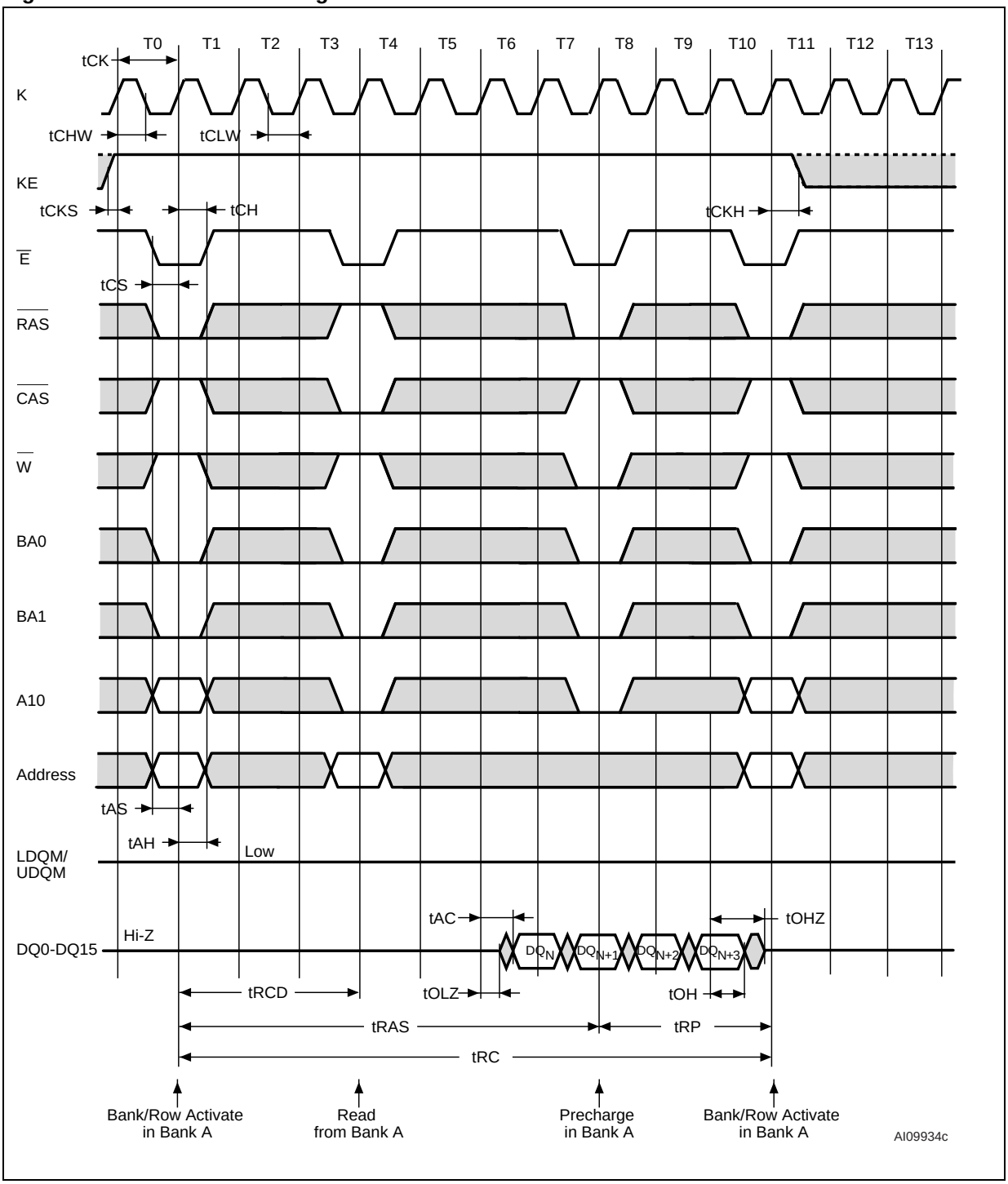
1. The unit t_{CK} is the system Clock cycle time.
2. A new command can be issued t_{RC} after the Self Refresh mode is exited.

Figure 4. Chip Enable Signal During Read, Write and Precharge



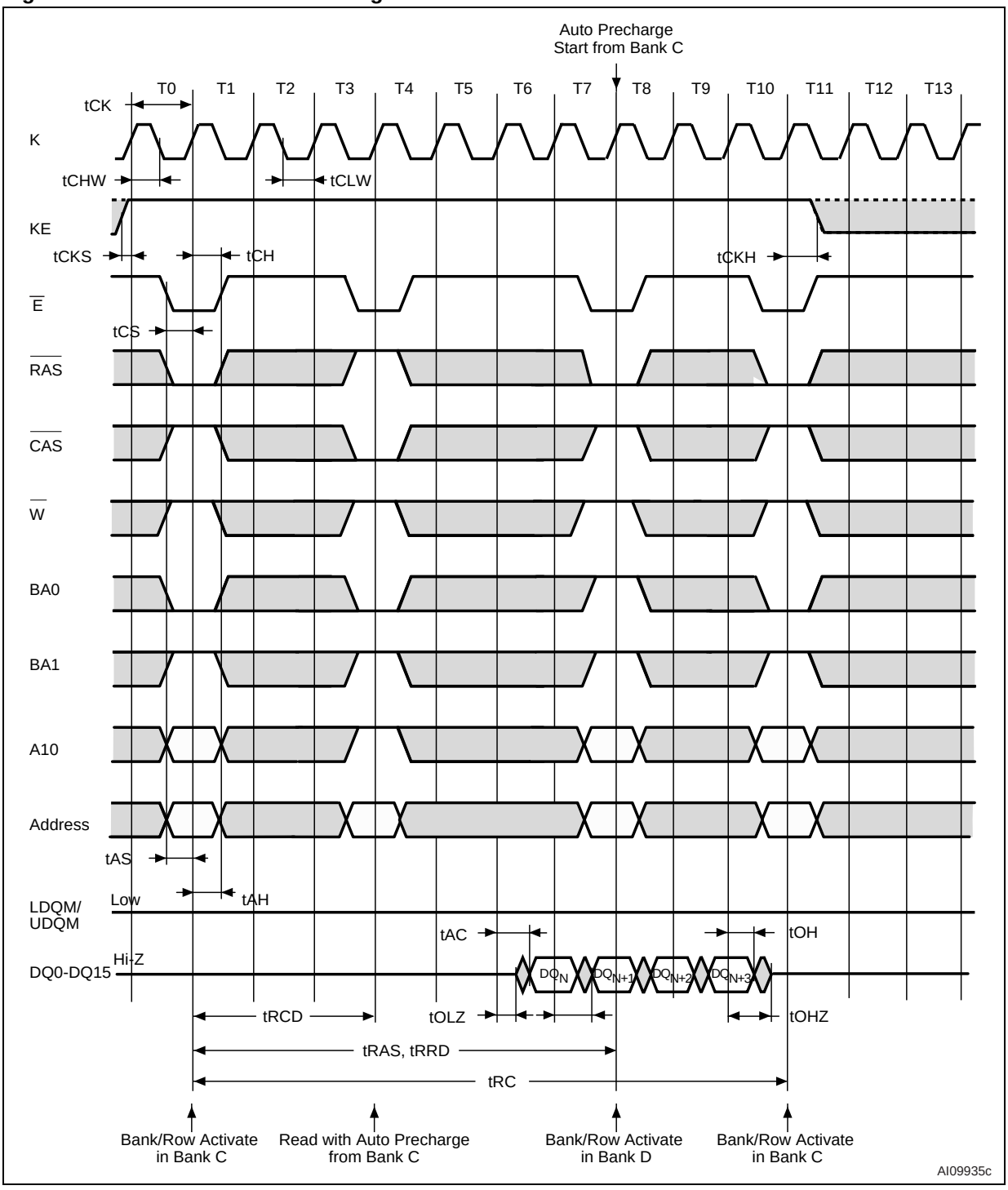
1. The Chip Enable signal, $\overline{E}$, must be issued at a minimum rate with respect to the other signals.
2. Burst Length = 4 Words, Latency = 3 clock cycles.
3. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A, DAan= Data n written to Column a in Bank A.

Figure 5. Read with Precharge AC Waveforms



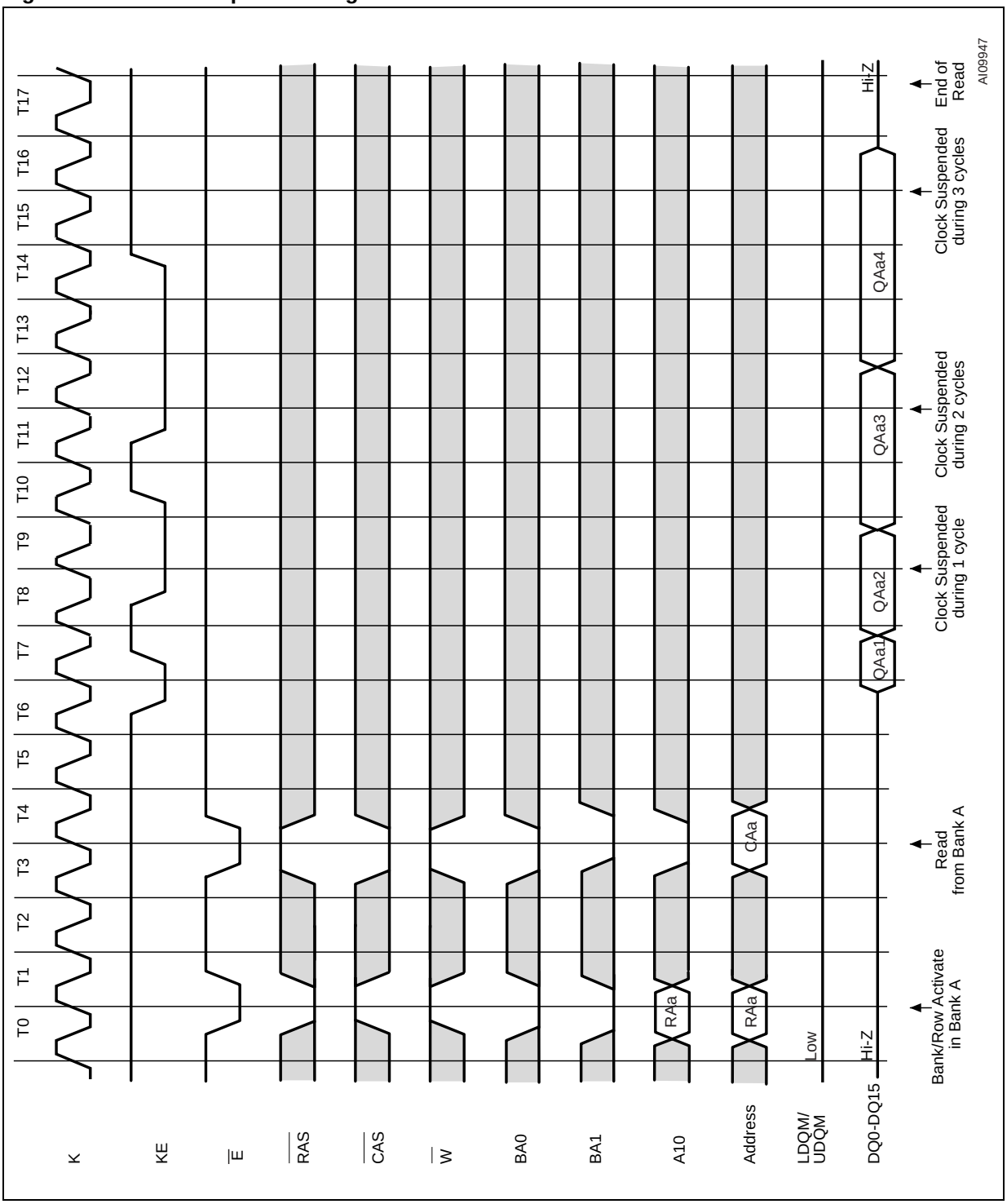
1. Burst Length = 4 Words, Latency = 3 clock cycles.

Figure 6. Read with Auto Precharge AC Waveforms



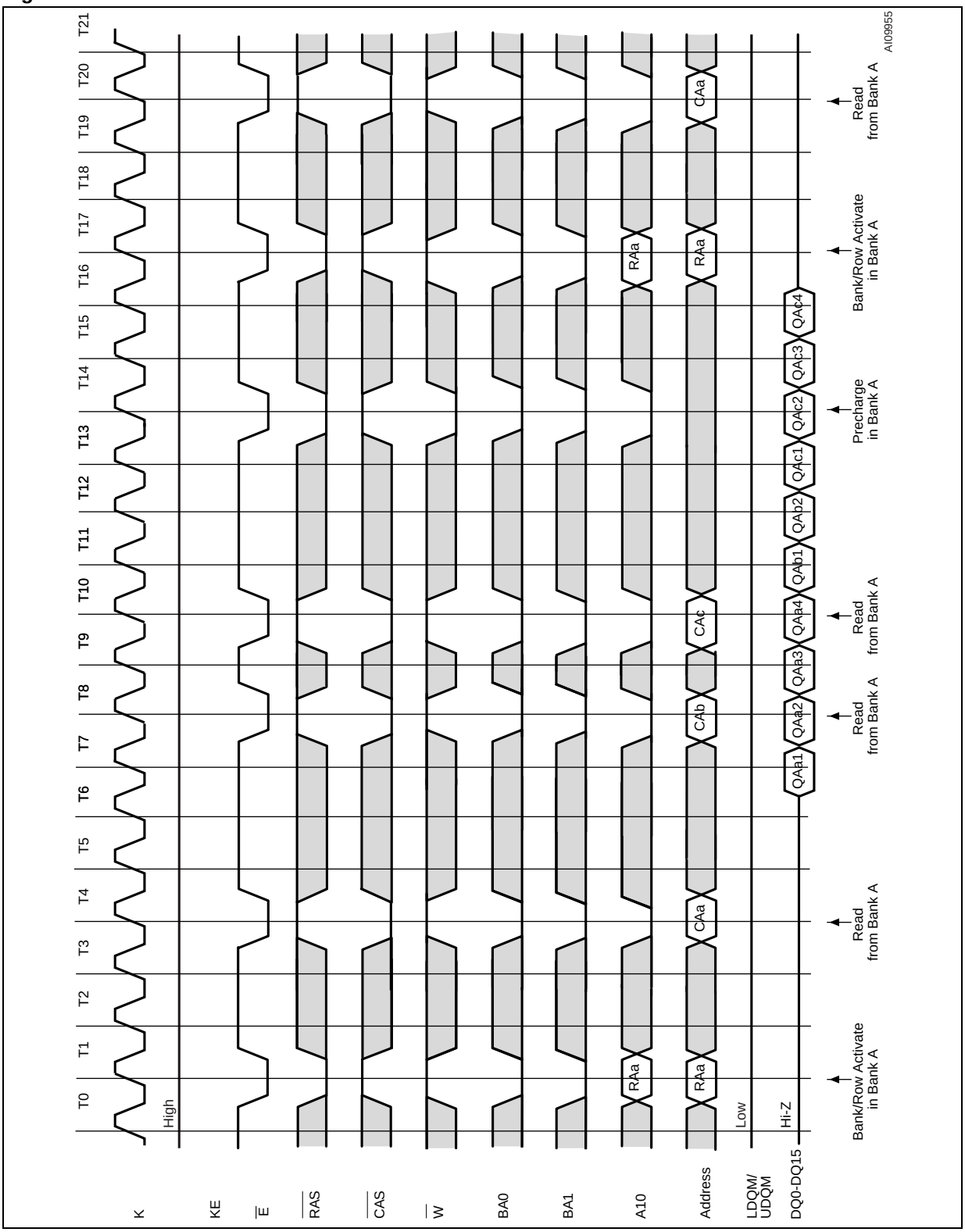
1. Burst Length = 4 Words, Latency = 3 clock cycles.

Figure 7. Clock Suspend During Burst Read AC Waveforms



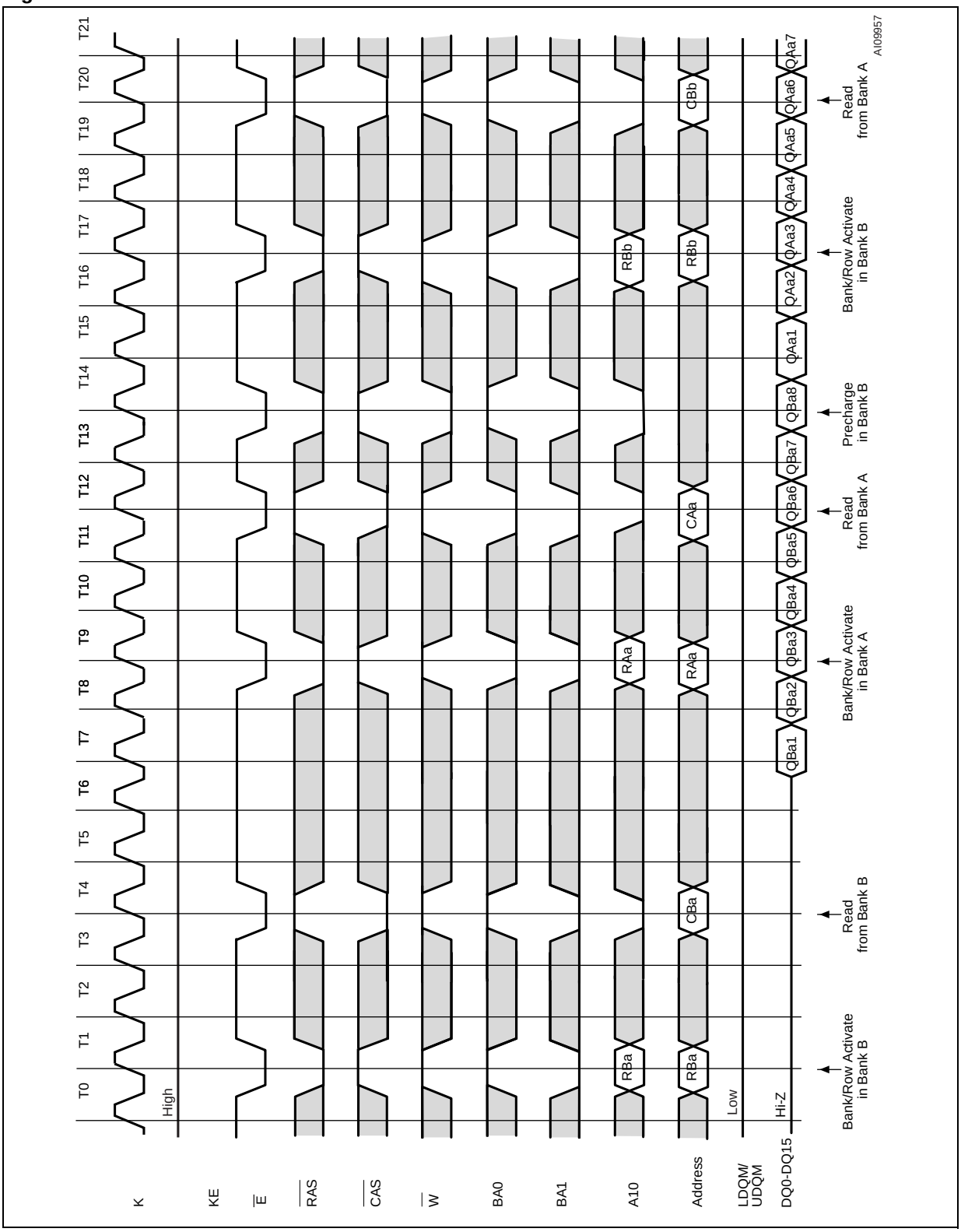
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A.

Figure 8. Random Column Read AC Waveforms



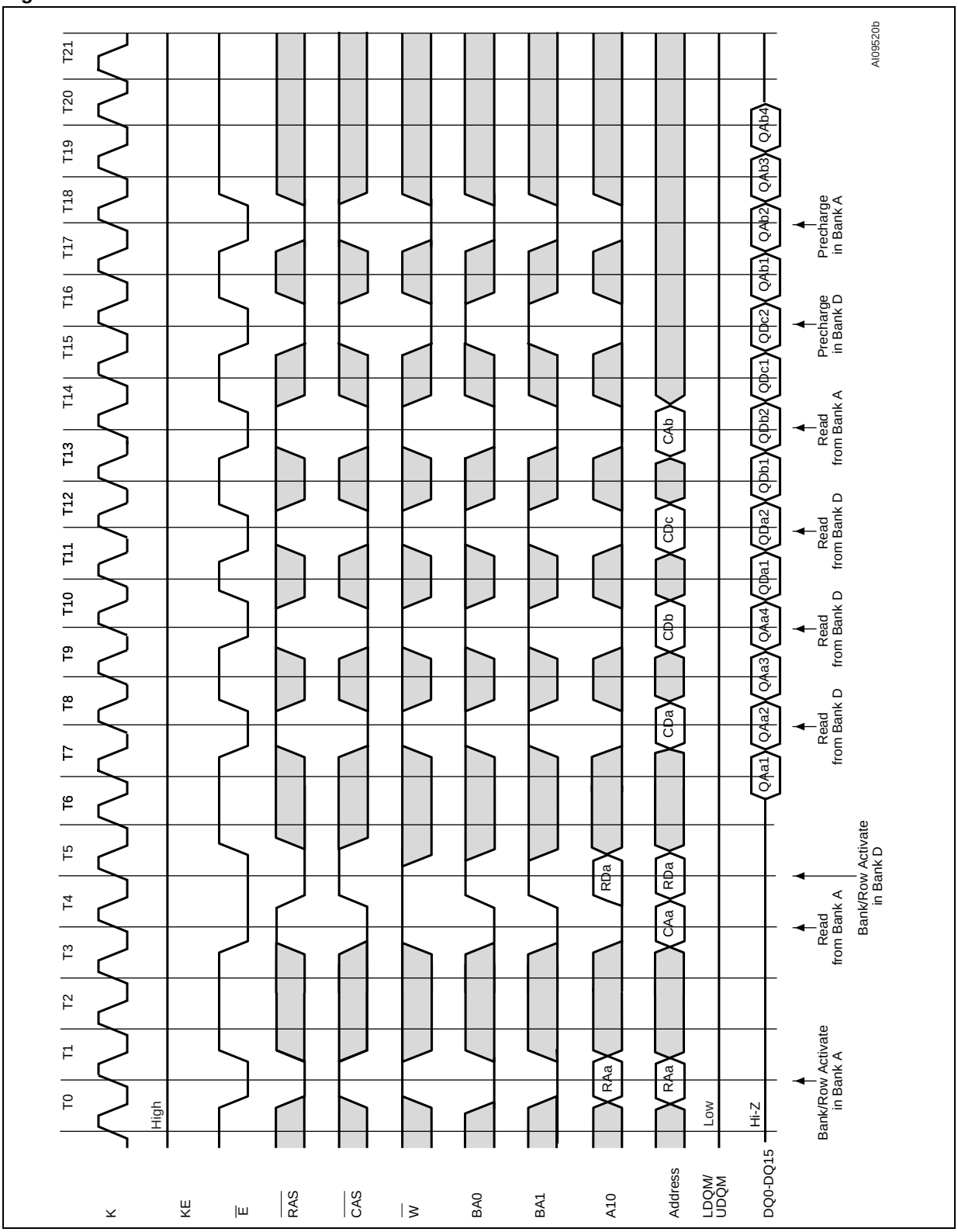
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from Column m in Bank A.

Figure 9. Random Row Read AC Waveforms



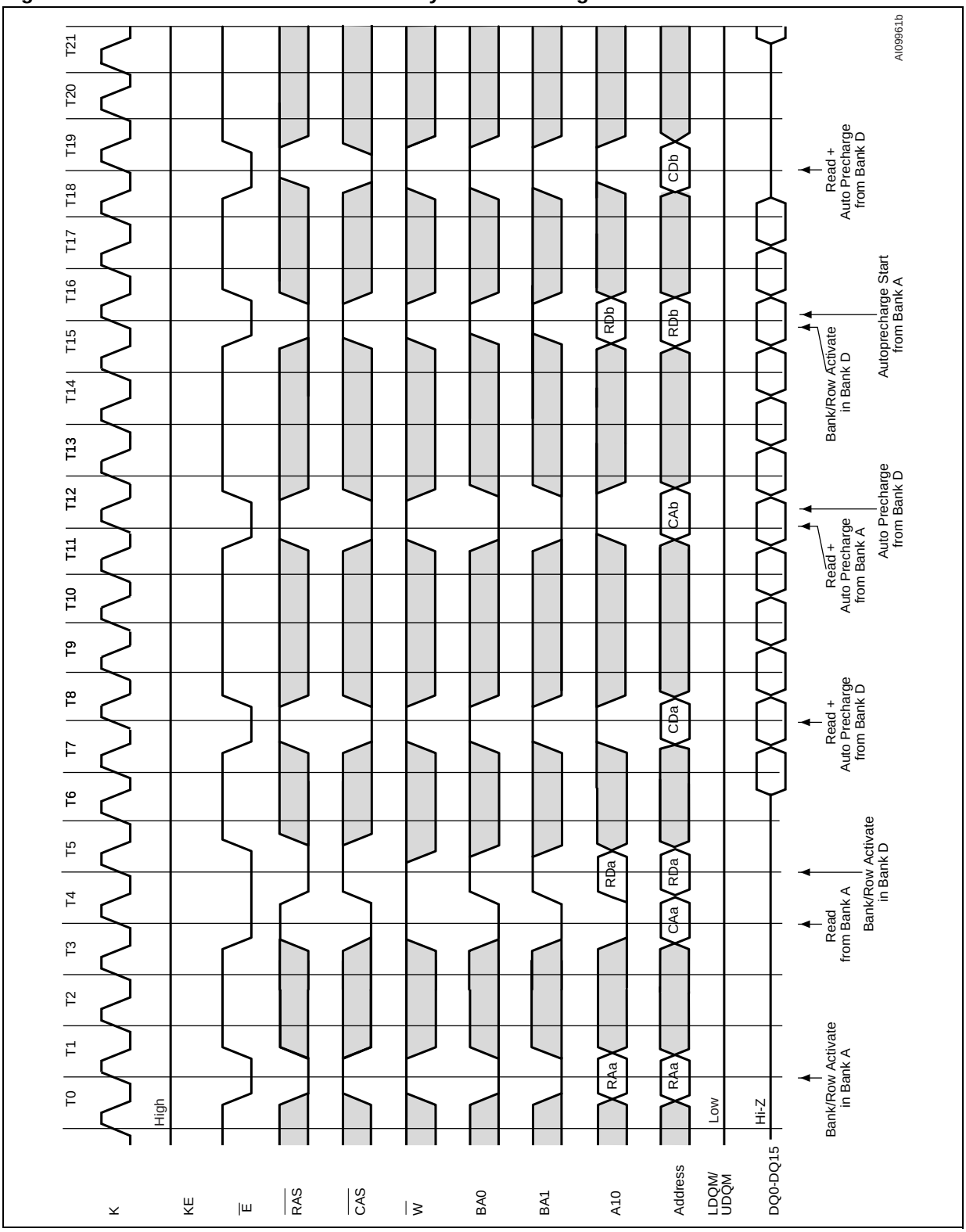
1. Burst Length = 8 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from row m in Bank A.

Figure 10. Column Interleaved Read AC Waveforms



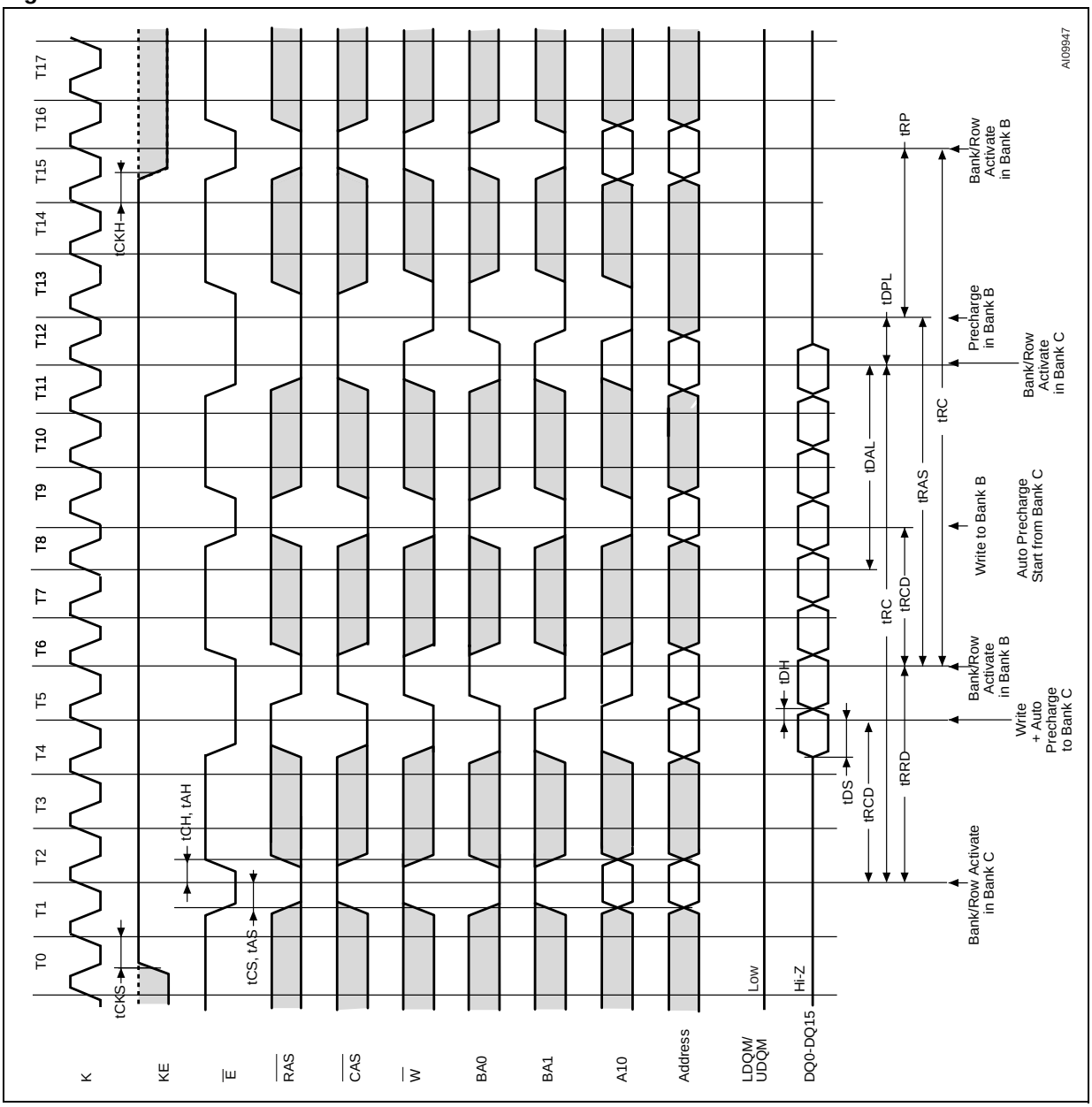
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAmn= Data n read from Column m in Bank A.

Figure 11. Burst Column Read Followed by Auto Precharge AC Waveforms



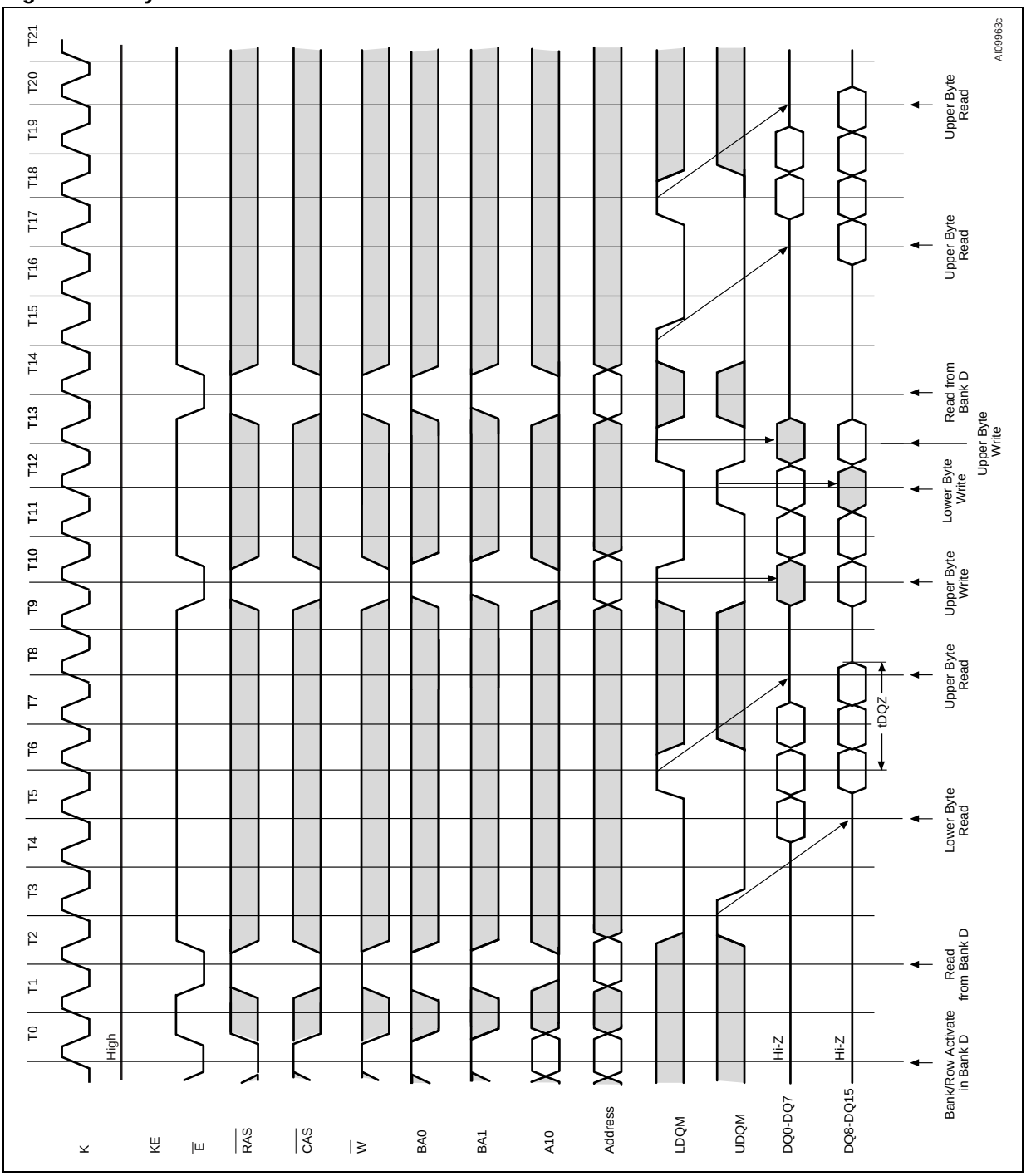
1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A.

Figure 12. Write AC Waveforms



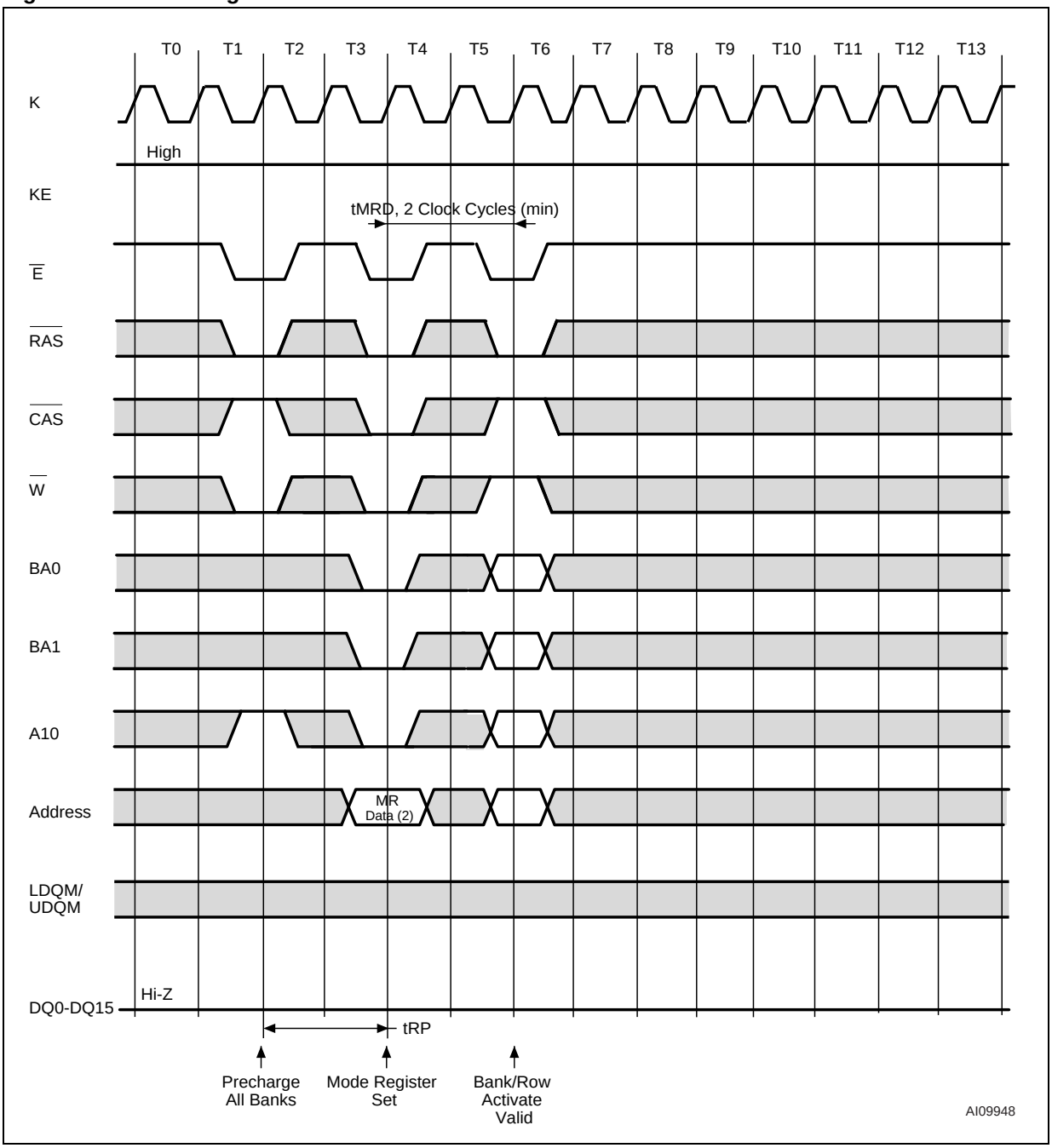
1. Burst Length = 4 Words.

Figure 13. Byte Write AC Waveforms



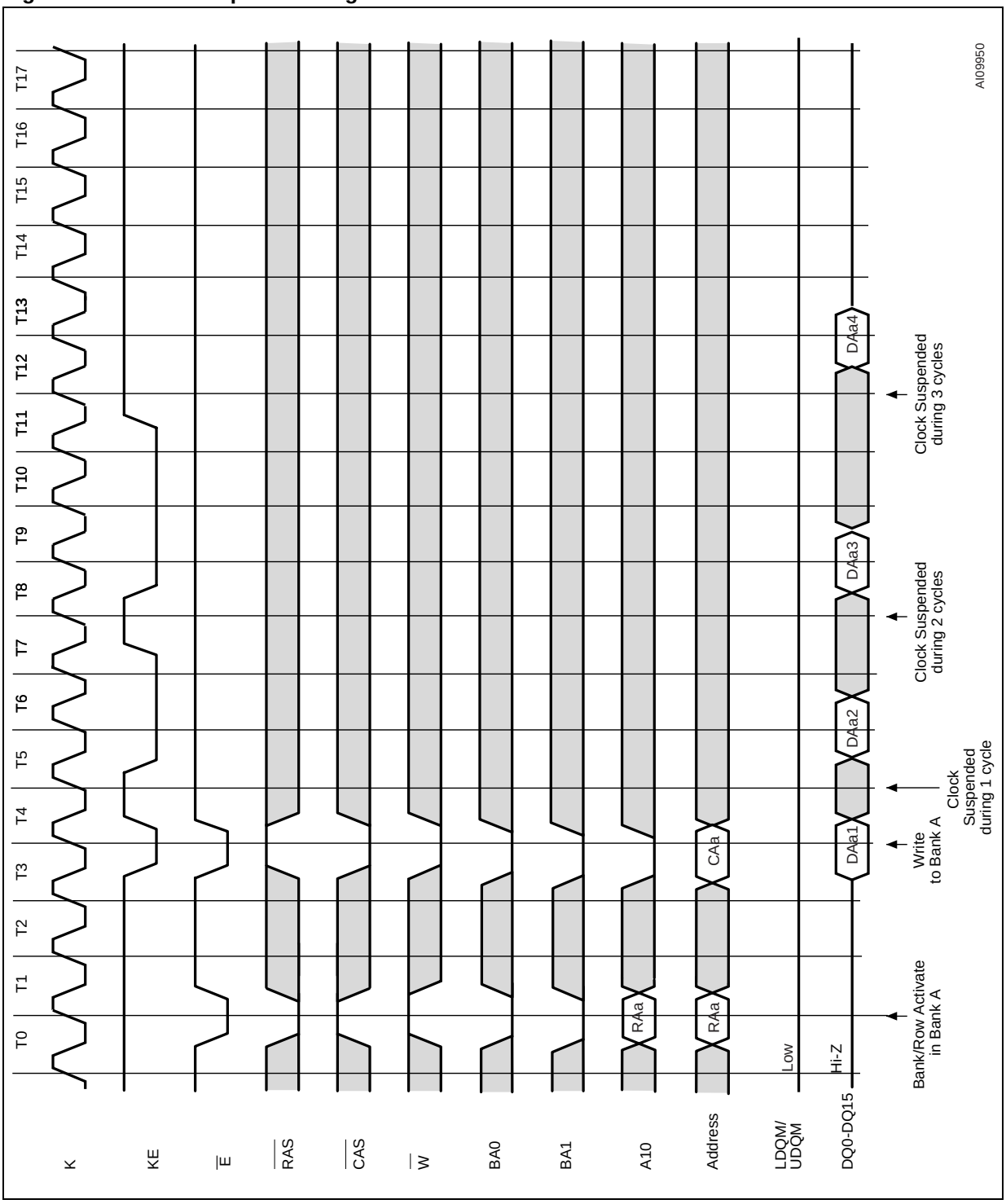
1. Burst Length = 4 Words.

Figure 14. Mode Register Set AC Waveforms



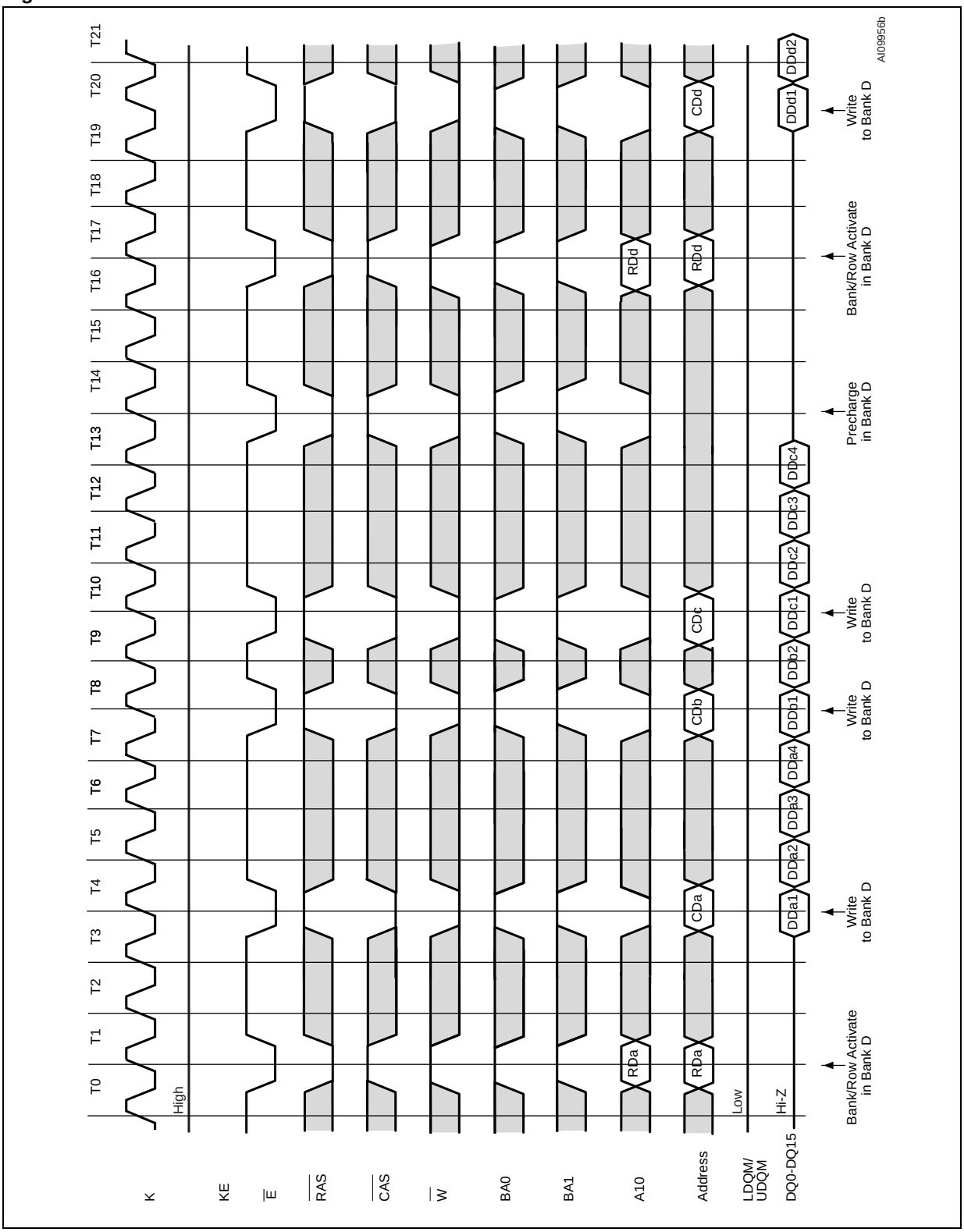
1. To program the Extended Mode Register, BA0 and BA1 must be set to ‘0’ and ‘1’ respectively, and A0 to A11 to the Extended Mode Register Data.
2. MR Data is the value to be written to the Mode Register.

Figure 15. Clock Suspend During Burst Write AC Waveforms



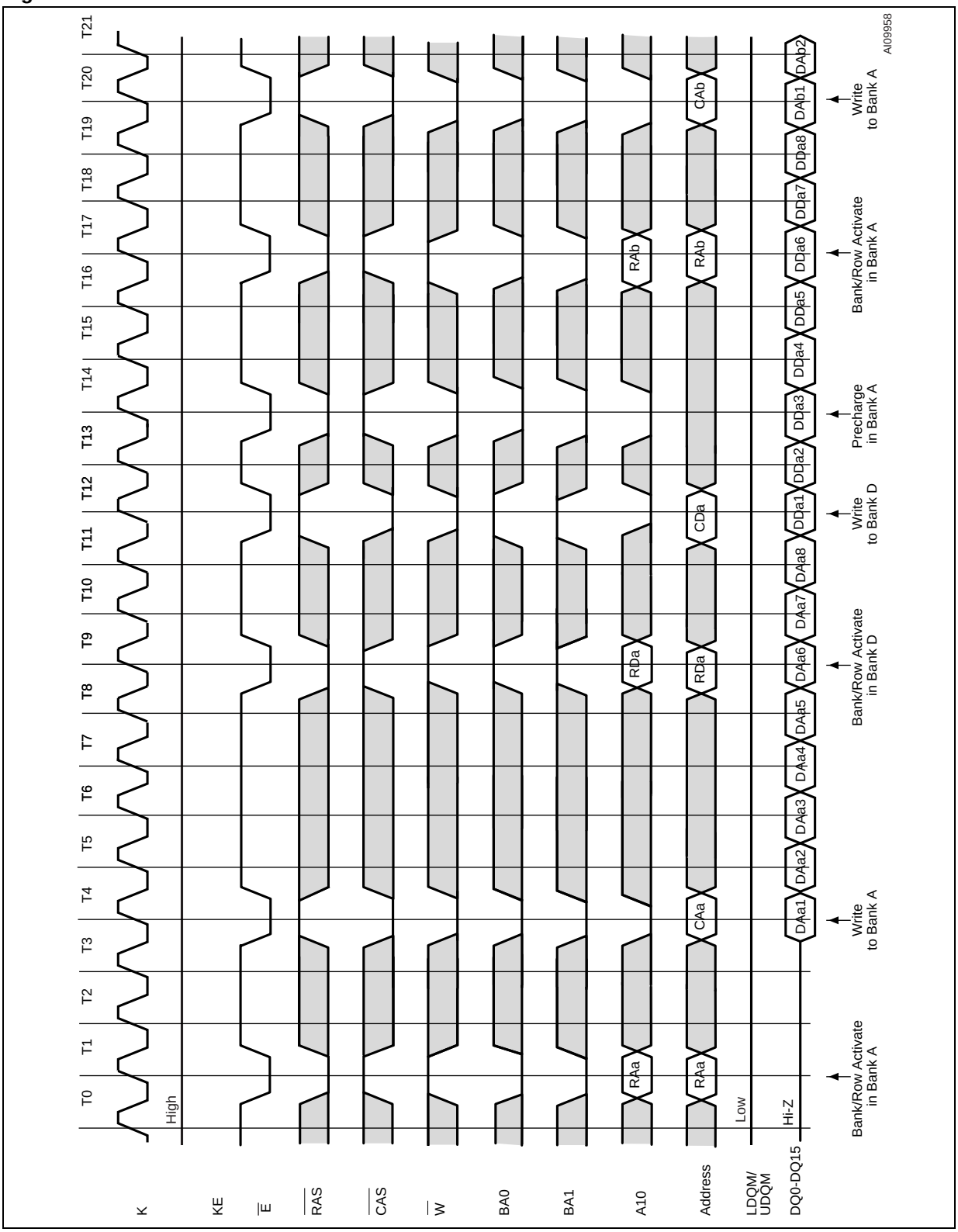
1. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAan= Data n Written to Column a in Bank A.

Figure 16. Random Column Write AC Waveforms



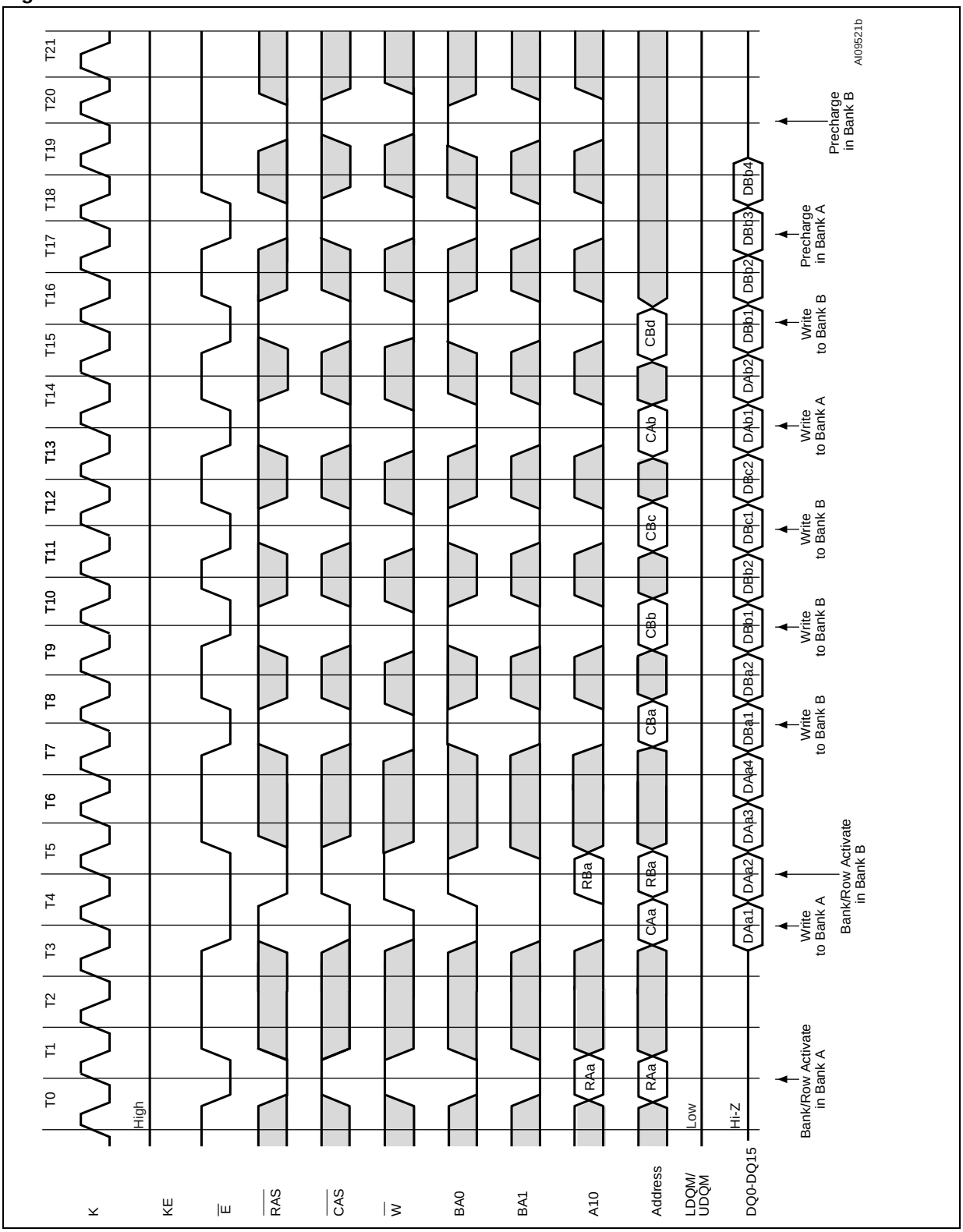
1. Burst Length = 4 Words.
2. RDa = Address of Row a in Bank D, CDa = Address of Column a in Bank D, DDmn= Data n written to Column m in Bank D.

Figure 17. Random Row Write AC Waveforms



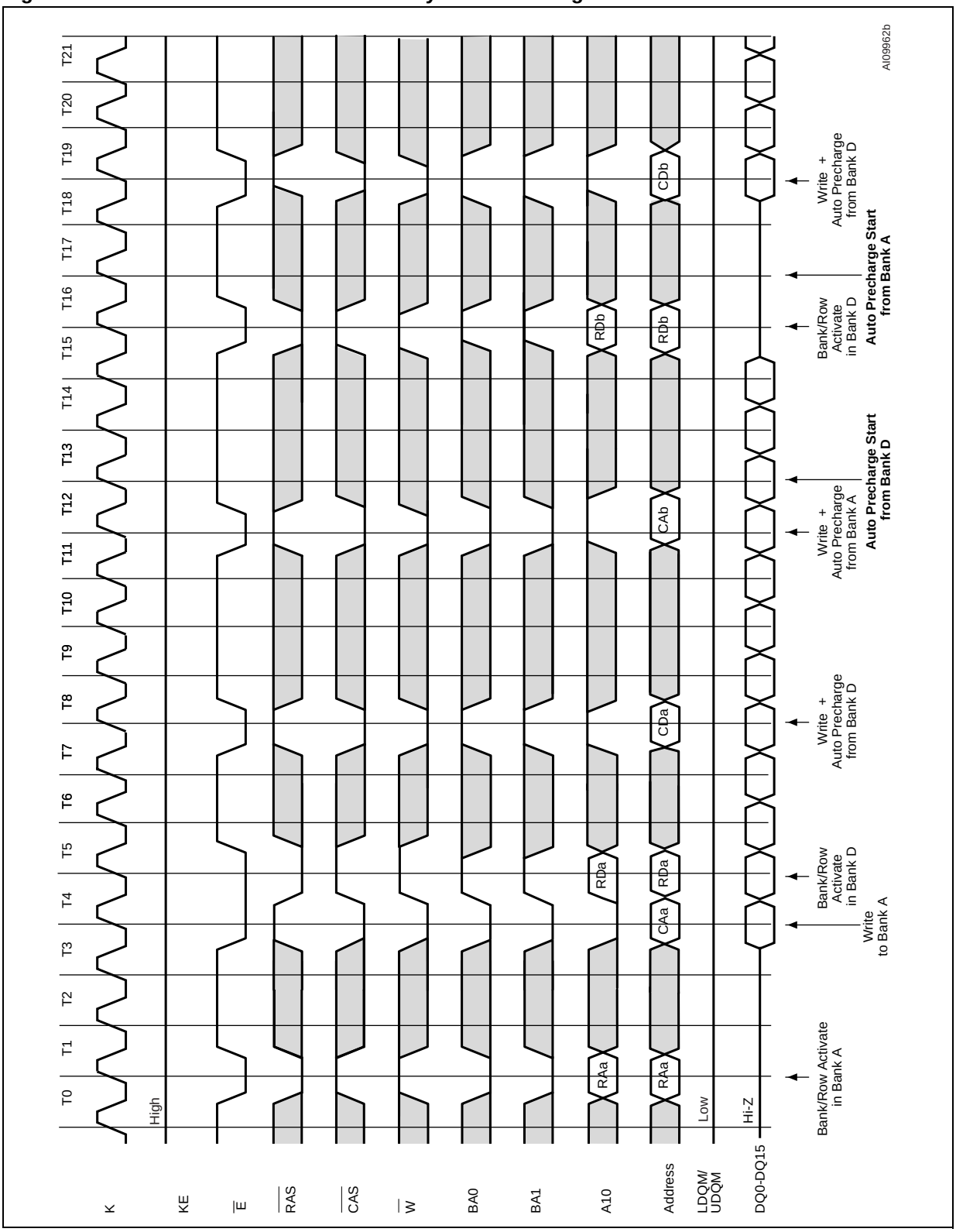
1. Burst Length = 8 Words.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAmn= Data n written to row m in Bank A.

Figure 18. Column Interleaved Write AC Waveforms



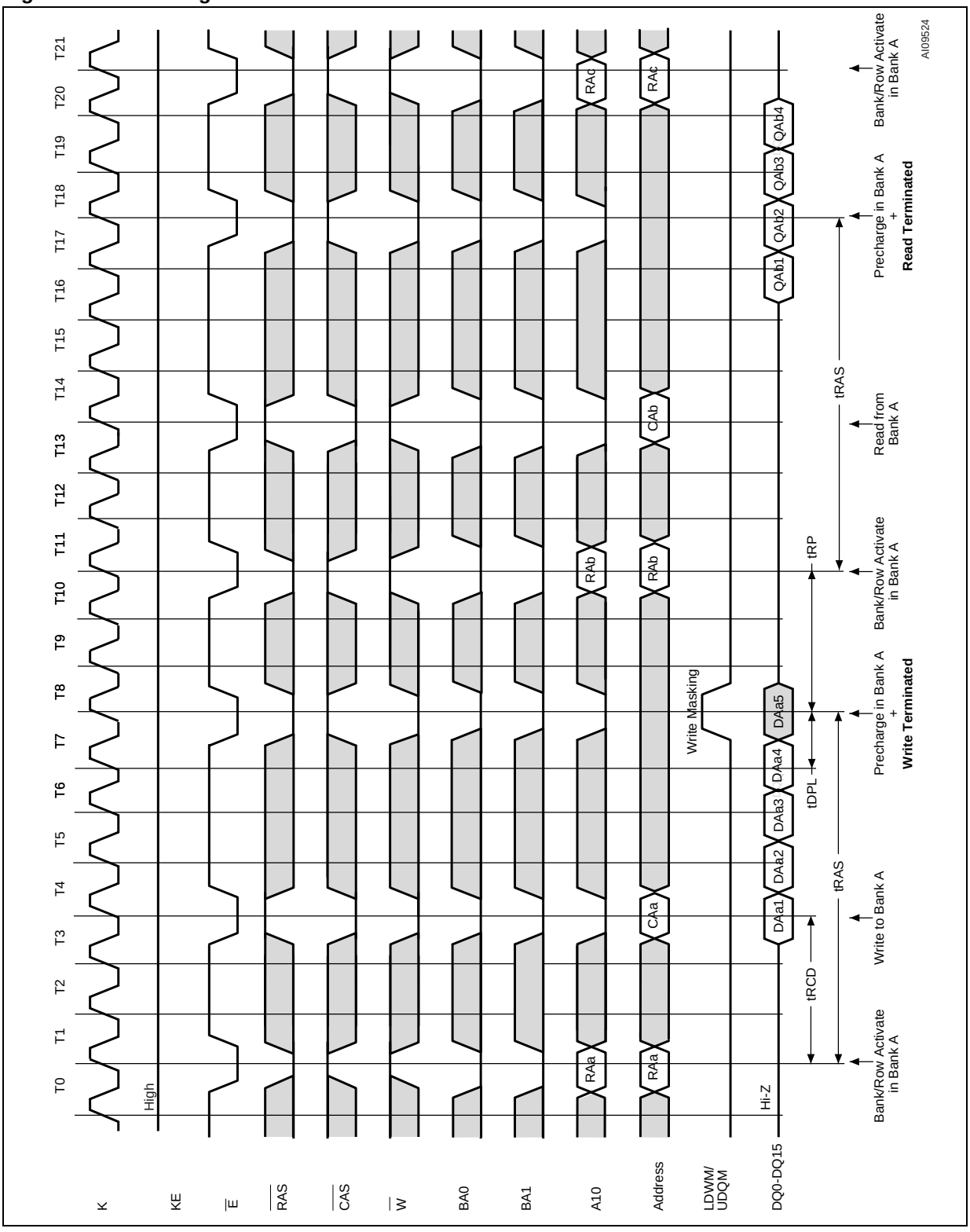
1. Burst Length = 4 Words.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, DAmn= Data n written to Column m in Bank A.

Figure 19. Burst Column Write Followed by Auto Precharge AC Waveforms



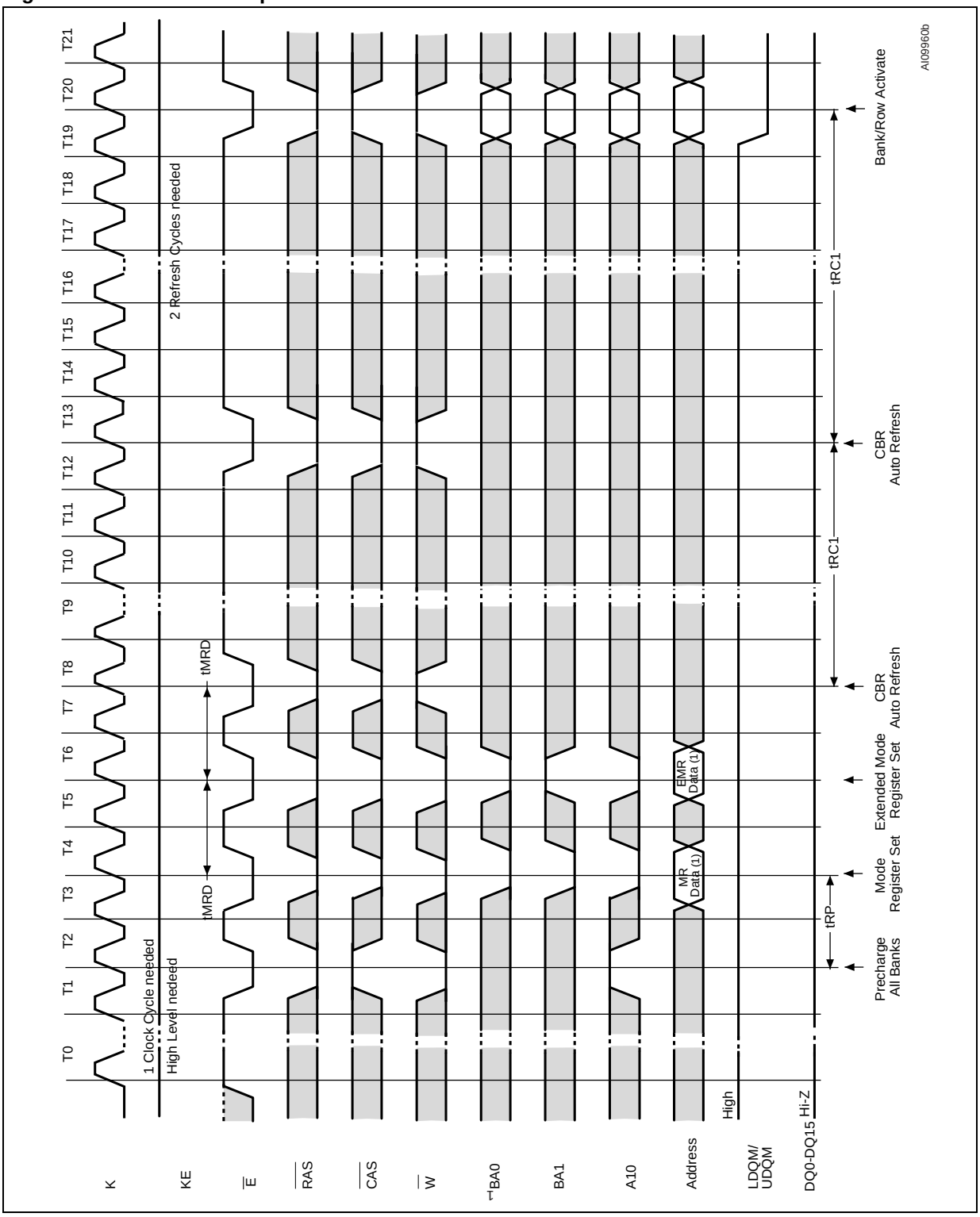
1. Burst Length = 4 Words
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A.

Figure 20. Precharge Termination



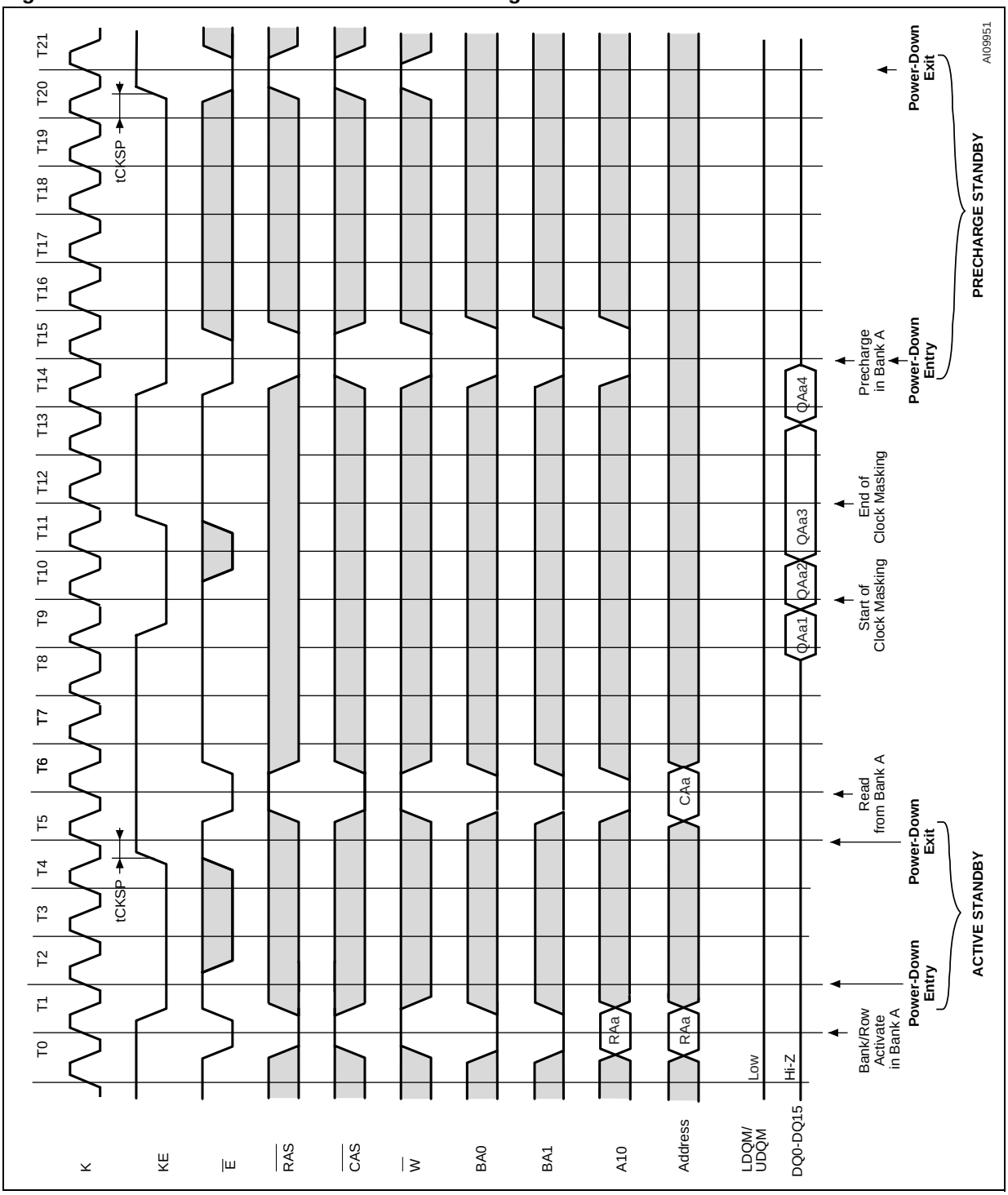
1. Burst Length = 8 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A, DAan= Data n written to Column a in Bank A.

Figure 21. Power-On Sequence



1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

Figure 22. Power-Down Mode and Clock Masking AC Waveforms



1. Burst Length = 4 Words, Latency = 3 clock cycles.
2. RAa = Address of Row a in Bank A, CAa = Address of Column a in Bank A, QAan= Data n read from Column a in Bank A.

Figure 23. Auto Refresh

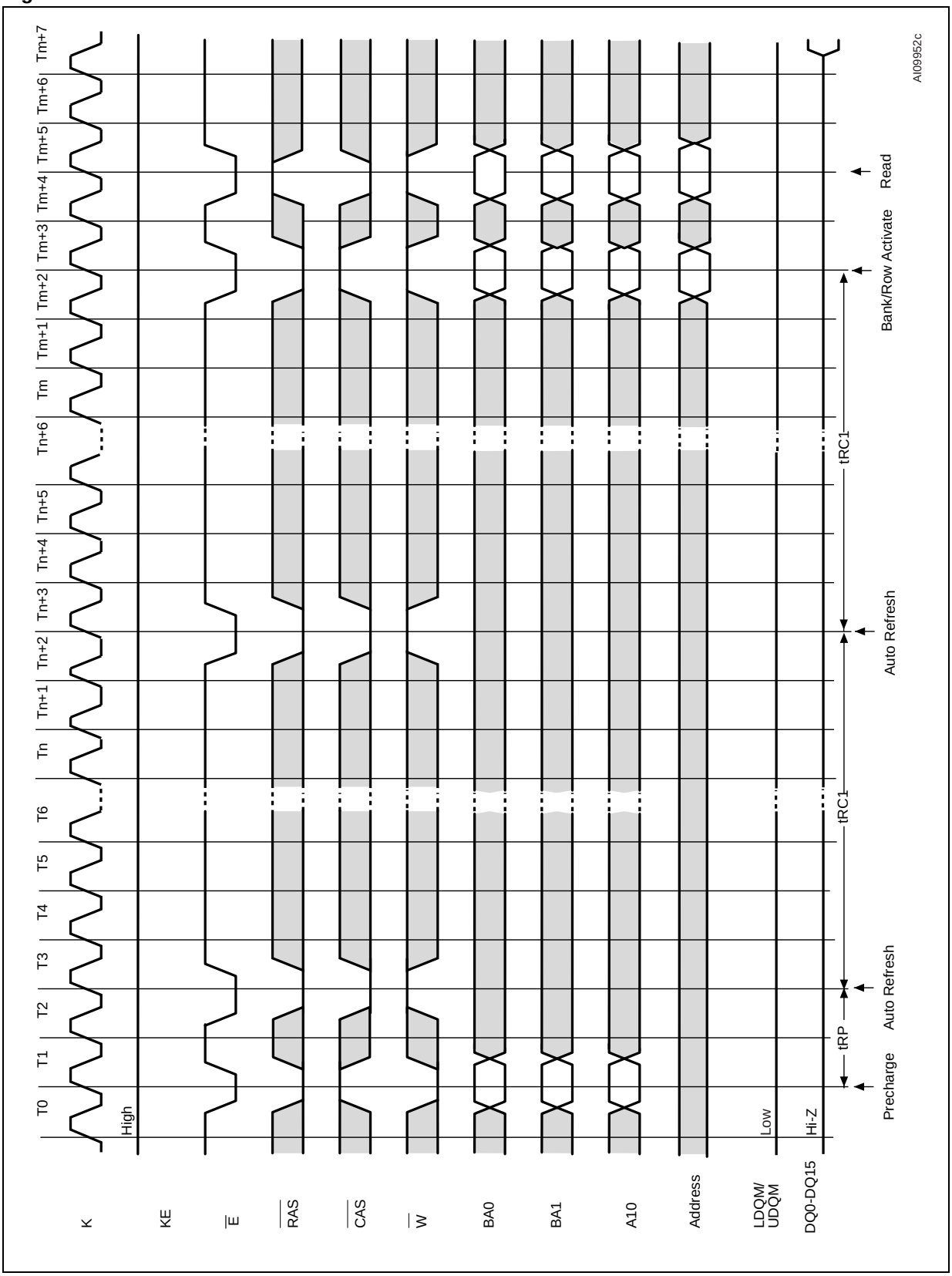


Figure 24. Self Refresh

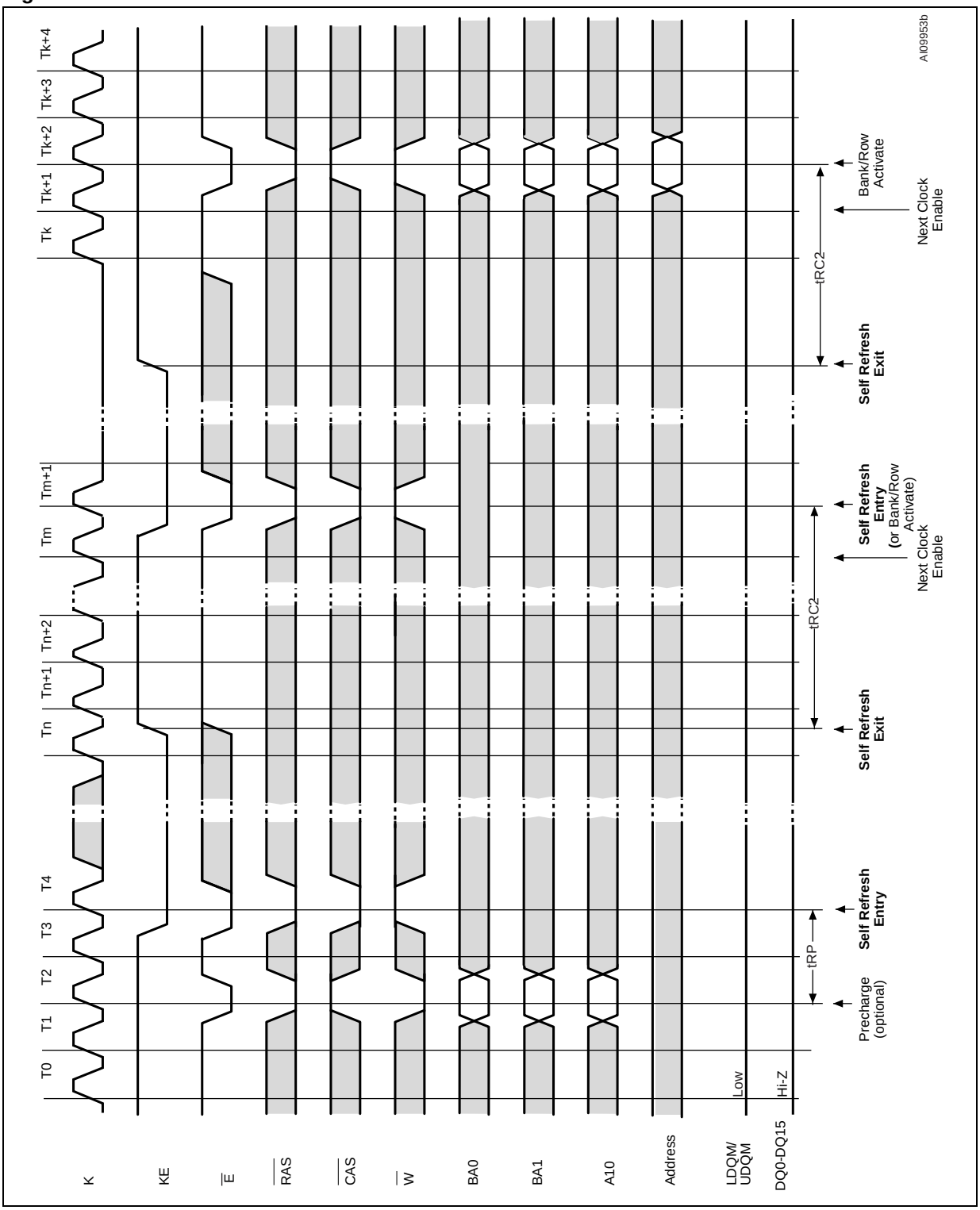
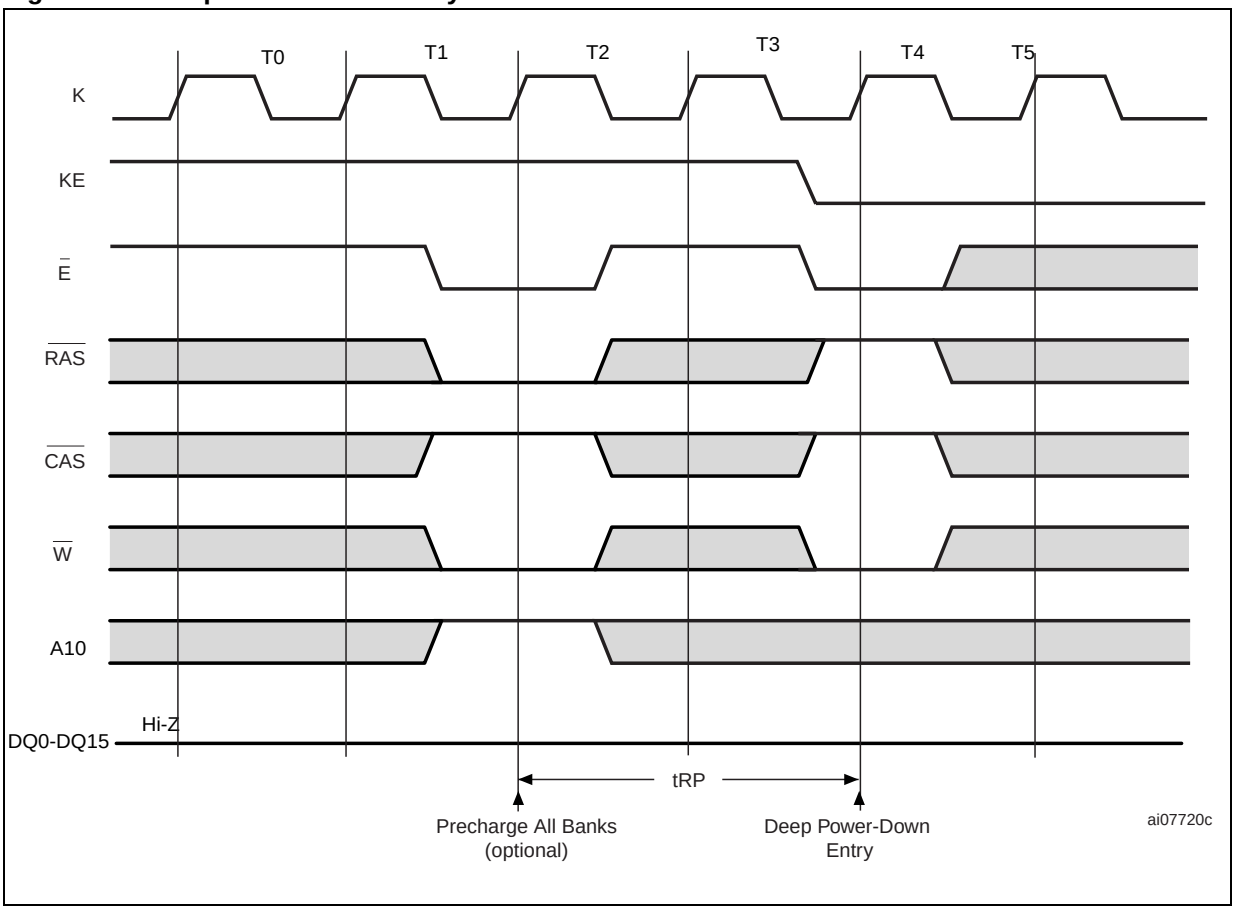
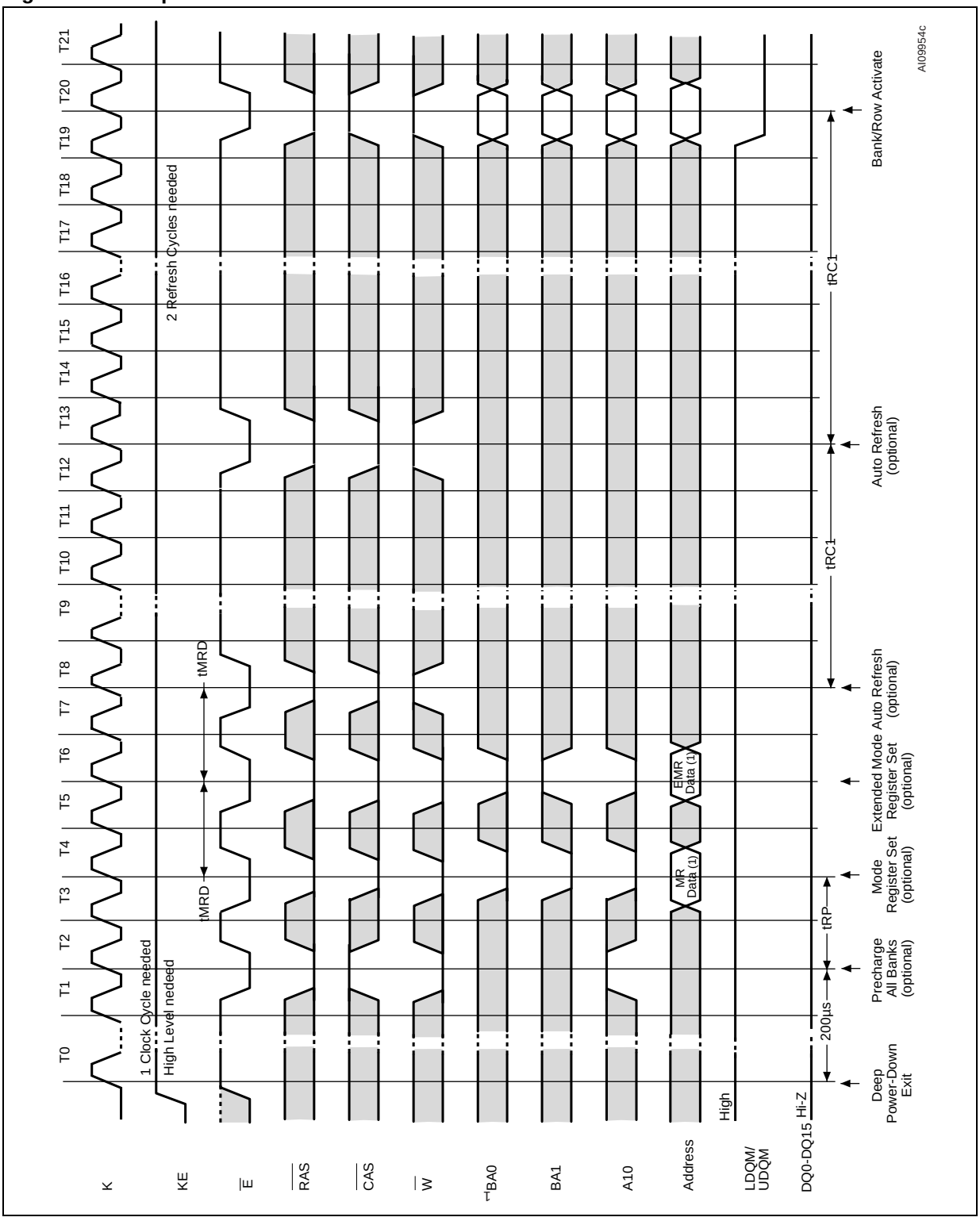


Figure 25. Deep Power-Down Entry AC Waveforms



1. BA0, BA1 and address bits A0 to A11 (except A10) are ‘Don’t Care’.

Figure 26. Deep Power-Down Exit AC Waveforms



1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

8 Part numbering

Table 15. Ordering Information Scheme

Example: M65KA128AL 10 W 5

Device Type

M65 = Low Power SDRAM

Delivery Form

K = Wafer Form

Operating Voltage, Mode, Bus Width

A = V_{DD} = V_{DDQ} = 1.8V, Standard LPSDRAM, x16

Array Organization

128 = 4 Banks x 2Mbit x 16

Option 1

A = One Chip Enable

Option 2

L = L Die

Speed Class

10 = 10ns

Package

W = Unsawn Wafer

Temperature Range

5 = –25 to 90°C

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

9 Revision history

Table 16. Document revision history

Date	Revision	Changes
28-Nov-2005	1	First Issue.
05-Jan-2006	2	Wafer and die specifications section removed.
28-Apr-2006	3	Datasheet status updated to Full Datasheet.

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