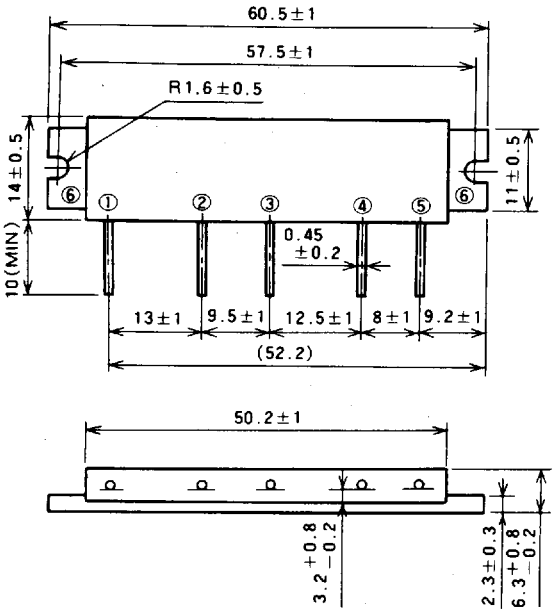
M67717

872~905MHz, 12.5V, 7W, FM MOBILE RADIO

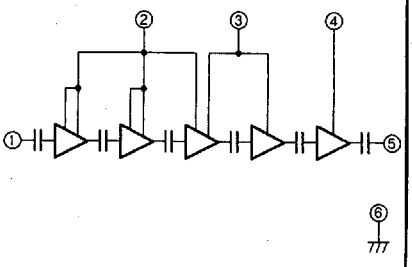
OUTLINE DRAWING

Dimensions in mm



H11

BLOCK DIAGRAM



PIN :
①Pin : RF INPUT
②Vcc1 : 1st. DC SUPPLY
③Vcc2 : 2nd. DC SUPPLY
④Vcc3 : 3rd. DC SUPPLY
⑤Po : RF OUTPUT
⑥GND : FIN

ABSOLUTE MAXIMUM RATINGS (Tc = 25℃ unless otherwise noted)

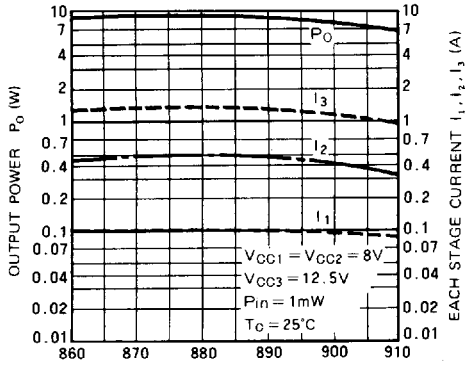
Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage		9	V
V_{CC2}			9	V
V_{CC3}			17	V
I_{CC}	Total current	$Z_G = Z_L = 50\,\Omega$	4	A
$P_{in(max)}$	Input power	$Z_G = Z_L = 50\,\Omega$, $V_{CC1} \leq 12.5V$	7	mW
$P_{O(max)}$	Output power	$Z_G = Z_L = 50\,\Omega$	10	W
$T_{C(OP)}$	Operation case temperature		−30~110	℃
T_{stg}	Storage temperature		−40~110	℃

ELECTRICAL CHARACTERISTICS (Tc = 25℃ unless otherwise noted)

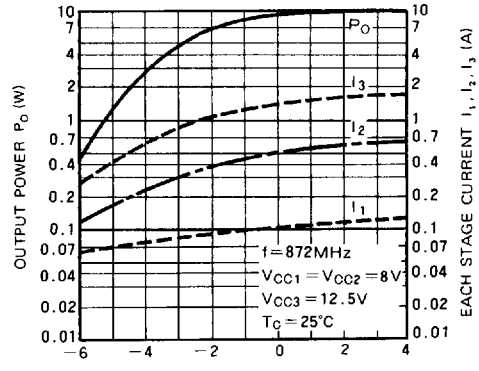
Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	$V_{CC1} = V_{CC2} = 8V$, $V_{CC3} = 12.5V$ $P_{in} = 1mW$ $Z_G = Z_L = 50\,\Omega$	872	905	MHz
P_O	Output power		7		W
η_T	Total efficiency		35		%
2fo	2nd. harmonic			−30	dB
ρ_{in}	Input VSWR			2.8	—
—	Load VSWR tolerance	$V_{CC1} = V_{CC2} = 8V$, $V_{CC3} = 15.2V$ $P_O = 7W$ (P_{in} : controlled), $Z_G = 50\Omega$ Load VSWR=20:1(All phase), 5sec.	No degradation		—

TYPICAL PERFORMANCE DATA

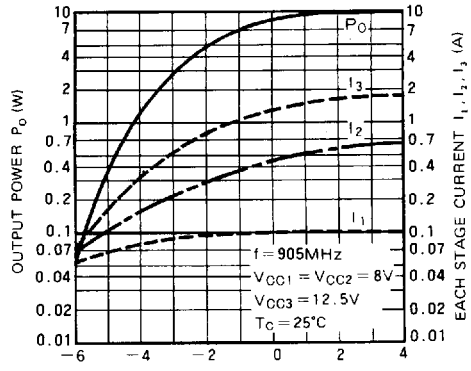
OUTPUT POWER, EACH STAGE CURRENT VS. FREQUENCY



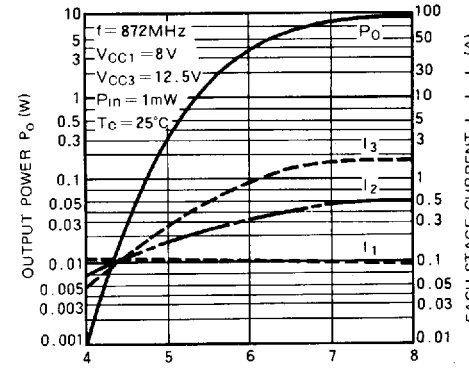
OUTPUT POWER, EACH STAGE CURRENT VS. INPUT POWER



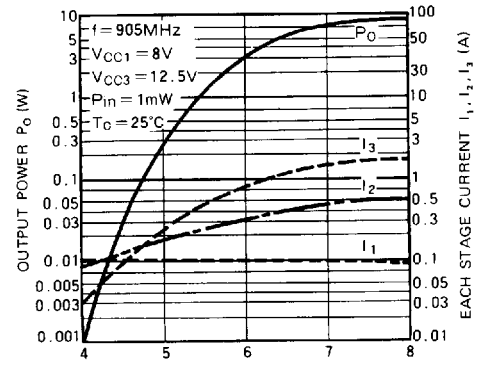
OUTPUT POWER, EACH STAGE CURRENT VS. INPUT POWER



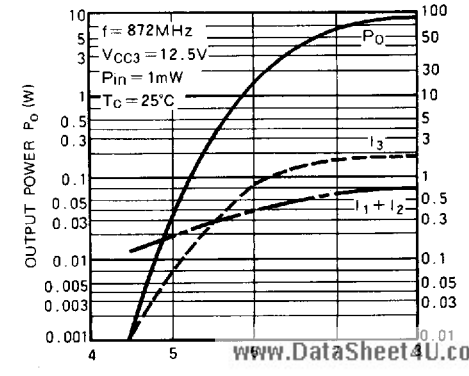
OUTPUT POWER, EACH STAGE CURRENT VS. 2nd STAGE DC SUPPLY VOLTAGE



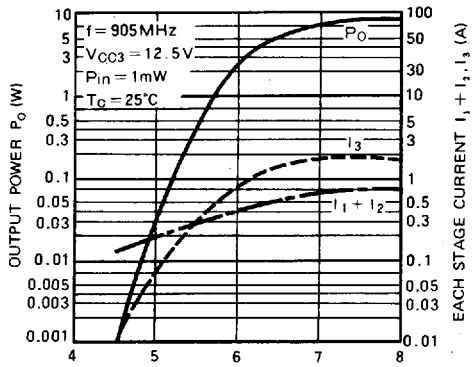
OUTPUT POWER, EACH STAGE CURRENT VS. 2nd STAGE DC SUPPLY VOLTAGE



OUTPUT POWER, EACH STAGE CURRENT VS. 1st AND 2nd STAGE DC SUPPLY VOLTAGE



OUTPUT POWER, EACH STAGE CURRENT VS. 1st AND 2nd STAGE DC SUPPLY VOLTAGE



1st & 2nd STAGE DC SUPPLY VOLTAGE $V_{CC1} = V_{CC2}$ (V)

DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to the following consideration when designing a heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistances between junction of incorporated transistors and case are shown in the followings.

a) First stage transistor
$R_{th(j-c)1} = 20°C/W$ (Typ.)

b) Second stage transistor
$R_{th(j-c)2} = 17.5°C/W$ (Typ.)

c) Third stage transistor
$R_{th(j-c)3} = 16°C/W$ (Typ.)

d) Fourth stage transistor
$R_{th(j-c)4} = 9°C/W$ (Typ.)

e) Final stage transistor
$R_{th(j-c)5} = 6.5°C/W$ (Typ.)

(2) V_{CC}, I_T, RF input & output power conditions at standard operation for each stage transistors are estimated as follows.

P_O = 7W, $V_{CC1} = V_{CC2}$ = 8V, V_{CC3} = 12.5V, P_{in} = 1mW, η_T = 35% (minimum ratings),

I_{1+2} = 0.781A (Total current from 1st stage to 4th stage)

I_3 = 1.1A (Current of 5th stage)

The conditions at standard operation for each stage transistors are shown in Table 1.

- Junction temperature of the first stage transistor
$T_{j1} = (V_{CC1} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (Note 1)
$= (8 \times 0.045 - 0.02 + 0.001) \times 20 + T_C$
$= 6.8 + T_C$ (°C)

Note 1: Case temperature of device

- Junction temperature of the second stage transistor
$T_{j2} = (V_{CC1} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C$
$= (8 \times 0.08 - 0.2 + 0.02) \times 17.5 + T_C$
$= 8.1 + T_C$ (°C)

- Junction temperature of the third stage transistor
$T_{j3} = (V_{CC2} \times I_{T3} - P_{O3} + P_{O2}) \times R_{th(j-c)3} + T_C$
$= (8 \times 0.16 - 0.5 + 0.2) \times 16 + T_C$
$= 15.7 + T_C$ (°C)

- Junction temperature of the fourth stage transistor
$T_{j4} = (V_{CC2} \times I_{T4} - P_{O4} + P_{O3}) \times R_{th(j-c)4} + T_C$
$= (8 \times 0.496 - 2 + 0.5) \times 9 + T_C$
$= 22.2 + T_C$ (°C)

- Junction temperature of the final stage transistor
$T_{j5} = (V_{CC3} \times I_{T5} - P_O + P_{O4}) \times R_{th(j-c)5} + T_C$
$= (12.5 \times 1.1 - 7 + 2) \times 6.5 + T_C$
$= 56.9 + T_C$ (°C)

Table 1: The conditions at standard operation

Stage	V_{CC} (V)	I_T (mA)	P_{in} (mW)	P_O (mW)
1st	8	45	1	20
2nd	8	80	20	200
3rd	8	160	200	500
4th	8	496	500	2000
5th	12.5	1100	2000	7000

2. Heat sink design

In thermal design of heat sink, keep the case temperature below 90°C at output power P_O = 7W and ambient temperature = 60°C.

The thermal resistance $R_{th(c-a)}$ (Note 2) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(7/0.35 - 7 + 0.001)}$$

$= 2.31$ (°C/W)

Note 2: Including the contact thermal resistance between device and heat sink

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistor become;

T_{j1} = 97°C, T_{j2} = 99°C, T_{j3} = 106°C, T_{j4} = 113°C, T_{j5} = 147°C at T_a = 60°C, T_C = 90°C.

Since the annual average of ambient temperature is 30°C, junction temperatures of each transistor become;

T_{j1} = 67°C, T_{j2} = 69°C T_{j3} = 76°C, T_{j4} = 76°C, T_{j5} = 117°C

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175°C, application under fully derated condition is ensured.