Preliminary

M69899VP

1:16 2.488 Gbps Demultiplexer [with Differential Outputs]

DESCRIPTION

The M69899VP demultiplexer chip is an integrated deserialization SONET OC-48 (2.488 Gbps) interface device. The chip performs serial-to-parallel functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based ATM applications.
The merits of SOI (Silicon-On-Insulator) technology, such as low voltage operation, low substrate noise and good compatibility with standard CMOS technology, are fully utilized in the chip design to achieve low jitter and low power operation and small package outline of 64-pin PQFP.

FEATURES

- Single 1.8 V power supply
- Supports 2.488 Gbps (OC-48, STM-16)
- Complies with ITU-T G958 specifications
- 16-bit differential PECL interface
- Low power consumption
- Available in 64 PQFP
- Parity check function

APPLICATIONS

- SONET/SDH systems
- Fiber optic systems
- High-speed back plane interconnect and point-to-point data links

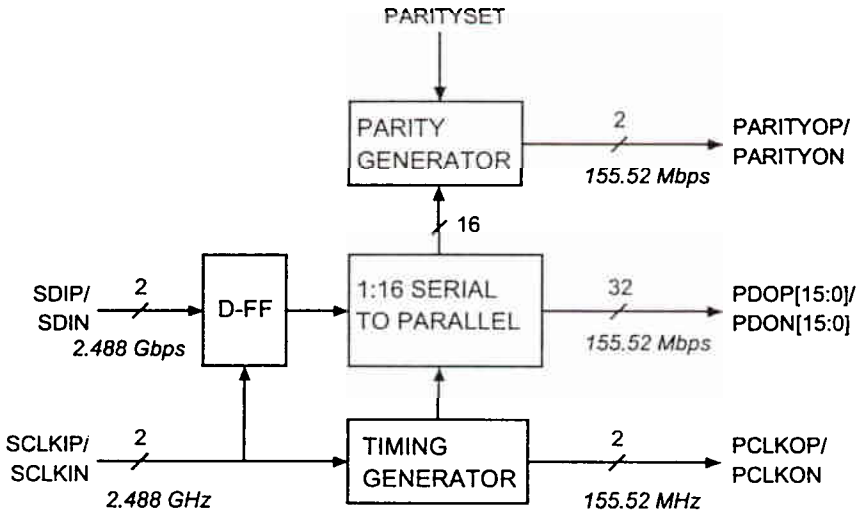

Figure 1 Functional Block Diagram

Table 1 Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNITS
Storage Temperature	-65		150	°C
Voltage on VDD with Respect to GND	-0.5		2.2	V
Voltage on any PECL Pin	0		2.2	V
ESD Rating (HBM model)	1000			V

Table 2 Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Ambient Temperature Under Bias	0		70	°C	
Junction Temperature Under Bias			110	°C	
Voltage on VDD with Respect to GND	1.71	1.8	1.89	V	
Power Consumption		280	340	mW	All Outputs Unterminated.
		430	550	mW	All Outputs Terminated.

Table 3 Differential PECL Input DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
VIL	Input Low Voltage	GND		VDD-1.4	V	
VIH	Input High Voltage	VDD-1.2		VDD-0.8	V	
ΔVINDIFF	Differential Input Voltage Swing	0.2		1.1	V	

Table 4 CMOS Input DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
VIL	Input Low Voltage	GND		VDD-1.3	V	
VIH	Input High Voltage	VDD-0.5		VDD	V	

Table 5 Differential PECL Output DC Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	CONDITIONS
VOL	Output Low Voltage	GND		0.1	V	
VOH	Output High Voltage	VDD-0.9		VDD-0.8	V	
ΔVOUTDIFF	Differential Output Voltage Swing	0.7		1.1	V	

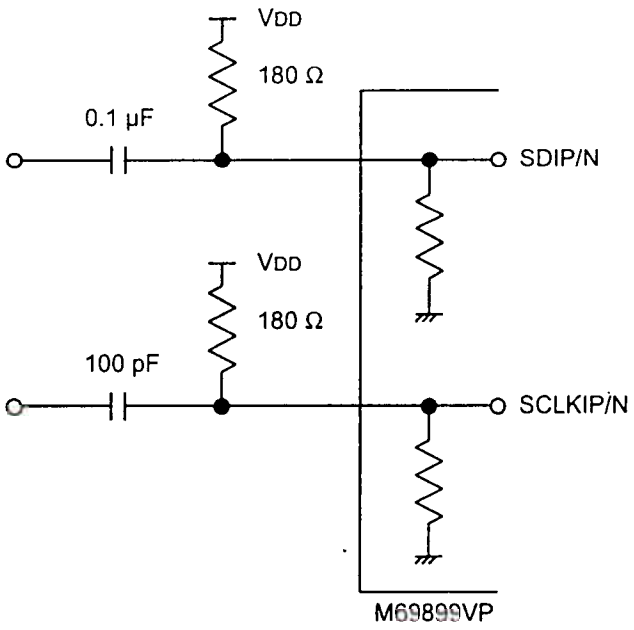

Figure 2 Input AC Coupled Termination

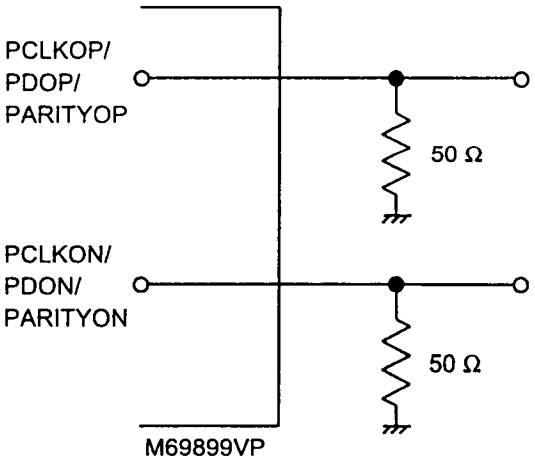

Figure 3 Differential PECL Output DC Termination

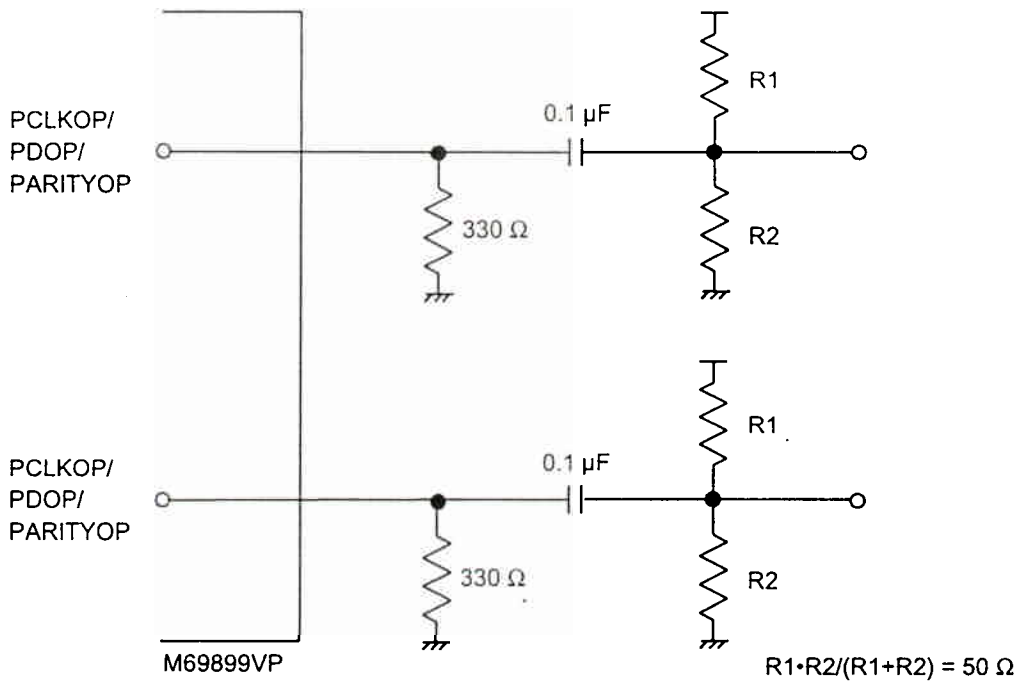

Figure 4 Differential PECL Output AC Termination

Table 6 AC Characteristics

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
TDS	SDIP/N Setup Time with Respect to SCLKIP/N	50		ps
TDH	SDIP/N Hold Time with Respect to SCLKIP/N	50		ps
TBD	Delay Time of PDOP/N		500	ps
	PCLKOP/N Duty Cycle	45	55	%
	PDOP/N Rise and Fall Time [1]		400	ps
	PCLKOP/N Rise and Fall Time [1]		300	ps

1. 10% - 90%

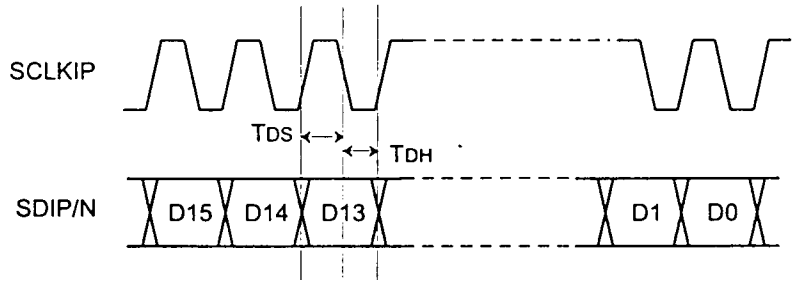

Figure 5 Input Timing

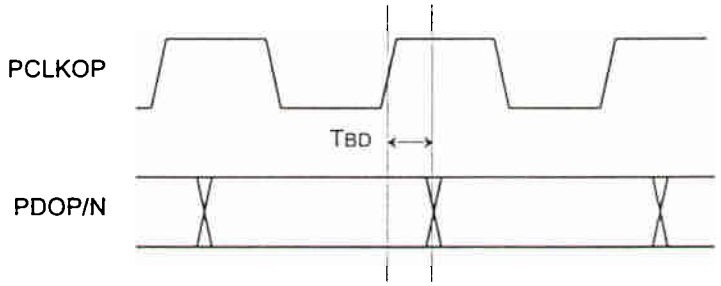

Figure 6 Output Timing

Table 7 Input/Output Pin Assignment

PIN NAME	LEVEL	I/O	PIN #	DESCRIPTION
SCLKIP SCLKIN	Differential PECL	I	11 10	Received serial clock.
SDIP SDIN	Differential PECL	I	14 13	Received serial data. These inputs are clocked by the SCLKIP/N inputs.
PARITYSET	CMOS	I	21	Used for setting parity check mode. See Table 8.
PDOP[15:0] PDON[15:0]	Differential PECL	O	Table 9	Differential parallel data output.
PCLKOP PCLKON	Differential PECL	O	6 5	Parallel output clock.
PARITYOP PARITYON	Differential PECL	O	24 23	Parallel output parity data. See Table 8.

Table 8 Parity Check Condition

PARITYSET	# of "High"s in PDOP[15:0]	PARITYOP	PARITYON
High	Even	High	Low
High	Odd	Low	High
Low	Even	Low	High
Low	Odd	High	Low

Table 9 PDOP/PDON Pin Assignment

PIN NAME	PIN #
PDOP0	4
PDOP1	62
PDOP2	60
PDOP3	58
PDOP4	56
PDOP5	54
PDOP6	52
PDOP7	46

PIN NAME	PIN #
PDOP8	44
PDOP9	42
PDOP10	40
PDOP11	38
PDOP12	36
PDOP13	30
PDOP14	28
PDOP15	26

PIN NAME	PIN #
PDON0	3
PDON1	61
PDON2	59
PDON3	57
PDON4	55
PDON5	53
PDON6	51
PDON7	45

PIN NAME	PIN #
PDON8	43
PDON9	41
PDON10	39
PDON11	37
PDON12	35
PDON13	29
PDON14	27
PDON15	25

Table 10 Common Pin Assignment

PIN NAME	LEVEL	PIN #	DESCRIPTION
VDD1	1.8 V	19	Core power supply.
VDD2	1.8 V	1, 8, 15, 17, 31, 33, 47, 49, 63	I/O power supply.
GND	GND	2, 9, 12, 16, 18, 20, 32, 34, 48, 50, 64	Ground.

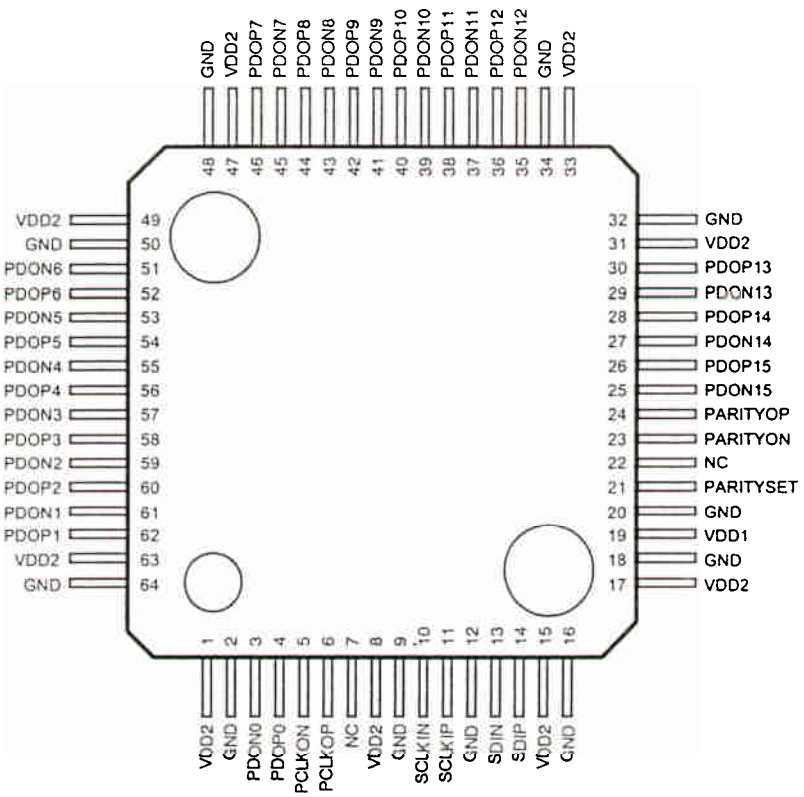

Figure 7 Pin Diagrams

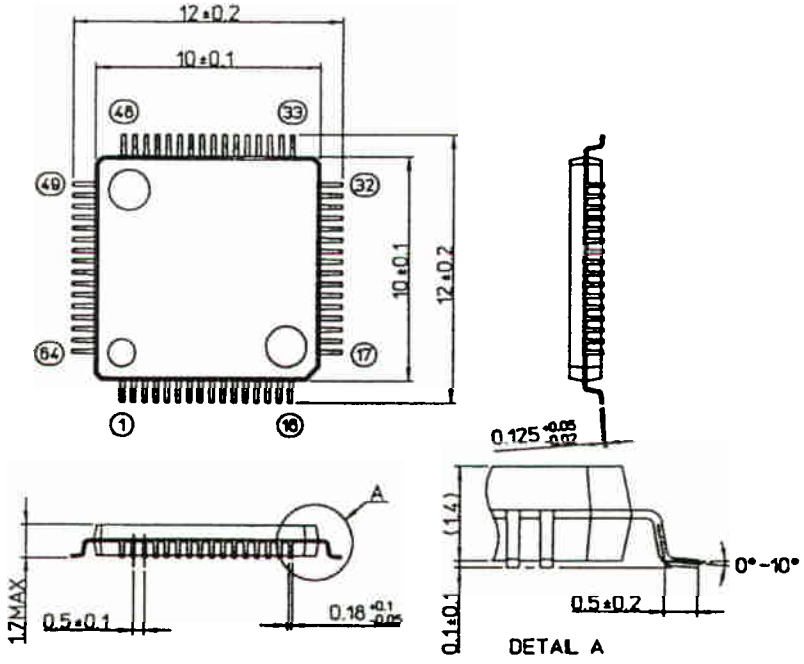

Figure 8 Package Information