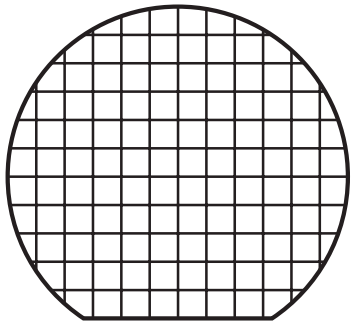
M69KB096AA

64 Mbit (4M x16)
1.8V Supply, 80MHz Clock Rate, Burst PSRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 1.7 to 1.95V core supply voltage
  - V_{CCQ} = 1.7 to 3.3V for I/O buffers
- ASYNCHRONOUS MODES
  - Asynchronous Random Read: 70ns and 85ns access time
  - Asynchronous Write
  - Asynchronous Page Read
    - Page Size: 16 words
    - Subsequent read within page: 20ns
- SYNCHRONOUS BURST READ AND WRITE MODES
  - Burst Write in Continuous Mode
  - Burst Read:
    - Fixed Length (4, 8, or 16 Words) or Continuous mde
    - Maximum Clock Frequency: 66MHz, 80MHz
    - Burst initial latency: 50ns (4 clock cycles) at 80MHz
    - Output delay: 9ns at 80MHz
- BYTE CONTROL BY $\overline{LB}$/$\overline{UB}$
- LOW POWER CONSUMPTION
  - Asynchronous Random Read Mode: < 25mA
  - Asynchronus Page Read Mode (subsequent read operations): < 15mA
  - Synchronous Burst Read
    Initial access: < 35mA
    Continuous Burst Read: < 15mA
  - Standby Current: 120µA
  - Deep Power-Down Current: 10µA (typ)

Figure 1. Package



Wafer

- LOW POWER FEATURES
  - Temperature Compensated Refresh (TCR)
  - Partial Array Refresh (PAR)
  - Deep Power-Down (DPD) Mode
- OPERATING TEMPERATURE
  - –30°C to +85°C

THE M69KB096AA IS ONLY AVAILABLE AS PART OF A MULTI-CHIP PACKAGE PRODUCT

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SUMMARY DESCRIPTION

The M69KB096AA is a 64 Mbit (67,108,864 bit) PSRAM, organized as 4,194,304 words by 16 bits. The memory array is implemented using a one transistor-per-cell topology, to achieve bigger array sizes.

This device is a high-speed CMOS, dynamic random-access memory. It provides a high-density solution for low-power handheld applications.

The M69KB096AA includes the industry standard Flash memory burst mode that dramatically increases read/write over that of other low-power SRAM or PSRAMs.

The PSRAM interface supports both asynchronous and burst-mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

PSRAMs are based on the DRAM technology, but have a transparent internal self-refresh mechanism that requires no additional support from the system memory controller, and has no significant impact on the device read/write performance.

The device has two configuration registers, accessible to the user to define the device operation: the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR). The Bus Configuration Register (BCR) indicates how the device interacts with the system memory bus. Overall, it is identical to its counterpart in burst-mode Flash memory devices. The Refresh Configuration Register (RCR) is used to control how the memory array refresh is performed. At power-up, these registers are automatically loaded with default settings and can be updated any time during normal operation.

To minimize the value of the standby current during self-refresh operations, the M69KB096AA includes three system-accessible mechanisms configured via the Refresh Configuration Register (RCR):

- The Temperature Compensated Refresh (TCR) is used to adjust the refresh rate according to the operating temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby.
- The Partial Array Refresh (PAR) performs a limited refresh of the part of the PSRAM array that contains essential data.
- The Deep Power-Down (DPD) mode completely halts the refresh operation. It is used when no essential data is being held in the device.

Figure 2. Logic Diagram

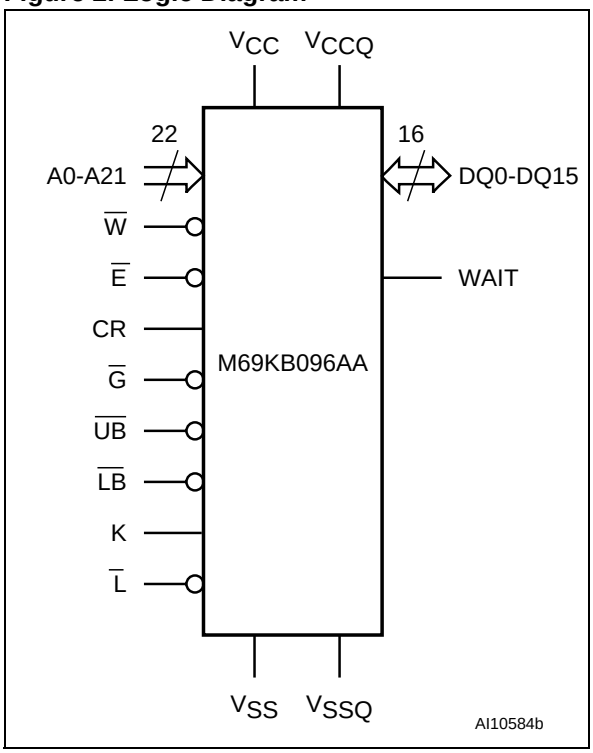


Table 1. Signal Names

A0-A21	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable Input
CR	Configuration Register Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
K	Clock Input
$\overline{L}$	Latch Enable Input
WAIT	Wait Output
V_{CC}	Core Supply Voltage
V_{CCQ}	Input/Output Buffers Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Buffers Ground

SIGNAL DESCRIPTIONS

The signals are summarized in Figure 2., Logic Diagram, and Table 1., Signal Names.

Address Inputs (A0-A21). The Address Inputs select the cells in the memory array to access during Read and Write operations.

Data Inputs/Outputs (DQ8-DQ15). The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a Write or Read operation, when Upper Byte Enable ($\overline{UB}$) is driven Low. When disabled, the Data Inputs/Outputs are high impedance.

Data Inputs/Outputs (DQ0-DQ7). The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a Write or Read operation, when Lower Byte Enable ($\overline{LB}$) is driven Low.

Chip Enable ($\overline{E}$). Chip Enable, $\overline{E}$, activates the device when driven Low (asserted). When deasserted (V_{IH}), the device is disabled and goes automatically in low-power Standby mode or Deep Power-down mode.

Output Enable ($\overline{G}$). Output Enable, $\overline{G}$, provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

Write Enable ($\overline{W}$). Write Enable, $\overline{W}$, controls the Bus Write operation of the memory. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

Upper Byte Enable ($\overline{UB}$). The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

Lower Byte Enable ($\overline{LB}$). The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both $\overline{LB}$ and $\overline{UB}$ are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}$ remains Low.

Clock Input (K). The Clock, K, is an input signal to synchronize the memory to the microcontroller or system bus frequency during Synchronous Burst Read and Write operations.

The Clock input is required during all synchronous operations, except in Standby and Deep Power-Down. It must be kept Low during asynchronous operations.

Configuration Register Enable (CR). When this signal is driven High, V_{IH}, Write operations load either the value of the Refresh Configuration Register (RCR) or the Bus configuration register (BCR).

Latch Enable ($\overline{L}$). The Latch Enable input is used to latch the address. Once the first address has been latched, the state of $\overline{L}$ controls whether subsequent addresses come from the address lines ($\overline{L} = V_{IL}$) or from the internal Burst counter ($\overline{L} = V_{IH}$).

The Latch Enable signal, $\overline{L}$, must be held Low, V_{IL}, during Asynchronous operations.

Wait (WAIT). The WAIT output signal provides data-valid feedback during Synchronous Burst Read and Write operations. The signal is gated by $\overline{E}$. Driving $\overline{E}$ High while WAIT is asserted may cause data corruption.

Once a Read or Write operation has been initiated, the WAIT signal goes active to indicate that the M69KB096AA device requires additional time before data can be transferred.

The WAIT signal also is used for arbitration when a Read or Write operation is launched while an on-chip refresh is in progress (see Figure 6., Collision Between Refresh and Read Operation and Figure 7., Collision between Refresh and Write Operation).

The WAIT signal on the M69KB096AA device is typically connected to a shared system-level WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

See the Operating Modes section for details on the WAIT signal operation.

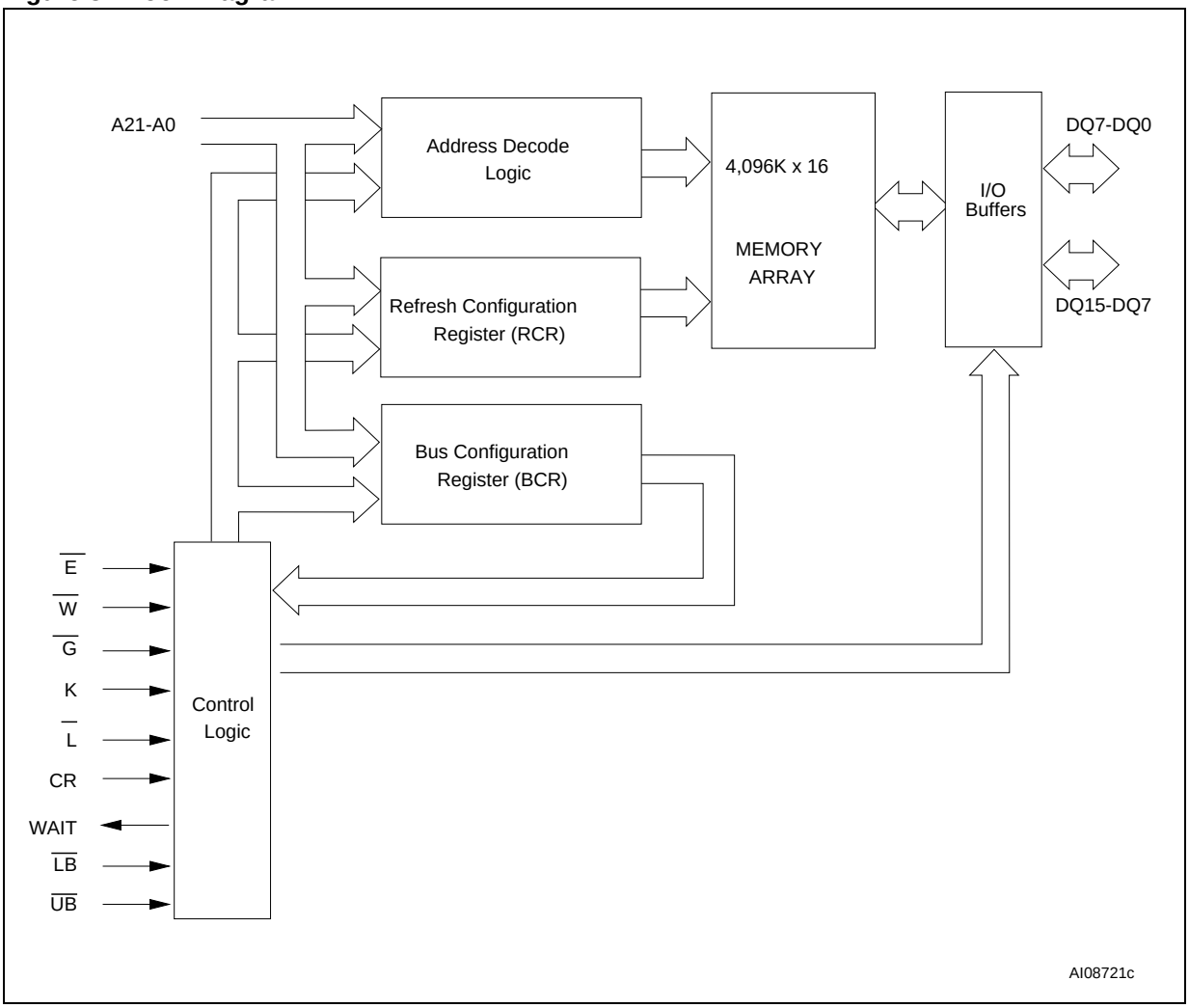
V_{CC} Supply Voltage. The V_{CC} Supply Voltage supplies the power for all operations (Read, Write, etc.) and for driving the refresh logic, even when the device is not being accessed.

V_{CCQ} Supply Voltage. V_{CCQ} provides the power supply for the I/O pins. This allows all Outputs to be powered independently from the core power supply, V_{CC}.

V_{SS} Ground. The V_{SS} Ground is the reference for all voltage measurements.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}. V_{SSQ} must be connected to V_{SS}.

Figure 3. Block Diagram



Note: Functional block diagram illustrates simplified device operation.

Table 2. Bus Modes– Asynchronous Mode

MODE	POWER	K	$\overline{L}$	$\overline{E}$	$\overline{G}$	$\overline{W}$	CR	$\overline{LB}$, $\overline{UB}$	WAIT (2)	DQ15-DQ0 (1)	NOTES
Asynchronous Read	Active > Standby	L	L	L	L	H	L	L[1]	Low Z	Data-Out	3
Asynchronous Write	Active > Standby	L	L	L	X	L	L	L[1]	Low Z	Data-In	3
Standby	Standby	L	X	H	X	X	L	X	High Z	High-Z	4,5
Write Configuration Register	Active	L	L	L	H	L	H	X	Low Z	High-Z	
Deep Power-Down (DPD)	Deep Power-Down	L	X	H	X	X	X	X	High-Z	High-Z	6

Table 3. Bus Modes– Synchronous Burst Mode

MODE	POWER	K	$\overline{L}$	$\overline{E}$	$\overline{G}$	$\overline{W}$	CR	$\overline{LB}$, $\overline{UB}$	WAIT (2)	DQ15-DQ0 (1)	NOTES
Initial Burst Read	Active > Standby	⮥	L	L	X	H	L	L	Low Z	Data-Out	3, 7, 8
Initial Burst Write	Active > Standby	⮥	L	L	H	L	L	X	Low Z	Data-In	3, 7, 8
Subsequent Burst Operation	Active > Standby	⮥	H	L	X	X	X	L	Low Z	Data-In or Data-Out	3, 7, 8
Burst Suspend	Active > Standby	X(9)	X	L	H	X	L	X	Low Z	High-Z	3, 7
Write Configuration Register	Active	⮥	L	L	H	L	H	X	Low Z	High-Z	7, 8
Deep Power-Down (DPD)	Deep Power-Down	L	X	H	X	X	X	X	High-Z	High-Z	6

Note: 1. When $\overline{LB}$ and $\overline{UB}$ are in select mode (Low), DQ15-DQ0 are affected. When only $\overline{LB}$ is in select mode, DQ7-DQ0 are affected. When only $\overline{UB}$ is in the select mode, DQ15-DQ8 are affected.
2. The WAIT polarity is configured through the Bus Configuration Register (BCR10).
3. The device consumes active power in this mode whenever addresses are changed.
4. When the device is in Standby mode, Address inputs and Data inputs/outputs are internally isolated from any external influence.
5. $V_{IN} = V_{CC}$ or 0V.
6. The device remains in Deep Power-Down mode until the RCR register is reconfigured.
7. The Synchronous Burst mode is initialized through the Bus Configuration Register (BCR15).
8. The clock polarity is configured through the Bus Configuration Register (BCR6).
9. The Clock signal, K, must remain stable during Burst Suspend operations.

OPERATING MODES

The M69KB096AA supports Asynchronous Random Read, Page Read and Synchronous Burst Read and Write modes.

The device mode is defined by the value that has been loaded into the Bus Configuration Register. The Page mode is controlled by the Refresh Configuration Register (RCR7).

Power-Up

PSRAM devices include an on-chip voltage sensor used to launch the power-up sequence. V_{CC} and V_{CCQ} must be applied simultaneously. Once they reach a stable level, equal to or higher than 1.70V, the device will require t_{VCHEL} to complete its self-initialization process. During the initialization period, the $\overline{E}$ signal should remain High. Once initialization has completed, the device is ready for normal operation. Initialization will configure the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) with their default settings (see Table 5., page 16, and Table 9., Refresh Configuration Register Definition).

See Figure 34., Power-Up AC Waveforms and Table 19., Power-Up AC Characteristics, for details on the Power-up timing.

Asynchronous Random Read and Write Modes

At power-up, the device is in Asynchronous Random Read mode. This mode uses the industry standard control bus ($\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$, $\overline{UB}$). Read operations are initiated by bringing $\overline{E}$, $\overline{G}$, and $\overline{LB}$, $\overline{UB}$ Low, V_{IL}, while keeping $\overline{W}$ High, V_{IH}. Valid data will be gated through the output buffers after the specific access time t_{AVQV} has elapsed.

The WAIT signal will remain active until valid data is output from the device and its state should be ignored.

Write operations occur when $\overline{E}$, $\overline{W}$, $\overline{LB}$ and $\overline{UB}$ are driven Low. During Asynchronous Random Write operations, the $\overline{G}$ signal is “don't care” and $\overline{W}$ will override $\overline{G}$. The data to be written is latched on the rising edge of $\overline{E}$, $\overline{W}$, $\overline{LB}$ or $\overline{UB}$ (whichever occurs first). During Write operations, the WAIT signal indicates to the system memory controller that data have been programmed into the memory.

During asynchronous operations (Page mode disabled), the $\overline{L}$ input can either be used to latch the address or kept Low, V_{IL}, during the entire Read/Write operation. The Clock input signal K must be held Low, V_{IL}.

See Figures 15, 16 and Table 15. for details of Asynchronous Read AC timing requirements.

See Figures 23, 24, 25, 26, and Table 17. for details of Asynchronous Write AC timing requirements.

Asynchronous Page Read Mode

The Asynchronous Page read mode gives greater performance, even than the traditional Asynchronous Random Read mode. The page mode is not available for write operations.

Asynchronous Page Read mode is enabled by setting RCR7 to ‘1’. $\overline{L}$ must be driven Low, V_{IL}, during all Asynchronous Page Read operations.

In Asynchronous Page Read mode, a Page of data is internally read. Each memory page consists of 16 Words, and has the same set of values on A4-A21; only of A0 to A3 differ. The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal, longer timings apply again.

During Asynchronous Page Read mode, the K input must be held Low, V_{IL}. $\overline{E}$ must be kept Low, V_{IL} upon completion of an Asynchronous Page Read operation. The WAIT signal remains active until valid data is output from the device.

See Figure 17. and Table 15. for details of the Asynchronous Page Read timing requirements.

Synchronous Burst Mode

Burst mode allows high-speed synchronous read and write operations.

In Synchronous Burst mode, the data is input or output to or from the memory array in bursts that are synchronized with the clock. After $\overline{E}$ goes Low, the data address is latched on the first rising edge of the Clock, K. During this first clock rising edge, the $\overline{W}$ signal indicates whether the operation is going to be a Read ($\overline{W}$=V_{IH}, Figure 4.) or Write ($\overline{W}$=V_{IL}, Figure 5.).

In Synchronous Burst mode, the number of Words to be input or output during a Synchronous Burst operation can be configured in the Bus Configuration Register, BCR, as fixed length (4 Words, 8 Words or 16 Words) or Continuous. In Synchronous Continuous Burst mode, the entire memory can be accessed sequentially in one Burst operation.

The Latency Counter, stored in the BCR11 to BCR13 bits of the BCR register, defines how many clock cycles elapse before the first data value is transferred between the processor and the M69KB096AA.

The WAIT output will be asserted as soon as a Synchronous Burst operation is initiated and will be deasserted to indicate when data is to be transferred into (or out of) the memory array. The WAIT signal is also asserted when a Continuous Burst Read or Write operation crosses a row boundary. The WAIT assertion allows time for the new row to

be accessed. It also allows any pending refresh operations to be performed (see Figure 22., Continuous Burst Read Showing an Output Delay for End-of-Row Condition (BCR8=0,1)).

The processor can access other devices without being submitted to the initial burst latency by suspending the burst operation. Burst operations can be suspended by halting the Clock signal, holding it High or Low. If another device needs to use the data bus while Burst operations are suspended, the Output Enable signal, $\overline{G}$, should be driven High, V_{IH}, to disable data outputs; otherwise, $\overline{G}$ can remain Low, V_{IL}. The WAIT output will remain asserted to prevent any other devices from using the processor WAIT line.

Burst operations can be resumed by taking $\overline{G}$ Low, V_{IL}, and then restarting the Clock as soon as valid data are available on the bus (see Figure 21., Synchronous Burst Read Suspend and Resume Waveforms).

Mixed Mode

When the BCR register is configured for synchronous operation, the device can support a combination of Synchronous Burst Read and Asynchronous Random Write operations.

The Asynchronous Random Write operation requires that the Clock signal remains Low, V_{IL}, during the entire sequence. The $\overline{L}$ signal can either be used to latch the target address or remain Low, V_{IL}, during the entire Write operation. $\overline{E}$ must return Low, V_{IL}, during Asynchronous and Burst operations. Note that the time, necessary to assure adequate refresh, is the same value as that for Asynchronous Read and Write mode.

Mixed-mode operation greatly simplifies the interfacing with traditional burst-mode Flash Memory Controllers.

Low-Power Modes

Standby Mode. During Standby, the device current consumption is reduced to the level necessary to perform the memory array refresh operation. Standby operation occurs when $\overline{E}$ is High, V_{IH}, and no transaction is in progress.

The device will enter Standby mode when a Read or Write operation is completed, or when the address and control inputs remain stable for an extended period of time. This “active” Standby mode will continue until address or control inputs change.

Temperature Compensated Refresh. The Temperature Compensated Refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature.

The leakage current of DRAM capacitive storage elements increases with the temperature. PSRAM devices, based on a DRAM architecture, consequently require increasingly frequent refresh operations to maintain data integrity as the temperature increases. At lower temperatures, the refresh rate can be decreased to minimize the standby current.

The TCR mechanism allows adequate refresh rates to be set at four different temperature thresholds. These are defined by setting the RCR5 and RCR6 bits of the Refresh Configuration Register, RCR. To minimize the self refresh current consumption, the selected setting must be higher than the operating temperature of the PSRAM device. As an example, if the operating temperature is +50°C, the +70°C setting must be selected; the +15°C and +45°C settings would result in inadequate refreshing and could cause data corruption.

See Table 9. for the definition of the Refresh Configuration Register bits.

Partial Array Refresh. The Partial Array Refresh (PAR) performs a limited refresh of part of the PSRAM array. This mechanism enables the device to reduce the standby current by refreshing only the part of the memory array that contains essential data. Different refresh options can be defined by setting the RCR0 to RCR2 bits of the RCR Register:

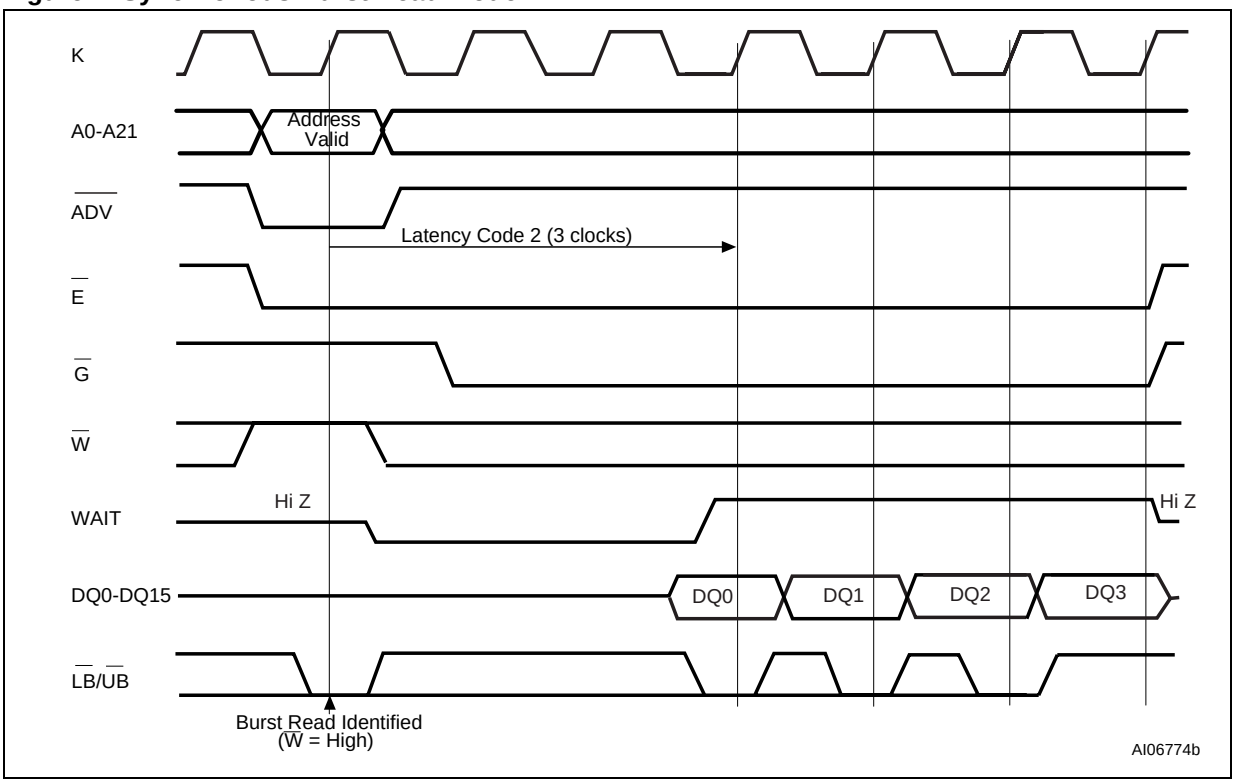
- Full array
- One half of the array
- One quarter of the array
- One eighth of the array
- None of the array.

These memory areas can be located either at the top or bottom of the memory array.

The WAIT signal is used for arbitration when a read/write operation is launched while an on-chip refresh is in progress. If locations are addressed while they are undergoing refresh, the WAIT signal will be asserted for additional clock cycles, until the refresh has completed (see Figure 6. and Figure 7., Collision between Refresh and Read or Write Operations). When the refresh operation is completed, the Read or Write operation will be allowed to continue normally.

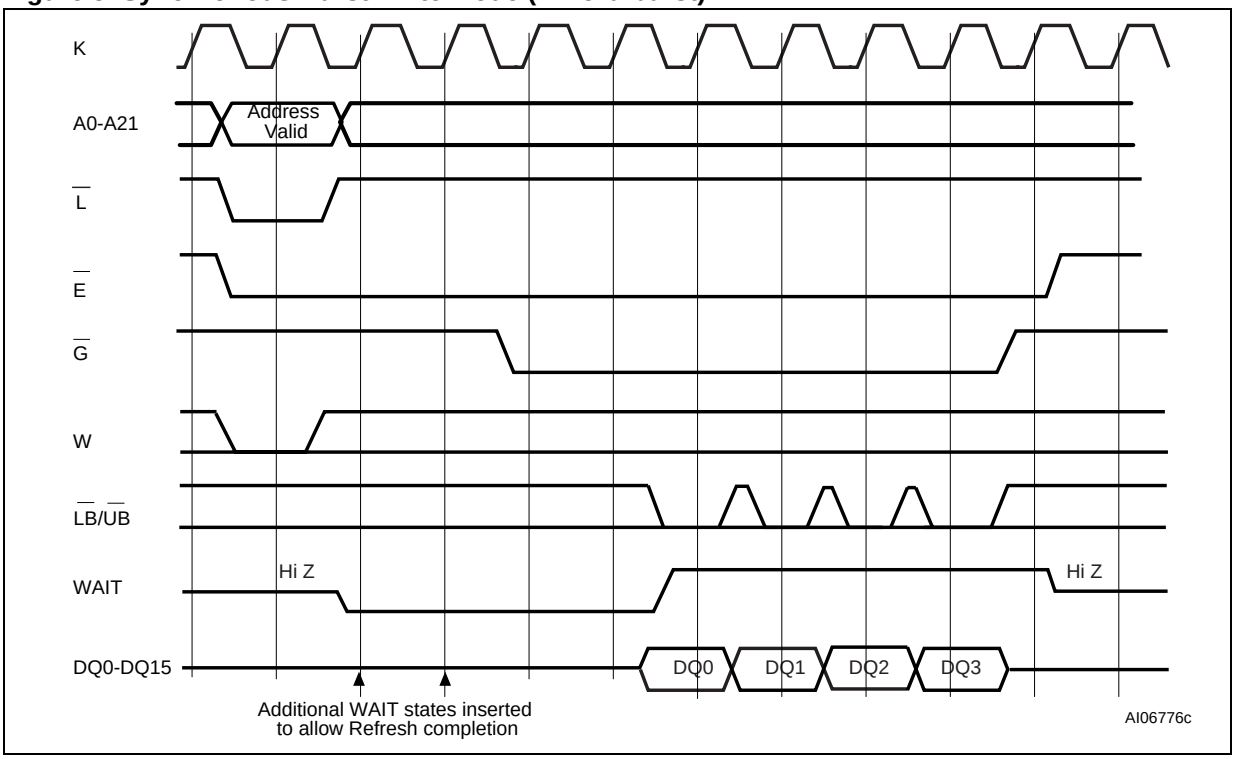
Deep Power-Down Mode. Deep power-down (DPD) mode is used by the system memory controller to de-activate the PSRAM device when its storage capabilities are not needed. All refresh-related operations are then disabled. When the Deep Power-Down mode is enabled, the data stored in the device become corrupted. When refresh operations have been re-enabled, the device will be available for normal operations after t_{VCHEL} (time to perform an initialization sequence). During this delay, the current consumption will be higher than the specified standby levels, but considerably lower than the active current.

Figure 4. Synchronous Burst Read Mode



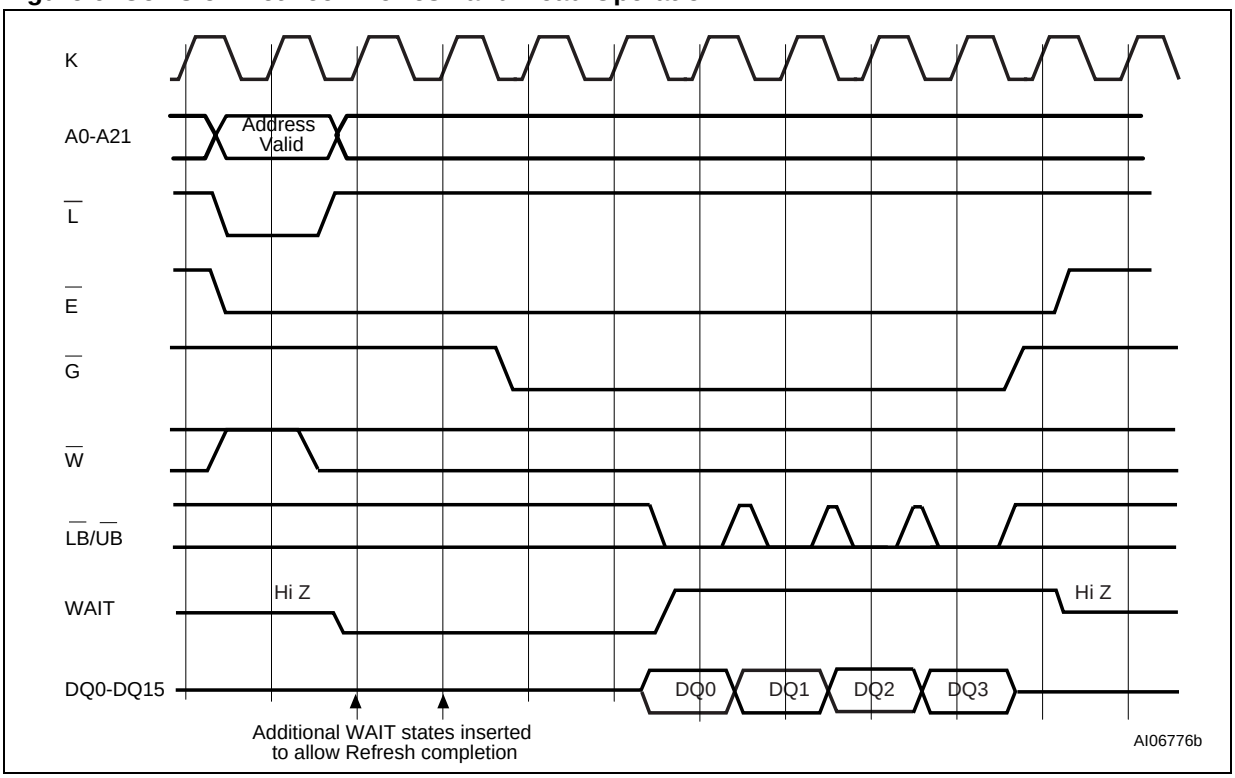
Note: Non-default BCR Register settings: 3 clock cycle latency; WAIT active Low; Hold Data one clock; WAIT asserted during delay.

Figure 5. Synchronous Burst Write Mode (4-word burst)



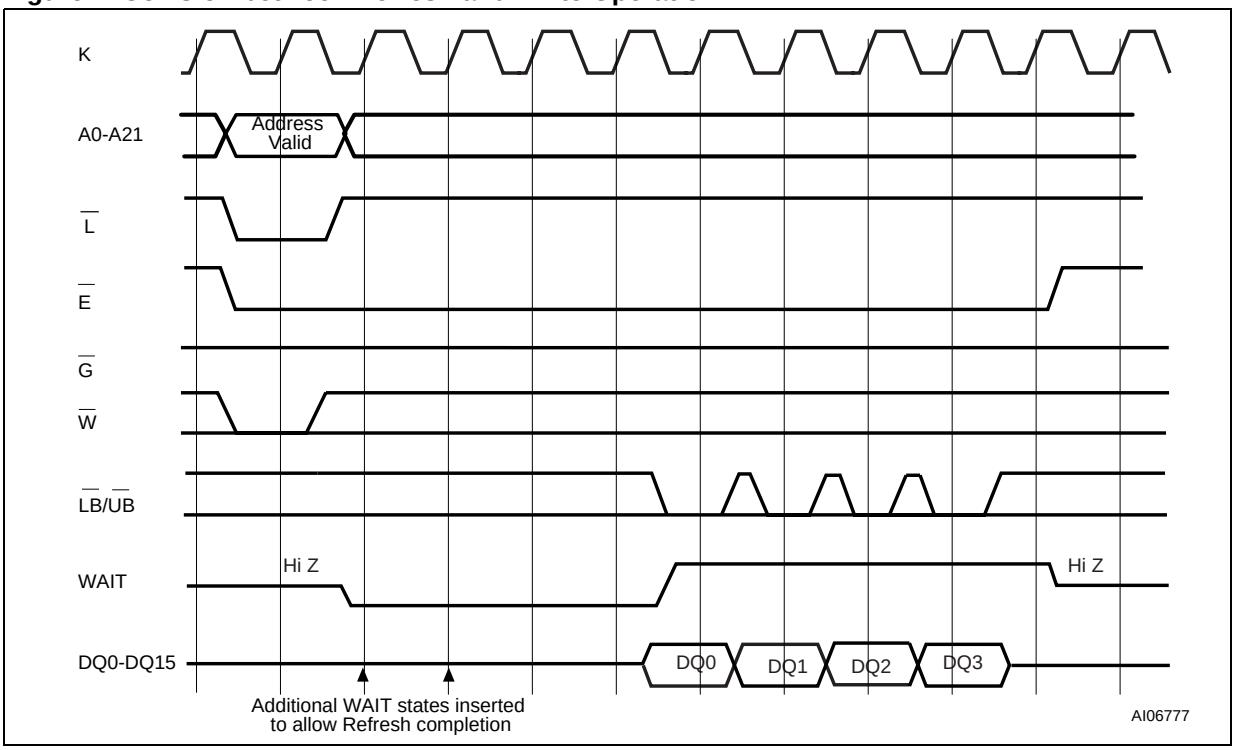
Note: Non-default BCR Register settings: 3 clock cycle latency; WAIT active Low; Hold Data one clock; WAIT asserted during delay.

Figure 6. Collision Between Refresh and Read Operation



Note: Additional Wait states inserted to allow Refresh completion.
Non-default BCR Register settings: 3 clock cycle latency; WAIT active Low; Hold Data one clock; WAIT asserted during delay.

Figure 7. Collision between Refresh and Write Operation



Note: Additional Wait states inserted to allow Refresh completion.
Non-default BCR Register settings: 3 clock cycle latency; WAIT active Low; Hold Data one clock; WAIT asserted during delay.

CONFIGURATION REGISTERS

Two write-only user-accessible configuration registers have been included to define device operation. These registers are automatically loaded with default settings during power-up, and can be updated any time the device is operating in a standby state.

The configuration registers (BCR and RCR) can be programmed and read using two methods:

- The CR Controlled Method (or Hardware Method)
- The Software Method.

Programming and Reading the Configuration Registers using the CR Controlled Method

The BCR and the RCR can be programmed and read using either a Synchronous or an Asynchronous Write and Read operation with the Configuration Register Enable input, CR, at V_{IH}. Address bit A19 selects the register to be programmed or read (see Table 4., Register Selection). The values placed on address lines A0 to A21 are latched into the register on the rising edge of L, E, or W, whichever occurs first. LB and UB are “don’t care”.

When CR is at V_{IL}, a Read or Write operation will access the memory array.

See Figures 27 and 33, Configuration Register Write in Asynchronous and Synchronous Modes.

Table 4. Register Selection

Register	Read or Write Operation	A19
RCR	Read/Write	0
BCR	Read/Write	1

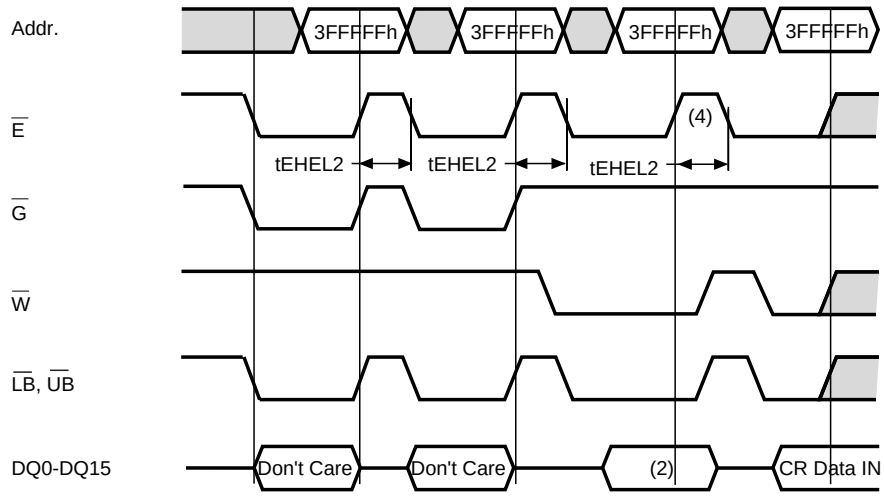
Programming and Reading the Configuration Registers by the Software Method

Each register can be read by issuing a Read Configuration Register sequence (see Figure 9., Read Configuration Register (Software Method), and programmed by issuing a Set Configuration Register sequence (see Figure 8., Set Configuration Register (Software Method). Both sequences must be issued in asynchronous mode.

The timings will be identical to those described in Table 15., Asynchronous Read AC Characteristics. The Chip Enable input, CR, is ‘don’t care’. Read Configuration Register and Set Configuration Register sequences both require 4 cycles:

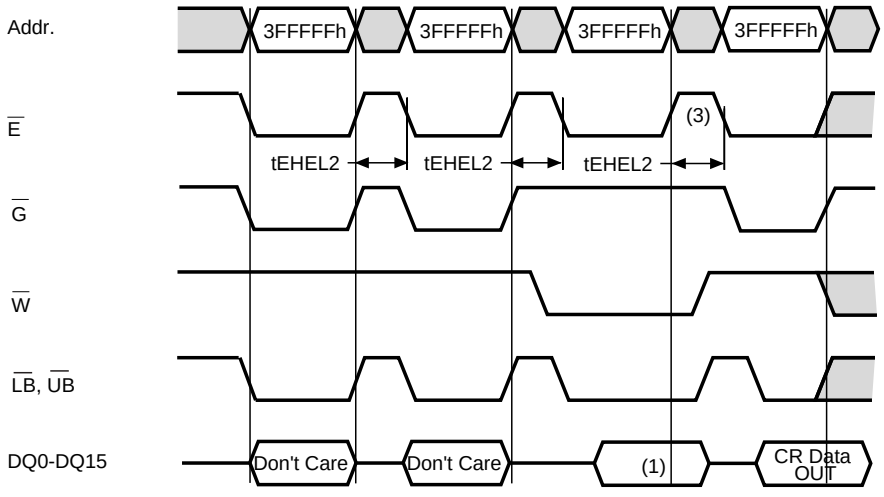
- 2 bus read and one bus write cycles to a unique address location, 3FFFFFh, indicate that the next operation will read or write to a configuration register. The data written during the third cycle must be ‘0000h’ to access the RCR and ‘0001h’ to access the BCR during the next cycle.
- The fourth cycle reads from or writes to the configuration register.

Figure 8. Set Configuration Register (Software Method)



Note: 1. Only the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) can be modified.
2. To program the BCR or the RCR on last bus write cycle, DQ0-DQ15 must be set to '0001h' and '000h' respectively.
3. The highest order address location is not modified during this operation.
4. The third write operation must be controlled by the Chip Enable signal.

Figure 9. Read Configuration Register (Software Method)



Note: 1. To read the BCR, RCR on last bus read cycle, DQ0-DQ15 must be set to '0001h', '000h' respectively.
2. The highest order address location is not modified during this operation.
3. The Chip Enable signal, E, must be held High for 150ns before reading the content of the Configuration Register.
4. The third write operation must be controlled by the Chip Enable signal.

Bus Configuration Register

The Bus Configuration Register (BCR) defines how the PSRAM interacts with the system memory bus. Overall, it is identical to its counterpart on burst mode Flash devices.

At power-up, BCR is initialized to 9D4Fh.

Refer to Table 5. for the description of the Bus Configuration Register Bits.

Operating Mode Bit (BCR15). The Operating Mode bit allows the Synchronous Burst mode or the Asynchronous mode (default setting) to be selected.

Latency Counter Bits (BCR13-BCR11). The Latency Counter bits are used to set the number of clock cycles between the beginning of a Read or Write operation and the first data becoming available. For correct operation, the number of clock cycles can only be equal to 3 or 4 (default settings) and the Latency Counter bits can only assume the values shown in Table 5., Bus Configuration Register Definition. See also Table 7., Latency Counter Configuration, and Figure 12., Example of Latency Counter Configuration).

WAIT Polarity Bit (BCR10). The WAIT Polarity bit indicates whether the WAIT output signal is active High or Low. As a consequence, it also determines whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

By default, the WAIT output signal is active High.

WAIT Configuration Bit (BCR8). The system memory controller uses the WAIT signal to control data transfer during Synchronous Burst Read Read and Write operations.

The WAIT Configuration bit is used to determine when the transition of the WAIT output signal between the asserted and the deasserted state occurs with respect to valid data available on the data bus.

When the Wait Configuration bit is set to ‘0’, data is valid or invalid on the first Clock rising edge immediately after the WAIT signal transition to the deasserted or asserted state.

When the Wait Configuration bit is set to ‘1’ (default settings), the WAIT signal transition occurs one clock cycle prior to the data bus going valid or invalid.

See Figure 10., WAIT Configuration Example, and Figure 11., Example of WAIT Configuration During Synchronous Burst Operation.

Clock Configuration Bit (BCR6). The Clock Configuration bit is used to configure the activeedge of the Clock signal, K, during Synchronous Burst Read or Write operations. When the Clock Configuration bit is set to ’1’ (default setting), the rising edge of the Clock is active. Configuring the active clock edge to the falling edge (BCR6 set to ‘0’) is not supported.

All of the waveforms shown in this datasheet correspond to a Clock signal active on the rising edge.

Driver Strength Bit (BCR5). The Driver Strength bit allows to set the output drive strength to adjust to different data bus loading. Normal driver strength (full drive) and reduced driver strength (a quarter drive) are available.

By default, outputs are configured at ‘half drive” strength.

Burst Wrap Bit (BCR3). The burst reads can be confined inside the 4, 8 or 16 Word boundary (wrap) or allowed to step across the boundary (no wrap). The Burst Wrap bit is used to select between ‘wrap’ and ‘no wrap’. If the Burst Wrap bit is set to ‘1’ (no wrap), the device outputs data sequentially regardless of burst boundaries. When Continuous Burst operation is selected, the internal address switches to 000000h if the read address passes the last address. By default, Burst wrap is selected.

See also Table 6., Burst Type Definition.

Burst Length Bits (BCR2-BCR0). The Burst Length bits set the number of Words to be output during a Synchronous Burst Read operation. They can be set for 4 Words, 8 Words, 16 Words or Continuous Burst (default settings), where all the Words are read sequentially regardless of address boundaries. Burst Write operations are always performed using the Continuous Burst mode.

Table 5. Bus Configuration Register Definition

Address Bits	Bus Configuration Register Bit	Description	Value	Description
A21-A20	-	-	Must be set to '0'	Reserved
A19	-	Register Select	0	Refresh Selected
			1	Bus Configuration Register Selected
A18-A16	-	-	Must be set to '0'	Reserved
A15	BCR15	Operating Mode Bit	0	Synchronous Burst mode
			1	Asynchronous mode (default)
A14	-	-	Must be set to '0'	Reserved
A13-A11	BCR13-BCR11	Latency Counter Bits (LC)	010	LC = 2 (3 Clock Cycles)
			011	LC= 3 (4 Clock Cycles) (default)
			Other configurations reserved	
A10	BCR10	WAIT Polarity Bit	0	WAIT Active Low
			1	WAIT Active High (default)
A9	-	-	Must be set to '0'	Reserved
A8	BCR8	Wait Configuration Bit	0	WAIT Asserted During Delay
			1	WAIT Asserted One Clock Cycle Before Delay (Default)
A7	-	-	Must be set to '0'	Reserved
A6	BCR6	Clock Configuration Bit	0	Not supported
			1	Rising Clock Edge (Default)
A5	BCR5	Driver Strength Bit	0	Full Drive (default)
			1	1/4 Drive
A4	-	-	Must be set to '0'	Reserved
A3	BCR3	Burst Wrap Bit	0	Wrap (default)
			1	No Wrap
A2-A0	BCR2-BCR0	Burst Length Bit	001	4 Words
			010	8 Words
			011	16 Words
			111	Continuous Burst (default)

Note: All Burst Write operations are performed in Synchronous Continuous Burst mode.

Table 6. Burst Type Definition

Mode	Start Add	4 Words (Sequential)	8 Words (Sequential)	16 Words (Sequential)	Continuous Burst
Wrap (BCR3='0')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6...
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7...
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8...
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9...
	4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10...
	5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11...
	6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12...
	7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13...
	...	...	...	...	...
	14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20...
	15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21...
No Wrap (BCR3='1')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	Same as for Wrap (Wrap /No Wrap has no effect on Continuous Burst)
	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	
	2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	
	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	
	4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	
	5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	
	6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	
	7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	
	...	...			
	14			14-15-16-17-18-19...-23-24-25-26-27-28-29	
	15			15-16-17-18-19-20...-24-25-26-27-28-29-30	

Table 7. Latency Counter Configuration

Latency Configuration Code	Maximum Input Clock Frequency		Unit
	Access Time 70ns Maximum Clock Rate in Burst Mode 80MHz	Maximum Clock Rate in Burst Mode 66MHz	
2 (3 Clock Cycles)	53 (18.75ns)	44 (22.7ns)(1)	MHz
3 (4 Clock Cycles)	80 (12.5ns)	66 (15.2ns)	MHz

Note: 1. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 10. WAIT Configuration Example

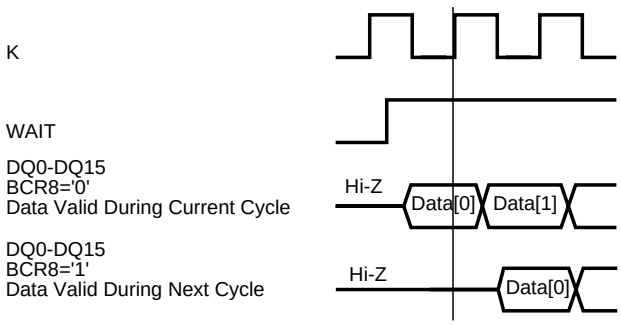


Figure 11. Example of WAIT Configuration During Synchronous Burst Operation

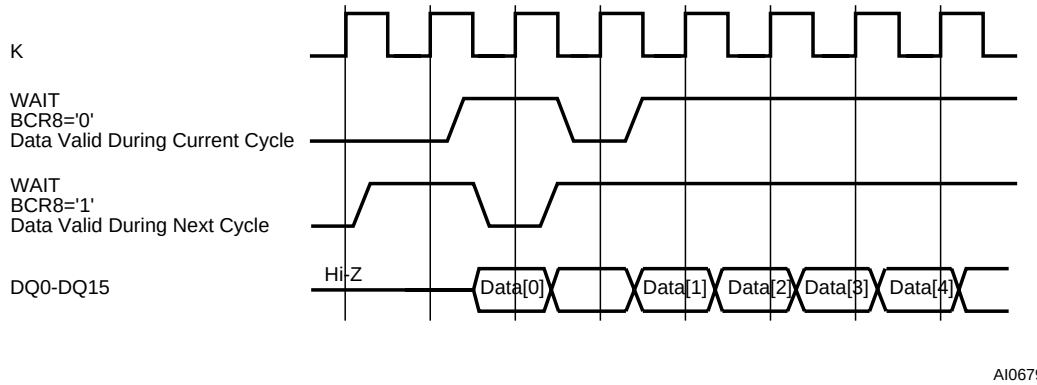
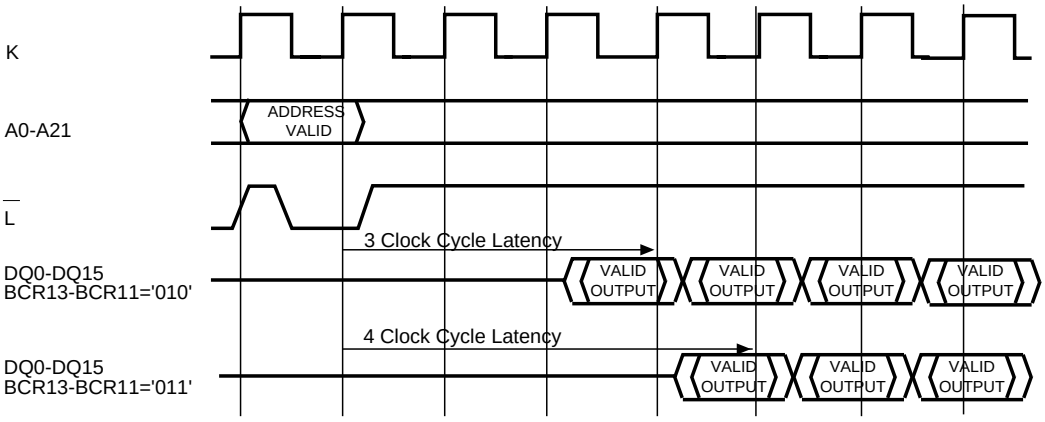


Figure 12. Example of Latency Counter Configuration



Refresh Configuration Register

The Refresh Configuration Register (RCR) is used for two purposes:

- to define how the self refresh of the PSRAM array is performed
- to enable Page Read operations.

Altering the self refresh parameters can dramatically reduce current consumption in Standby mode.

At power-up, RCR is initialized to 0070h.

Refer to Table 9. for the description of the Refresh Configuration Register Bits.

Page Mode Operation Bit (RCR7). The Page Mode operation bit determines whether the Asynchronous Page Read mode is enabled. At power-up, the RCR7 bit is set to '0', and so the Asynchronous Page Read mode is disabled.

Temperature Compensated Refresh Bits (RCR6-RCR5). The Temperature Compensated Refresh bits allow an adequate refresh rate to be selected at one of four different temperature thresholds: +15°C, +45°C, +70°C, and +85°C. The default setting is +85°C. See the Temperature Compensated Refresh section for more details.

Deep Power-Down Bit (RCR4). The Deep Power-Down bit enables or disables all refresh-related operations. The Deep Power-Down mode is enabled when the RCR4 bit is set to '0', and remains enabled until this bit is set to '1'. At power-up, the Deep Power-Down mode is disabled.

See the Deep Power-Down section for more details.

Partial Array Refresh Bits (RCR2-RCR0). The Partial Array Refresh bits allow refresh operations to be restricted to a portion of the total PSRAM array. The refresh options can be full array, one eighth, one quarter, one half, or none of the array. These memory areas can be located either at the top or bottom of the memory array. By default, the full memory array is refreshed (see Table 8., Address Patterns for Partial Array Refresh).

Table 8. Address Patterns for Partial Array Refresh

RCR2	RCR1	RCR0	Refreshed Area	Address Space	Size of Refreshed Area	Density
0	0	0	Full Array (Default)	000000h-3FFFFFh	4 Mbitsx16	64 Mbits
0	0	1	Bottom Half of the Array	000000h-1FFFFFh	2 Mbitsx16	32 Mbits
0	1	0	Bottom First Quarter of the Array	000000h-0FFFFFh	1 Mbitsx16	16 Mbits
0	1	1	Bottom First Eighth of the Array	000000h-07FFFFh	512Kbitsx 16	8 Mbits
1	0	0	None of the Array	0	0	0
1	0	1	Top Half of the Array	200000h-3FFFFFh	2 Mbitsx16	32 Mbits
1	1	0	Top Quarter of the Array	300000h-3FFFFFh	1 Mbitsx16	16 Mbits
1	1	1	Top One-Eighth of the Array	380000h-3FFFFFh	512Kbitsx 16	8 Mbits

Note: RCR4 is set to '1'.

Table 9. Refresh Configuration Register Definition

Address Bits	Bus Configuration Register Bit	Description	Value	Description
A21-A20	-	-	Must be set to '0'	Reserved
A19	-	Register Select	0	Refresh Selected
			1	Bus Configuration Register Selected
A18-A8	-	-	Must be set to '0'	Reserved
A7	RCR7	Page Mode Operation Bit	0	Page Read Mode Disabled (Default)
			1	Page Read Mode Enabled
A6-A5	RCR6-RCR5	Temperature Compensated Refresh Bits	11	+85°C (Default)
			00	+70°C
			01	+45°C
			10	+15°C
A4	RCR4	Deep Power-Down Bit	0	Deep Power-Down Enabled
			1	Deep Power-Down Disabled (Default)
A3	-	-	Must be set to '0'	Reserved
A2-A0	RCR2-RCR0	Partial Array Refresh Bits	000	See Table 8., Address Patterns for Partial Array Refresh
			001	
			010	
			011	
			100	
			101	
			110	
			111	

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 10. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	–30	85	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{CC}	Core Supply Voltage	–0.2	2.45	V
V_{CCQ}	Input/Output Buffer Supply Voltage	–0.2	4.0	V
V_{IO}	Input or Output Voltage	–0.5	4.0 or V_{CCQ}+0.3 (1)	V

Note: 1. Whichever is the lower.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 11., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 11. Operating and AC Measurement Conditions

Parameter		M69KB096AA		Unit
		Min	Max	
V_{CC} Supply Voltage		1.7	1.95	V
V_{CCQ} Input/Output Buffer Supply Voltage		1.7	3.3	V
Ambient Operating Temperature		–30	85	°C
Load Capacitance (C_L)		30		pF
Output Circuit Protection Resistance (R_1, R_2)	V_{CCQ} = 1.8V	2.7		kΩ
	V_{CCQ} = 2.5V	3.7		kΩ
	V_{CCQ} = 3.0V	4.5		kΩ
Input Pulse Voltages		0	V_{CC}	V
Input and Output Timing Ref. Voltages		$V_{CC}/2$		V
Output Transition Timing Ref. Voltages		$V_{RL} = 0.3V_{CC}$; $V_{RH} = 0.7V_{CC}$		V
Input Rise and Fall Time (tτ)			1.6	ns

Note: 1. All voltages are referenced to V_{SS}.

Figure 13. AC Measurement I/O Waveform

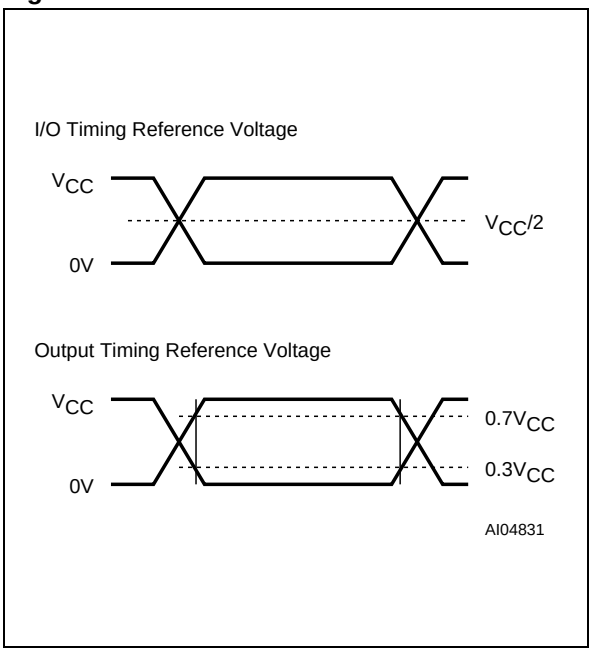
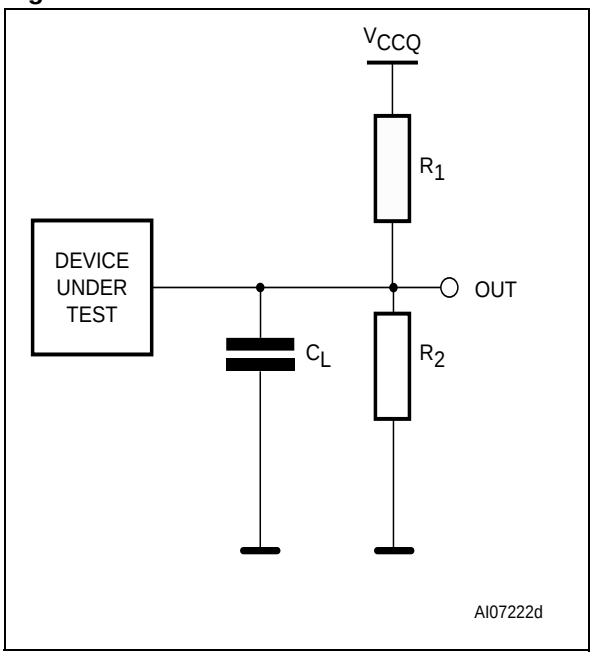


Figure 14. AC Measurement Load Circuit



Note: 1. Logic states '1' and '0' correspond to AC test inputs driven at VCCQ and VSS respectively. Input timings begin at VCCQ/2 and output timings end at VCCQ/2. Input rise and fall time (10% to 90%) are lower than 1.6ns.
2. All the tests are performed with the outputs configured as Full drive strength (BCR[5]=0).

Table 12. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V		6	pF
C_{IO}	Data Input/Output Capacitance	V_{IO} = 0V		6	pF

Note: 1. These parameters are not fully tested.

Table 13. DC Characteristics

Symbol	Parameter	Test Condition		Min.	Typ	Max.	Unit
I_{CC1} (1)	Operating Current: Asynchronous Random Read/Write	V_{IN} =V_{IH} or V_{IL}, $\overline{E}$ = V_{IL}, I_{OUT} = 0mA	70ns			25	mA
			85ns			20	mA
I_{CC1P} (1)	Operating Current: Asynchronous Page Read		70ns			15	mA
			85ns			12	mA
I_{CC2} (1)	Operating Current: Initial Access, Burst Read/Write		80MHz			35	mA
			66MHz			30	mA
I_{CC3R}(1)	Operating Current: Continuous Burst Read		80MHz			18	mA
			66MHz			15	mA
I_{CC3W}(1)	Operating Current: Continuous Burst Write		80MHz			35	mA
			66MHz			30	mA
I_{SB}(2)	V_{CC} Standby Current	V_{IN} = V_{CCQ} or 0V, $\overline{E}$ = V_{IH}				120	µA
I_{LI}	Input Leakage Current	0V ≤V_{IN} ≤V_{CC}				1	µA
I_{LO}	Output Leakage Current	$\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}				1	µA
I_{ZZ}(3)	Deep-Power Down Current	V_{IN} = V_{IH} or V_{IL}			10		µA
V_{IH}	Input High Voltage			1.4		V_{CCQ} + 0.2	V
V_{IL}	Input Low Voltage			–0.2		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.2mA		0.8V_{CCQ}			V
V_{OL}	Output Low Voltage	I_{OL} = 0.2mA				0.2V_{CCQ}	V

Note: 1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive the output capacitance expected in the actual system.
2. I_{SB}(Max) values are measured with RCR2 to RCR0 bits set to '000' (full array refresh) and RCR6 to RCR5 bits set to '11' (temperature compensated refresh threshold at +85°C). In order to achieve low standby current, all inputs must be driven either to V_{CCQ} or V_{SS}. ISB may be slightly higher for up to 500 ms after power-up or when entering Standby mode.
3. The Operating Temperature is +25°C.

Table 14. PAR and TCSR Specifications and Conditions

Symbol	Parameter	Test Condition	Refreshed Memory Areas	Maximum Operating Temperature(2)				Unit
				+15°C RCR[6-5]=10	+45°C RCR[6-5]=01	+70°C RCR[6-5]=00	+85°C RCR[6-5]=11	
I_{SB}(1)	Maximum Standby Current in TCSR and PAR Modes	$V_{IN} = V_{IH}$ or V_{IL}, $\overline{E} = V_{IH}$	Full	70	85	105	120	µA
			1/2	65	80	100	115	
			1/4	60	75	95	110	
			1/8	57	70	90	105	
			0	50	55	60	70	

Note: 1. In order to achieve low standby current, all inputs must be driven to either VCCQ or VSS. ISB may be slightly higher for up to 500 ms after power-up or when entering Standby mode.
2. RCR values for 85°C are 100 percent tested. TCR values for 15°C, 45°C and 70°C are sampled only.

Figure 15. Asynchronous Random Read AC Waveforms

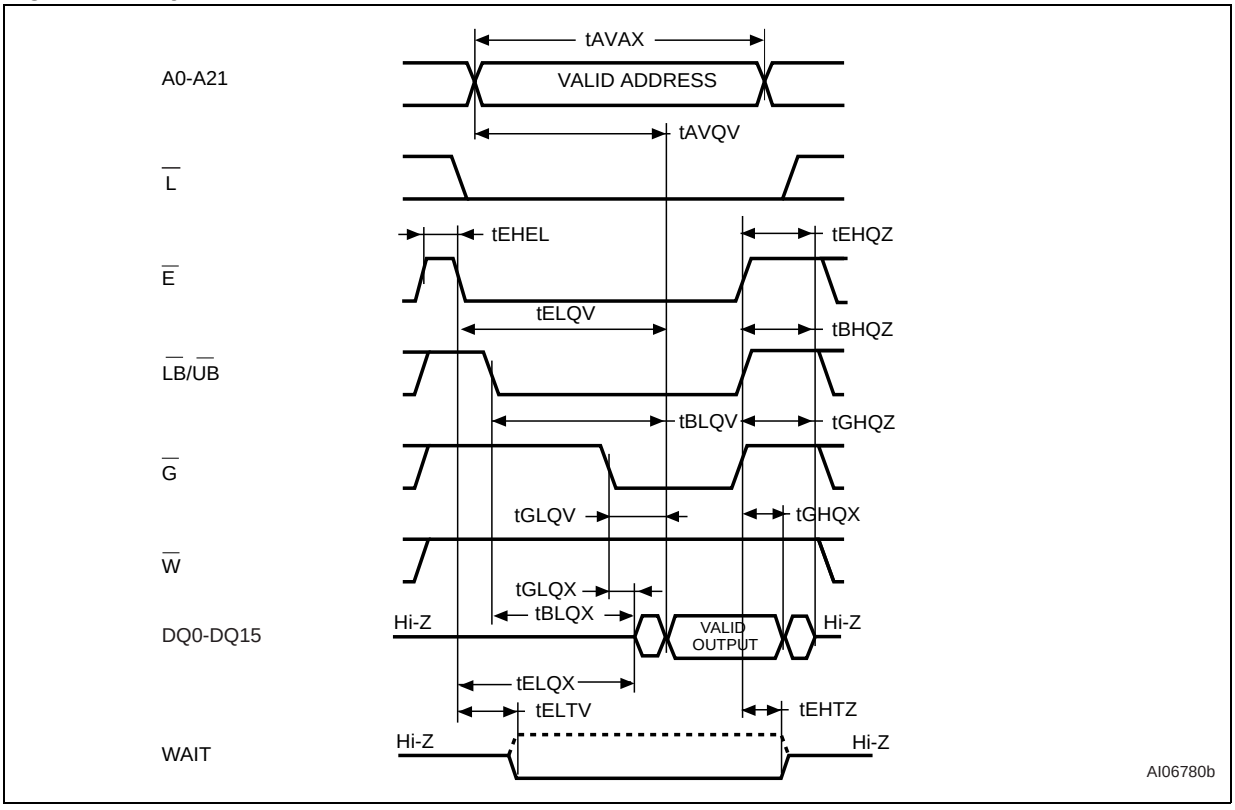


Figure 16. $\overline{L}$ Controlled Asynchronous Random Read AC Waveforms

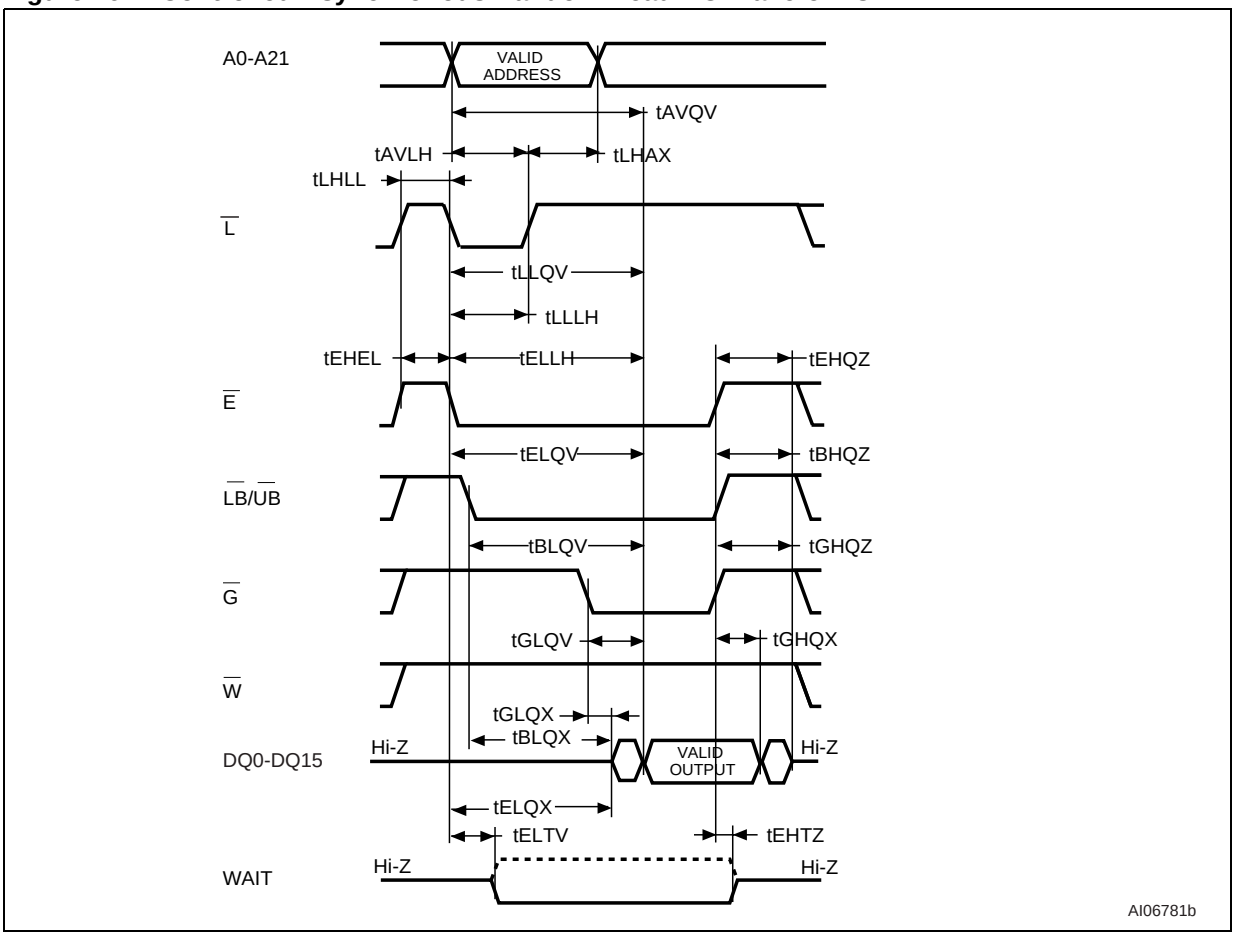


Figure 17. Asynchronous Page Read AC Waveforms

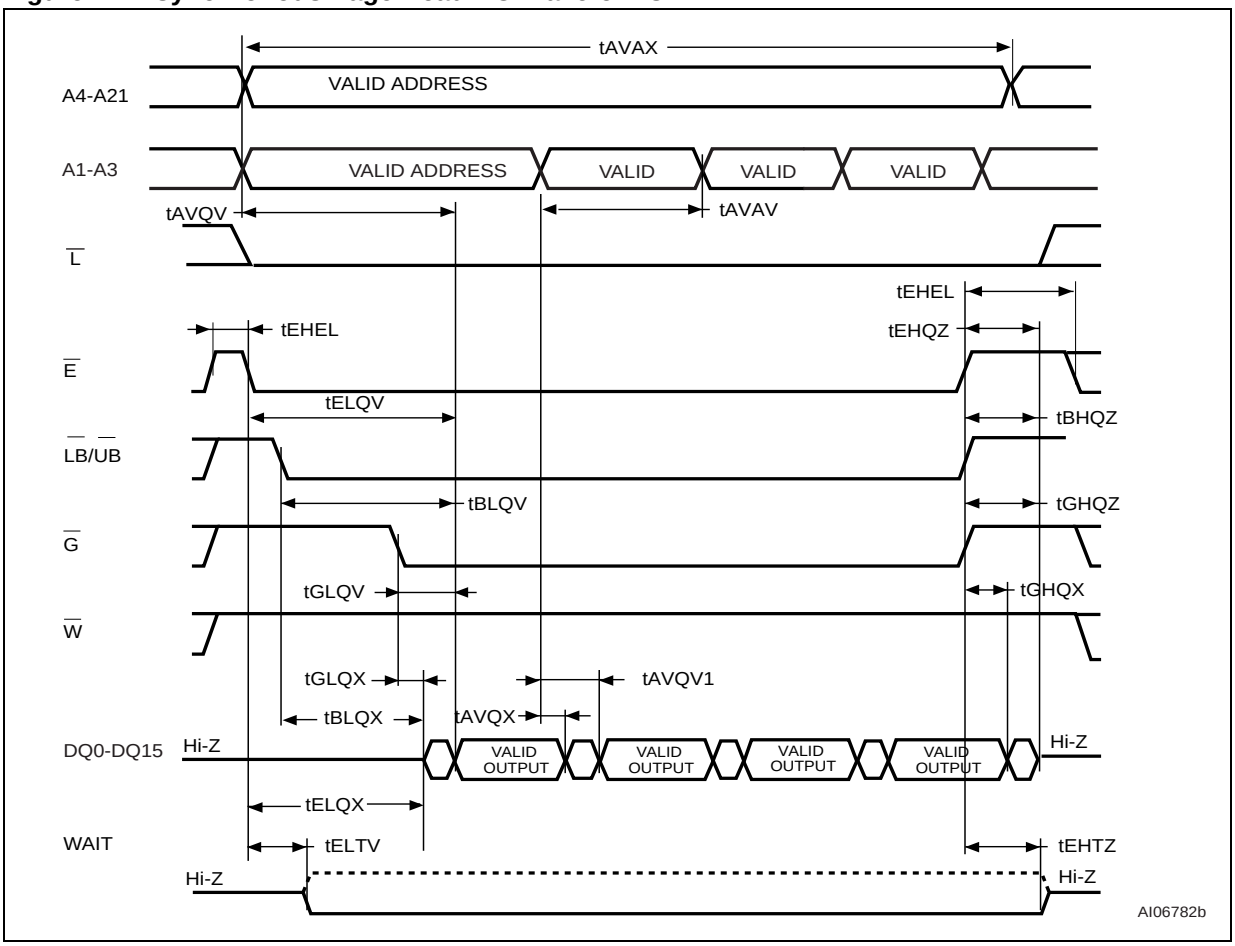
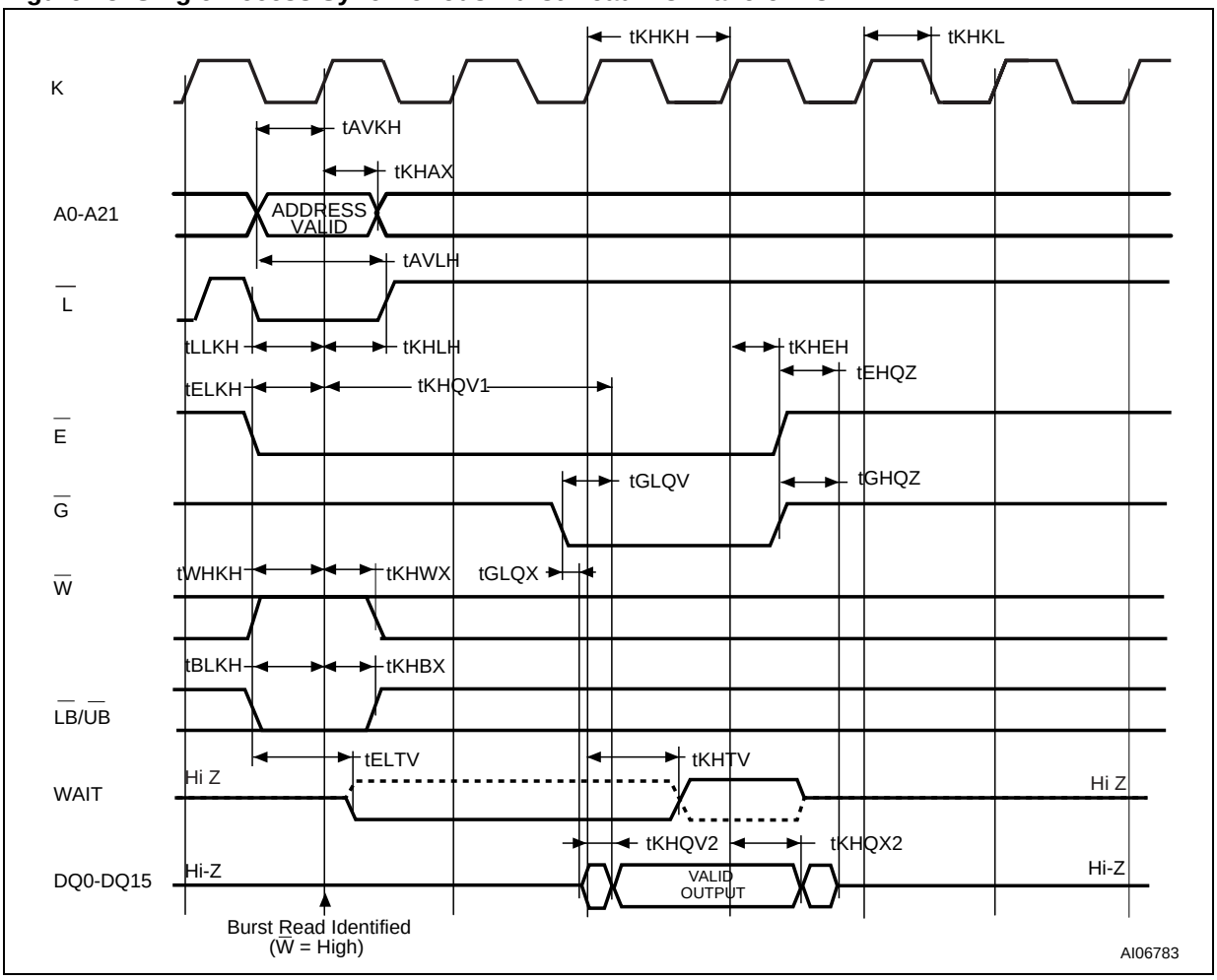


Table 15. Asynchronous Read AC Characteristics

Symbol	Alt.	Parameter	M69KB096AA				Unit
			70ns		85ns		
			Min	Max	Min	Max	
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70		85	ns
t_{LLQV}	t_{AADV}	$\overline{L}$ Low to Output Valid		70		85	ns
t_{AVQV1}	t_{APA}	Page Access Time		20		25	ns
t_{LHAX}	t_{AVH}	$\overline{L}$ High to Address Transition	5		5		
t_{AVLH}	t_{AVS}	Address Valid to $\overline{L}$ High	10		10		
t_{BLQV}	t_{BA}	Upper/Lower Byte Enable Low to Output Valid		70		85	ns
t_{BHQZ}(4)	t_{BHZ}	Upper/Lower Byte Enable High to Output Hi-Z		8		8	ns
t_{BLQX}(3)	t_{BLZ}	Upper/Lower Byte Enable Low to Output Transition	10		10		ns
t_{EHEL}	t_{CBPH}	Chip Enable High between Subsequent Mixed-Mode Read Operations	5		5		ns
t_{ELEH}(2)	t_{CEM}	Maximum Chip Enable Pulse Width		8		8	µs
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{EHTZ}		Chip Enable high to WAIT High-Z		8		8	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid (Chip Select Access Time)		70		85	ns
t_{ELLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	10		10		ns
t_{EHQZ}(4)	t_{HZ}	Chip Enable High to Output Hi-Z		8		8	ns
t_{ELQX}(3)	t_{LZ}	Chip Enable Low to Output Transition	10		10		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	5		5		ns
t_{AVQX}	t_{OHA}	Data Hold from Address Change	5		5		ns
t_{GHQZ}(4)	t_{OHZ}	Output Enable High to Output Hi-Z		8		8	ns
t_{GLQX}(3)	t_{OLZ}	Output Enable Low to Output Transition	5		5		ns
t_{AVAV}	t_{PC}	Page Cycle Time	20		25		
t_{AVAX}	t_{RC}	Read Cycle Time	70		85		ns
t_{LLLH}	t_{VP}	$\overline{L}$ Pulse Width Low	10		10		ns
t_{LHLL}	t_{VPH}	$\overline{L}$ Pulse Width High	10		10		ns

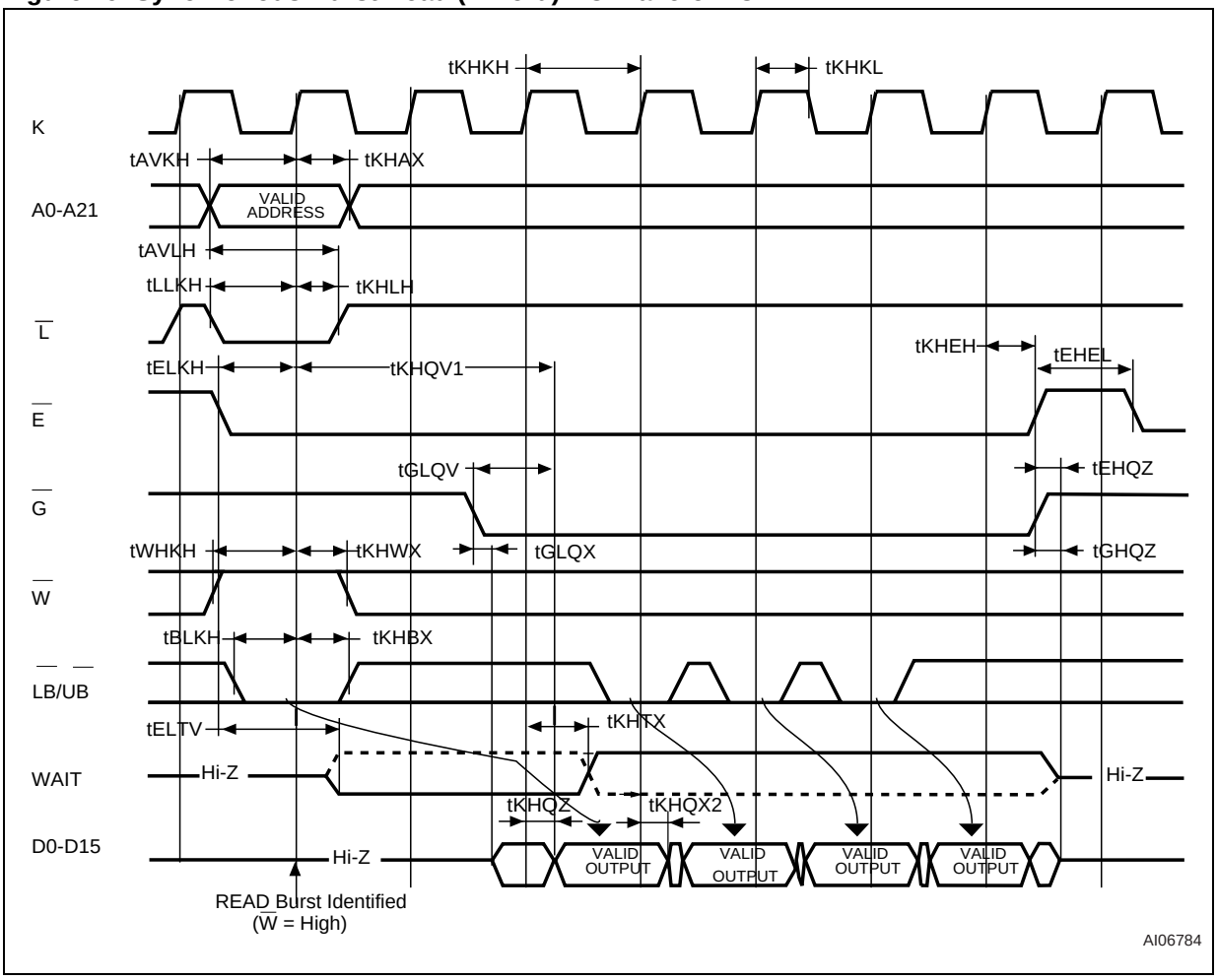
Note: 1. All the tests are performed with the outputs configured in “Full drive” strength (BCR5=’0’).
2. The timing is related to Asynchronous Page mode only.
3. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14.. The transition timings measure a transition of 100mV between the High-Z level ($V_{CCQ}/2$) and V_{OH} or V_{OL}.
4. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14.. The High-Z timings measure a transition of 100mV between V_{OH} or V_{OL} and $V_{CCQ}/2$.

Figure 18. Single Access Synchronous Burst Read AC Waveforms



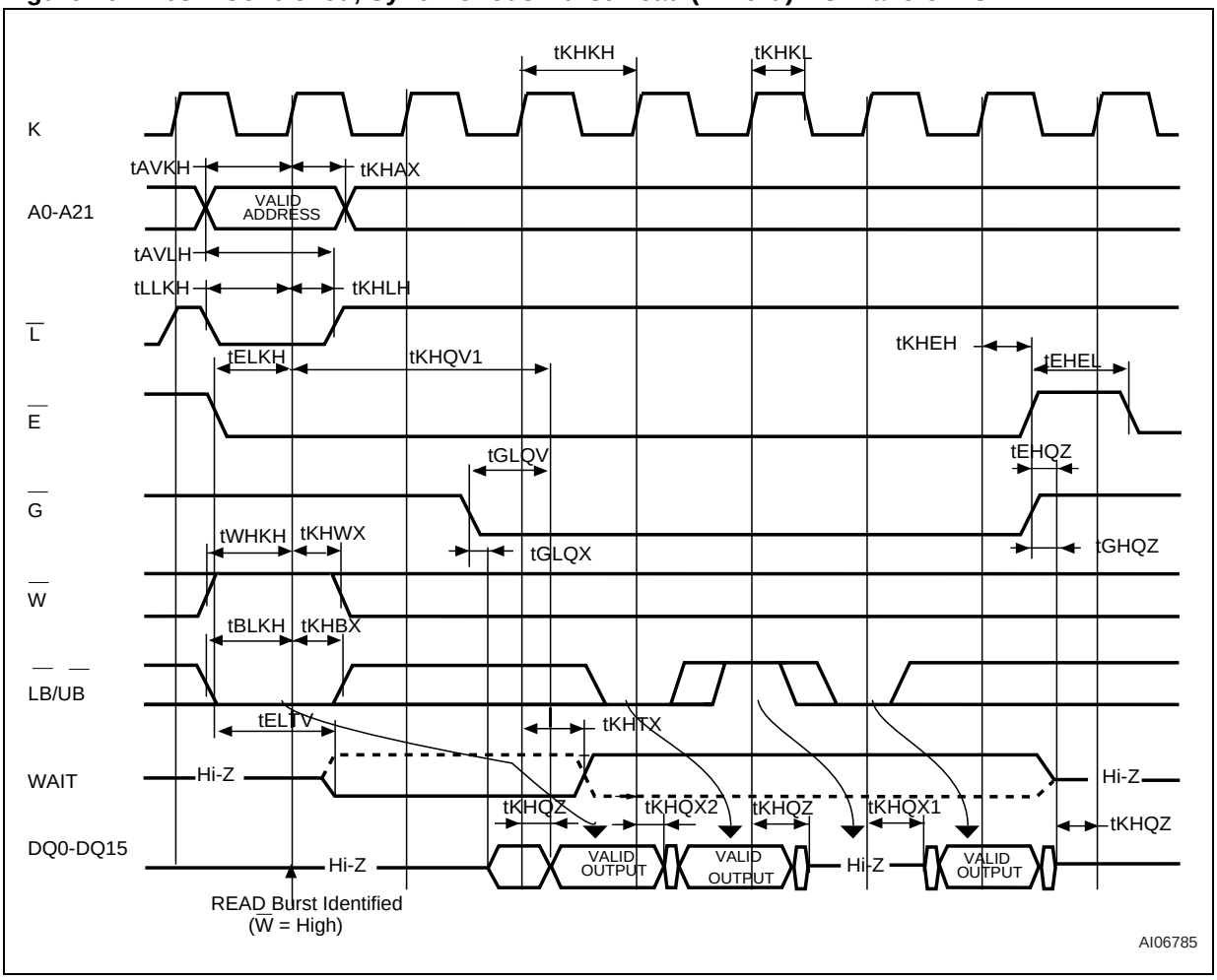
Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low; WAIT asserted during delay.
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 19. Synchronous Burst Read (4-word) AC Waveforms



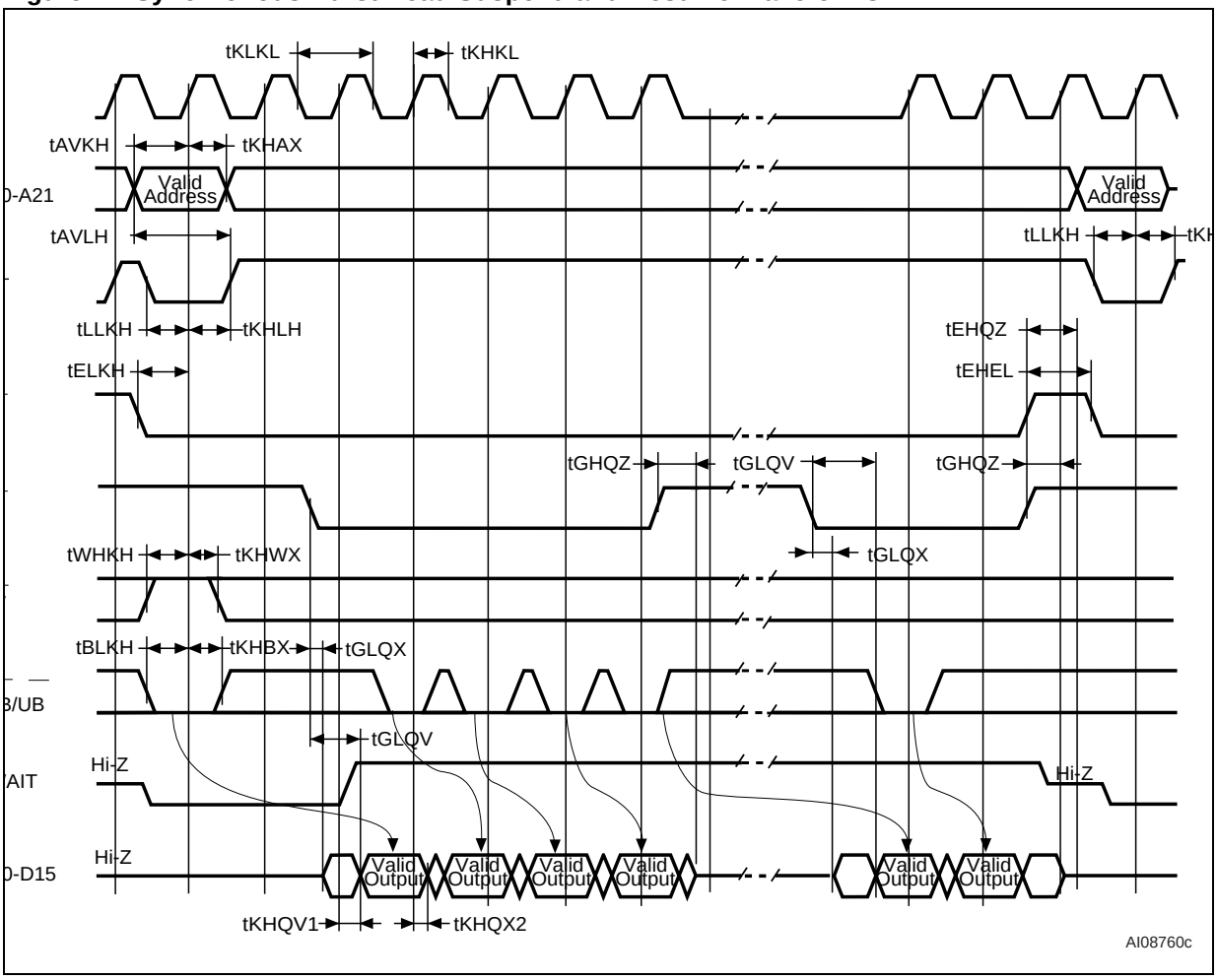
Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low; WAIT asserted during delay.
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 20. $\overline{LB}$/$\overline{UB}$ Controlled, Synchronous Burst Read (4-word) AC Waveforms



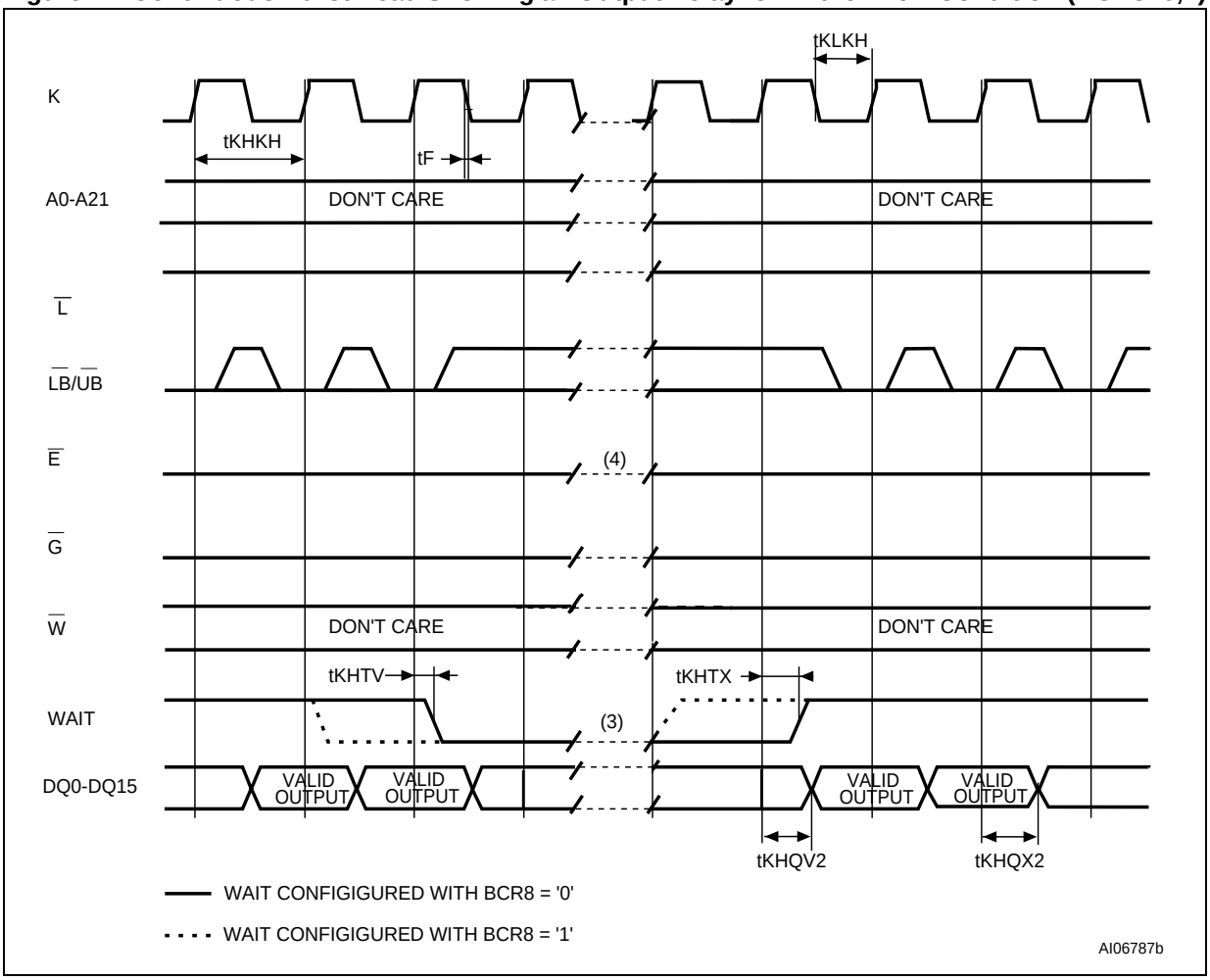
Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low; WAIT asserted during delay.
2. The Burst Length bits BCR0 to BR2 are set to '001' (4 Words).
3. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 21. Synchronous Burst Read Suspend and Resume Waveforms



Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low; WAIT asserted during delay.
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 22. Continuous Burst Read Showing an Output Delay for End-of-Row Condition (BCR8=0,1)



Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low, WAIT asserted during delay; Burst Wrap bit BCR3 set to '0' (wrap).
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.
3. WAIT will be asserted for a maximum of 2xLC Cycles (LC being the Latency code set through BCR[13-11]).
4. $\overline{E}$ must not remain Low longer that t_{ELEH}.

Table 16. Synchronous Burst Read AC Characteristics

Symbol	Alt.	Parameter	M69KB096AA				Unit
			80MHz		66MHz		
			Min	Max	Min	Max	
t_{KHQV1}	t_{ABA}	Burst Access Time		46.5		56	ns
t_{KHQV2}	t_{ACLK}	Delay From Clock High to Output Valid		9		11	ns
t_{AVLH}	t_{AVS}	Address Valid to $\overline{L}$ High	10		10		ns
t_{GLQV}	t_{BOE}	Delay From Output Enable Low to Output Valid in Burst mode		20		20	ns
t_{EHEL}(5)	t_{CBPH}	Chip Enable High between Subsequent Mixed-Mode Read Operations	5		5		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{ELEH}(5)	t_{CEM}	Maximum Chip Enable Low Pulse		8		8	ns
t_{KHKH}(4)	t_{CLK}	Clock Period	12.5	20	15	20	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	4.5	20	5	20	ns
t_{KHAX} t_{KHBX} t_{KHWX} t_{KHEH} t_{KHLH}	t_{HD}	Hold Time From Active Clock Edge	2		2		ns
t_{EHQZ}(2)	t_{HZ}	Chip Enable High to Output Hi-Z		8		8	ns
t_R t_F	t_{KHKL}	Clock Rise Time Clock Fall Time		1.8		2.0	ns
t_{KHTV} t_{KHTX}	t_{KHTL}	Clock High to WAIT Valid Clock High to WAIT Transition		9		11	ns
t_{KHQZ}	t_{KHZ}	Clock High to Output Hi-Z	3	8	3	8	ns
t_{KHQX1}	t_{KLZ}	Clock High to Output Transition	2	5	2	5	ns
t_{KHQX2}	t_{KOH}	Output Hold from Clock High	2		2		ns
t_{KHKL} t_{KLKH}	t_{KP}	Clock High to Clock Low Clock Low to Clock High	4		5		ns
t_{GHQZ}(2)	t_{OHZ}	Output Enable High to Output Hi-Z		8		8	ns
t_{GLQX}(3)	t_{OLZ}	Output Enable Low to Output Transition	5		5		ns
t_{AVKH} t_{LLKH} t_{BLKH} t_{WHKH} t_{CHKH}	t_{SP}	Set-up Time to Active Clock Edge	3		3		ns

Note: 1. All the tests are performed with the outputs configured in “Full drive” strength (BCR5=‘0’).
2. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14.. The High-Z timings measure a transition of 100mV between V_{OH} or V_{OL} and $V_{CCQ}/2$.
3. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14.. The transition timings measure a transition of 100mV between the High-Z level ($V_{CCQ}/2$) and V_{OH} or V_{OL}.
4. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.
5. When configured in Synchronous mode (BCR15 = 0), a refresh opportunity must be provided every t_{ELEH}. A refresh opportunity is satisfied by either of the following two conditions: $\overline{E} = V_{IH}$ during Clock input K rising edge or $E = V_{IH}$ for longer than 15ns.

Figure 23. Chip Enable Controlled, Asynchronous Write AC Waveforms

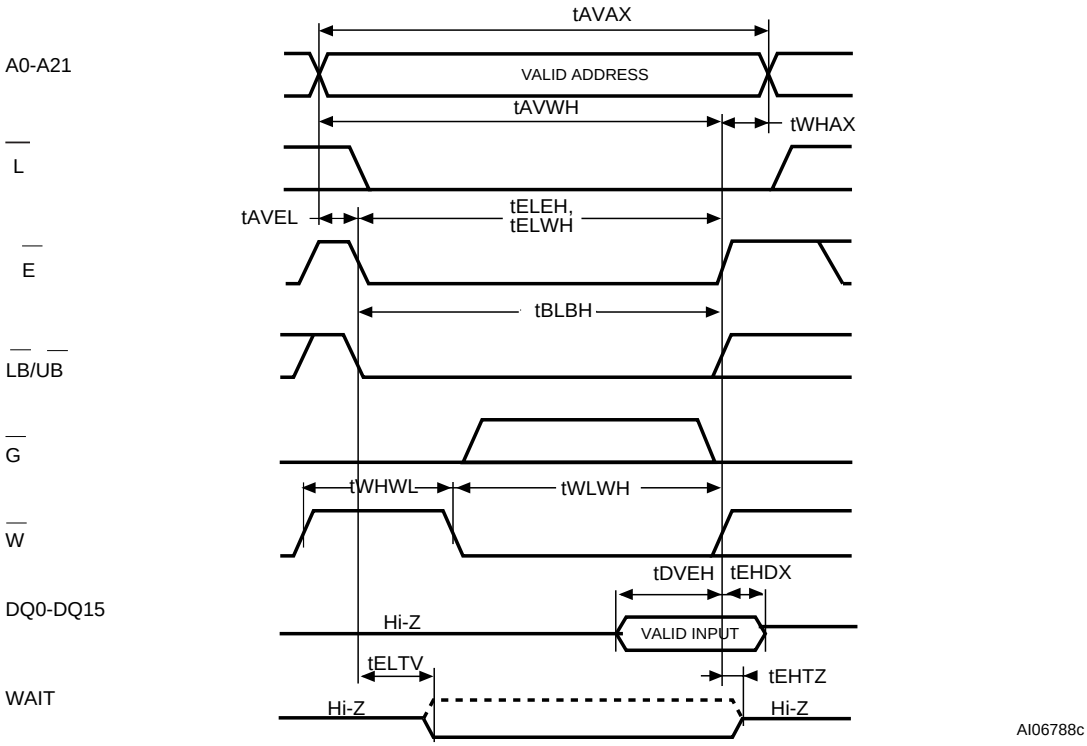


Figure 24. $\overline{LB}$/$\overline{UB}$ Controlled, Asynchronous Write AC Waveforms

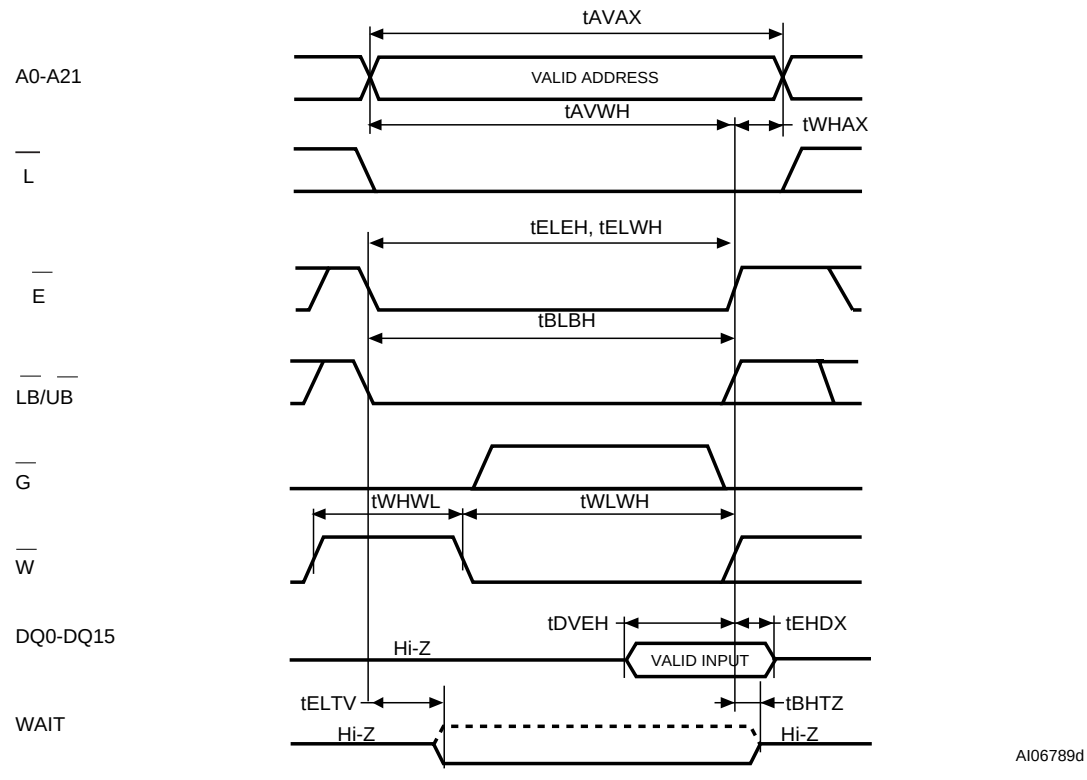


Figure 25. Write Enable Controlled, Asynchronous Write AC Waveforms

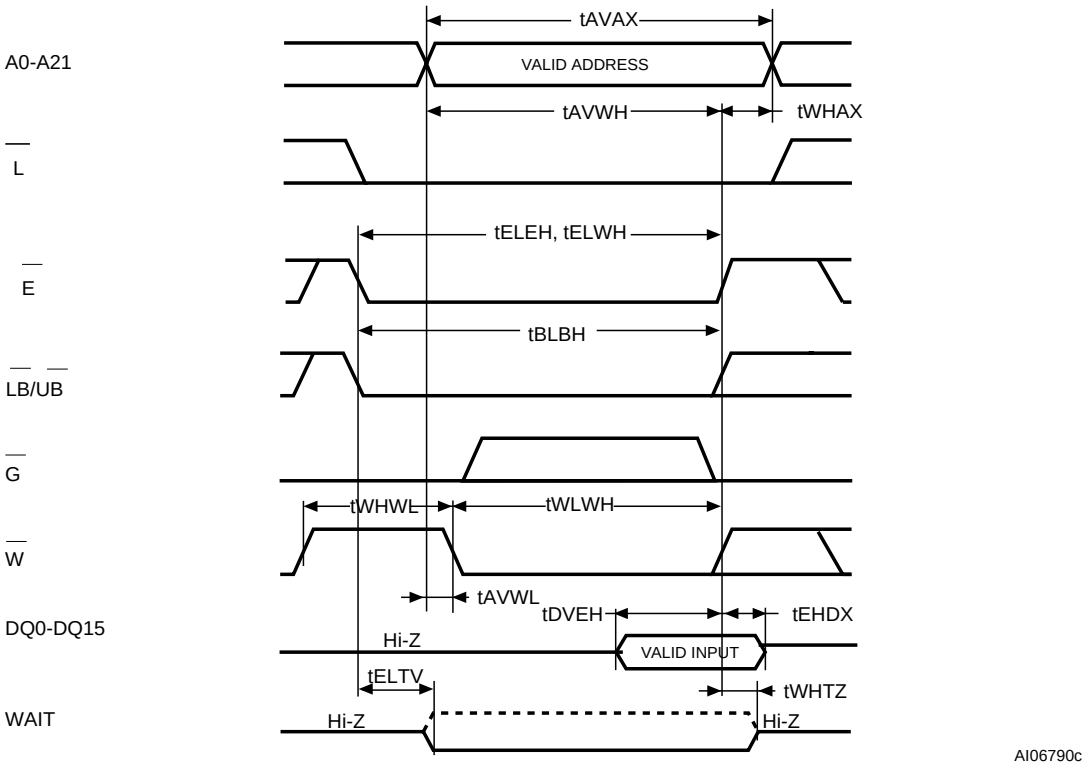


Figure 26. $\overline{L}$ Controlled, Asynchronous Write AC Waveforms

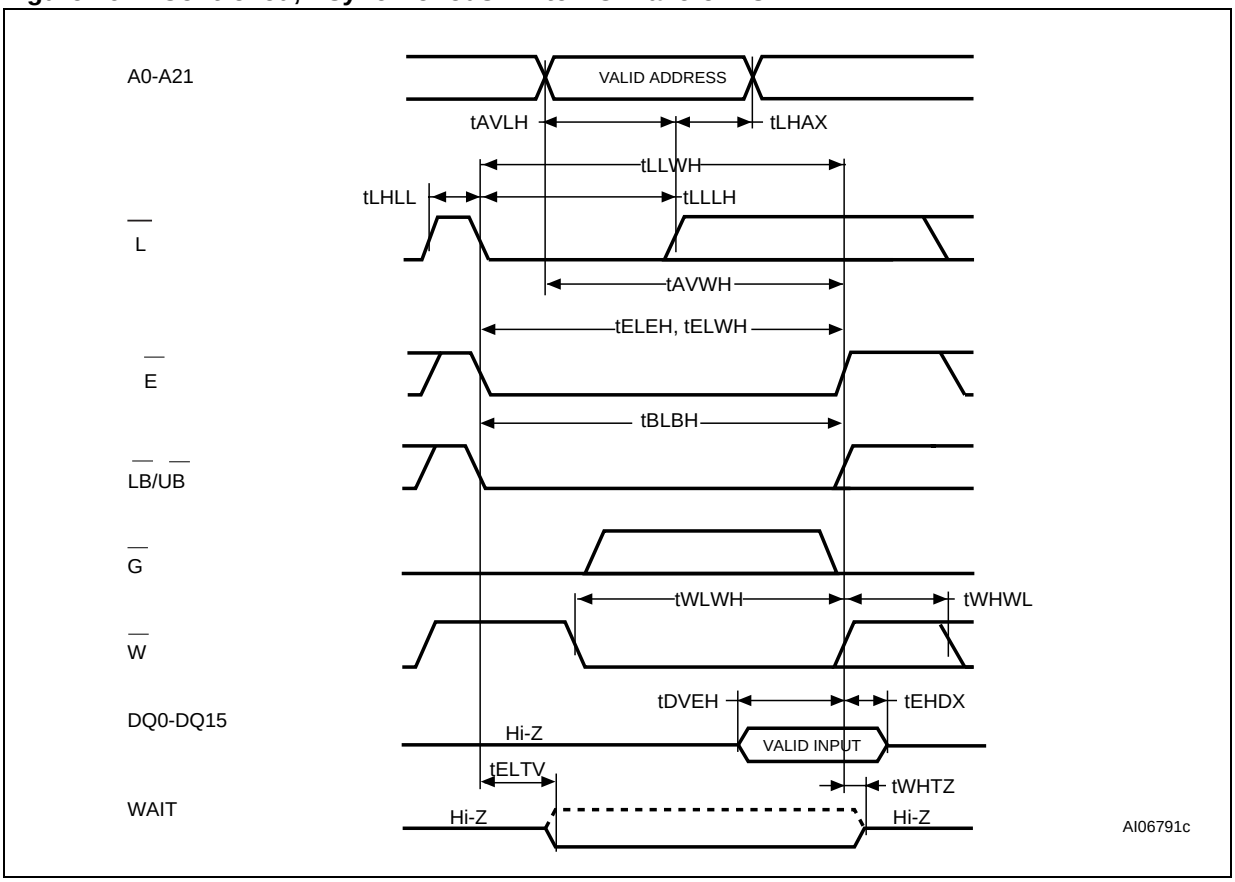
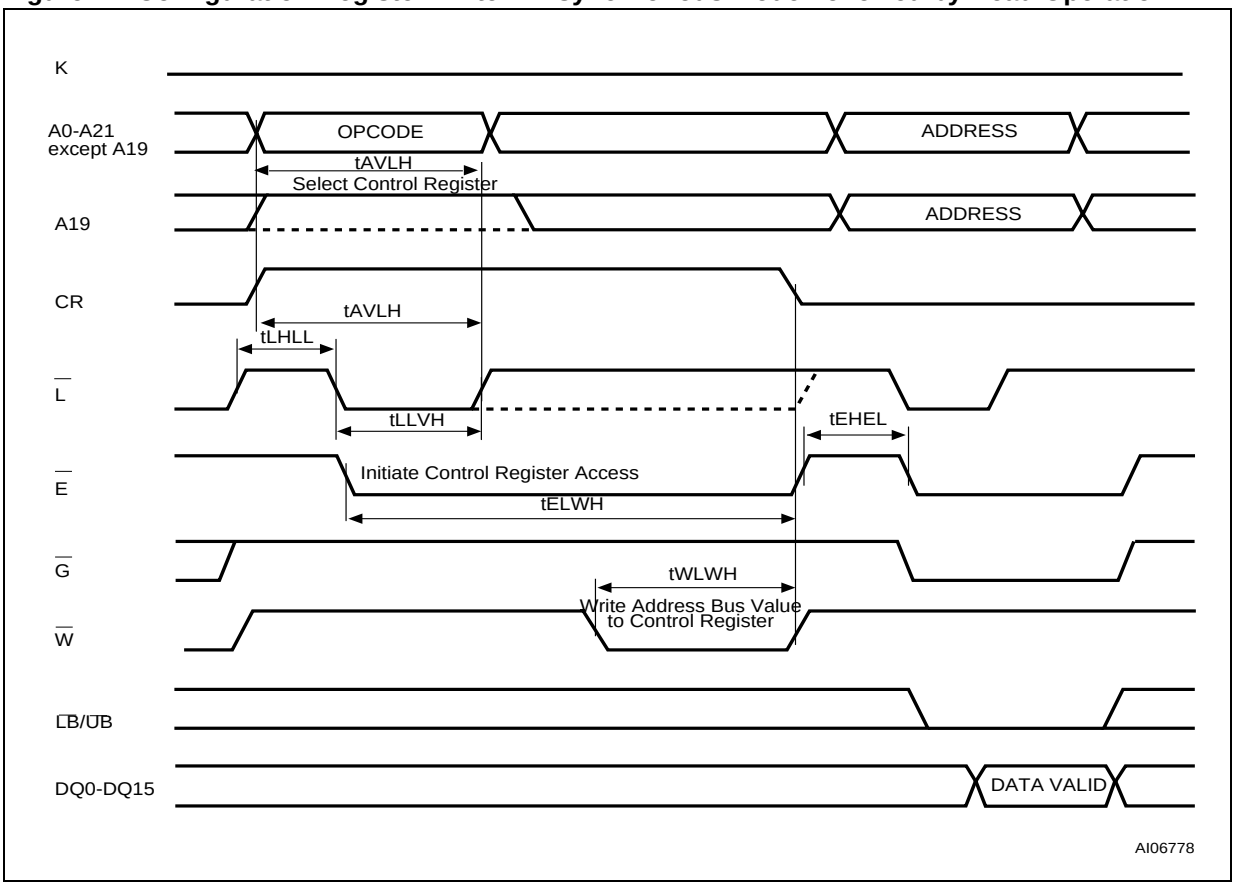
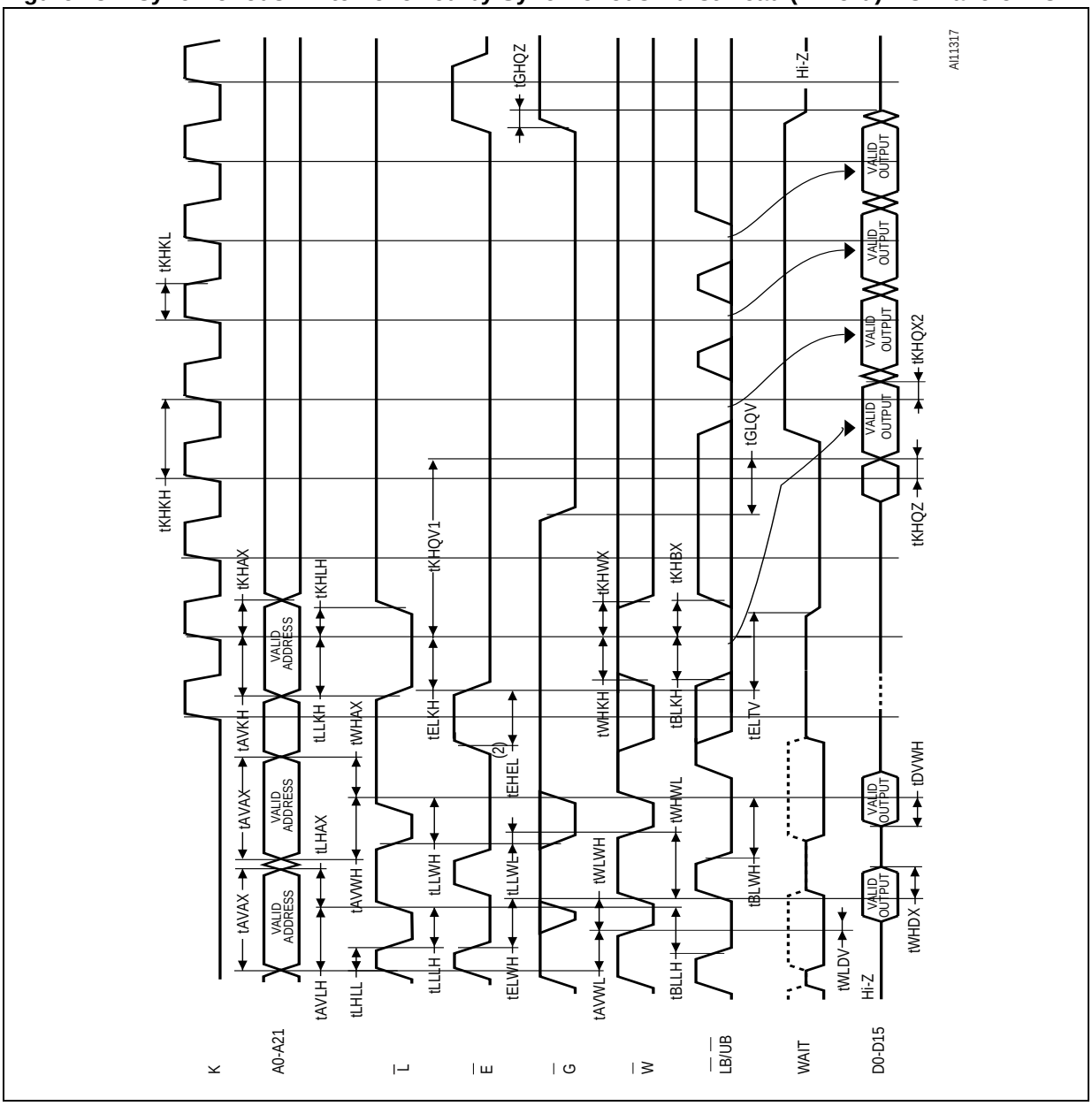


Figure 27. Configuration Register Write in Asynchronous Mode Followed by Read Operation



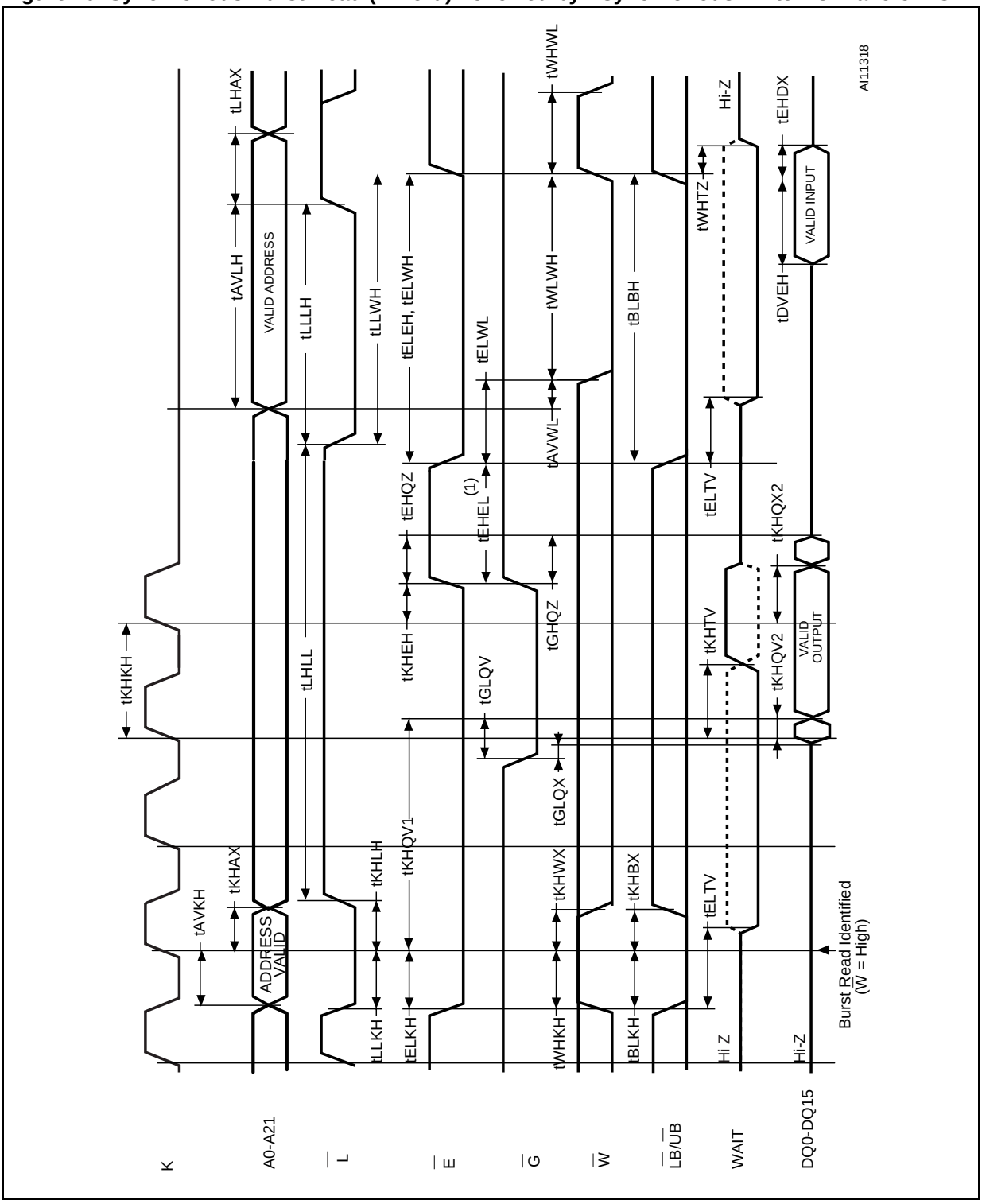
Note: 1. Non default BCR Register settings: Latency code two (three clocks); WAIT active Low; Hold data one clock; WAIT asserted during delay.
2. A19 = V_{IL} to load RCR; A19 = V_{IH} to load BCR.

Figure 28. Asynchronous Write Followed by Synchronous Burst Read (4-word) AC Waveforms



Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low; WAIT asserted during delay.
2. When configured in Synchronous mode (BCR15 = 0), a refresh opportunity must be provided every t_{ELEH}. A refresh opportunity is satisfied by either of the following two conditions: $\overline{E} = V_{IH}$ during Clock input K rising edge or $E = V_{IH}$ for longer than 15ns.
3. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 29. Synchronous Burst Read (4-word) Followed by Asynchronous Write AC Waveforms



Note: 1. When configured in Synchronous mode (BCR15 = 0), a refresh opportunity must be provided every t_{ELEH}. A refresh opportunity is satisfied by either of the following two conditions: $\overline{E} = V_{IH}$ during Clock input K rising edge or $E = V_{IH}$ for longer than 15ns.

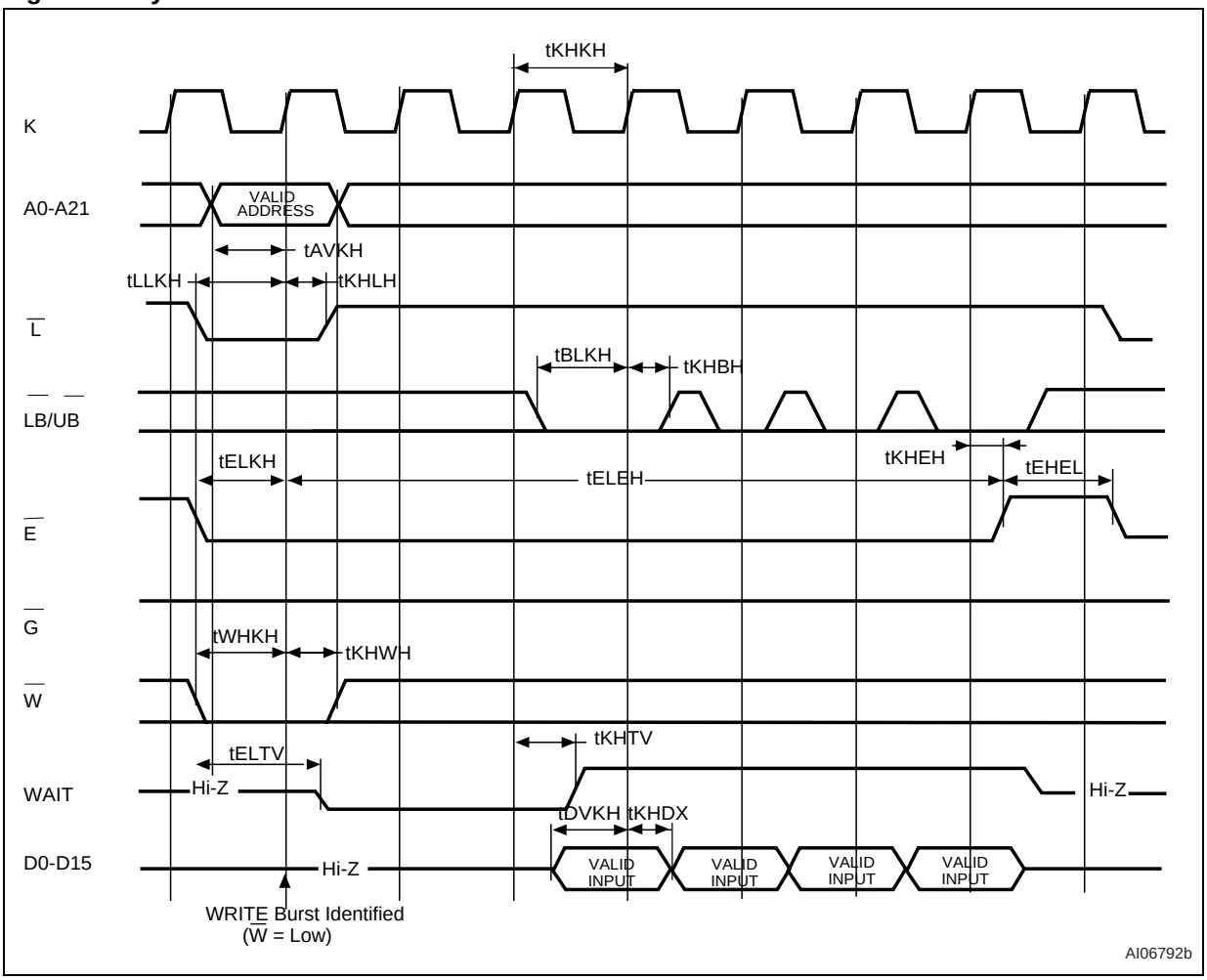
Table 17. Asynchronous Write AC Characteristics

Symbol	Alt.	Parameter	M69KB096AA				Unit
			70ns		85ns		
			Min	Max	Min	Max	
t_{AVEL} t_{AVWL} t_{AVBL} t_{LLWL} t_{ELWL}	t_{AS}	Address Setting Time	0		0		µs
t_{LHAX}	t_{AVH}	$\overline{L}$ High to Address Transition	5		5		ns
t_{AVLH}	t_{AVS}	Address Valid to $\overline{L}$ High	10		10		ns
t_{AVWH} t_{AVBH}	t_{AW}	Address Valid to Write Enable High Address Valid to Upper/Lower Byte Enable Transition	70		85		ns
t_{BLBH} t_{BLEH} t_{BLWH}	t_{BW}	Upper/Lower Byte Enable Low to End of Write Operation	70		85		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{AXCH}	t_{CKA}	In Mixed-Mode Operation: Delay between Address Transition in Asynchronous Write mode and Clock High in Burst Read mode	70		85		ns
t_{EHEL}	t_{CPH}	Chip Enable High between Subsequent Asynchronous Operations	5		5		ns
t_{ELLH} t_{BLLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	10		10		ns
t_{ELBH} t_{ELWH}	t_{CW}	Chip Enable Low to End of Write Operation	70		85		ns
t_{EHDX} t_{WHDX} t_{BHDX}	t_{DH}	Input Hold from End of Write Operation	0		0		ns
t_{DVEH} t_{DVBH} t_{DVWH}	t_{DW}	Data to Write Time Overlap	23		23		ns
t_{LLLH}	t_{VP}	$\overline{L}$ Pulse Width Low	10		10		ns
t_{LHLL}	t_{VPH}	$\overline{L}$ Pulse Width High	10		10		ns
t_{LLWH}	t_{VS}	$\overline{L}$ Low to Write Enable High	70		85		ns
t_{AVAX} t_{WHWH}	t_{WC}	Write Cycle Time	70		85		ns
t_{WLBH} t_{WLEH} t_{WLWH}	t_{WP}	Write Pulse Width	46		55		ns
t_{WHWL}	t_{WPH}	Write Enable Pulse Width High	10		10		ns
t_{WHAX}	t_{WR}	Write Enable High to Address Transition	0		0		ns
t_{WLDV}	t_{WHZ}	Write Enable Low to Data Valid		8		8	ns

Symbol	Alt.	Parameter	M69KB096AA				Unit
			70ns		85ns		
			Min	Max	Min	Max	
t_{AVEL} t_{AVWL} t_{AVBL} t_{LLWL} t_{ELWL}	t_{AS}	Address Setting Time	0		0		µs
t_{LHAX}	t_{AVH}	$\overline{L}$ High to Address Transition	5		5		ns
t_{EHTZ} t_{BHTZ} t_{WHTZ}	t_{HZ}	Chip Enable High to WAIT Hi-Z $\overline{LB}$/$\overline{UB}$ High to WAIT Hi-Z Write Enable High to WAIT Hi-Z		8		8	ns

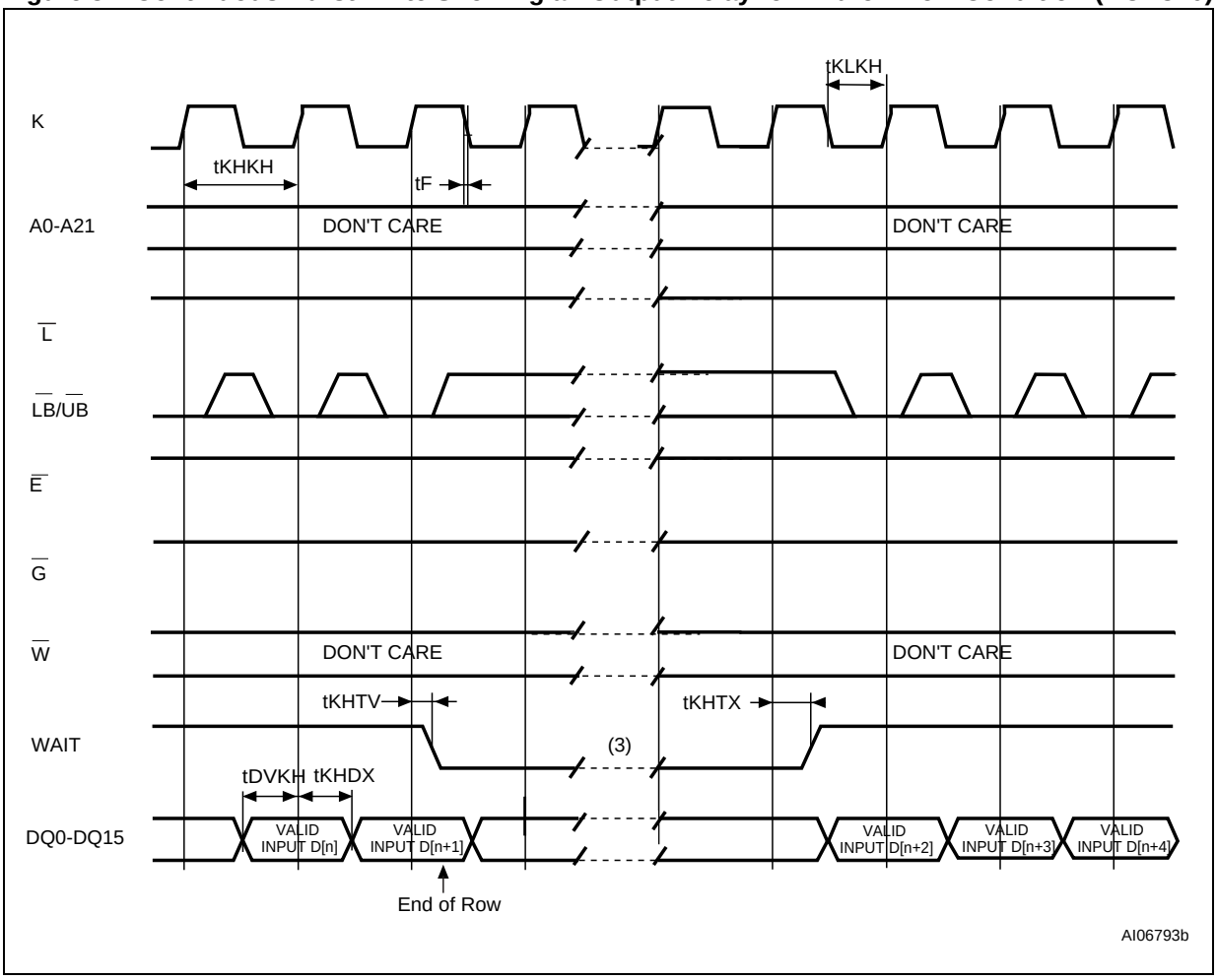
Note: 1. WE# LOW time must be limited to t_{CEM} (8 µs).
2. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14. The transition timings measure a transition of 100 mV between the High-Z level ($V_{CCQ/2}$) and V_{OH} or V_{OL}.
3. These timings have been obtained with the AC Measurement Load Circuit shown on Figure 14. The High-Z timings measure a transition of 100 mV between V_{OH} or V_{OL} and $V_{CCQ/2}$.

Figure 30. Synchronous Burst Write AC Waveform



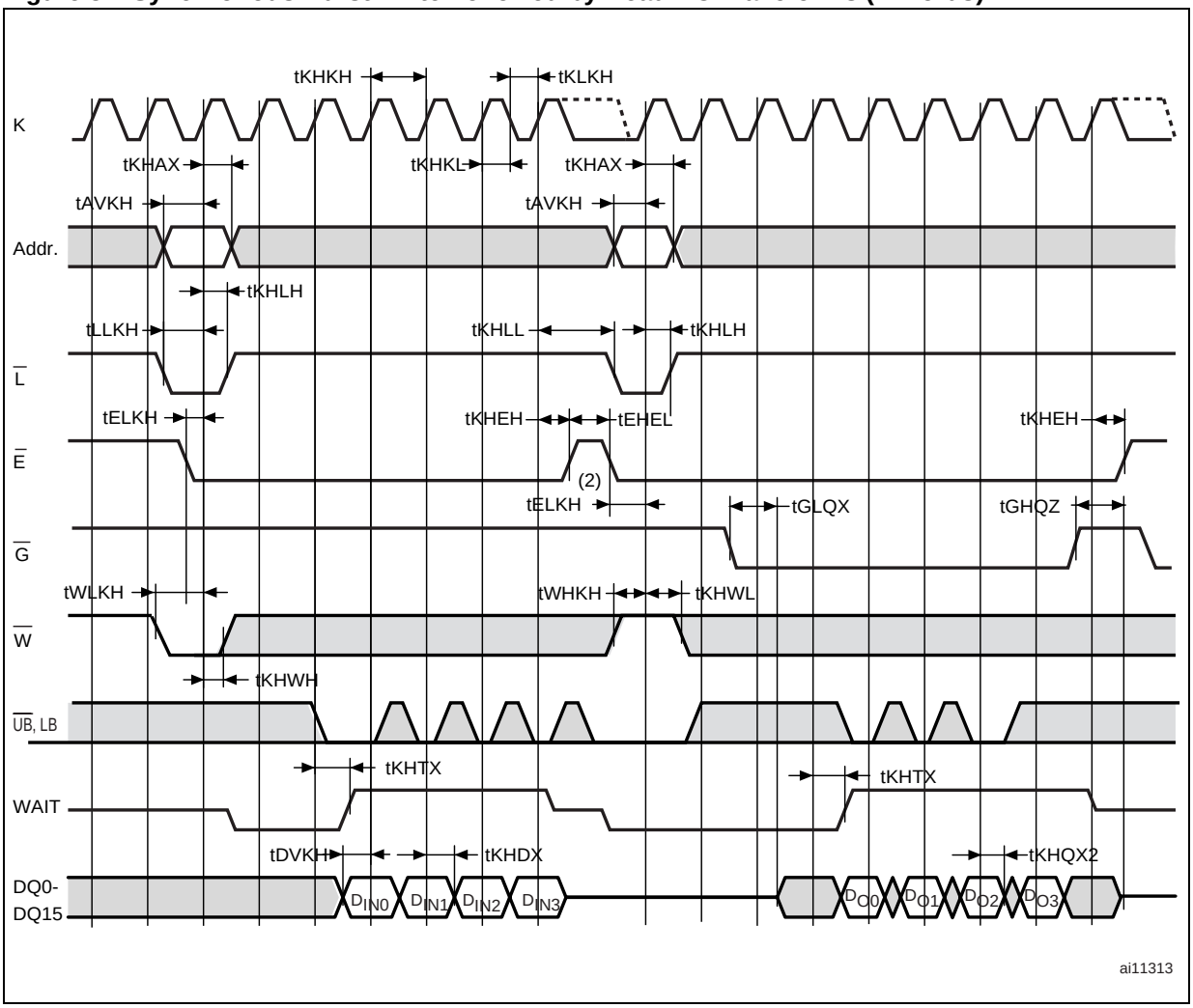
Note: 1. Non default BCR Register settings: Latency code two (three clocks); WAIT active Low; WAIT asserted during delay.
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 31. Continuous Burst Write Showing an Output Delay for End-of-R ow Condition (BCR8=0)



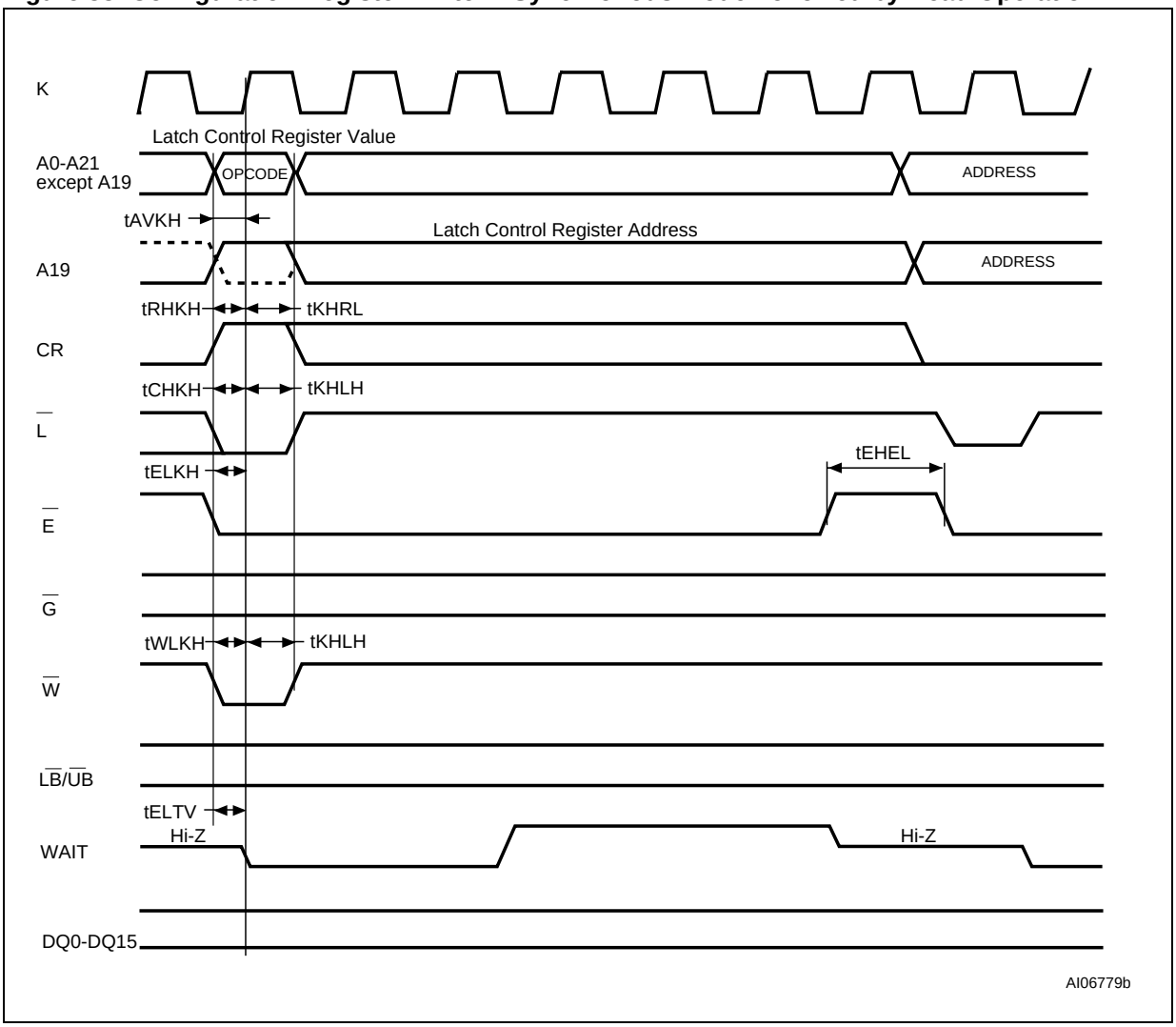
Note: 1. Non default BCR Register settings: 3 clock cycle latency; WAIT active Low, Burst Wrap bit BCR3 set to '0' (wrap).
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.
3. WAIT will be asserted for a maximum of (2xLC)+1 cycles (LC being the Latency Code set through BCR[13-11])
4. Taking $\overline{E}$ high or $\overline{L}$ Low will abort the Burst operation and the writing of the first data.

Figure 32. Synchronous Burst Write Followed by Read AC Waveforms (4 Words)



Note: 1. The Latency type can set to fixed or variable mode. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0). In fixed Latency mode, row boundary crossing
2. $\overline{E}$ can remain Low between the Burst Read and Burst Write operation, but it must not be held Low for longer than t_{ELEH}.

Figure 33. Configuration Register Write in Synchronous Mode Followed by Read Operation



Note: 1. Non default BCR Register settings: Latency code two (three clocks); WAIT active Low; Hold data one clock; WAIT asserted during delay.
2. A19 = V_{IL} to load RCR; A19 = V_{IH} to load BCR.

Table 18. Synchronous Burst Write AC Characteristics

Symbol	Alt.	Parameter	M69KB096AA				Unit
			80MHz		66MHz		
			Min	Max	Min	Max	
t_{EHEL}(1)	t_{CBPH}	Chip Enable High between Subsequent Mixed-Mode Read Operations	5		5		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{KHKH}(2)	t_{CLK}	Clock Period	12.5	20	15	20	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	4.5	20	5	20	ns
t_{KHAX} t_{KHBH} t_{KHWH} t_{KHEH} t_{KHLH} t_{KHRL}	t_{HD}	Hold Time From Active Clock Edge	2		2		ns
t_R t_F	t_{KHKL}	Clock Rise Time Clock Fall Time		1.8		2.0	ns
t_{KHTV}	t_{KHTL}	Clock High to WAIT Valid		9		11	ns
t_{KHKL}	t_{KP}	Clock High to Clock Low	4		5		ns
t_{AVKH} t_{BLKH} t_{WHKH} t_{WLKH} t_{CHKH} t_{RHKH}	t_{SP}	Set-up Time to Active Clock Edge	3		3		ns
t_{ELEH}(1)	t_{CEM}	Maximum Chip Enable Pulse Width		8		8	µs

Note: 1. When configured in Synchronous mode (BCR15 = 0), a refresh opportunity must be provided every t_{ELEH}. A refresh opportunity is satisfied by either of the following two conditions: $\overline{E} = V_{IH}$ during Clock input K rising edge or $\overline{E} = V_{IH}$ for longer than 15ns.
2. Clock rates lower than 50MHz (clock period higher than 20ns) are allowed as long as t_{ELKH} specifications are met.

Figure 34. Power-Up AC Waveforms

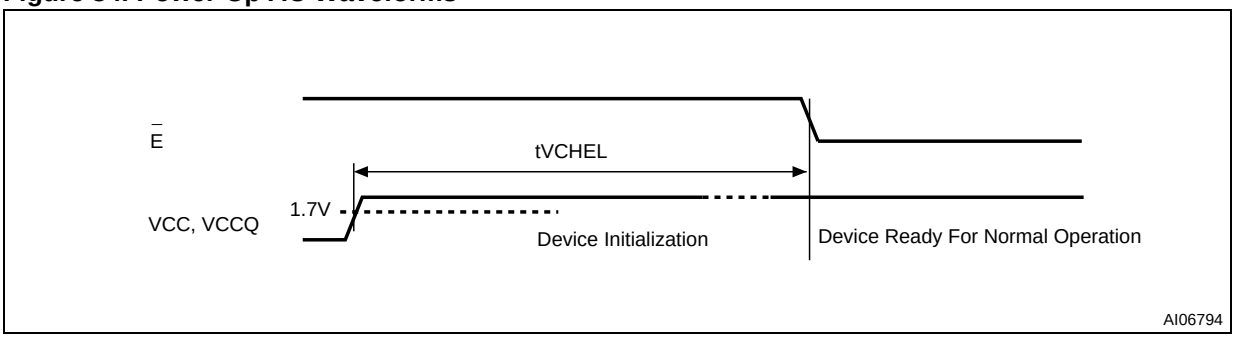


Table 19. Power-Up AC Characteristics

Symbol	Alt.	Parameter	M69KB096AA				Unit
			70ns		85ns		
			Min	Max	Min	Max	
t_{VCHEL}	t_{PU}	Initialization delay		150		150	µs

PART NUMBERING

Table 20. Ordering Information Scheme

Example: M69KB096 A A 70 C W 8

Device Type
M69 = PSRAM

Mode
K =Tested Die

Operating Voltage
B = V_{CC} = 1.7 to 1.95V, Burst, Address/Data Bus Standard x16

Array Organization
096 = 64 Mbit (4Mb x16)

Option
A = 1 Chip Enable

Die Revision
A = Revision A

Speed Class
70 = 70ns
85 = 85ns

Maximum Clock Frequency
A= 66 MHz Max Clock Frequency in Burst Read Mode
C= 80MHz Max Clock Frequency in Burst Read Mode

Package
W = Unsawn Wafer

Operating Temperature
8 = –30 to 85 °C

The notation used for the device number is as shown in Table 20.. Not all combinations are necessarily available. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

REVISION HISTORY

Table 21. Document Revision History

Date	Rev.	Revision Details
13-Oct-2004	0.1	First Issue.
11-Feb-2005	0.2	I_{SB} current for Standard Leakage option added in FEATURES SUMMARY. I_{SB} current for Standard Leakage option added in Table 13., DC Characteristics and test conditions updated. I_{TCR} current for Standard Leakage option added in Table 14., Temperature Compensated Refresh Specifications and Conditions. I_{PAR} current for Standard Leakage option added in Table 15., Partial Array Refresh Specifications and Conditions. Standard Leakage option added in Table 20., Ordering Information Scheme.
29-Apr-2005	1.0	Root Part Number changed to M69KB096AA. 104MHz maximum clock frequency and Low Leakage option removed. Temperature range updated to –30°C to +85°C. Clock Input (K). definition updated. Figure 3., Block Diagram modified. Bus Modes Tables 2, 3 and Synchronous Burst Mode paragraph updated. Output Impedance Bit (BCR5) renamed Driver Strength and definition updated. R1 and R2 updated in Table 13., DC Characteristics and Refresh Specifications and Conditions tables merged into Table 14.. Figures 15, 16, and 17 describing Asynchronous Read AC waveforms updated. Figures 18, 19, 20, 21 and 22 describing Synchronous Read AC waveforms updated. Figures 23, 24, and 25, describing Asynchronous Write AC waveforms updated. t_{AVWL} and t_{AVBL} added in Table 17., Asynchronous Write AC Characteristics. Figures 28 and 29 added. Figures 30, 31, and 32, describing Synchronous Write AC waveforms updated. Figure 32., Synchronous Burst Write Followed by Read AC Waveforms (4 Words) added. t_{RHKH} and t_{KHRL} added in Table 18., Synchronous Burst Write AC Characteristics Table 21., Bond Pad Location and Identification modified to express the pad coordinates from the center of the die.
16-June-2005	2.0	, FEATURES SUMMARY, OPERATING MODES and Figure 5., Synchronous Burst Write Mode (4-word burst) modified.
18-Aug-2005	3.0	Updated Note 2 in Table 13., page 23, added notes to Table 14., page 24 and Table 17., page 40. Deleted Note 5 from Table 15., page 27.
12-Dec-2005	4	Clock rate added in datasheet title. Test conditions for I_{CC1}, I_{CC1P}, I_{CC2}, I_{CC3R}, I_{CC3W} and I_{SB} updated in Table 13., DC Characteristics.
19-Jan-2006	5	Section Wafer and die specifications removed.