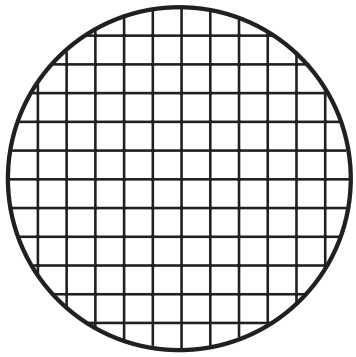
M69KB128AB

128 Mbit (8Mb x16) 1.8V Supply, Burst PSRAM

Preliminary Data

Feature summary

- Supply Voltage
  - V_{CC} = 1.7 to 1.95V core supply voltage
  - V_{CCQ} = 1.7 to V_{CC} for I/O buffers
- User-selectable Operating Modes
  - Asynchronous Modes: Random Read, and Write, Page Read
  - Synchronous Modes: NOR-Flash, Full Synchronous (Burst Read and Write)
- Asynchronous Random Read
  - Access Times: 70ns
- Asynchronous Page Read
  - Page Size: 4, 8 or 16 Words
  - Subsequent Read Within Page: 20ns
- Burst Read
  - Fixed Length (4, 8, 16 or 32 Words) or Continuous
  - Maximum Clock Frequency: 80 and 104MHz
  - Output delay: 7ns at 104MHz
- Low Power Consumption
  - Active Current: < 25mA
  - Standby Current: 200µA
  - Deep Power-Down Current: 10µA
- Low Power Features
  - Partial Array Self Refresh (PASR)
  - Deep Power-Down (DPD) Mode
- Operating Temperature
  - –30°C to +85°C



Wafer

M69KB128AB IS ONLY AVAILABLE AS PART OF A MULTI-CHIP PACKAGE

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1 Summary description

The M69KB128AB is a 128 Mbit (134,217,728 bit) PSRAM, organized as 8,388,608 Words by 16 bits. It uses a high-speed CMOS DRAM technology implemented using a one transistor-per-cell topology that achieves bigger array sizes. It provides a high-density solution for low-power handheld applications.

The M69KB128AB is supplied by a 1.7 to 1.95V supply voltage range.

The PSRAM interface supports various operating modes: Asynchronous Random Read and Write, Asynchronous Page Read and Synchronous mode that increases read/write speed.

In Asynchronous Random Read mode, the M69KB128AB is compatible with low power SRAMs. In Asynchronous Page mode the device has much shorter access times within the page that make it is compatible with the industry standard PSRAMs.

Two types of Synchronous modes are available:

- Flash-NOR: the device operates in Synchronous mode for read operations and Asynchronous mode for write operations.
- Full Synchronous: the device supports Synchronous transfers for both read and write operations.

The M69KB128AB features three configuration registers:

- Two user-programmable registers used to define the device operation: the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR).
- A read-only Device ID Register (DIDR) containing device identification.

The Bus Configuration Register (BCR) indicates how the device interacts with the system memory bus. The Refresh Configuration Register (RCR) is used to control how the memory array refresh is performed. At Power-Up, these registers are automatically loaded with default settings and can be updated any time during normal operation.

PSRAMs are based on the DRAM technology, but have a transparent internal self-refresh mechanism that requires no additional support from the system memory microcontroller.

To minimize the value of the Standby current during self-refresh operations, the M69KB128AB includes two system-accessible mechanisms configured via the Refresh Configuration Register (RCR):

- The Partial Array Self Refresh (PASR) performs a limited refresh of the part of the PSRAM array that contains essential data.
- The Deep Power-Down (DPD) mode completely halts the refresh operation. It is used when no essential data is being held in the device.

Figure 1. Logic diagram

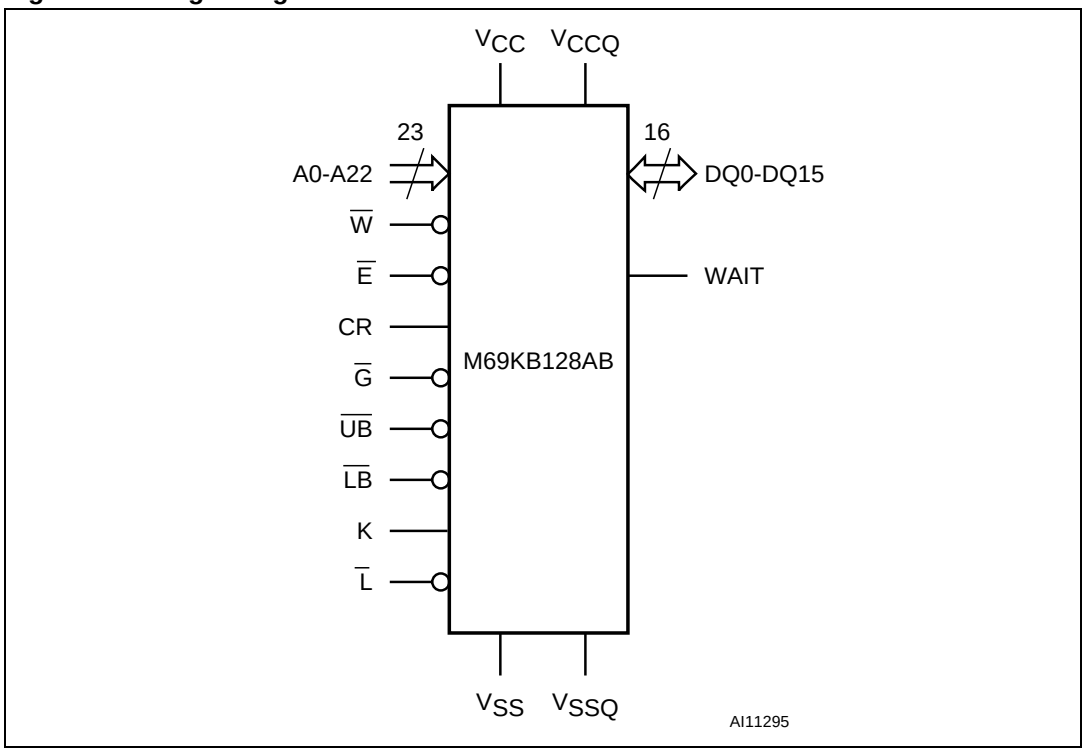
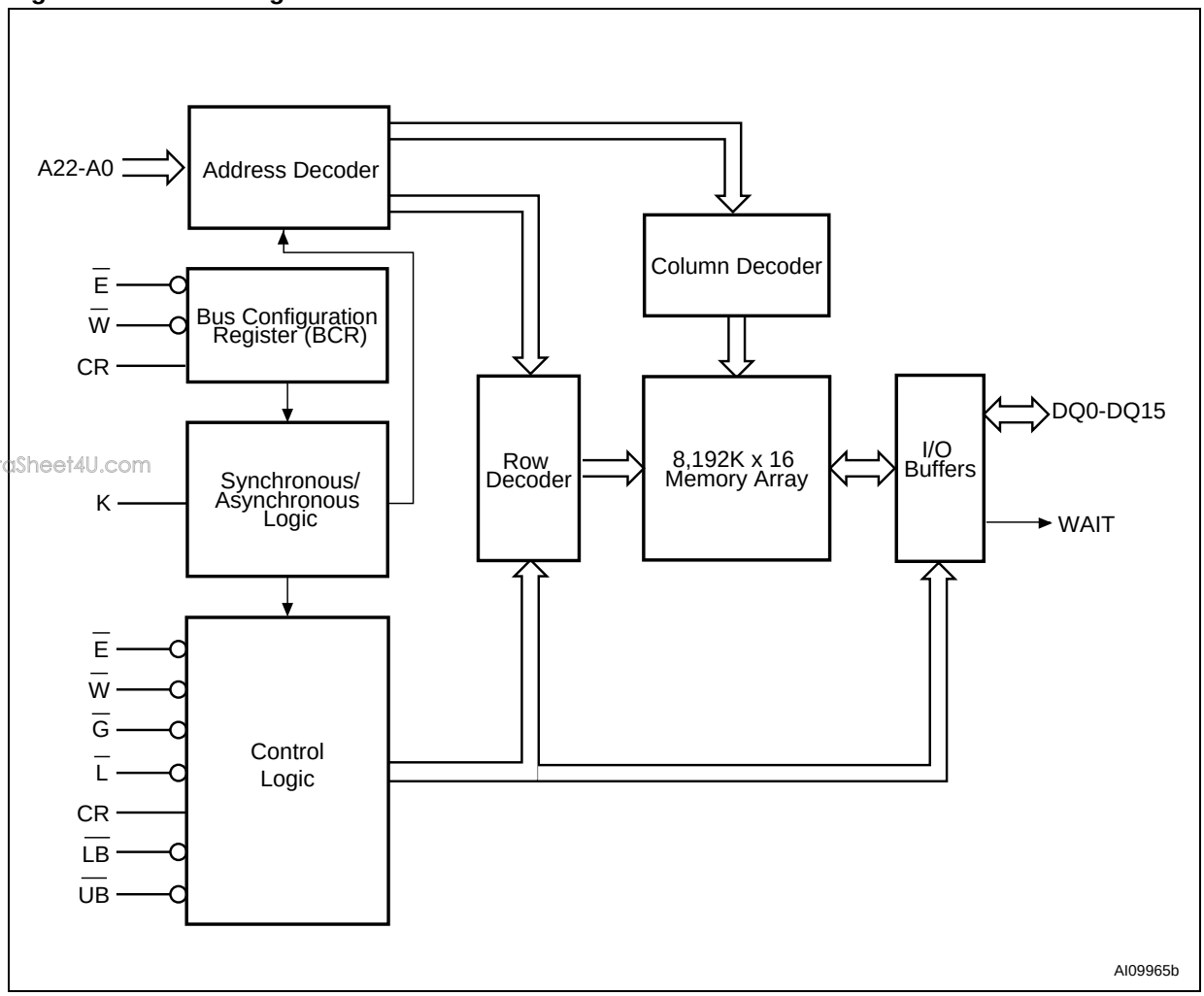


Table 1. Signal names

A0-A22	Address Inputs
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable Input
CR	Configuration Register Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
K	Clock Input
$\overline{L}$	Latch Enable Input
WAIT	Wait Output
V_{CC}	Core Supply Voltage
V_{CCQ}	Input/Output Buffers Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Buffers Ground

Figure 2. Block diagram



1. This functional block diagram illustrates simplified device operation.

2 Signal descriptions

The signals are summarized in *Figure 1: Logic diagram*, and *Table 1: Signal names*.

2.1 Address Inputs (A0-A22)

The Address Inputs select the cells in the memory array to access during read and write operations.

2.2 Data Inputs/Outputs (DQ8-DQ15)

The Upper Byte Data Inputs/Outputs carry the data to or from the upper part of the selected address during a write or read operation, when Upper Byte Enable ($\overline{UB}$) is driven Low. When disabled, the Data Inputs/Outputs are high impedance.

2.3 Data Inputs/Outputs (DQ0-DQ7)

The Lower Byte Data Inputs/Outputs carry the data to or from the lower part of the selected address during a write or read operation, when Lower Byte Enable ($\overline{LB}$) is driven Low. When disabled, the Data Inputs/Outputs are high impedance.

2.4 Chip Enable ($\overline{E}$)

Chip Enable, $\overline{E}$, activates the device when driven Low (asserted). When deasserted (V_{IH}), the device is disabled and goes automatically in low-power Standby mode or Deep Power-Down mode, according to the RCR settings.

2.5 Output Enable ($\overline{G}$)

When held Low, V_{IL}, the Output Enable, $\overline{G}$, enables the Bus Read operations of the memory.

2.6 Write Enable ($\overline{W}$)

Write Enable, $\overline{W}$, controls the Bus Write operation of the memory. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

2.7 Upper Byte Enable ($\overline{UB}$)

The Upper Byte Enable, $\overline{UB}$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a write or read operation.

2.8 Lower Byte Enable ($\overline{LB}$)

The Lower Byte Enable, $\overline{LB}$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}$ and $\overline{UB}$ are disabled (High), the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as $\overline{E}$ remains Low.

2.9 Clock Input (K)

The Clock, K, is an input signal to synchronize the memory to the microcontroller or system bus frequency during Synchronous Burst Read and Write operations. The Clock input signal increments the device internal address counter.

The addresses are latched on the rising edge of the Clock K, when $\overline{L}$ is Low during Synchronous Bus operations.

Latency counts are defined from the first Clock rising edge after $\overline{L}$ falling edge to the first data input latched or the first data output valid.

The Clock input is required during all synchronous operations and must be kept Low during asynchronous operations.

2.10 Configuration Register Enable (CR)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the Refresh Configuration Register (RCR) or the Bus Configuration Register (BCR) according to the value of A19.

2.11 Latch Enable ($\overline{L}$)

In Synchronous mode, addresses are latched on the rising edge of the Clock K when the Latch Enable input, $\overline{L}$ is Low. In Asynchronous mode, addresses are latched on $\overline{L}$ rising edge.

2.12 Wait (WAIT)

The WAIT output signal provides data-valid feedback during Synchronous Burst Read and Write operations. The signal is gated by $\overline{E}$. Driving $\overline{E}$ High while WAIT is asserted may cause data corruption.

Once a read or write operation has been initiated, the WAIT signal goes active to indicate that the M69KB128AB device requires additional time before data can be transferred.

The WAIT signal also is used for arbitration when a Read or Write operation is launched while an on-chip refresh is in progress (see *Figure 6: Refresh Collision during Synchronous Read Operation in Variable Latency mode*).

Typically, the WAIT pin of the M69KB128AB can be connected to a shared WAIT signal used by the processor to coordinate transactions with multiple memories on the synchronous bus.

See *Section 3: Power-up* for details on the WAIT signal operation.

2.13 V_{CC} Supply Voltage

The V_{CC} Supply Voltage is the core supply voltage.

2.14 V_{CCQ} Supply Voltage

V_{CCQ} provides the power supply for the I/O pins. This allows all Outputs to be powered independently from the core power supply, V_{CC}.

2.15 V_{SS} Ground

The V_{SS} Ground is the reference for all voltage measurements.

2.16 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{CCQ}. V_{SSQ} must be connected to V_{SS}.

3 Power-up

To guarantee correct operation, a specific Power-Up sequence must be followed to initialize the M69KB128AB. Power must be applied simultaneously to V_{CC} and V_{CCQ}. Once V_{CC} and V_{CCQ} have reached a stable level (see *Figure 35: Deep Power-Down entry and exit AC waveforms* and *Figure 34: Power-Up AC waveforms*), the device will require t_{VCHEL} to complete its self-initialization process. During the initialization period, the $\overline{E}$ signal must remain High. Once initialization has completed, the device is ready for normal operation.

Initialization will load the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) with their default settings (see *Table 9: Bus Configuration Register Definition*, and *Table 11: Refresh Configuration Register Definition*).

4 Low-power modes

4.1 Standby

When the device is in Standby, the current consumption is reduced to the level necessary to perform the memory array refresh operation. The device will enter Standby when a read or write operation is completed, depending on the operating mode (Asynchronous, NOR-Flash Synchronous or Full Synchronous).

For details on how to enter Standby, refer to *Table 3: Standard asynchronous operating modes*, *Table 5: Asynchronous Write Operations (NOR-Flash Synchronous mode)* and *Table 6: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

4.2 Deep Power-Down

Deep Power-Down (DPD) is used by the system memory microcontroller to disable the PSRAM device when its storage capabilities are not needed. All refresh operations are then disabled.

For the device to enter Deep Power-Down, bit 4 of the RCR must be set to ‘0’ and Chip Enable, $\overline{E}$, must go High, V_{IH}. When the Deep Power-Down is enabled, the data stored in the device may be corrupted and BCR, RCR and DIDR content are saved.

To exit Deep Power-Down, the Chip Enable signal, $\overline{E}$, must be held Low, V_{IL}, for a minimum time of $t_{EHEL(DP)}$. Bit 4 of the RCR will be automatically set to ‘1’. Once the Deep Power-Down is exited, the device will be available for normal operations after t_{VCHEL} (time to perform an initialization sequence) During this delay, the current consumption will be higher than the specified Standby levels, but considerably lower than the active current. The content of the registers will be restored after Deep Power-Down.

For details on how to enter Deep Power-Down, refer to *Table 3: Standard asynchronous operating modes*, *Table 5: Asynchronous Write Operations (NOR-Flash Synchronous mode)* and *Table 6: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

4.3 Partial Array Self Refresh

The Partial Array Self Refresh (PASR) performs a limited refresh of part of the PSRAM array. This mechanism enables the device to reduce the Standby current by refreshing only the part of the memory array that contains essential data. Different refresh options can be defined by setting the RCR0 to RCR2 bits of the RCR:

- Full array
- One eighth of the array
- One half of the array
- One quarter of the array
- None of the array.

These memory areas can be located either at the top or bottom of the memory array.

The WAIT signal is used for arbitration when a read/write operation is launched while an on-chip refresh is in progress. If locations are addressed while they are undergoing refresh, the WAIT signal will be asserted for additional clock cycles, until the refresh has completed (see *Figure 6: Refresh Collision during Synchronous Read Operation in Variable Latency mode*). When the refresh operation is completed, the read or write operation will be allowed to continue normally.

5 Standard asynchronous operating modes

The M69KB128AB supports Asynchronous Read and Write modes (Random Read, Page Read, Asynchronous Write).

The device is put in Asynchronous mode by setting bit 15 (BCR15) of the BCR to '1'. The Page mode is controlled by the Refresh Configuration Register (bit RCR7).

During asynchronous operations, the WAIT signal should be ignored and the Clock input signal K should be held Low, V_{IL}.

Refer to *Table 3: Standard asynchronous operating modes* for a detailed description of asynchronous operating modes.

5.1 Asynchronous Read and Write modes

At Power-Up, the device defaults to Asynchronous Random Read mode (bit BCR15 set to '1'). This mode uses the industry standard control bus ($\overline{E}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$, $\overline{UB}$). Read operations are initiated by bringing $\overline{E}$ and $\overline{G}$ Low, V_{IL}, while keeping $\overline{W}$ High, V_{IH}. Valid data will be gated through the output buffers after the specific access time t_{ELQV} has elapsed.

Write operations occur when $\overline{E}$ and $\overline{W}$ are Low. During Asynchronous Random Write operations, the $\overline{G}$ signal is 'don't care' and $\overline{W}$ will override $\overline{G}$. The data to be written is latched on the rising edge of $\overline{E}$, $\overline{W}$, $\overline{LB}$ or $\overline{UB}$ (whichever occurs first). The write operation is terminated by de-asserting $\overline{E}$, $\overline{W}$, $\overline{LB}$ or $\overline{UB}$.

The $\overline{L}$ input can either be used to latch the address or kept Low, V_{IL}, during the entire read/write operation.

See *Figure 14* and *Figure 15*, and *Table 17* for details on Asynchronous Read AC waveforms and characteristics and *Figure 18*, *Figure 19*, *Figure 20*, and *Figure 19* for details of Asynchronous Write AC waveforms and characteristics.

5.2 Asynchronous Page Read mode

Asynchronous Page Read mode is enabled by setting RCR7 to '1'. The Latch Enable, $\overline{L}$, and the Chip enable $\overline{E}$ must be held Low, V_{IL} during Asynchronous Page Read operations.

A Page of data is internally read. A memory page may consist of 4, 8 or 16 Words. During a 4-Word page access, all the address bits except A0 to A1 should be fixed. During a 8-Word and 16-Word page access, all address bits are fixed except A0 to A2 and A0 to A3, respectively (see *Table 2: Page mode characteristics*).

The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal, longer timings apply again.

The Page mode is not available for write operations.

See *Figure 16* and *Table 17* for details of the Asynchronous Page Read timing requirements.

Table 2. Page mode characteristics

Page Size	Page Read Address	Page Read Start Address	Page Read Direction
4 Words	A0-A1	Don't Care	Don't Care
8 Words	A0-A2	Don't Care	Don't Care
16 Words	A0-A3	Don't Care	Don't Care

5.3 Configuration Registers Asynchronous Read and Write

Programming the registers (BCR and RCR) and reading the registers (BCR, RCR and DIDR) can be performed using the CR controlled method in standard Asynchronous mode.

Table 3. Standard asynchronous operating modes

Asynchronous Modes(1)	Power	L	E	W	G	UB	LB	WAIT	CR	A19	A18	A0-A17 A20-A22	DQ0-DQ7	DQ8-DQ15
Word Read	Active (I_{CC})	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Low-Z	V_{IL}	Valid			Output Valid	Output Valid
Lower Byte Read					V_{IL}	V_{IH}	V_{IL}		V_{IL}	Valid			Output Valid	High-Z
Upper Byte Read					V_{IL}	V_{IL}	V_{IH}		V_{IL}	Valid			High-Z	Output Valid
Word Write				V_{IL}	X	V_{IL}	V_{IL}		V_{IL}	Valid			Input Valid	Input Valid
Lower Byte Write					X	V_{IH}	V_{IL}		V_{IL}	Valid			Input Valid	Invalid
Upper Byte Write					X	V_{IL}	V_{IH}		V_{IL}	Valid			Invalid	Input Valid
Read Configuration Register (CR Controlled Method)				V_{IH}	V_{IL}	V_{IL}	V_{IL}		V_{IH}	00(RCR) 10(BCR) X1(DIDR) (2)		X	BCR/ RCR/DIDR Content	
Program Configuration Register (CR Controlled)(3)				V_{IH}	X	X	X			00(RCR) 10(BCR) (2)		BCR/ RCR Data	High-Z	
No Operation	Active (I_{CC})	X	V_{IL}	X	X	X	X		V_{IL}	X	X	X	X	
Deep Power-Down(4)	Deep Power-Down (I_{CCPD})		V_{IH}	X	X	X	X	High-Z	X	X	X	X	High-Z	
Standby	Standby (I_{PASR})		V_{IH}	X	X	X	X		V_{IL}	X	X	X	High-Z	

1. The Clock signal, K, must remain Low in asynchronous operating mode.
2. A18 and A19 are used to select the BCR, RCR or DIDR registers.
3. BCR and RCR only.
4. Bit 4 of the Refresh Configuration Register must be set to '0', bit 4 (BCR4) of the Bus Configuration Register must be set to '0', and $\overline{E}$ has to be maintained High, V_{IH}, during Deep Power-Down mode.

6 Synchronous operating modes

The synchronous modes allow high-speed read and write operations synchronized with the clock. Refresh cycles are indicated to the host system by asserting the WAIT signal that, in turn, stalls the microcontroller.

The M69KB128AB supports two types of synchronous modes:

- **NOR-Flash**:- this mode greatly simplifies the interfacing with traditional burst-mode Flash memory microcontrollers.
- **Full Synchronous**: both read and write are performed in Synchronous mode.

All the options related to the synchronous modes can be configured through the Bus Configuration Register, BCR. In particular, the device is put in Synchronous mode, either NOR-Flash or Full Synchronous, by setting bit BCR15 of the Bus Configuration Register to '0'.

The device will automatically detect whether the NOR-Flash or the Full Synchronous mode is being used by monitoring the Clock, K, and the Latch Enable, $\overline{L}$, signals. If a rising edge of the Clock K is detected while $\overline{L}$ is held Low, V_{IL} (active), the device operates in Full Synchronous mode.

6.1 NOR-Flash Synchronous mode

In this mode, the device operates in synchronous mode for read operations, and in asynchronous mode for write operations.

Asynchronous write operations are performed at Word level, with $\overline{LB}$ and $\overline{UB}$ Low. The data is latched on $\overline{E}$, $\overline{W}$, $\overline{LB}$, $\overline{UB}$, whichever occurs first. RCR and BCR registers can be programmed in NOR-Flash Asynchronous Write mode, using the CR controlled method (see *Section 7.1: Programming the Registers by the CR controlled method*). A Program Configuration Register operation can only be issued if the device is in idle state and no burst operations are in progress. NOR-Flash Asynchronous Write operations are described in *Table 5: Asynchronous Write Operations (NOR-Flash Synchronous mode)*.

Synchronous read operations are also performed at Word level. They are controlled by the state of $\overline{E}$, $\overline{L}$, $\overline{G}$, $\overline{W}$, $\overline{LB}$ and $\overline{UB}$ signals when a rising edge of the clock signal, K, occurs. The initial Burst Read access latches the Burst start address. The number of Words to be output is controlled by bits 0 to 2 of the BCR. The first data will be output after a number of clock cycles, also called Latency. NOR-Flash Synchronous Burst Read operations are described in *Table 6: Synchronous Read Operations (NOR-Flash Synchronous mode)*.

When a Burst Write operation is initiated or when switching from NOR-Flash mode to Full Synchronous mode, the delay from $\overline{E}$ Low to Clock High, t_{ELKH}, should not exceed 20ns. However, when it is not possible to meet these specifications, special care must be taken to keep addresses stable after driving the Write Enable signal, $\overline{W}$, Low.

Write operations are considered as Asynchronous operations until the device detects a valid clock edge and hence the address setup time of t_{AVWL} must be satisfied (see *Figure 5: Switching from Asynchronous to Synchronous Write operation*).

6.2 Full Synchronous mode

In Full Synchronous mode, the device performs read and write operations synchronously. Synchronous Read and Write operations are performed at Word level.

The initial Burst Read and Write access latches the Burst start address. The number of Words to be output or input during Synchronous Read and Write operations is controlled by bits 0 to 2 of the BCR.

During Burst Read and Write operations, the first data will be output after a number of clock cycles defined by the Latency value.

Programming the registers (BCR and RCR) and reading the registers (BCR, RCR and DIDR) can be performed using the CR controlled method in Full Synchronous mode.

Full Synchronous operations are described in *Table 7: Full Synchronous mode*.

6.3 Synchronous Burst Read and Write

During Synchronous Burst Read or Write operations, addresses are latched on the rising edge of the Clock K when $\overline{L}$ is Low and data are latched on the rising edge of K. The Write Enable, $\overline{W}$, signal indicates whether the operation is going to be a read ($\overline{W}=V_{IH}$) or a write ($\overline{W}=V_{IL}$).

The WAIT output will be asserted as soon as a Synchronous Burst operation is initiated and will be deasserted to indicate when data are to be transferred to (or from) the memory array.

The Burst Length is the number of Words to be output or input during a Synchronous Burst Read or Write operation. It can be configured as 4, 8, 16 or 32 Words or continuous through bit BCR0 to BCR2 or the Burst Configuration Register. The Latency defines the number of clock cycles between the beginning of a Burst Read operation and the first data output (counting from the first Clock edge where $\overline{L}$ was detected Low) or between the beginning of a Burst Write operation and the first data input. The Latency can be set through bits BCR13 to BCR11 of the Bus Configuration Register (see *Table 4: Operating Frequency versus Latency*).

The latency can also be configured to fixed or variable by programming bit BCR14. By default, the Latency Type is set to variable.

Synchronous Read operations are performed in both fixed and variable latency mode while Synchronous Write operations are only performed with fixed latency.

See *Figure 24*, *Note 1*, and *Figure 30*, *Note 31*, for details on Synchronous Read and Write AC waveforms, respectively.

6.3.1 Variable Latency

In Variable Latency mode, the latency programmed in the BCR is not guaranteed and is maintained only if there is no conflict with a refresh operation.

The Latency set in the BCR is applicable only for an initial burst read access, when no refresh request is pending. For a given latency value, the Variable Latency mode allows higher operating frequencies than the Fixed Latency mode (see *Table 4: Operating Frequency versus Latency* and *Figure 3: Latency configuration (Variable Latency mode, no Refresh collision)*).

Burst Write operations are always performed at fixed latency, even if BCR14 is configured to Variable Latency (see *Section 6.3.2: Fixed Latency*).

Monitoring of the WAIT signal is recommended for reliable operation in this mode.

See *Figure 24*. and *Figure 31* for details on Synchronous Burst Read and Write AC waveforms in Variable Latency mode.

6.3.2 Fixed Latency

The latency programmed in the BCR is the real latency. The number of clock cycles is calculated by taking into account the time necessary for a refresh operation and the time necessary for an initial Burst access. This limits the operating frequency for a given latency value (see *Table 4: Operating Frequency versus Latency* and *Figure 4: Latency configuration (Fixed Latency mode)*).

It is recommended to use the Fixed Latency mode if the microcontroller cannot monitor the WAIT signal.

6.3.3 Row Boundary crossing

Row boundary crossings between adjacent rows may occur during Burst Read and Write operations. Row boundary crossings are not handled automatically by the PSRAM.

The microcontroller must stop the Burst operation at the row boundary and restart it at the beginning of the next row. Burst operations must be stopped by driving the Chip Enable signal, $\overline{E}$, High, after the WAIT signal falling edge. $\overline{E}$ must transition:

- Before the third Clock cycle after the WAIT signal goes Low if BCR[8] = 0
- Before the fourth Clock cycle after WAIT signal goes Low if BCR[8] = 1.

Refer to *Figure 26* and *Figure 30* for details on how to manage row boundary crossings during burst operations.

6.4 Synchronous Burst Read Interrupt

Ongoing Burst Read operations can be interrupted to start a new Burst cycle by either of the following means:

- Driving $\overline{E}$ High, V_{IH}, and then Low, V_{IL} on the next clock cycle (recommended). If necessary, refresh cycles will be added during the new Burst operation to schedule any outstanding refresh. If Variable Latency mode is set, additional wait cycles will be added if a refresh operation is scheduled during the Synchronous Burst Read Interrupt. WAIT monitoring is mandatory for proper system operation.
- Starting a new Synchronous Burst Read operation without toggling $\overline{E}$.

An ongoing Burst Read operation can be interrupted only after the first valid data is output. When a new Burst access starts, I/O signals immediately become high impedance.

6.5 Synchronous Burst Write Interrupt

Ongoing Burst Write operations can be interrupted to start a new Burst cycle by either of the following means:

- Driving $\overline{E}$ High, V_{IH}, and then Low, V_{IL} on the next clock cycle (recommended),
- Starting a new Synchronous Burst Write without toggling $\overline{E}$. Considering that Burst Writes are always performed in Fixed Latency mode, refresh is never scheduled. A maximum Chip Enable, $\overline{E}$, low time (t_{ELEH}) must be respected for proper device operation.

An ongoing Burst Write can be interrupted only after the first data is input. When a new Burst access starts, I/O signals immediately become high impedance.

See *Figure 27: Burst Read Interrupted by Burst Read or Write AC waveforms* and *Figure 32: Burst Write Interrupted by Burst Write or Read AC waveforms* for details on Burst Read and Burst Write interrupt AC waveforms, respectively.

6.6 Synchronous Burst Read and Write Suspend

Synchronous Burst Read and Write operations can be suspended by halting the Clock K holding it either High or Low. The status of the I/O signals will depend on the status of Output enable input, $\overline{G}$. The device internal address counter is suspended and data outputs become high impedance t_{GHQZ} after the rising edge of the Output Enable signal, $\overline{G}$. It is prohibited to suspend the first data output at the beginning of a Synchronous Burst Read.

See *Figure 25* for details on the Synchronous Burst Read and Write Suspend mechanisms.

During Synchronous Burst Read and Synchronous Burst Write Suspend operations, the WAIT output will be asserted. Bit BCR8 of the Bus Configuration Register is used to configure when the transition of the WAIT output signal between the asserted and the deasserted state occurs with respect to valid data available on the data bus.

Table 4. Operating Frequency versus Latency

Latency Mode	Configured Latency (Clock Cycles)	Latency (Clock Cycles)		Max Input Clock Frequency (MHz)	
		Normal	If Refresh Collision	104 MHz	80 MHz
Variable Latency BCR14 = 0 (Default)	2 (3 clock cycles)	3	5	66	52
	3 (4 clock cycles) (default)	4	7	104	80
Fixed Latency BCR14 = 1	2 (3 clock cycles)	3		33	33
	3 (4 clock cycles) (default)	4		52	52
	4 (5 clock cycles)	5		66	66
	5 (6 clock cycles)	6		75	75
	6 (7 clock cycles)	7		104	80
	All Others	-		-	-

Table 5. Asynchronous Write Operations (NOR-Flash Synchronous mode)

Asynchronous Operations	Power	K	$\overline{L}$	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{UB}$, $\overline{LB}$	WAIT	CR	A19	A18	A0-A22	DQ0-DQ15
Word Write	Active (I_{CC})	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	Low-Z	V_{IL}	Valid			Input Valid
Program Configuration Register (CR Controlled)(1)			V_{IL}	V_{IL}	V_{IL}	V_{IH}	X		V_{IH}	00(RCR) 10(BCR)		RCR/BCR Data	High-Z
No Operation	Active (I_{CC})		V_{IH}	X	X	X	X		V_{IL}	X			X
Standby	Standby (I_{PASR})		X	V_{IH}	X	X	X	High-Z	V_{IL}	X			High-Z
Deep Power-Down	Deep Power-Down (I_{CCPD})		X	V_{IH}	X	X	X		X	X			High-Z

1. BCR and RCR only.

Table 6. Synchronous Read Operations (NOR-Flash Synchronous mode)

Synchronous Operations(1)	Power	K	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$, $\overline{UB}$	WAIT	CR	A19	A18	A0-A22(2)	DQ15-DQ0
Initial Burst Read	Active (I_{CC})	⮥	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	Low-Z	V_{IL}	Valid	Valid	Valid	Output Valid
Subsequent Burst Read		⮥	V_{IL}	V_{IH}	X	X	V_{IL}(3)		V_{IL}	X			Output Valid
Read Configuration Register (CR Controlled Method)		⮥	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}		V_{IH}	00(RCR) 10(BCR) X1(DIDR)		X	RCR/BCR/DIDR Content
No Operation	Active (I_{CC})	V_{IL}	V_{IL}	X	X	X	X		V_{IL}	X			X
Standby	Standby (I_{PASR})	V_{IL}	V_{IH}	X	X	X	X	High-Z	V_{IL}	X			High-Z
Deep Power-Down	Deep Power-Down (I_{CCPD})	V_{IL}	V_{IH}	X	X	X	X		X	X			High-Z

1. Burst Read Interrupt, Suspend and Terminate are described in dedicated paragraph of the *Section 6: Synchronous operating modes*.
2. Except A18 and A19.
3. The above table shows the device behavior if both $\overline{LB}$ and $\overline{UB}$ are asserted, V_{IL}. If either $\overline{LB}$ or $\overline{UB}$ is High, V_{IH}, only one Byte will be input or output, according to the status of $\overline{W}$.

Table 7. Full Synchronous mode

Synchronous Mode(1)	Power	K	$\overline{E}$	$\overline{L}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$, $\overline{UB}$	WAIT	CR	A19	A18	A0-A22(2)	DQ15-DQ0
Initial Burst Read	Active (I_{CC})	↑	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	Low-Z	V_{IL}	Valid	Valid	Valid	X
Subsequent Burst Read		↑	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}(3)		V_{IL}	X	X		Output Valid
Initial Burst Write		↑	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X		V_{IL}	Valid	Valid	Valid	Input Valid
Subsequent Burst Write		↑	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}(2)		X	X	X	X	Input Valid
Program Configuration Register (CR Controlled)		↑	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X		V_{IH}	00(RCR) 10(BCR)		RCR/BCR Data	X
Read Configuration Register (CR Controlled Method)		↑	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}		V_{IH}	00(RCR) 10(BCR) X1(DIDR)		X	RCR/BCR/ DIDR Content
No Operation	Active (I_{CC})	V_{IL}	V_{IL}	X	X	X	X		V_{IL}	X			X
Standby	Standby (I_{PASR})	V_{IL}	V_{IH}	X	X	X	X	High-Z	V_{IL}	X			High-Z
Deep Power-Down	Deep Power-Down (I_{CCPD})	V_{IL}	V_{IH}	X	X	X	X		X	X			High-Z

1. Burst Read Interrupt, Suspend, Terminate and Burst Write Interrupt, Suspend and Terminate are described in dedicated paragraph of the *Section 6: Synchronous operating modes*.
2. Except A18 and A19.
3. The above table shows the device behavior if both $\overline{LB}$ and $\overline{UB}$ are asserted, V_{IL}. If either $\overline{LB}$ or $\overline{UB}$ is High, V_{IH}, only one Byte will be input or output, according to the status of $\overline{W}$.

Figure 3. Latency configuration (Variable Latency mode, no Refresh collision)

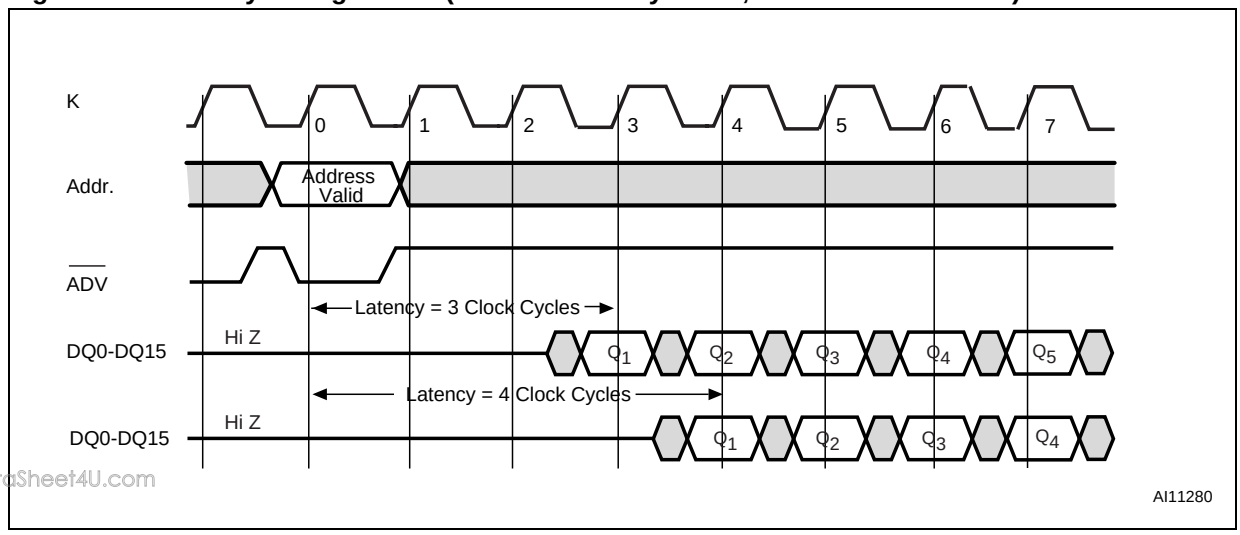
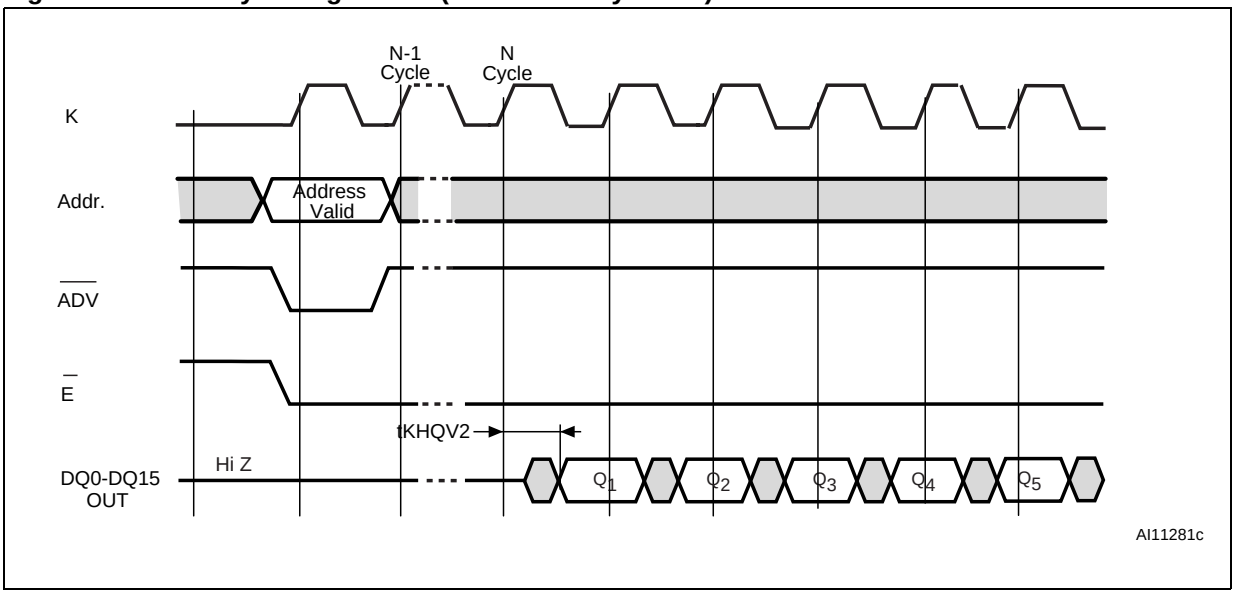


Figure 4. Latency configuration (Fixed Latency mode)



1. See *Table 21: Synchronous Burst Read AC characteristics* for details on the synchronous read AC Characteristics shown in the above waveforms.

Figure 5. Switching from Asynchronous to Synchronous Write operation

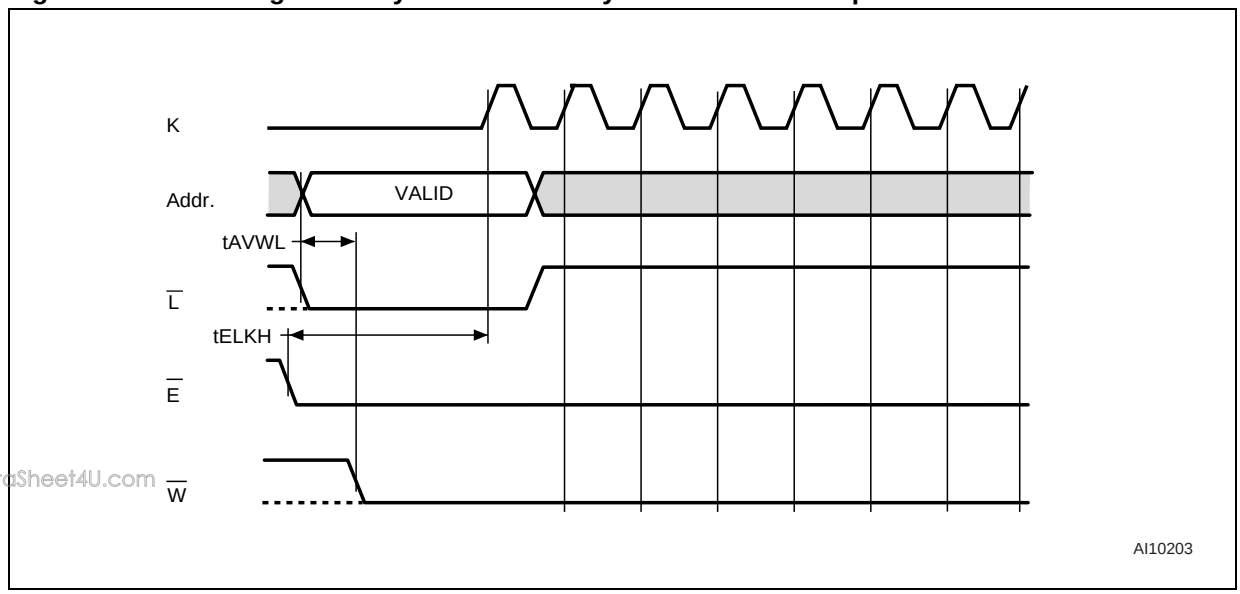
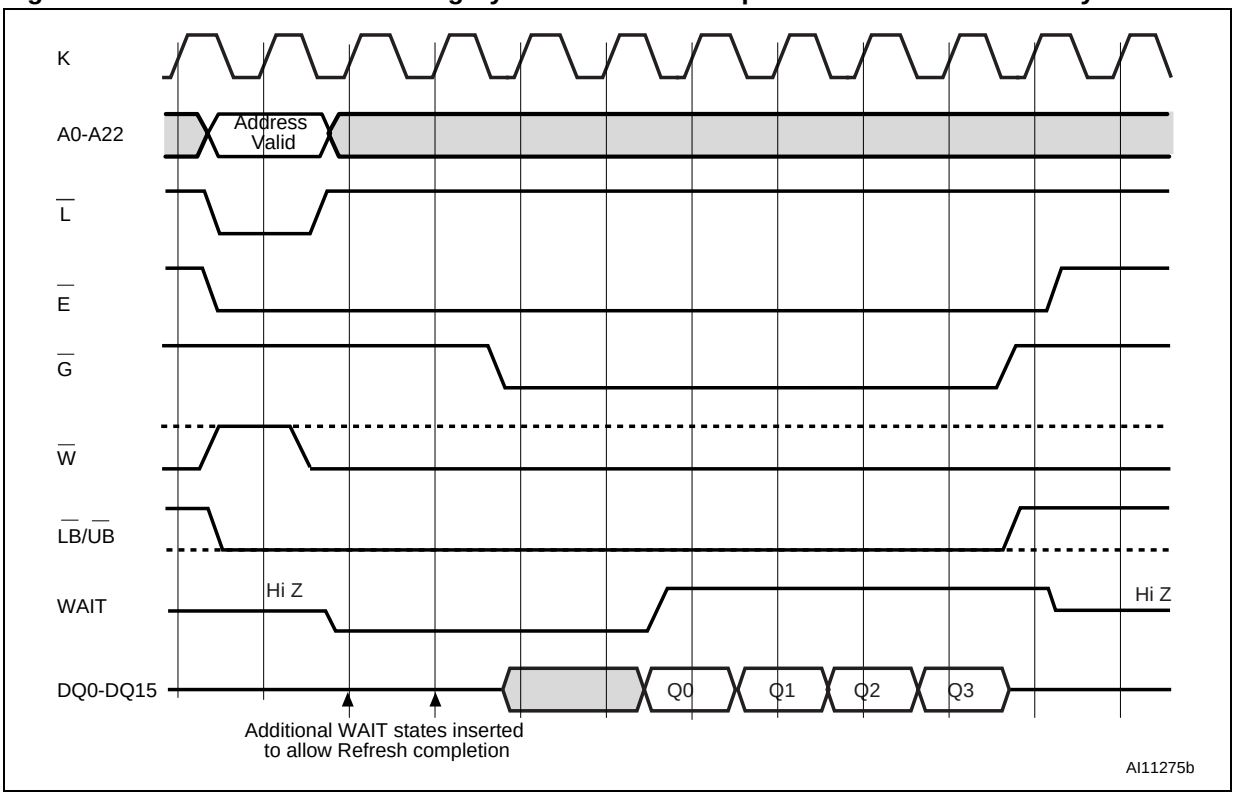


Figure 6. Refresh Collision during Synchronous Read Operation in Variable Latency mode



1. Additional Wait states are inserted to allow Refresh completion.
The latency is set to 3 clock cycles (BCR13-BCR11 = 010). The WAIT must be active Low, V_{IL}, (BCR10 = 0) and asserted during delay (BCR8= 0).

7 Configuration registers

The M69KB128AB features three registers:

- The Bus Configuration Register (BCR)
- The Refresh Configuration Register (RCR)
- The Device ID Register (DIDR).

BCR and RCR are user-programmable registers that define the device operating mode. They are automatically loaded with default settings during Power-Up, and selected by address bits A18 and A19 (see *Table 8: Register Selection*).

DIDR is a read-only register that contains information about the device identification. It is selected by setting address bit A18 to '1' with A19 'don't care' (see *Table 8: Register Selection*).

The configuration registers (only BCR and RCR) can be programmed and read using two methods:

- The CR Controlled Method (or Hardware Method)
- The Software Method.

7.1 Programming the Registers by the CR controlled method

7.1.1 Read Configuration Register

The content of a register is read by issuing a read operation with Configuration Register Enable signal, CR, High, V_{IH}. Address bits A18 and A19 select the register to be read (see *Table 8: Register Selection*). The value contained in the register is then available on data bits DQ0 to DQ15.

The BCR, RCR and DIDR can be read either in normal asynchronous or synchronous mode.

The CR pin has to be driven high prior to any access.

See *Table 6* and *Table 7* for a detailed description of Configuration register Read by the CR Controlled methods and *Figure 17* and *Figure 28*, CR Controlled Configuration Register Read waveforms in asynchronous and synchronous mode.

7.1.2 Program Configuration Register

BCR and RCR registers can be programmed by issuing a bus write operation, in asynchronous or synchronous mode (NOR-Flash or Full Synchronous), with Configuration Register Enable signal, CR, High, V_{IH}. Address bits A18 and A19 allow to select between BCR and RCR (see *Table 8: Register Selection*).

In synchronous mode, the values placed on address lines A0 to A15 are latched on the rising edge of $\overline{L}$, $\overline{E}$, or $\overline{W}$, whichever occurs first.

In asynchronous mode, a register is programmed by toggling $\overline{L}$ signal.

$\overline{LB}$ and $\overline{UB}$ are 'don't care'. The CR pin has to be driven high prior to any access.

Refer to *Table 5* and *Table 7* for a detailed description of Configuration Register Program by the CR Controlled method and to *Figure 22* and *Figure 33*, showing CR controlled Configuration Register Program waveforms in asynchronous and synchronous mode.

Table 8. Register Selection

Register	Read or Write Operation	A18	A19
RCR	Read/Write	0	0
BCR	Read/Write	0	1
DIDR	Read-Only	1	X

7.2 Programming and Reading the Registers by the software method

All registers (BCR, RCR, DIDR) can be read by issuing a Read Configuration Register sequence (see *Figure 8: Read Configuration Register (Software Method)*.

BCR and RCR can be programmed by issuing a Set Configuration Register sequence (see *Figure 7: Set Configuration Register (Software Method)*.

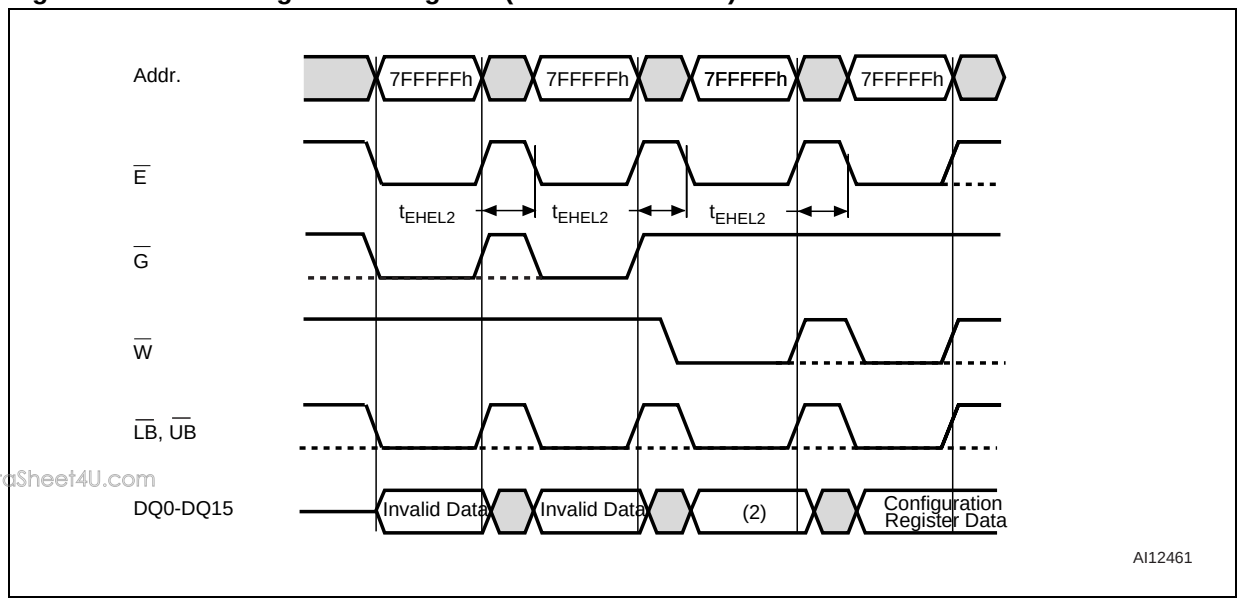
The timings will be identical to those described in *Table 17: Asynchronous Read AC characteristics*. The Configuration Register Enable input, CR, is 'don't care'.

Read Configuration Register and Set Configuration Register sequences both require 4 read or write cycles. These cycles will be executed in asynchronous mode, whatever the device operating mode:

1. 2 bus read and one bus write cycles to a unique address location, 7FFFFFh, indicate that the next operation will read or write to a configuration register. The data written during the third cycle must be '0000h' to access the RCR, '0001h' to access the BCR and '0002h' to access the DIDR during the next cycle.
2. The fourth cycle reads from or writes to the configuration register.

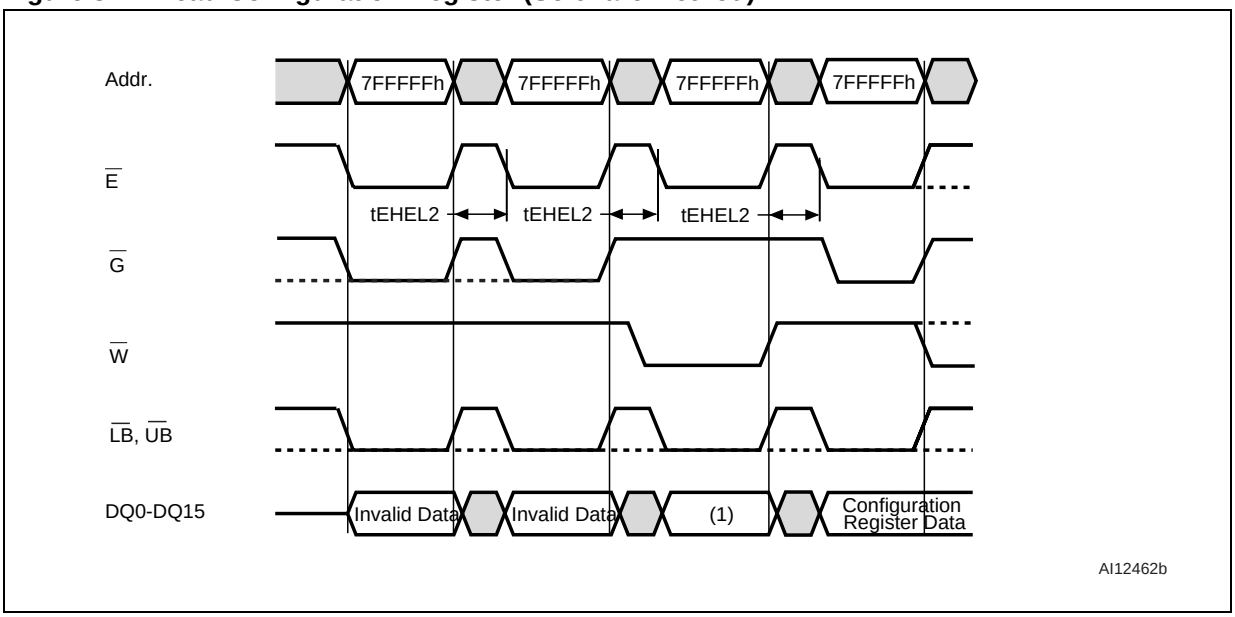
The timings for programming and reading the registers by the software method are identical to the asynchronous write and read timings.

Figure 7. Set Configuration Register (Software Method)



1. Only the Bus Configuration Register (BCR) and the Refresh Configuration Register (RCR) can be modified.
2. To program the BCR or the RCR on last bus write cycle, DQ0-DQ15 must be set to '0001h' and '0000' respectively.
3. The highest order address location is not modified during this operation.
4. The control signal $\overline{E}$ must be toggled as shown in the above figure.

Figure 8. Read Configuration Register (Software Method)



1. To read the BCR, RCR or DIDR on last bus read cycle, DQ0-DQ15 must be set to '0001h', '0000' and '0002' respectively.
2. The highest order address location is not modified during this operation.
3. The control signal $\overline{E}$ must be toggled as shown in the above figure.

7.3 Bus Configuration Register

The Bus Configuration Register (BCR) defines how the PSRAM interacts with the system memory bus. All the device operating modes are configured through the BCR, except the Page mode which is configured through the RCR.

Refer to *Table 9* for the description of the Bus Configuration Register Bits.

7.3.1 Operating Mode Bit (BCR15)

The Operating Mode bit allows the Synchronous mode or the Asynchronous mode (default setting) to be selected. Selecting the Synchronous mode will allow the device to operate either in NOR Flash mode or in full Synchronous Burst mode.

The device will automatically detect that the NOR Flash mode is being used by monitoring a rising edge of the Clock signal, K, when $\overline{L}$ is Low. If this should not be the case, the device operates in full Synchronous mode.

7.3.2 Latency Type (BCR14)

The Latency Type bit is used to configure the latency type. When the Latency Type bit is set to ‘0’, the device operates in variable latency mode (only available for Synchronous Read mode). When it is ‘1’, the fixed latency mode is selected and the latency is defined by the values of bits BCR13 to BCR11.

Refer to *Table 3* and *Table 4* for examples of fixed and variable latency configuration.

7.3.3 Latency Counter Bits (BCR13-BCR11)

The Latency Counter bits are used to set the number of clock cycles between the beginning of a read or write operation and the first data output or input.

The Latency Counter bits can only assume the values shown in *Table 9: Bus Configuration Register Definition* (see also *Figure 3* and *Figure 4*).

7.3.4 WAIT Polarity Bit (BCR10)

The WAIT Polarity bit indicates whether the WAIT output signal is active High or Low. As a consequence, it also determines whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state (see *Figure 10: WAIT polarity*).

By default, the WAIT output signal is active High.

7.3.5 WAIT Configuration Bit (BCR8)

The system memory microcontroller uses the WAIT signal to control data transfer during Synchronous Burst Read and Write operations.

The WAIT Configuration bit is used to determine when the transition of the WAIT output signal between the asserted and the deasserted state occurs with respect to valid data available on the data bus. When the Wait Configuration bit is set to ‘0’, data is valid or invalid on the first Clock rising edge immediately after the WAIT signal transition to the deasserted or asserted state. When the Wait Configuration bit is set to ‘1’ (default settings), the WAIT signal transition occurs one clock cycle prior to the data bus going valid or invalid.

See *Figure 9: WAIT configuration example* for an example of WAIT configuration.

7.3.6 Driver Strength Bits (BCR5-BCR4)

The Driver Strength bits allow to set the output drive strength to adjust to different data bus loading. Normal driver strength (full drive) and reduced driver strength (half drive and a quarter drive) are available.

By default, outputs are configured at ‘half drive” strength.

7.3.7 Burst Wrap Bit (BCR3)

Burst Read operations can be confined inside the 4, 8, 16 or 32 Word boundary (wrap) or allowed to step across the boundary (no wrap). The Burst Wrap bit is used to select between ‘wrap’ and ‘no wrap’. If the Burst Wrap bit is set to ‘1’ (no wrap), the device outputs data sequentially regardless of burst boundaries. When Continuous Burst operation is selected, the internal address switches to 000000h if the read address passes the last address. By default, Burst wrap is disabled (see also *Table 10: Burst type definition*).

7.3.8 Burst Length Bits (BCR2-BCR0)

The Burst Length bits set the number of Words to be output or input during a Synchronous Burst Read or Write operation. They can be set for 4 Words, 8 Words, 16 Words, 32 Words or Continuous Burst (default settings), where all the Words are output or input sequentially regardless of address boundaries (see also *Table 10: Burst type definition*).

Table 9. Bus Configuration Register Definition

Address Bits	Bus Configuration Register Bits	Name	Value	Description
A15	BCR15	Operating Mode Bit	0	Synchronous Mode (NOR Flash or Full Synchronous Mode)
			1	Asynchronous Mode (Default)
A14	BCR14	Latency Type	0	Variable Latency (Default)
			1	Fixed Latency
A13-A11	BCR13-BCR11	Latency Counter Bits	010	3 Clock Cycles
			011	4 Clock Cycles (Default)
			100	5 Clock Cycles
			101	6 Clock Cycles
			110	7 Clock Cycles
			Other Configurations Reserved(1)	
A10	BCR10	WAIT Polarity Bit	0	WAIT Active Low
			1	WAIT Active High (default).See *Figure 10: WAIT polarity*.
A9	-	-	Must be set to '0'	Reserved(1)
A8	BCR8	Wait Configuration Bit	0	WAIT Asserted During Delay (see *Figure 9: WAIT configuration example*).
			1	WAIT Asserted One Clock Cycle Before Delay (Default)
A7-A6	-	-	Must be set to '0'	Reserved(1)
A5-A4	BCR5-BCR4	Driver Strength Bits	00	Full Drive
			01	1/2 Drive (Default)
			10	1/4 Drive
			11	Reserved(1)
A3	BCR3	Burst Wrap Bit	0	Wrap
			1	No Wrap (Default)
A2-A0	BCR2-BCR0	Burst Length Bit	001	4 Words
			010	8 Words
			011	16 Words
			100	32 Words
			111	Continuous Burst (default)
			Other Configurations Reserved(1)	

1. Programming the BCR with reserved value will force the device to use the default register settings.

Table 10. Burst type definition

Mode	Start Add	4 Words (Sequential) BCR2-BCR0=001b	8 Words (Sequential) BCR2-BCR0=010b	16 Words (Sequential) BCR2-BCR0=011b	32 Words (Sequential) BCR2-BCR0=100b	Continuous Burst BCR2-BCR0=111b
Wrap (BCR3='0')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-...-14-15	0-1-2-3-...-30-31	0-1-2-3-..-511-.
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-...-14-15-0	1-2-3-...-30-31-0	1-2-3-4-...-510-511-
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-...-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-...-511-
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-...-15-0-1-2	3-4-5-...-31-0-1-2	3-4-5-...-511-
	4		4-5-6-7-0-1-2-3	4-5-...-15-0-1-2-3	4-5-6-...-31-0-1-2-3	4-5-...-511-
	5		5-6-7-0-1-2-3-4	5-6-7-...-15-0-1-...-4	5-6-7-..-31-0-1-..-4	5-6-7-...-511-
	6		6-7-0-1-2-3-4-5	6-7-8-...-15-0-1-...-5	6-7-8-...-31-0-1-...-5	6-7-8-...-511-
	7		7-0-1-2-3-4-5-6	7-8-9-...15-0-1-...-6	7-8-9-...-31-0-1-...-6	7-8-9-...-511-
	...	...	...	...	...	...
	14			14-15-0-1-2-...-13	14-15-...-31-0-...-13	14-...511-
	15			15-0-1-2-...-14	15-0-1-...-31-0-...-14	15-...511-
	...	...	...	...	...	...
	30				30-31-0-...-28-29	30-...-511-
	31				31-0-1-...-29-30	31-...-511-
No Wrap (BCR3='1')	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-...-14-15	0-1-2-3-...-30-31	0-1-2-3-..-511-.
	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-..-15-16	1-2-3-4-...-32	1-2-3-4-...-512-
	2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-...-17	2-3-4-...-33	2-3-4-5-...-513-
	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-...-18	3-4-5-...-34	3-4-5-...-514-
	4		4-5-6-7-8-9-10-11	4-5-6-...-19	4-5-6-...-35	4-5-6-...-515-
	5		5-6-7-8-9-10-11-12	5-6-7-...-20	5-6-7-...-36	5-6-7-...-516-
	6		6-7-8-9-10-11-12-13	6-7-8-...-21	6-7-8-...-37	6-7-8-...-517-
	7		7-8-9-10-11-12-13-14	7-8-9-...-22	7-8-9-...-38	7-8-9-...-518-
	...	...				...
	14			14-15-...-29	14-15-16-...-46	14-...-525-
	15			15-16-17-...-30	15-16-17-...-47	15-...-526-
	...	...				...
	30				30-31-0-...-28-62	30-...-541-
	31				31-0-1-...-29-63	31-...-542-

Figure 9. WAIT configuration example

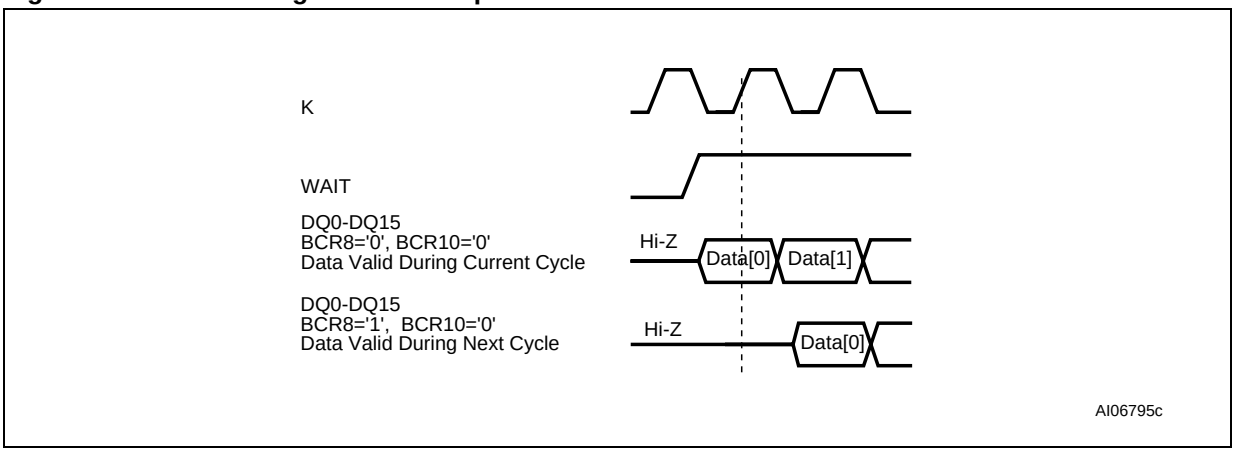
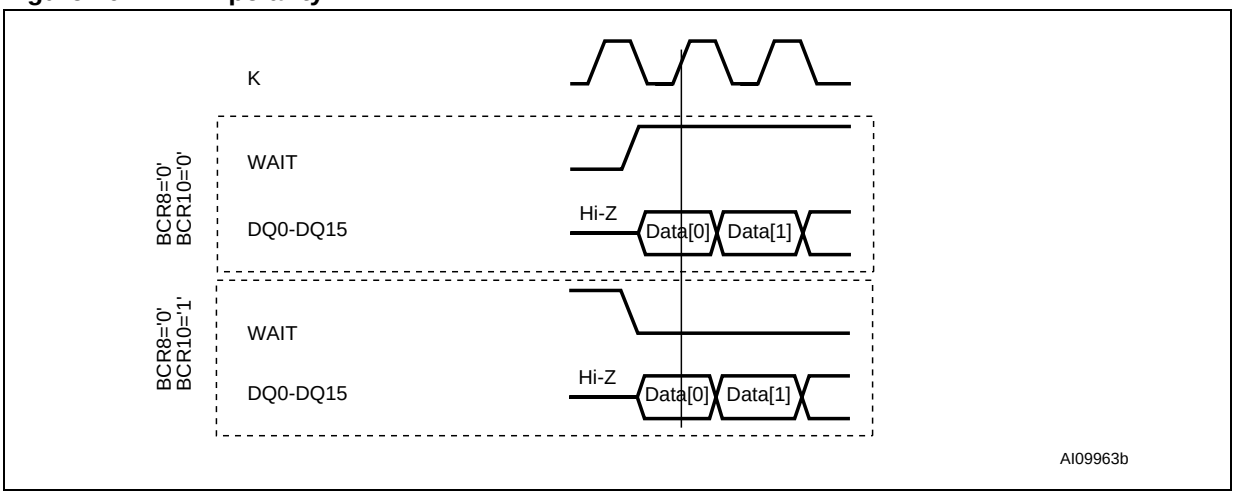


Figure 10. WAIT polarity



7.4 Refresh Configuration Register

The role of the Refresh Configuration Register (RCR) is:

- to define how the self refresh of the PSRAM array is performed,
- to select the Deep Power-Down mode,
- to enable Page Read operations.

Refer to *Table 11* for the description of the Refresh Configuration Register Bits.

7.4.1 Page Mode Operation Bit (RCR7)

The Page Mode operation bit determines whether the Asynchronous Page Read mode is enabled. At power-up, the RCR7 bit is set to ‘0’, and the Asynchronous Page Read mode is disabled.

7.4.2 Deep Power-Down Bit (RCR4)

The Deep Power-Down bit enables or disables all refresh-related operations. The Deep Power-Down mode is enabled when the RCR4 bit is set to ‘0’, and remains enabled until this bit is set to ‘1’. At power-up, the Deep Power-Down mode is disabled.

See the *Section 4.2: Deep Power-Down* for more details.

7.4.3 Partial Array Refresh Bits (RCR2-RCR0)

The Partial Array Refresh bits allow refresh operations to be restricted to a portion of the total PSRAM array. The refresh options can be full array, one half, one quarter, one eighth or none of the array. These memory areas can be located either at the top or bottom of the memory array. By default, the full memory array is refreshed.

Table 11. Refresh Configuration Register Definition

Address Bits	Refresh Configuration Register Bits	Name	Value	Description
A15-A8	-	-	Must be set to ‘0’	Reserved
A7	RCR7	Page Mode Operation Bit	0	Page Read Mode Disabled (Default)
			1	Page Read Mode Enabled
A6-A5	-	-	Must be set to ‘0’	Reserved
A4	RCR4	Deep Power-Down Bit	0	Deep Power-Down Enabled
			1	Deep Power-Down Disabled (Default)
A3	-	-	Must be set to ‘0’	Reserved
A2-A0	RCR2-RCR0	Partial Array Refresh Bits	000	Full Array Refresh (Default)
			001	Refresh of the Bottom Half of the Array
			010	Refresh of the Bottom Quarter of the Array
			011	Refresh of the Bottom Eighth of the Array
			100	None of the Array
			101	Refresh of the Top Half of the Array
			110	Refresh of the Top Quarter of the Array
			111	Refresh of the Top Eighth of the Array

7.5 Device ID Register

The Device ID Register (DIDR) is a read-only register that contains the Manufacturer code. It is preprogrammed by STMicroelectronics and cannot be modified by the user.

Refer to *Table 12* for the description of the Bus Configuration Register Bits.

Table 12. Device ID Register Definition

Address Bits	Device ID Register Bits	Name	Value	Description
A15	DIDR15	Row Length	0	128 Words
			1	256 Words
A14-A11	DIDR14-DIDR11	Design Version	0000	A
			0001	B
			0010	C
			0011	D
			1111	P
			Other Configurations Reserved	
A10-A8	DIDR10-DIDR8	Device Density	000	16 Mbits
			001	256 Mbits
			010	64 Mbits
			011	128 Mbits
			100	32 Mbits
			Other Configurations Reserved	
A7-A5	DIDR7-DIDR5	PSRAM Generation	001	1.0
			010	1.5
			011	2.0
			Other Configurations Reserved	
A4-A0	DIDR4-DIDR0	Device ID	00001	Cypress
			00010	Infineon
			00011	Micron
			00100	Renesas
			01111	STMicroelectronics
			Other Configurations Reserved	

8 Maximum Rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 13. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–30	+85	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{CC}	Core Supply Voltage	–0.2	2.45	V
V_{CCQ}	Input/Output Buffer Supply Voltage	–0.2	2.45	V
V_{IO}	Input or Output Voltage	–0.2	2.45	V

9 DC and AC parameters

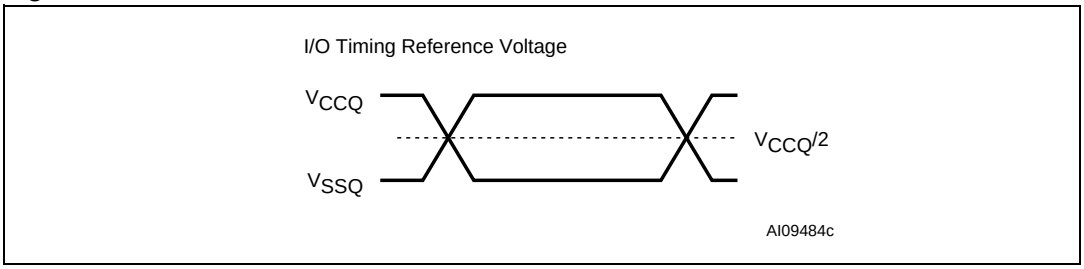
This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 14: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 14. Operating and AC measurement conditions

Parameter(1)	Min	Max	Unit
V_{CC} Supply Voltage	1.7	1.95	V
V_{CCQ} Input/Output Buffer Supply Voltage	1.7	1.95	V
Load Capacitance (C_L)	30		pF
Output Circuit Protection Resistance (R)	50		Ω
Input Pulse Voltages(2)	0	V_{CC}	V
Input and Output Timing Ref. Voltages(2)	$V_{CC}/2$		V
Input Rise Time t_r and Fall Time t_f(2)(3)		1	V/ns

1. All voltages are referenced to V_{SS}.
2. V_{CC}=V_{CCQ}
3. Referenced to V_{SS}.

Figure 11. AC measurement I/O waveform



1. Logic states ‘1’ and ‘0’ correspond to AC test inputs driven at V_{CCQ} and V_{SS} respectively. Input timings begin at $V_{CCQ}/2$ and output timings end at $V_{CCQ}/2$.

Figure 12. AC Input transitions

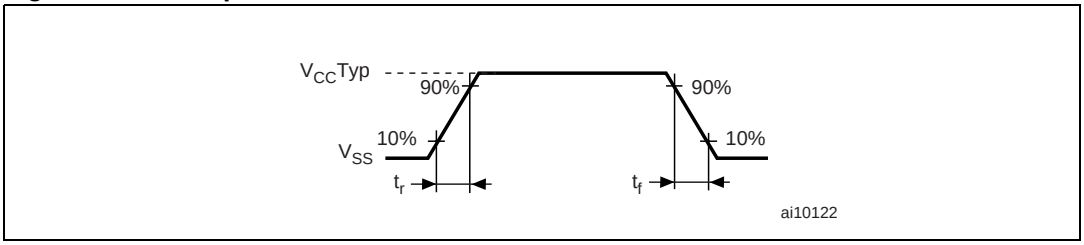


Figure 13. AC measurement load circuit

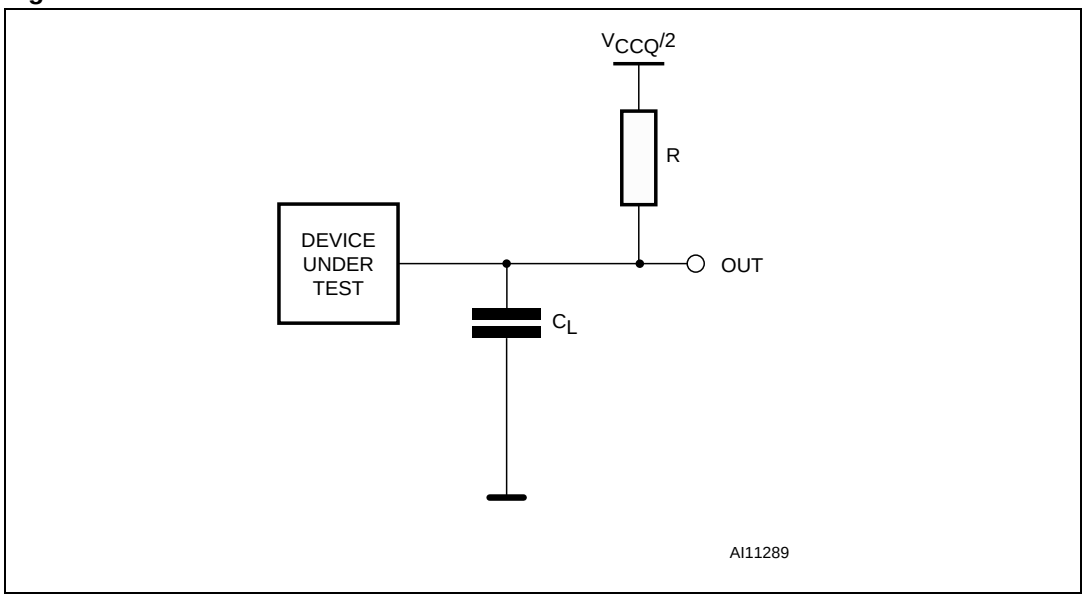


Table 15. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, V_{IN} = 0V	2	6	pF
C_{IO}	Data Input/Output Capacitance		3.5	6	pF

Table 16. DC characteristics

Symbol	Parameter	Refreshed Array	Test Conditions			Min.	Typ.	Max.	Unit
V_{OH}(1)	Output High Voltage		I_{OH} = –0.2mA			0.8V_{CCQ}			V
V_{OL}(1)	Output Low Voltage		I_{OL} = 0.2mA					0.2V_{CCQ}	V
V_{IH}(2)	Input High Voltage					V_{CCQ}–0.4		V_{CCQ} + 0.2	V
V_{IL}(3)	Input Low Voltage					–0.2		0.4	V
I_{LI}	Input Leakage Current		V_{IN} = 0 to V_{CCQ}					1	µA
I_{LO}	Output Leakage Current		$\overline{G}$ = V_{IH} or $\overline{E}$ = V_{IH}					1	µA
I_{CC1}(4)	Asynchronous Read/Write Random at t_{RC} min		V_{IN} = 0V or V_{CCQ}, I_{OUT} = 0mA, $\overline{E}$ = V_{IL}		70ns			25	mA
I_{CC2}(4)	Asynchronous Page Read		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}		70ns			15	mA
I_{CC3}(4)	Burst, Initial Read/Write Access		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}		104MHz			35	mA
					80MHz			30	mA
I_{CC4R}(4)	Continuous Burst Read		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}		104MHz			30	mA
					80MHz			25	mA
I_{CC4W}(4)	Continuous Burst Write		V_{IN} = 0V or V_{CCQ} I_{OUT} = 0mA, $\overline{E}$ = V_{IL}		104MHz			35	mA
					80MHz			30	mA
I_{PASR}(4)	Partial Array Refresh Standby Current	Full Array	V_{IN} = 0V or V_{CCQ} $\overline{E}$ = V_{CCQ}					200	µA
		1/2 Array						170	µA
		1/4 Array						155	µA
		1/8 Array						150	µA
		None						140	µA
I_{SB}(5)	Standby Current		V_{IN} = 0V or V_{CCQ}, $\overline{E}$ = V_{CCQ}					200	µA
I_{CCPD}	Deep-Power Down Current		V_{IN} = 0V or V_{CCQ}, V_{CC}, V_{CCQ} = 1.95V; T_A= +85°C				3	10	µA

1. BCR5-BCR4 = 01 (default settings).
2. Input signals may overshoot to V_{CCQ}+ 1.0V for periods of less than 2ns during transitions.
3. Output signals may undershoot to V_{SS} – 1.0V for periods of less than 2ns during transitions.
4. This parameter is specified with all outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected for the actual system.
5. I_{SB} maximum value is measured at +85°C with PAR set to Full Array. In order to achieve low standby current, all inputs must be driven either to V_{CCQ} or V_{SSQ}. I_{SB} might be slightly higher for up to 500ms after Power-up, or when entering Standby mode.

Table 17. Asynchronous Read AC characteristics

Symbol	Alt.	Parameter[1]	70ns		Unit
			Min	Max	
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70	ns
t_{AVLH} t_{RHLH}	t_{AVS}	Address Valid to $\overline{L}$ High Configuration Register High to $\overline{L}$ High	5		ns
t_{BLQV}	t_{BA}	Upper/Lower Byte Enable Low to Output Valid		70	ns
t_{BHQZ}[2]	t_{BHZ}	Upper/Lower Byte Enable High to Output Hi-Z		8	ns
t_{BLQX}[3]	t_{BLZ}	Upper/Lower Byte Enable Low to Output Transition	10		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid		70	ns
t_{ELLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	7		ns
t_{EHEL}	t_{CPH}	Chip Enable High between Subsequent Asynchronous Operations	5		ns
t_{EHQZ}[2]	t_{HZ}	Output Enable High to Output Hi-Z Chip Enable High to Output Hi-Z		8	ns
t_{ELQX}[3]	t_{LZ}	Chip Enable Low to Output Transition	10		ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		20	ns
t_{GHQZ}[2]	t_{OHZ}	Output Enable Low to Output Hi-Z		8	ns
t_{GLQX}[3]	t_{OLZ}	Output Enable Low to Output Transition	3		ns
t_{AVAX}	t_{RC}	Read Cycle Time	70		ns
t_{LLLH}	t_{VP}	Latch Enable Low Pulse Width	5		ns
t_{LHLL}	t_{VPH}	Latch Enable High Pulse Width	10		ns
t_{LLQV}	t_{AADV}	Latch Enable Low to Output Valid		70	ns
t_{LHAX} t_{LHRL}	t_{AVH}	Latch Enable High to Address Transition Latch Enable High to Configuration Register Low	2		ns

1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 13: AC measurement load circuit*.
2. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.
3. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.

Table 18. Asynchronous Page Read AC characteristics

Symbol	Alt.	Parameter[1]	70ns		Unit
			Min	Max	
t_{AVQV1}	t_{APA}	Page Access Time	20		ns
t_{AVAV}	t_{PC}	Page Cycle Time	20		ns
t_{ELEH}	t_{CEM}	Maximum Chip Enable Pulse Width		4	µs
t_{AVQX}	t_{OH}	Data Hold from Address Change	5		ns

1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 13: AC measurement load circuit*.

Figure 14. Asynchronous Random Read AC waveforms

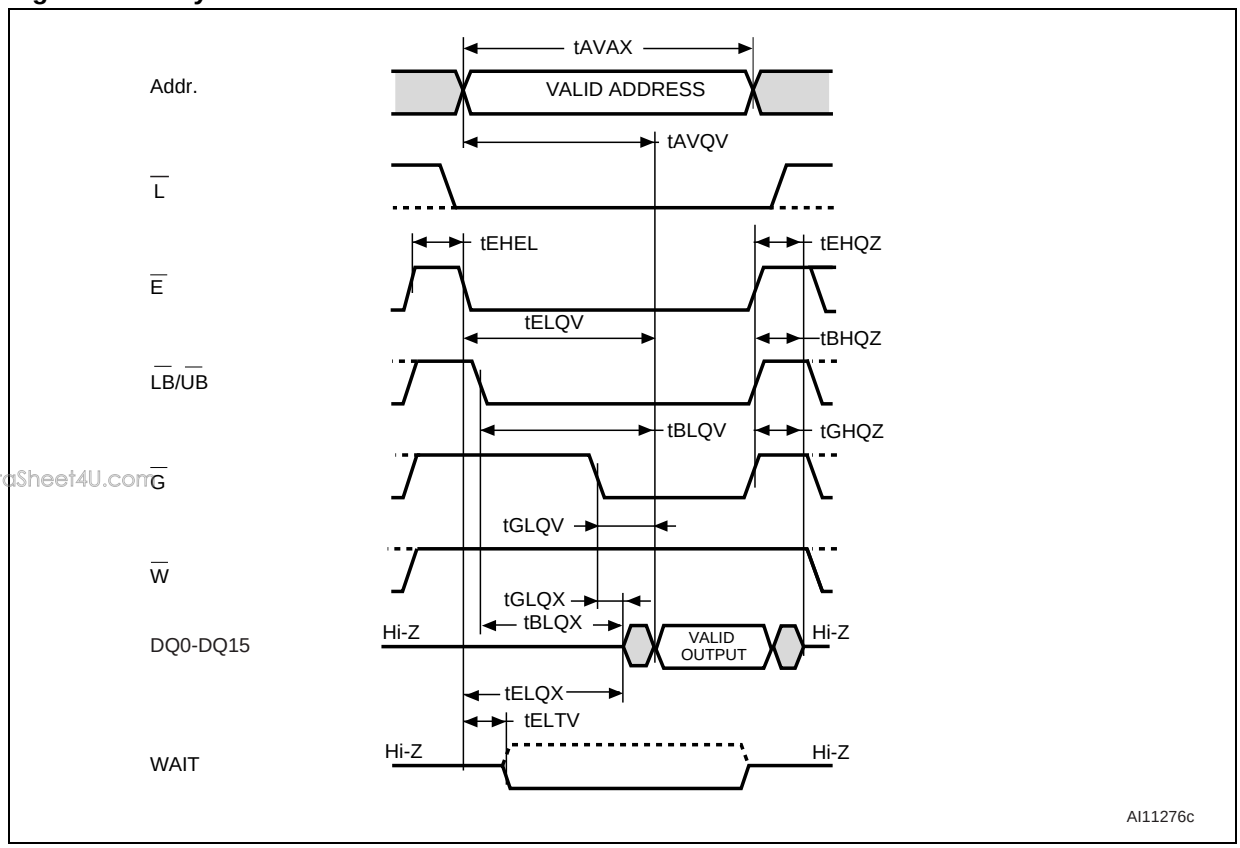


Figure 15. Latch Enable Controlled, Asynchronous Random Read AC waveforms

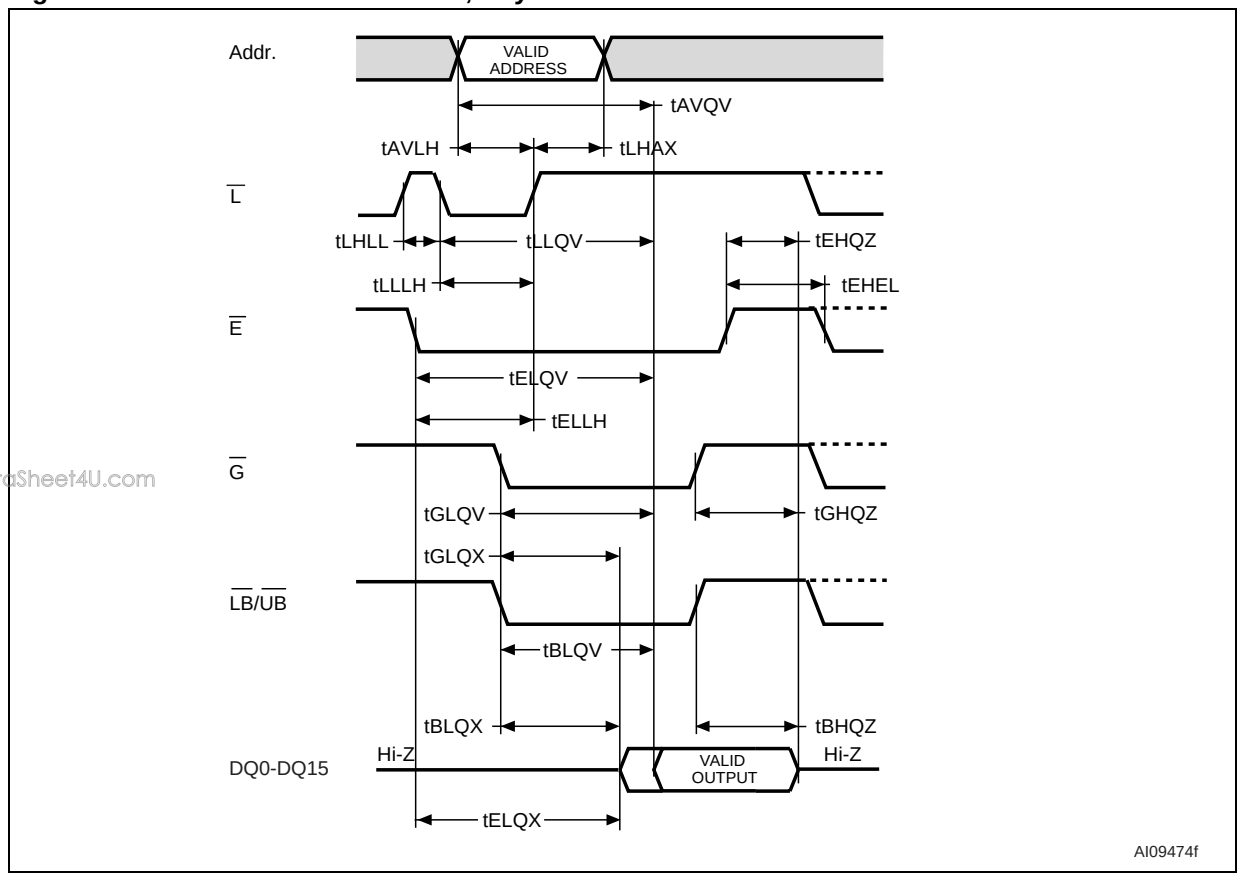
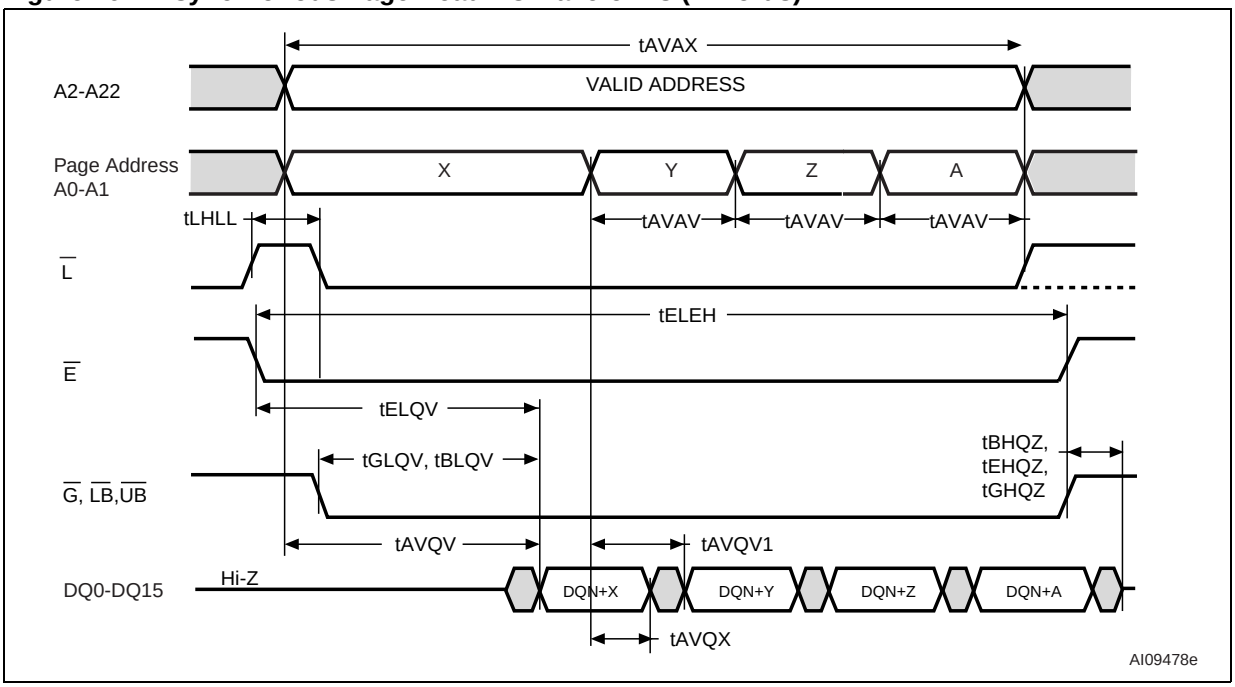
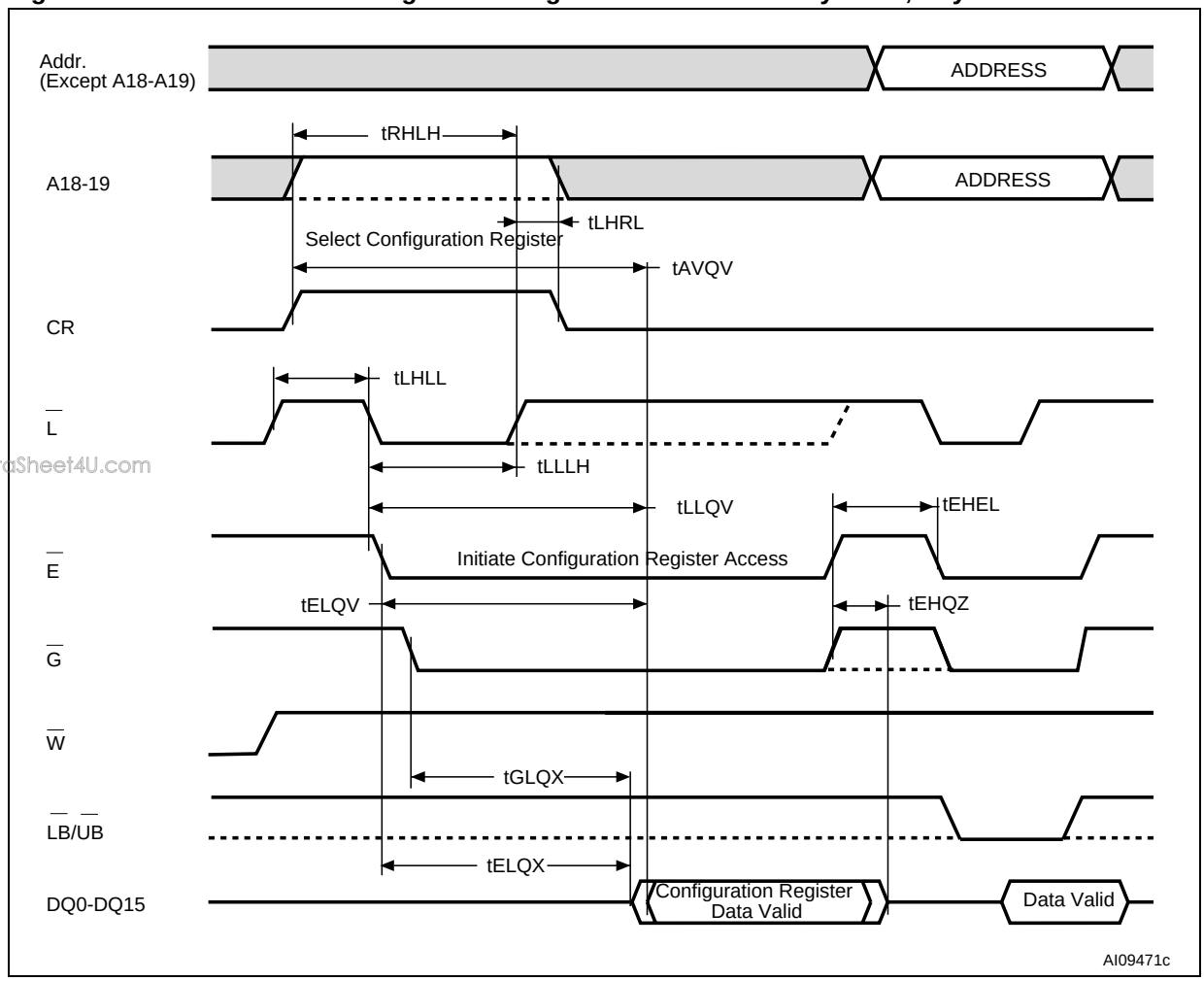


Figure 16. Asynchronous Page Read AC waveforms (4 Words)



1. Any address can be used as starting address.

Figure 17. CR Controlled Configuration Register Read followed by Read, Asynchronous mode



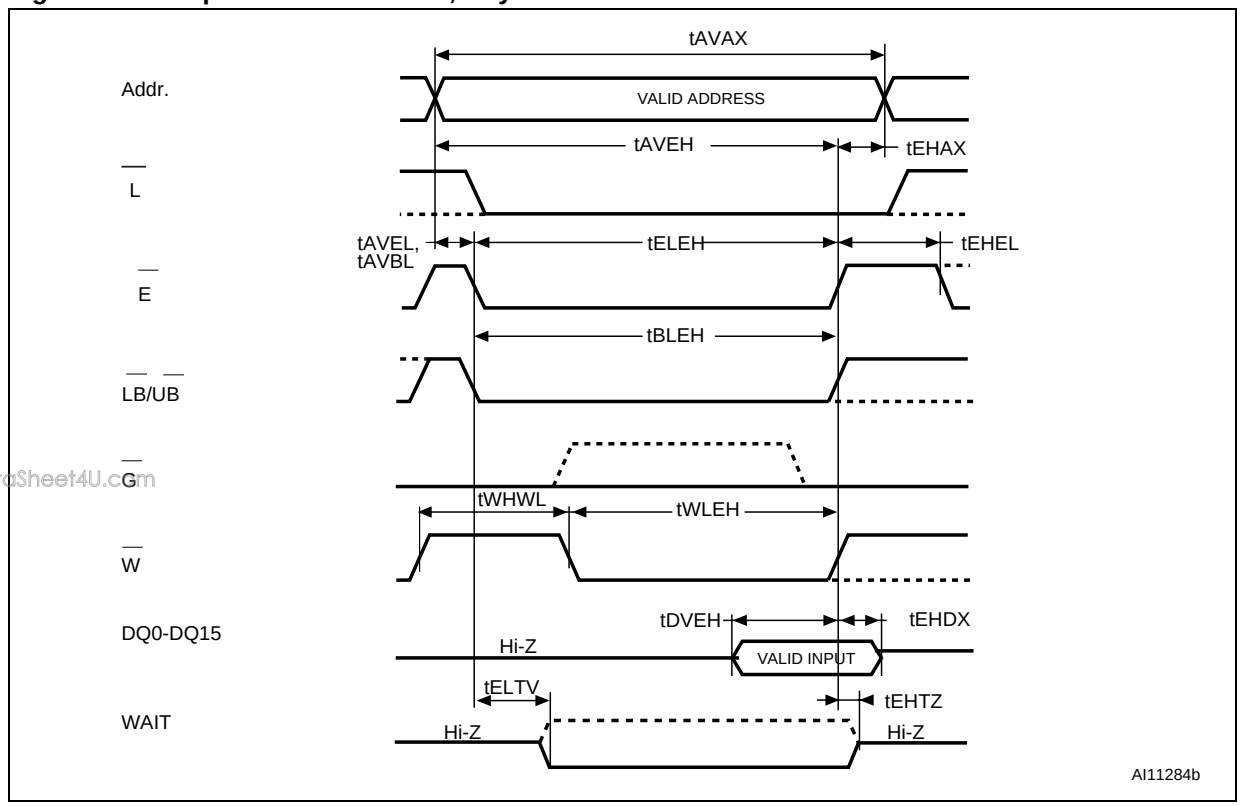
1. A18-A19 must be set to ‘00b’ to select RCR, ‘01b’ to select the BCR and ‘1Xb’ to select the DIDR.

Table 19. Asynchronous Write AC characteristics

Symbol	Alt.	Parameter[1]	70ns		Unit
			Min	Max	
t_{AVBL}, t_{AVEL}, t_{AVWL}, t_{LLWL}	t_{AS}	Address Set-up to Beginning of Write Operation	0		ns
t_{AVLH}, t_{RHLH}	t_{AVS}	Address Valid to Latch Enable High Configuration Register High to Latch Enable High	5		ns
t_{AVWH}, t_{AVEH}, t_{AVBH}	t_{AW}	Address Set-up to End of Write Operation	70		ns
t_{AVAX}	t_{WC}	Write Cycle Time	70		ns
t_{BLBH}, t_{BLEH} t_{BLWH}	t_{BW}	Upper/Lower Byte Enable Low to End of Write Operation	70		ns
t_{ELTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	ns
t_{EHEL}	t_{CPH}	Chip Enable High between Subsequent Asynchronous Operations	5		ns
t_{ELLH}	t_{CVS}	Chip Enable Low to $\overline{L}$ High	7		ns
t_{ELWH} t_{ELEH} t_{ELBH}	t_{CW}	Chip Enable Low to End of Write Operation	70		ns
t_{EHDX}, t_{WHDX}, t_{BHDX}	t_{DH}	Input Hold from Write	0		ns
t_{ELWH}, t_{DVBH}, t_{DVEH} t_{DVWH}	tDW	Input Valid to Write Setup Time	20		ns
t_{EHTZ}, t_{BHTZ}[2]	t_{HZ}	Chip Enable High to WAIT Hi-Z $\overline{LB}$/$\overline{UB}$ High to WAIT Hi-Z Write Enable High to WAIT Hi-Z		8	ns
t_{LHAX}, t_{LHRL}	t_{AVH}	Latch Enable High to Address Transition or Latch Enable High to Configuration Register Low	2		ns
t_{LLLH}	t_{VP}	Latch Enable Low Pulse Width	5		ns
t_{LHLL}	t_{VPH}	Latch Enable High Pulse Width	10		ns
t_{LLWH}	t_{VS}	Latch Enable Low to Write Enable High	70		ns
t_{WHQZ}	t_{WHZ}	Beginning of Asynchronous Write to Data Output Hi-Z		10	ns
t_{WLBH}, t_{WLEH}, t_{WLWH}[3]	t_{WP}	Write Pulse Width	45		ns
t_{WHWL}	t_{WPH}	Write Enable Pulse Width High	10		ns
t_{WHAX}, t_{EHAX}, t_{BHAX}	t_{WR}	Write Recovery Time	0		ns

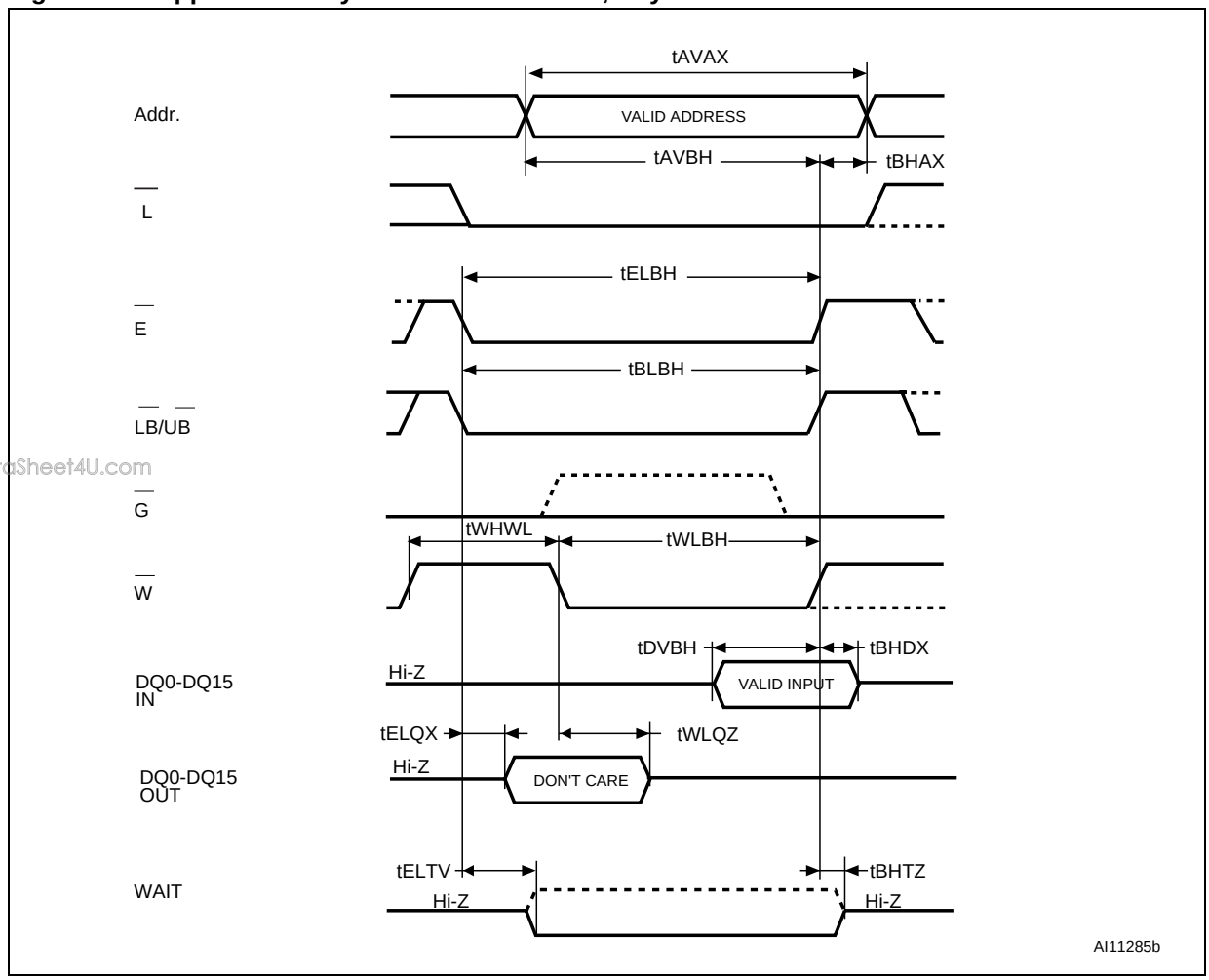
1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 13: AC measurement load circuit*.
2. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.
3. $\overline{W}$ Low time must be limited to t_{EHEL}.

Figure 18. Chip Enable controlled, Asynchronous Write AC waveforms



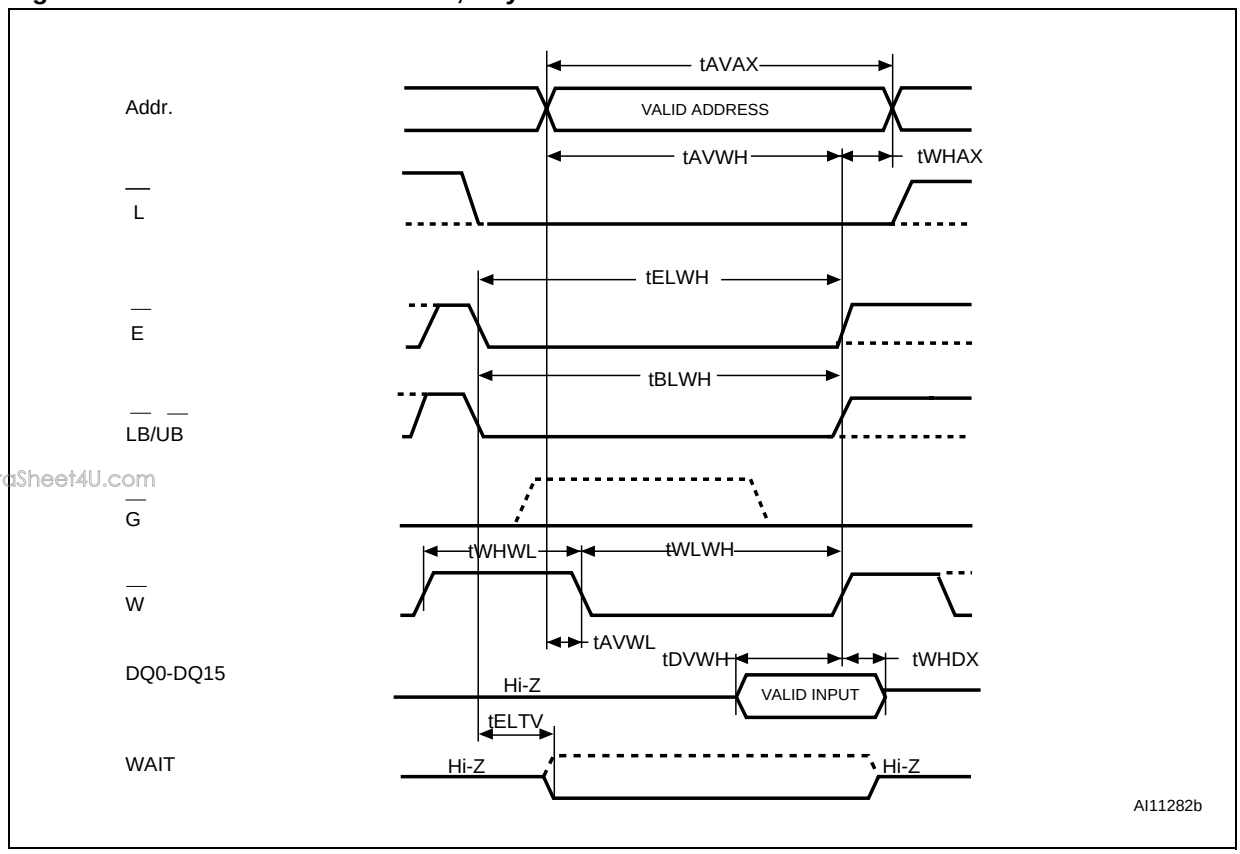
1. Data Inputs are Hi-Z if $\overline{E}$ is High, V_{IH}.

Figure 19. Upper/Lower Byte Enable controlled, Asynchronous Write AC waveforms



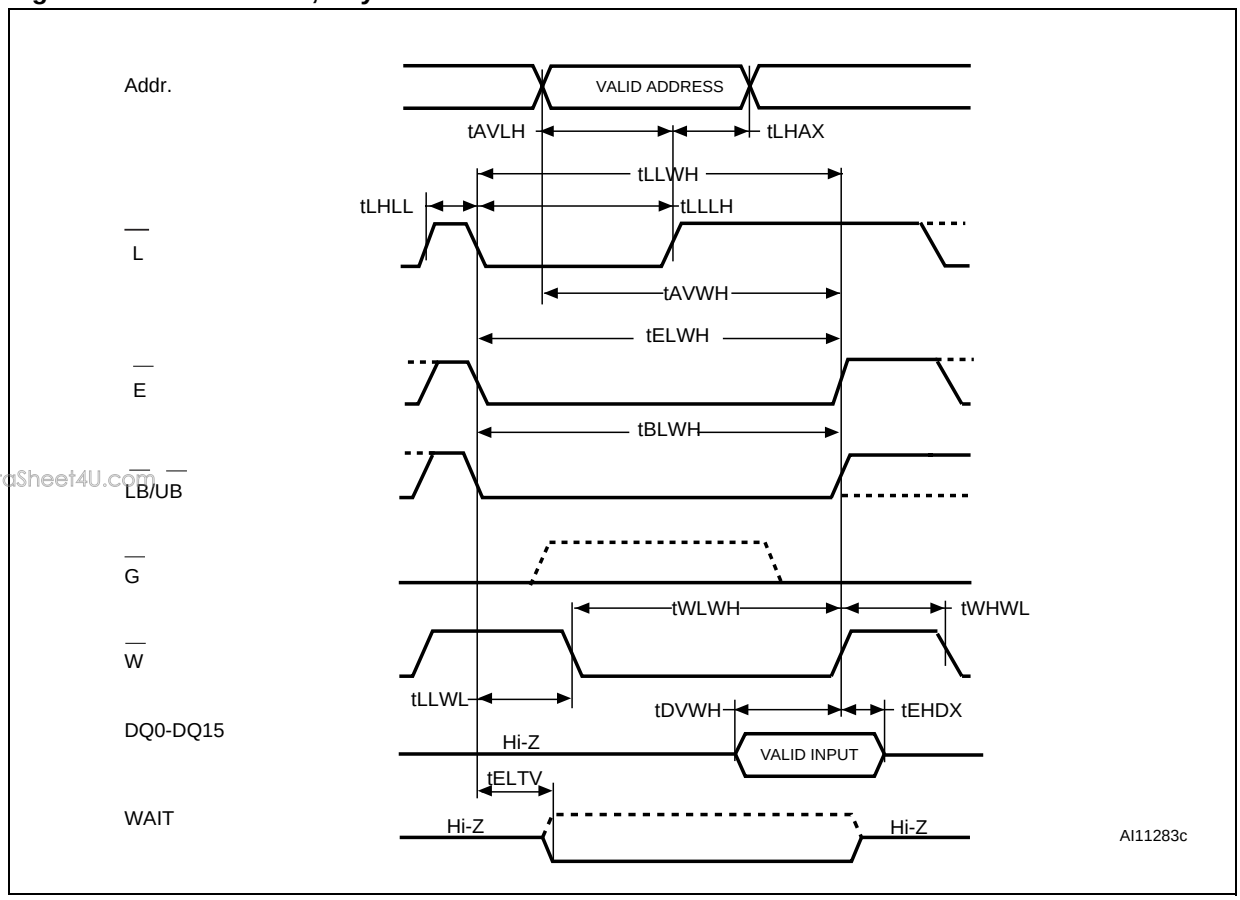
1. Data Inputs are Hi-Z if $\overline{E}$ is High, V_{IH}.

Figure 20. Write Enable controlled, Asynchronous Write AC waveforms



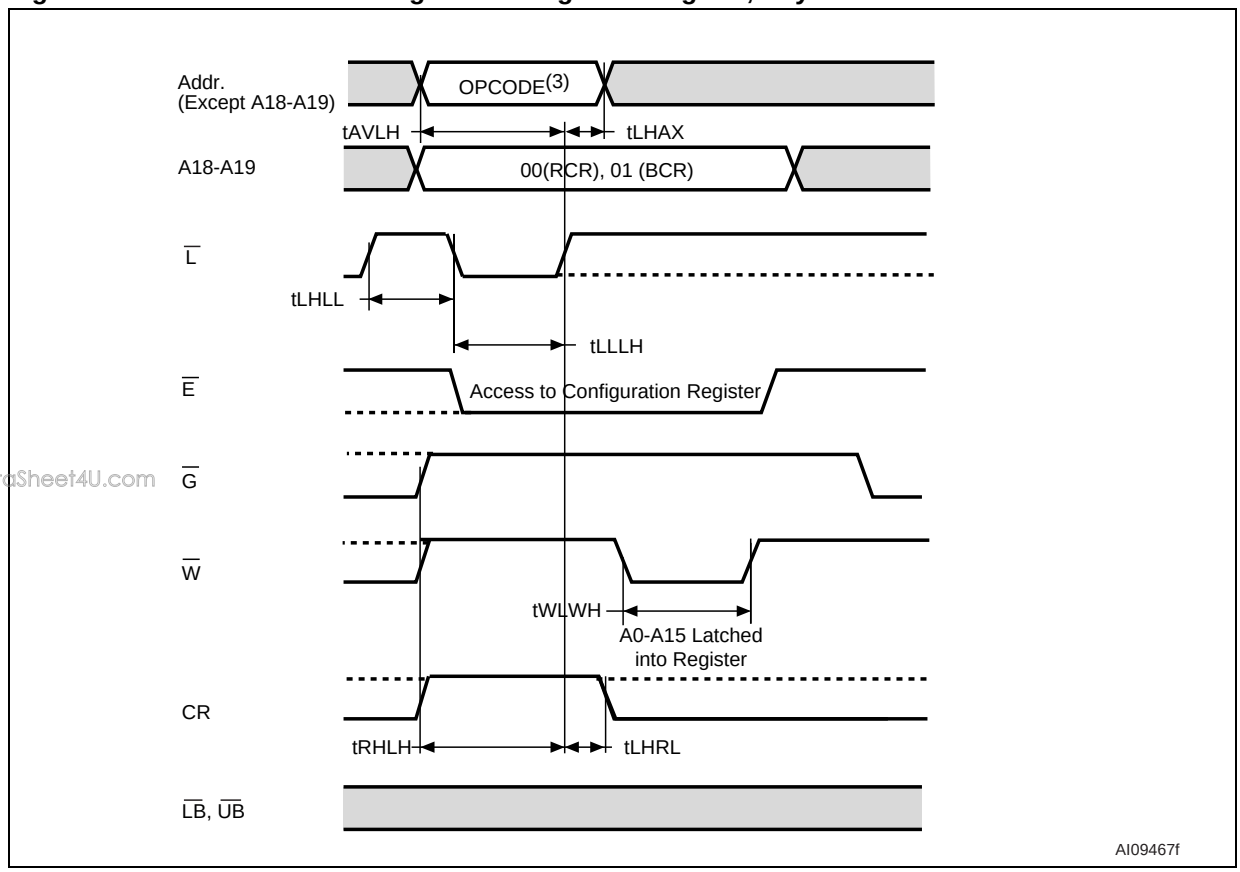
1. Data Inputs are Hi-Z if $\overline{E}$ is High, V_{IH}.

Figure 21. $\overline{L}$ controlled, Asynchronous Write AC waveforms



1. Data Inputs are Hi-Z if $\overline{E}$ is High, V_{IH}.

Figure 22. CR controlled Configuration Register Program, Asynchronous mode



1. Only the content of the Bus Configuration Register (BCR) and Refresh Configuration Register (RCR) can be modified.
2. Data Inputs/Outputs are not used.
3. The Opcode is the value to be written the configuration register.
4. $\overline{W}$ must go High after $\overline{L}$ goes High
5. CR is latched on the rising edge of $\overline{L}$. There is no setup requirement of CR with respect to $\overline{E}$.

Table 20. Clock related AC timings

Symbol	Alt.	Parameter	104 MHz		80 MHz		Unit
			Min.	Max.	Min.	Max.	
f_{CLk}	**f_{CLk}**	Clock frequency		104		80	MHz
t_{KHKH}	t_{CLK}	Clock Period	9.62		12.5		ns
t_R t_F	t_{KHKL}	Clock Rise Time Clock Fall Time		1.6		1.8	ns
t_{KHKL} t_{KLKH}	t_{KP}	Clock High to Clock Low Clock Low to Clock High	3		4		ns
t_{KHDZ}	t_{KHZ}	Clock High to Output Hi-Z	3	8	3	8	ns
t_{KHDX}	t_{KLZ}	Clock High to Output Transition	2	5	2	5	ns

Table 21. Synchronous Burst Read AC characteristics

Symbol	Alt.	Parameter[1]	104 MHz		80 MHz		Unit
			Min.	Max.	Min.	Max.	
t_{AVQV}	t_{AA}	Address Valid to Output Valid (Fixed Latency)		70		70	ns
t_{LLQV}	t_{AADV}	Latch Enable Low to Output Valid (Fixed Latency)		70		70	ns
t_{KHQV1}	t_{ABA}	Burst to Read Access Time (Variable Latency)		35		46	ns
t_{KHQV2}	t_{ACLK}	Clock High to Output Delay		7		9	ns
t_{GLQV}	t_{BOE}	Delay From Output Enable Low to Output Valid in Burst mode		20		20	ns
t_{EHEL}[2]	t_{CBPH}	Chip Enable High between Subsequent Operations in Full-Synchronous or NOR-Flash mode.	5		6		ns
t_{ELEH}[2]	t_{CEM}	Chip Enable Pulse Width		4		4	µs
t_{ELTV} t_{LLTV}	t_{CEW}	Chip Enable Low to WAIT Valid Latch Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid		70		70	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	3		4		ns
t_{KHAX} t_{KHBH} t_{KHWL} t_{KHEH} t_{KHLH} t_{KHQX}	t_{HD}	Hold Time From Active Clock Edge	2		2		ns
t_{EHQZ} t_{EHTZ}[3]	t_{HZ}	Chip Enable High to Output Hi-Z or WAIT Hi-Z		8		8	ns
t_{KHTX} t_{KHTV}	t_{KHTL}	Clock High to WAIT Valid		7		9	ns
t_{KHQX1}	t_{KLZ}	Clock High to Output Transition	2	5	2	5	ns
t_{KHQX2}	t_{KOH}	Output Hold from Clock High	2		2		ns
t_{GHQZ}[3]	t_{OHZ}	Output Enable High to Output Hi-Z		8		8	ns
t_{GLQX}[4]	t_{OLZ}	Output Enable Low to Output Transition	3		3		ns
t_{AVKH} t_{RHKH} t_{QVKH} t_{LLKH} t_{BLKH} t_{WHKH}	t_{SP}	Set-up Time to Active Clock Edge	3		3		ns

1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 13: AC measurement load circuit*.
2. A refresh opportunity must be offered every t_{ELEH}. A refresh opportunity is possible either if $\overline{E}$ is High during the rising edge of K; or if $\overline{E}$ is High for longer than 15ns.
3. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.
4. The Low-Z timings measure a 100mV transition from the Hi-Z ($V_{CCQ}/2$) level to either V_{OH} or V_{OL}.

Figure 23. Clock input AC waveform

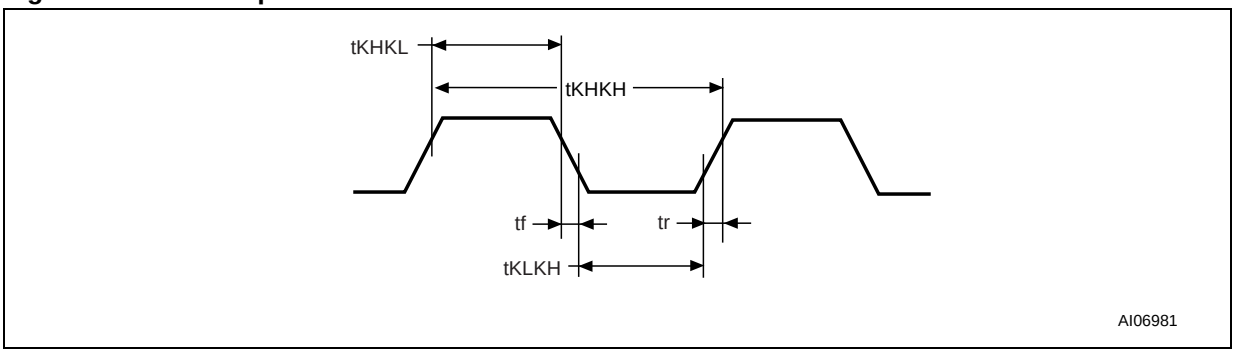
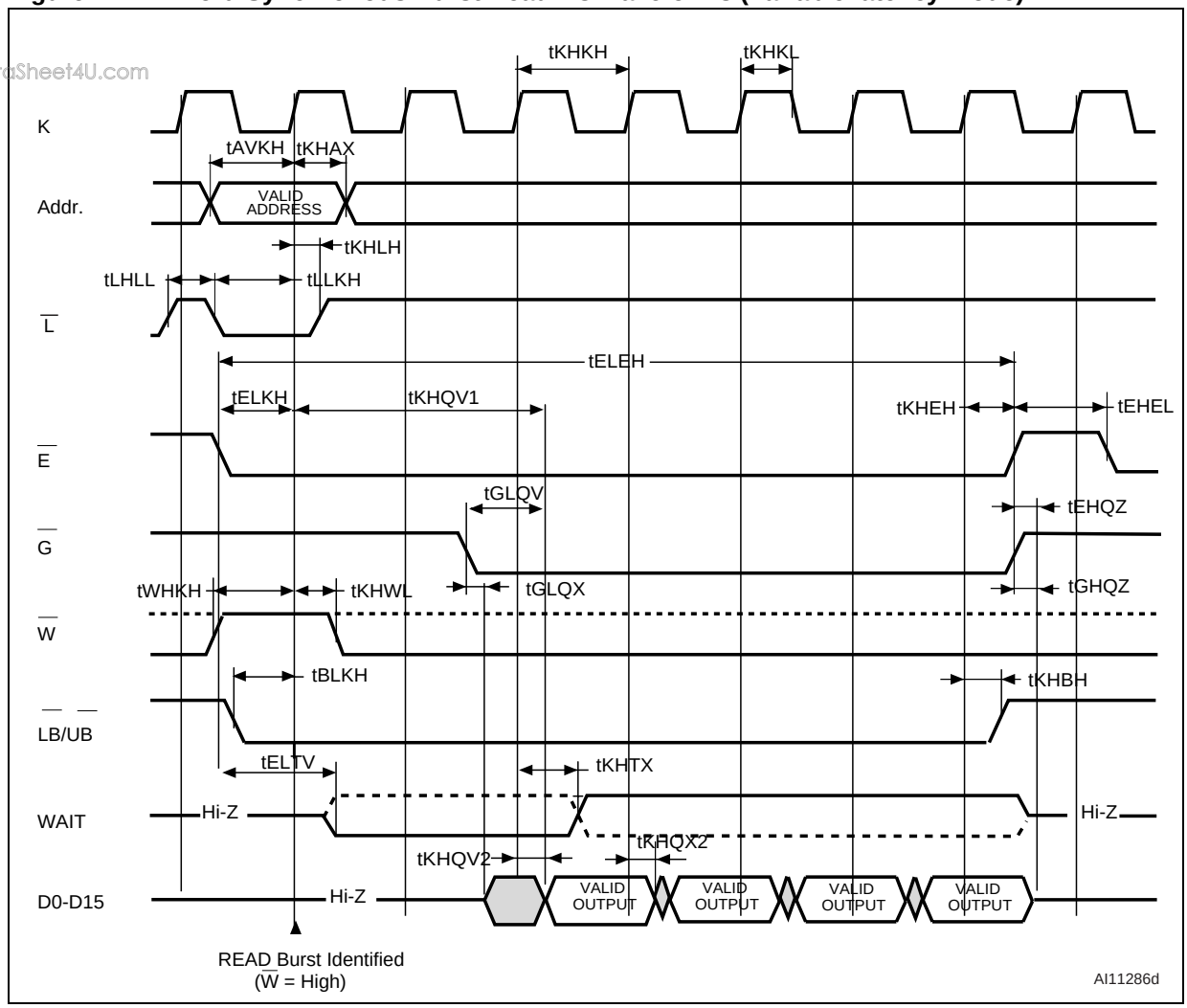
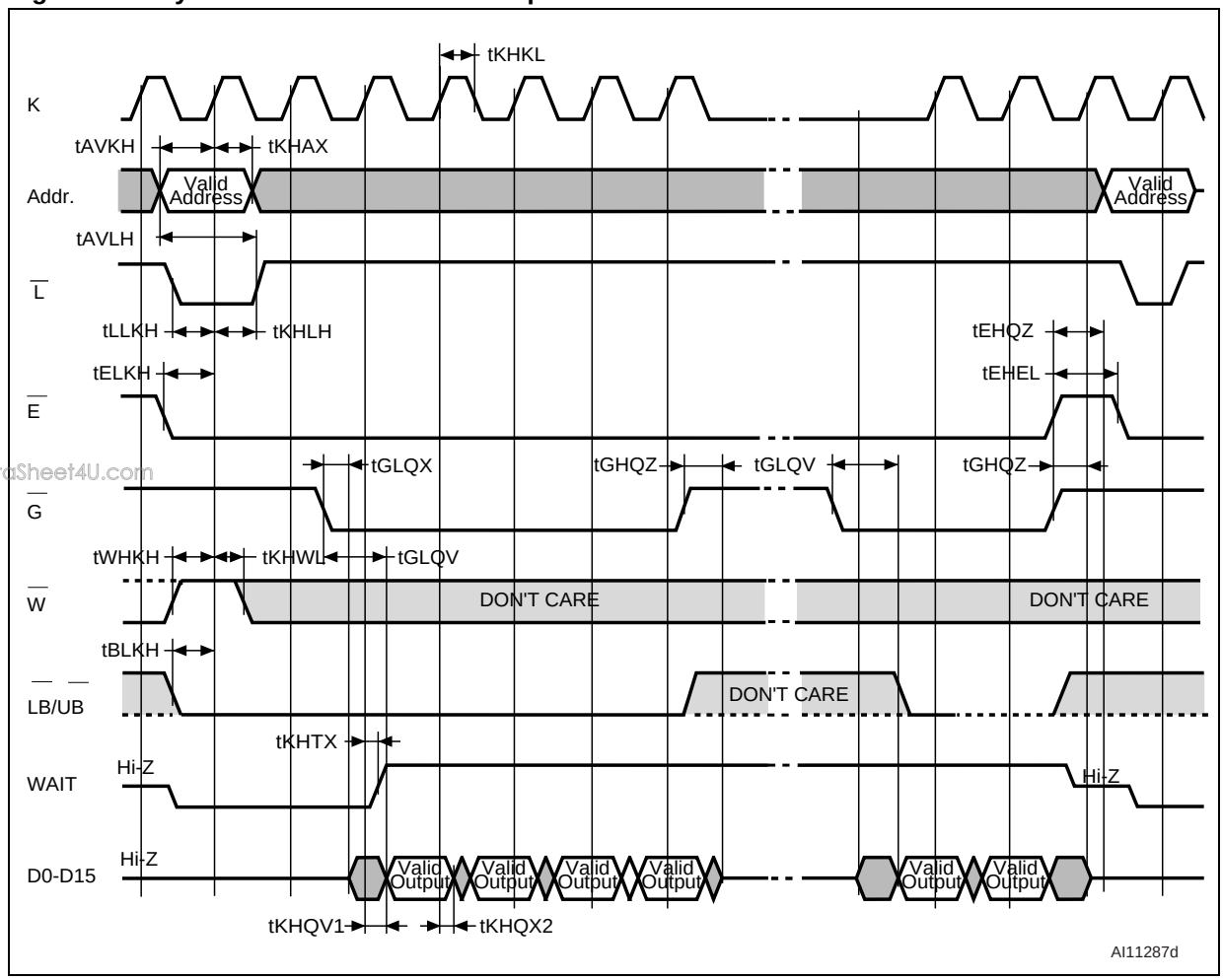


Figure 24. 4-Word Synchronous Burst Read AC waveforms (Variable latency mode)



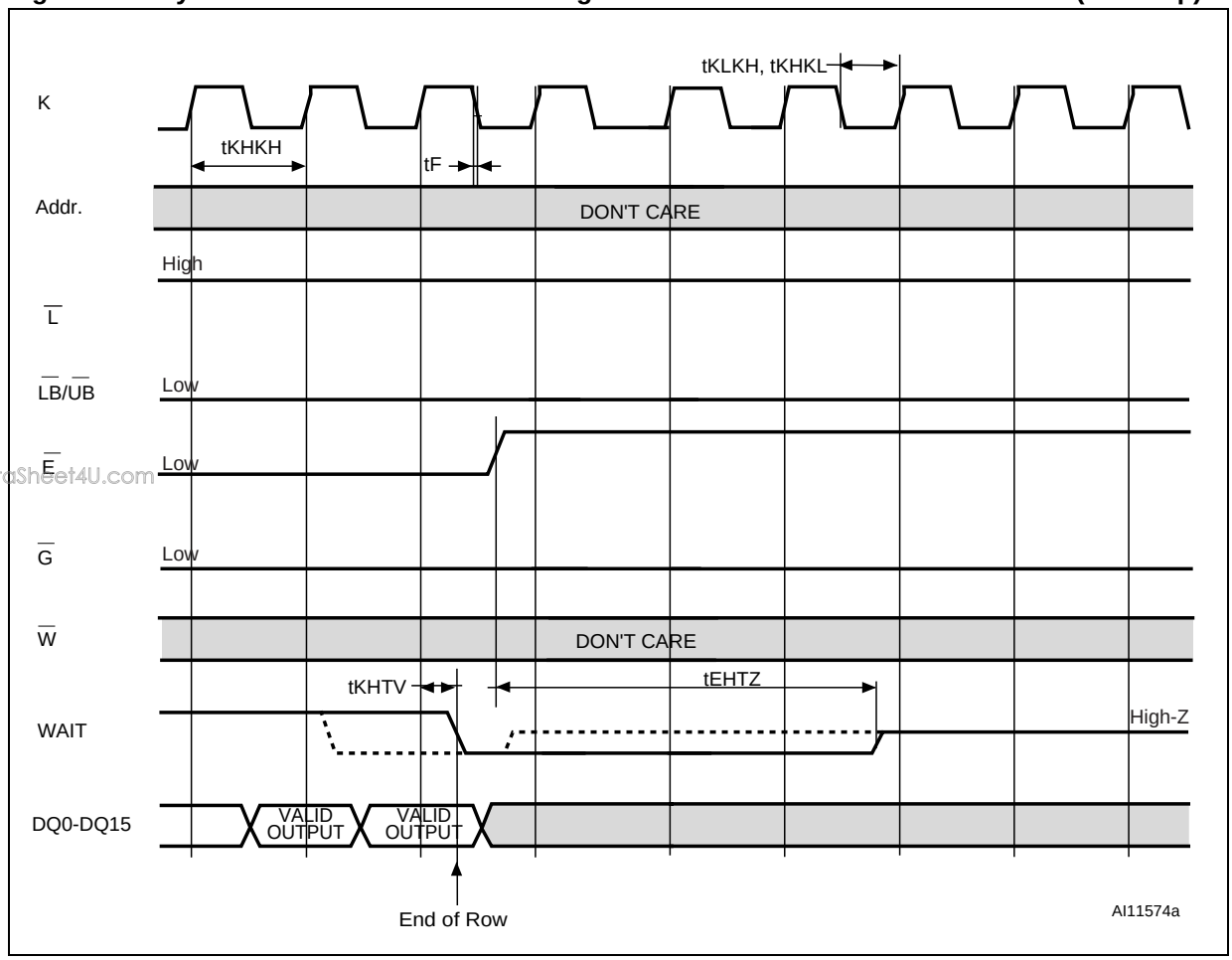
1. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 25. Synchronous Burst Read Suspend and Resume AC waveforms



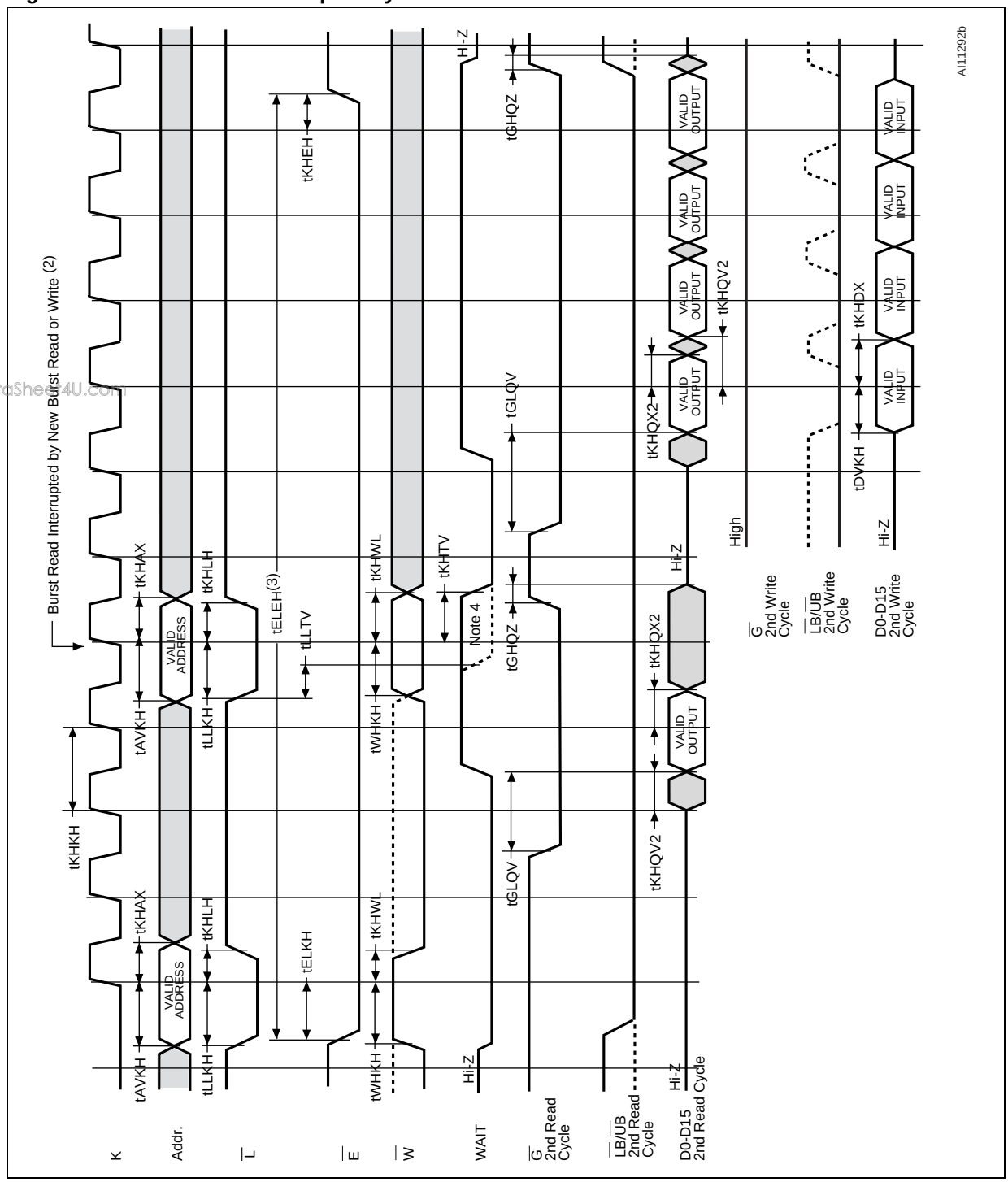
1. The latency Type (BCR14) can be set to fixed or variable during Burst Read Suspend operations.The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).
2. During Burst Read Suspend operations, the Clock signal must be stable (High or Low).
3. $\overline{G}$ can be held Low, V_{IL}, during Burst Suspend operations. If so, data output remain valid.

Figure 26. Synchronous Burst Read Showing End-of-Row Condition AC waveforms (No Wrap)



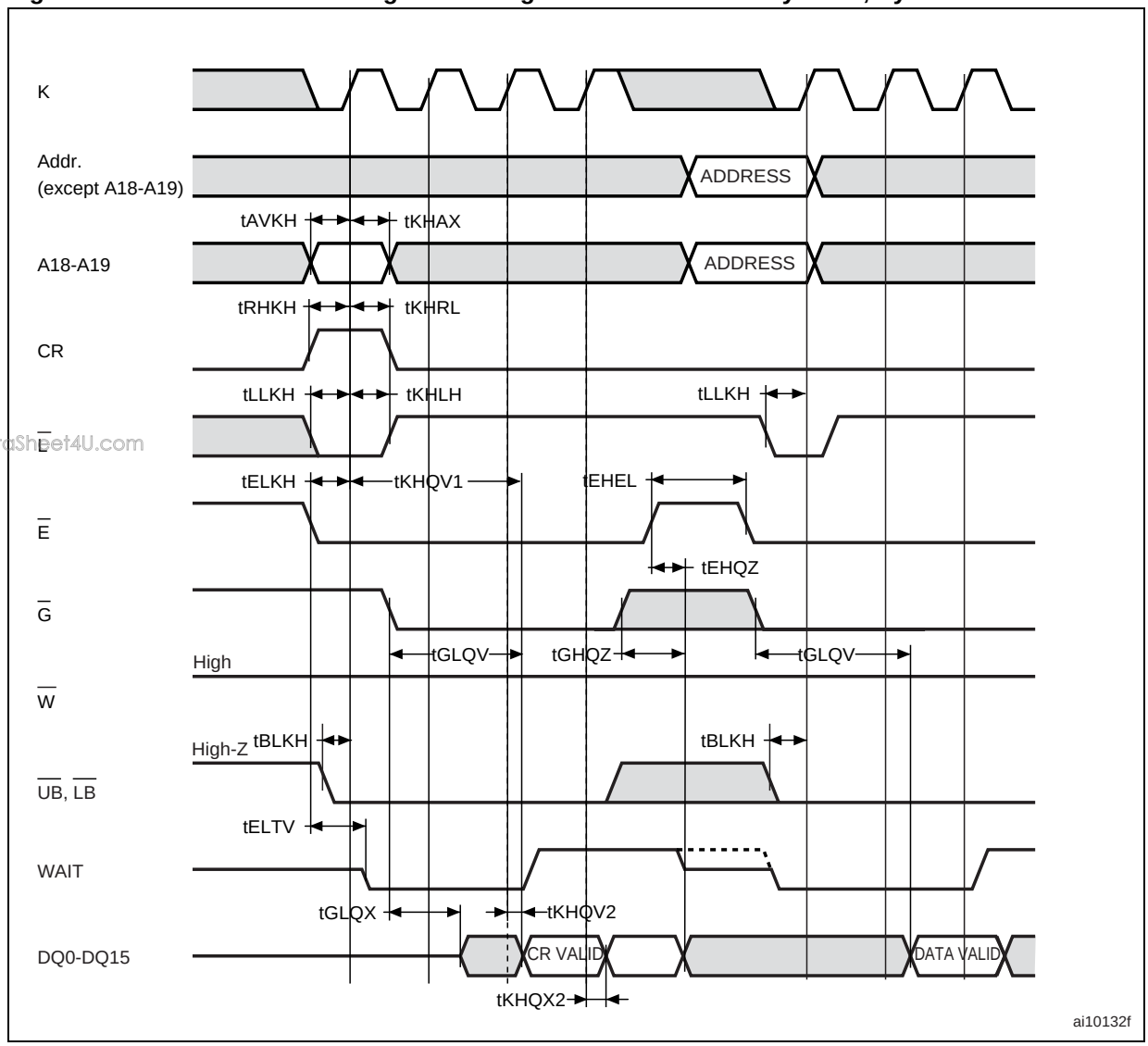
1. The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 27. Burst Read Interrupted by Burst Read or Write AC waveforms



1. The latency Type (BCR14) can be set to fixed or variable.The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). WAIT is active Low (BCR10=0), and is asserted during delay (BCR8=0). All Burst operations are given for variable latency and no refresh collision.
2. The Burst Read is interrupted during the first allowable clock cycle, i.e. after the first data is received by the microcontroller.
3. $\overline{E}$ can remain Low, V_{IL}, between burst operations, but it must not remain Low for longer than t_{ELEH}.
4. If the latency is variable, WAIT is asserted t_{KHTV} after $\overline{L}$ is clocked Low. If the latency is fixed, WAIT is asserted t_{LLTV} after $\overline{L}$ falling edge.

Figure 28. CR Controlled Configuration Register Read followed by Read, Synchronous mode



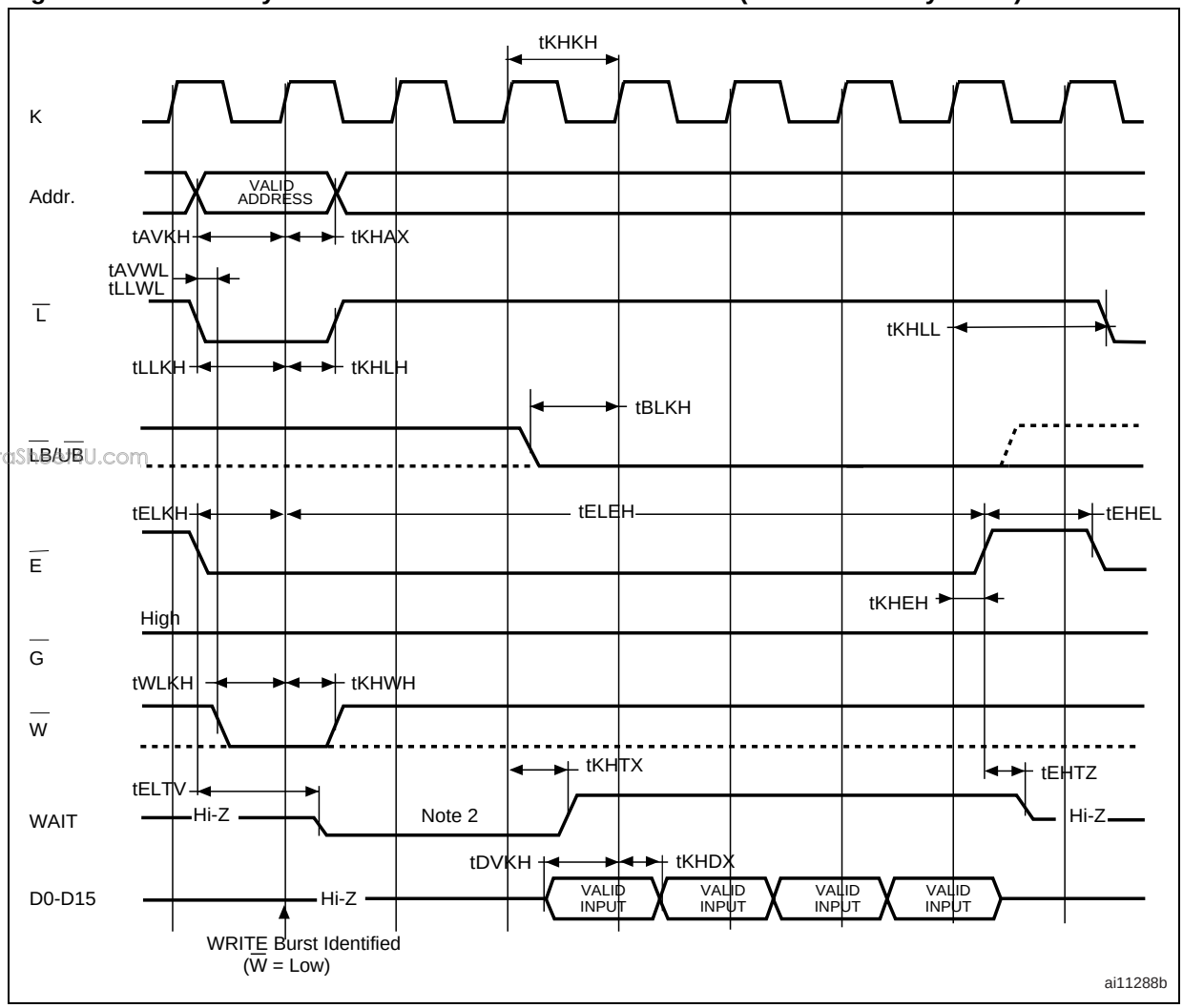
1. A18-A19 must be set to ‘00b’ to select RCR, ‘01b’ to select BCR and ‘1Xb’ to select the DIDR.

Table 22. Synchronous Burst Write AC characteristics

Symbol	Alt.	Parameter[1]	104MHz		80MHz		Unit
			Min	Max	Min	Max	
t_{AVWL} t_{LLWL}[2]	t_{AS}	Address Set-up to Beginning of Write Operation	0		0		ns
t_{AVKH} t_{DVKH} t_{WLKH} t_{LLKH} t_{BLKH} t_{WHKH} t_{WHWL}	t_{SP}	Set-up Time to Active Clock Edge	3		3		ns
t_{EHEL}[3]	t_{CBPH}	Chip Enable High between Subsequent Operations in Full-Synchronous or NOR-Flash mode.	5		6		ns
t_{ELEH}[3]	t_{CEM}	Maximum Chip Enable Low Pulse		4		4	µs
t_{ELTV} t_{LLTV}	t_{CEW}	Chip Enable Low to WAIT Valid	1	7.5	1	7.5	ns
t_{ELKH}	t_{CSP}	Chip Enable Low to Clock High	3		4		ns
t_{KHAX} t_{KHRL} t_{KHLH} t_{KHDX} t_{KHEH} t_{KHBH} t_{KHWH}	t_{HD}	Hold Time From Active Clock Edge	3		3		ns
t_{KHLL}	t_{KADV}	Last Clock Rising Edge to Latch Enable Low	15		15		ns
t_{EHDZ} t_{EHTZ}[4]	t_{HZ}	Chip Enable High to Input Hi-Z or WAIT Hi-Z		8		8	ns
t_{KHTV} tKHTX	t_{KHTL}	Clock High to WAIT Valid or Low		7		9	ns
t_{LHAX}	t_{AVH}	Latch Enable High to Address Transition (Fixed Latency)	2		2		ns

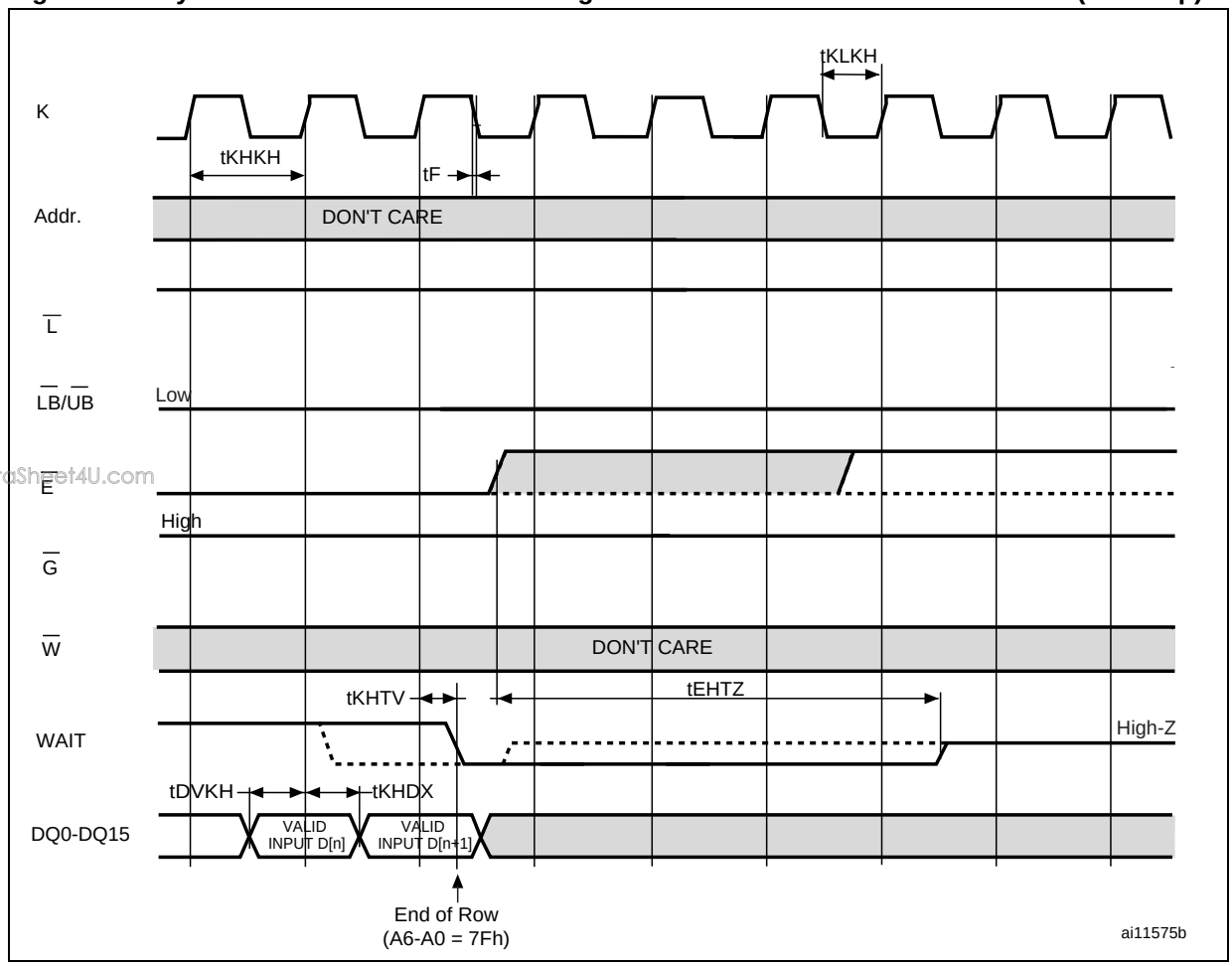
1. These timings have been obtained in the measurement conditions described in *Table 14: Operating and AC measurement conditions* and *Figure 13: AC measurement load circuit*.
2. t_{AVWL} and t_{LLWL}, are required if t_{ELKH}> 20ns.
3. A refresh opportunity must be offered every t_{ELEH}. A refresh opportunity is possible either if $\overline{E}$ is High during the rising edge of K; or if $\overline{E}$ is High for longer than 15ns.
4. The Hi-Z timings measure a 100mV transition from either V_{OH} or V_{OL} to $V_{CCQ}/2$.

Figure 29. 4-Word Synchronous Burst Write AC waveforms (Variable latency mode)



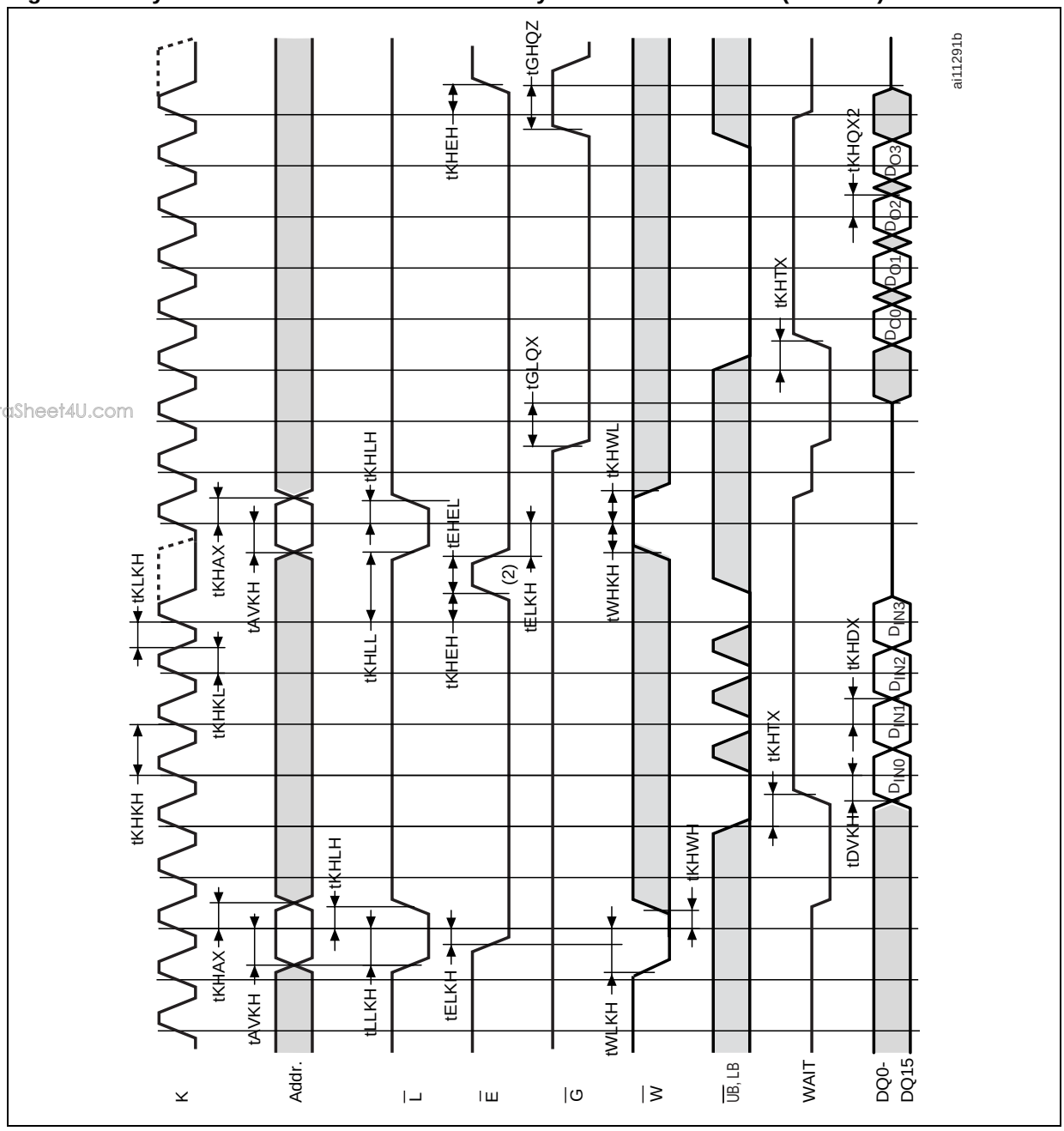
1. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and asserted during delay (BCR8=0).
2. The WAIT signal must remain asserted for LC clock cycles (LC Latency code), whatever the Latency mode (fixed or variable).
3. t_{AVLL} and t_{LLWL}, are required if t_{ELKH}> 20ns.

Figure 30. Synchronous Burst Write Showing End-of-Row Condition AC waveforms (No Wrap)



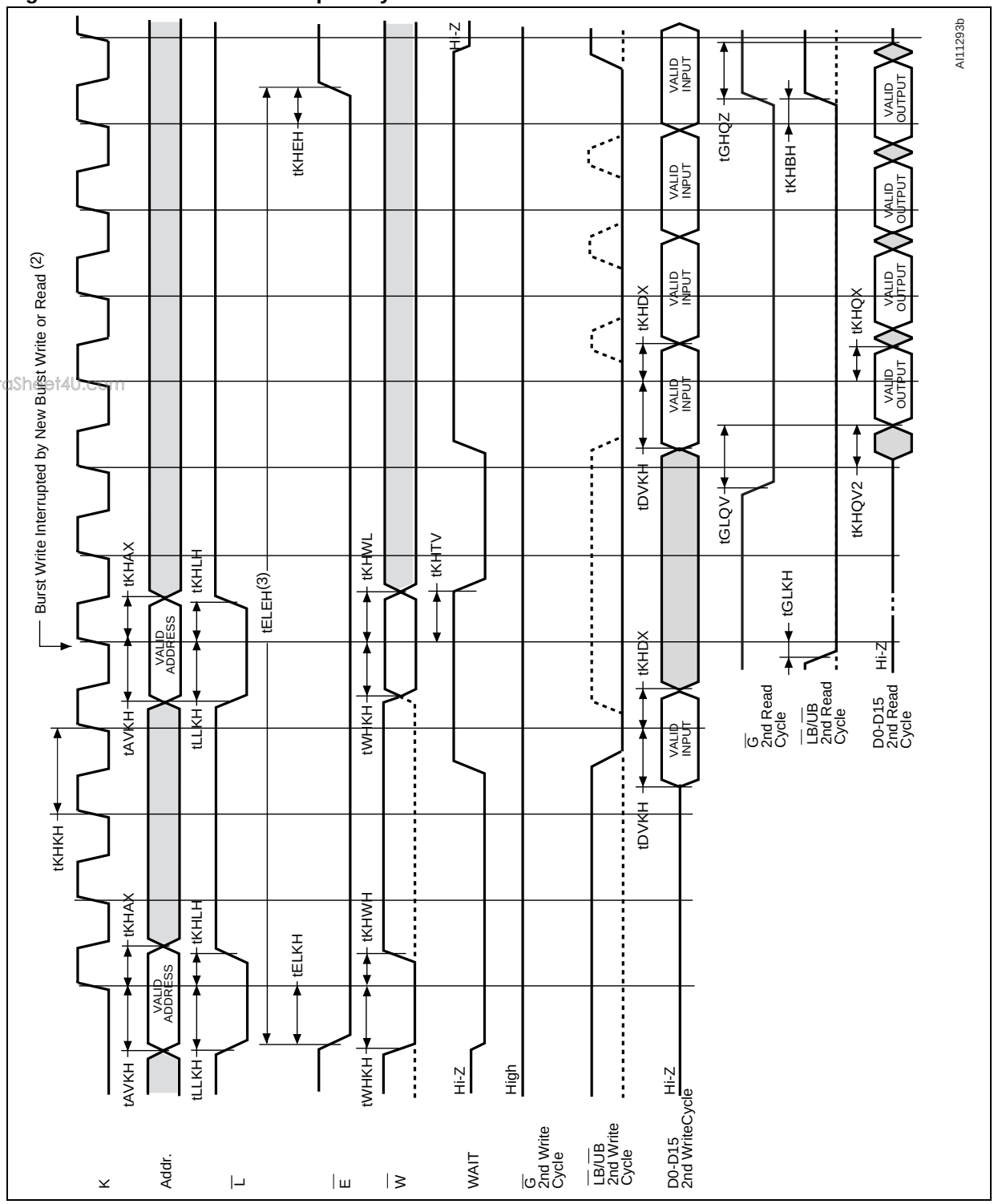
1. The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).

Figure 31. Synchronous Burst Write Followed by Read AC waveforms (4 Words)



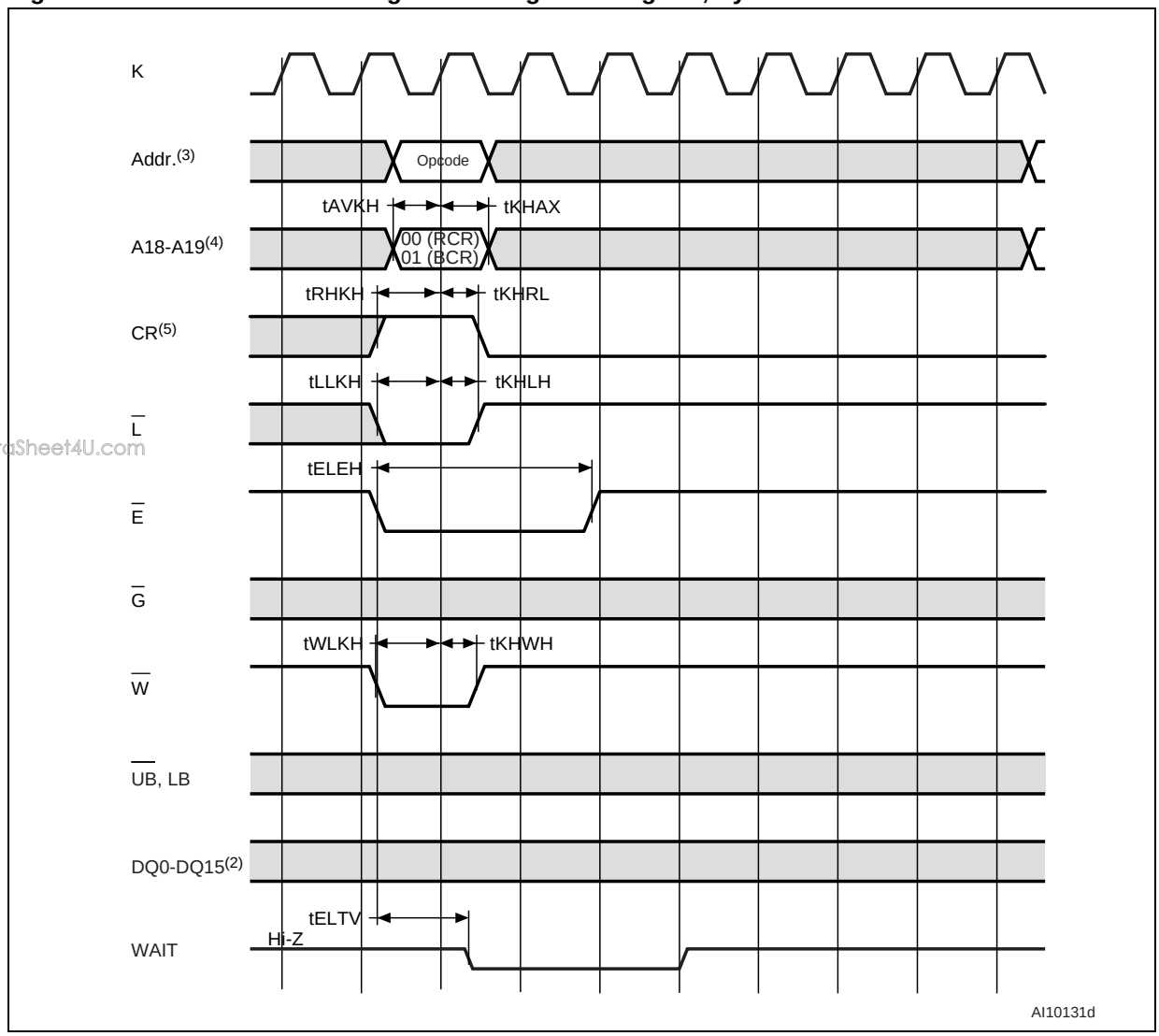
1. The Latency type can set to fixed or variable mode. The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). The WAIT signal is active Low (BCR10=0), and is asserted during delay (BCR8=0).
2. $\overline{E}$ can remain Low between the Burst Read and Burst Write operation, but it must not be held Low for longer than t_{ELEH}.

Figure 32. Burst Write Interrupted by Burst Write or Read AC waveforms



1. The latency Type (BCR14) can be set to fixed or variable.The Latency is set to 3 clock cycles (BCR13-BCR11 = 101). WAIT is active Low (BCR10=0), and is asserted during delay (BCR8=0). All Burst operations are given for variable latency and no refresh collision.
2. The Burst Write is interrupted during the first allowable clock cycle, i.e. after the first Word written to the memory.
3. $\overline{E}$, can remain Low, V_{IL}, between burst operations, but it must not remain Low for longer than t_{ELEH}.

Figure 33. CR Controlled Configuration Register Program, Synchronous mode

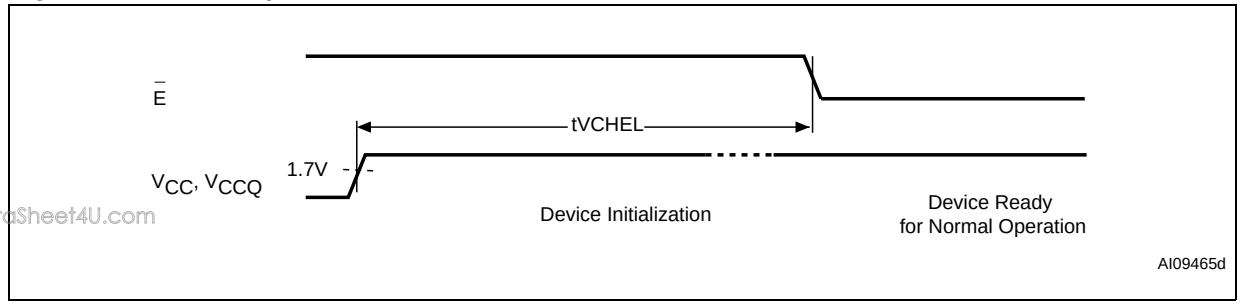


1. Only the Configuration Register (BCR) and the Refresh Configuration Register (RCR) can be modified.
2. Data Inputs/Outputs are not used.
3. The Opcode is the value to be written in the Configuration Register.
4. A19 gives the Configuration Register address.
5. CR initiates the Configuration Register Access.

Table 23. Power-Up and Deep Power-Down AC characteristics

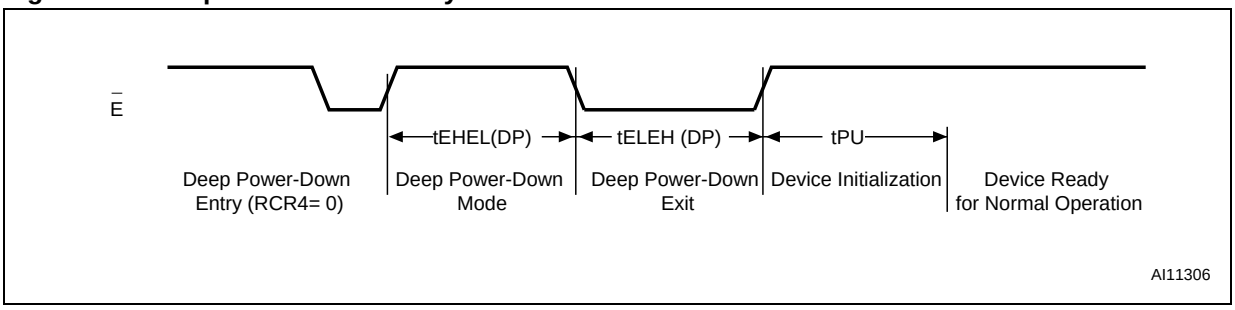
Symbol	Alt.	Parameter	Min	Max	Unit
t_{VCHEL}	t_{PU}	Initialization delay after Power-Up or Deep Power-Down Exit	150		µs
$t_{EHEL(DP)}$	t_{DPD}	Deep Power-Down Entry to Deep Power-Down Exit	10		µs
$t_{ELEH(DP)}$	t_{DPDX}	Chip Enable Low to Deep Power-Down Exit	10		µs

Figure 34. Power-Up AC waveforms



1. Power must be applied to V_{CC} prior to or at the same time as V_{CCQ}.

Figure 35. Deep Power-Down entry and exit AC waveforms



10 Part Numbering

Table 24. Ordering information scheme

Example: M69 K B 128 A B C W 8

Device Type

M69 = PSRAM

Mode

K = Bare Die

Operating Voltage

B = V_{CC} = 1.7 to 1.95V, Burst, Address/Data bus standard x16

Array Organization

128 = 128 Mbit (8Mb x16)

Option 1

A = 1 Chip Enable

Option 2

B = B Die

Maximum Clock Frequency

C = 80MHz max clock frequency in burst Read mode

D = 104MHz max clock frequency in burst Read mode

Package

W = Wafer form

Operating Temperature

8 = –30 to 85 °C

The notation used for the device number is as shown in *Table 24*. Not all combinations are necessarily available. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest STMicroelectronics Sales Office.

11 Revision history

Table 25. Document revision history

Date	Revision	Changes
07-Jul-2006	1	Initial release.

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