

COS/MOS INTEGRATED CIRCUITS

PRELIMINARY DATA

7-STAGE DIVIDER

- LOW POWER DISSIPATION
- LOW OUTPUT IMPEDANCE ON BOTH HIGH AND LOW STATE
- WIDE SUPPLY VOLTAGE RANGE: 5 to 15V
- HIGH NOISE IMMUNITY
- INPUTS FULLY PROTECTED

The M738/M740/M741/M747 are integrated circuits constructed in COS/MOS technology for use as frequency dividers in electronic organs. All the devices consist of 7 stages of binary division connected to give five divider blocks for the M741/M747 and four divider blocks for the M738/M740. The information transfer occurs on the positive going edge of the clock, for M740 and M747, and the negative going edge of the clock for M738/M741, and each output features a symmetrical impedance buffer (300Ω typ. at $V_{DD} = 10V$). They are available in 14 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

V_{DD}^{**}	Supply voltage	-0.5 to 15	V
V_I	Input voltage (at any pin)	-0.5 to $V_{DD} + 0.5$	V
P_{tot}	Total power dissipation (per package)	200	mW
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	-40 to 85	°C

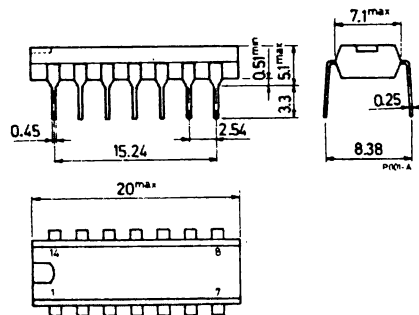
* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

** All voltages values are referred to V_{SS} pin voltage.

ORDERING NUMBERS: M 7XX B1 for dual in-line plastic package

MECHANICAL DATA

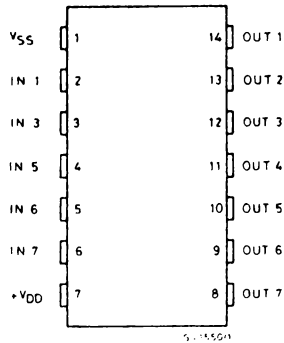
Dimensions in mm



M 738/M 740 M 741 / M 747

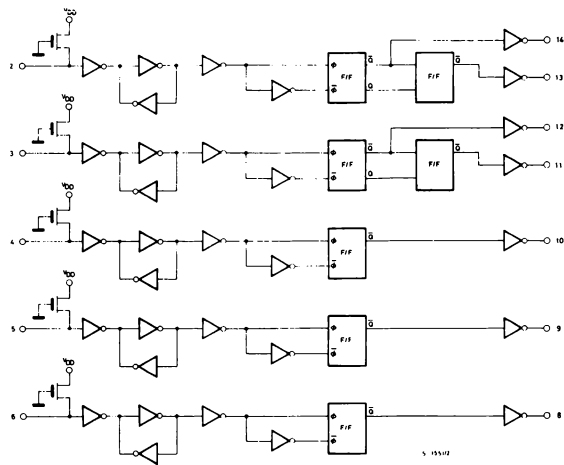
CONNECTION DIAGRAMS

For M741/M747

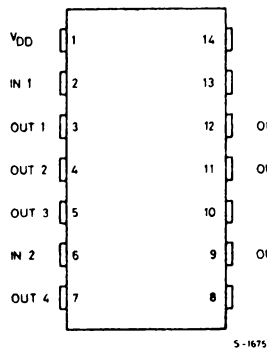


FUNCTIONAL DIAGRAMS

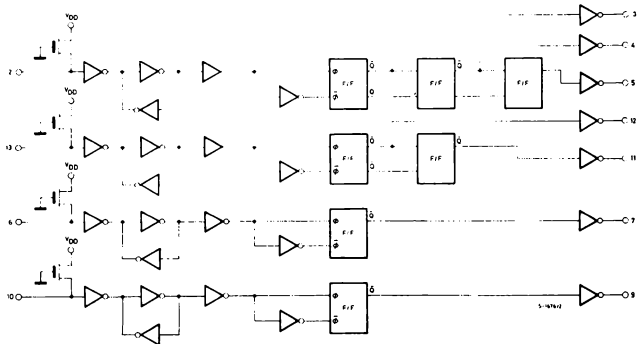
For M741/M747



For M738/M740



For M738/M740



RECOMMENDED OPERATING CONDITIONS

Parameter		V _{DD} (V)	Min.	Typ.	Max.	Unit
V _{DD}	Supply voltage		5		15	V
V _I	Input voltage		-0.5	V _{DD} + 0.5		V
T _{OP}	Operating temperature		-40		85	°C
t _w	Width of clock pulse (high or low)	5		200		ns
		10		100		

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Typical values are at $T_{amb} = 25^{\circ}\text{C}$

Parameter	Test conditions		Values									Unit
	V_O (V)	V_{DD} (V)	-40°C			25°C			85°C			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{CCL} Quiescent supply current	$V_i = V_{DD}$	5			5			5			300	μA
		10			10			10			600	
		15			50			50			2000	
V_{OH} High level output voltage	$I_o = 0$	5	4.99			4.99			4.95			V
		10	9.99			9.99			9.95			
		15	14.99			14.99			14.95			
V_{OL} Low level output voltage	$I_o = 0$	5		0.01			0.01			0.05	V	
		10		0.01			0.01			0.05		
		15		0.01			0.01			0.05		
I_{OL} Output drive current N-channel		0.5	5	0.5		0.5	0.8		0.45		mA	
		0.5	10	1		1	1.6		0.95			
		0.5	15	1.6		1.6	2.5		1.55			
I_{OH} Output drive current P-channel		4.5	5	-0.5		-0.5	-0.8		-0.45		mA	
		9.5	10	-1		-1	-1.6		-0.95			
		14.5	15	-1.6		-1.6	-2.5		-1.55			
I_{IL} Input current	$V_i = 0$	15				3	30	100			μA	
I_{IH} Input current	$V_i = V_{DD}$	15		1				1		1	μA	

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

Parameter	Test conditions	Values			Unit		
		V_{DD} (V)	Min.	Typ.		Max.	
t_{PLH} , t_{PHL} Propagation delay time from inputs to:	1 division stage outputs	$C_L = 15\text{ pF}$ on all outputs see timing diagram	5			500	ns
			10			250	
	2 division stage outputs		5			1000	ns
			10			500	
	3 division stage outputs		5			1500	ns
			10			750	
t_{TLH} , t_{THL} Output transition time		5			500	ns	
		10			250		
f_{max} Maximum toggle frequency	$C_L = 15\text{ pF}$ on all outputs	5	0.6	2.5		MHz	
		10	2	5			
* Cross talk immunity level				70		dB	
C_i Input capacitance				5		pF	

* Send a frequency of 20 kHz to input V_{I1} charge output V_{O1} with $5\text{ k}\Omega$ and 15 pF , measure the level of the 10 kHz frequency present at all outputs.

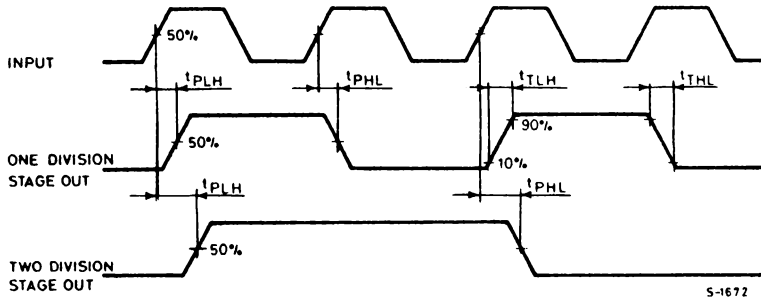
$$\text{Cross talk level} = 20 \log \frac{V_{O1} (10\text{ kHz})}{V_{OX} (10\text{ kHz})}$$

With the exception of V_{O1} , the output where the 10 kHz signal is greatest is V_{OX} .
This operation is repeated for all the inputs.

M 738 / M 740 M 741 / M 747

TIMING DIAGRAM

For M740/M747



For M738/M741

