

MITSUBISHI <DIGITAL ASSP>
M74HC643-1P/FP

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

DESCRIPTION

The M74HC643-1 is an integrated circuit chip consisting of eight bus transceivers with inverted and noninverted outputs.

FEATURES

- High-fanout 3-state output : ($I_{OL}=24\text{mA}$, $I_{OH}=-24\text{mA}$)
- High-speed : 8ns typ. ($C_L=50\text{pF}$, $V_{CC}=5\text{V}$)
- Low power dissipation : $25\mu\text{W}/\text{package}$, max
($V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$, quiescent state)
- High noise margin : 30% of V_{CC} , min ($V_{CC}=4.5, 6\text{V}$)
- Capable of driving 60 74LSTTL loads
- Wide operating voltage range : $V_{CC}=2\sim 6\text{V}$
- Wide operating temperature range : $T_a=-40\sim +85^\circ\text{C}$

APPLICATION

General purpose, for use in industrial and consumer digital equipment

FUNCTION

Use of silicon gate technology allows the M74HC643-1 to maintain the low power dissipation and high noise margin characteristics of the standard CMOS logic 4000B series while giving high-speed performance equivalent to the 74LS643. The circuit is designed to suppress the increased switching noise that normally occurs at high output currents. Two buffers with 3-state inverted and noninverted outputs have their inputs and outputs mutually connected and can be used as buffers in both directions.

The input/output direction is controlled by direction input DIR.

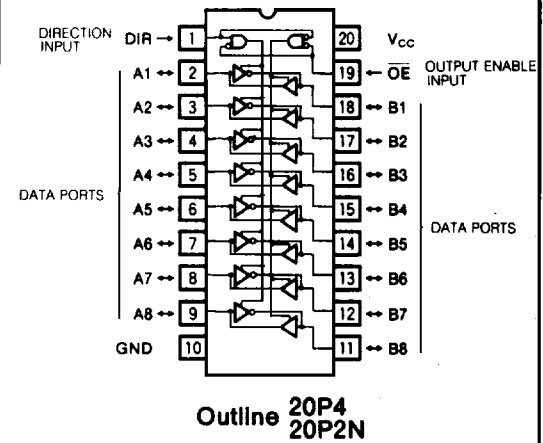
When DIR is high-level, the A data ports are set as input terminals and the B data ports are set as output terminals. When DIR is low-level, the B data ports are set as input terminals and the A data ports are set as output terminals. When output enable input OE is high-level, A and B both become high impedance state and are separated.

FUNCTION TABLE (Note 1)

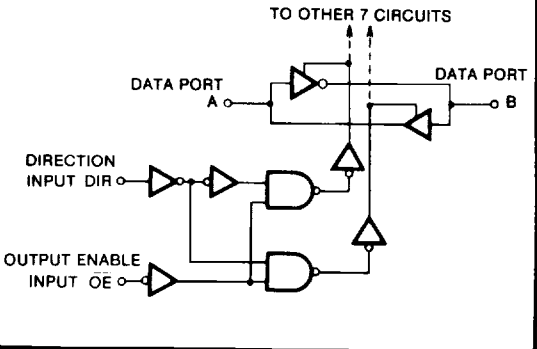
Inputs		Data ports	
OE	DIR	A	B
L	L	O	I
L	H	I	O
H	X	Z	Z

- Note 1 : I : Input pin
 O : Output pin (noninverted output)
 \bar{O} : Output pin (inverted output)
 Z : High impedance state (A and B are separated)
 X : Irrelevant

PIN CONFIGURATION (TOP VIEW)



LOGIC DIAGRAM (EACH TRANSCEIVER)



OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

ABSOLUTE MAXIMUM RATINGS ($T_a = -40 \sim +85^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.5 \sim +7.0$	V
V_i	Input voltage		$-0.5 \sim V_{CC} + 0.5$	V
V_o	Output voltage		$-0.5 \sim V_{CC} + 0.5$	V
I_{IK}	Input protection diode current	$V_i < 0V$	-20	mA
		$V_i > V_{CC}$	20	
I_{OK}	Output parasitic diode current	$V_o < 0V$	-20	mA
		$V_o > V_{CC}$	20	
I_o	Output current		± 50	mA
I_{CC}	Supply/GND current	V_{CC}, GND	± 200	mA
P_d	Power dissipation	(Note 2)	500	mW
T_{stg}	Storage temperature		$-65 \sim +150$	$^\circ\text{C}$

Note 2 : M74HC643-1FP : $T_a = -40 \sim +75^\circ\text{C}$ and $T_a = 75 \sim 85^\circ\text{C}$ are derated at $-7\text{mW}/^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim +85^\circ\text{C}$)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	2		6	V
V_i	Input voltage	0		V_{CC}	V
V_o	Output voltage	0		V_{CC}	V
T_{opr}	Operating temperature	-40		+85	$^\circ\text{C}$
t_r, t_f	Input rise time, fall time	$V_{CC} = 2.0V$	0	500	ns/V
		$V_{CC} = 4.5V$	0	50	
		$V_{CC} = 6.0V$	0	30	

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits					Unit	
			25 $^\circ\text{C}$			$-40 \sim +85^\circ\text{C}$			
			$V_{CC}(V)$	Min	Typ	Max	Min		Max
V_{IH}	High-level input voltage	$V_o = 0.1V, V_{CC} = 0.1V$ $ I_o = 20\mu A$	2.0	1.5			1.5	V	
			4.5	3.15			3.15		
			6.0	4.2			4.2		
V_{IL}	Low-level input voltage	$V_o = 0.1V, V_{CC} = 0.1V$ $ I_o = 20\mu A$	2.0			0.5		0.5	V
			4.5			1.35		1.35	
			6.0			1.8		1.8	
V_{OH}	High-level output voltage	$V_i = V_{IL}, V_{IH}$	$I_{OH} = -20\mu A$	2.0	1.9			1.9	V
			$I_{OH} = -20\mu A$	4.5	4.4			4.4	
			$I_{OH} = -20\mu A$	6.0	5.9			5.9	
			$I_{OH} = -24mA$	4.5	3.83			3.70	
V_{OL}	Low-level output voltage	$V_i = V_{IH}, V_{IL}$	$I_{OL} = 20\mu A$	2.0			0.1	0.1	V
			$I_{OL} = 20\mu A$	4.5			0.1	0.1	
			$I_{OL} = 20\mu A$	6.0			0.1	0.1	
			$I_{OL} = 24mA$	4.5			0.44	0.53	
I_{IH}	High-level input current	$V_i = 6V$	6.0			0.1	1.0	μA	
I_{IL}	Low-level input current	$V_i = 0V$	6.0			-0.1	-1.0	μA	
I_{OZH}	Off-state high-level output current	$V_i = V_{IH}, V_{IL}, V_o = V_{CC}$	6.0			0.5	5.0	μA	
I_{OZL}	Off-state low-level output current	$V_i = V_{IH}, V_{IL}, V_o = GND$	6.0			-0.5	-5.0	μA	
I_{CC}	Static supply current	$V_i = V_{CC}, GND, I_o = 0\mu A$	6.0			5.0	50.0	μA	

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_a = 25°C)

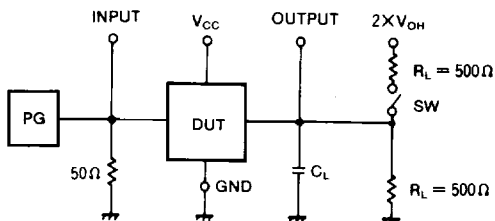
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{TLH}	Low-to high-level and high-to low-level output transition time	C _L = 50pF (Note 4)			10	ns
t _{THL}					10	ns
t _{PLH}			Low-to high-level and high-to low-level output propagation time (A - B, B - A)			16
t _{PHL}				16	ns	
t _{PLZ}	Low-level and high-level output disable time	C _L = 5 pF (Note 4)			25	ns
t _{PHZ}	(OE - A, B)				25	ns
t _{PZL}	Low-level and high-level output enable time	C _L = 50pF (Note 4)			27	ns
t _{PZH}	(OE - A, B)				27	ns

SWITCHING CHARACTERISTICS (V_{CC} = 2~6V, T_a = -40~+85°C)

Symbol	Parameter	Test conditions	Limits					Unit	
			25°C			-40~+85°C			
			V _{CC} (V)	Min	Typ	Max	Min		Max
t _{TLH}	Low-to high-level and high-to low-level output transition time	C _L = 50pF (Note 4)	2.0		17	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t _{THL}			2.0		24	60		75	ns
			4.5		6	12		15	
			6.0		4	10		13	
t _{PLH}	Low-to high-level and high-to low-level output propagation time (A-B, B-A)		2.0		26	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t _{PHL}			2.0		25	85		105	ns
			4.5		9	17		21	
			6.0		7	14		18	
t _{PLZ}	Low-level and high-level output disable time (OE - A, B)		2.0		21	140		175	ns
			4.5		9	28		35	
			6.0		8	24		30	
t _{PHZ}			2.0		24	140		175	ns
			4.5		12	28		35	
			6.0		10	24		30	
t _{PZL}	Low-level and high-level output enable time (OE - A, B)		2.0		35	140		175	ns
			4.5		12	28		35	
			6.0		9	24		30	
t _{PZH}			2.0		36	140		175	ns
			4.5		13	28		35	
			6.0		10	24		30	
C _I	Input capacitance				10		10	pF	
C _O	Off-state output capacitance	OE = V _{CC}			15		15	pF	
C _{PD}	Power dissipation capacitance (Note 3)			53.5				pF	

Note 3 : C_{PD} is the equivalent internal capacitance of the IC calculated from operation supply current under no-load conditions (per transceiver). The power dissipated during operation under no-load condition is calculated using the following formula :
 $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_1 + I_{CC} \cdot V_{CC}$

Note 4 : Test Circuit



Parameter	SW
t _{TLH} , t _{THL}	Open
t _{PLH} , t _{PHL}	Open
t _{PLZ}	Closed
t _{PHZ}	Open
t _{PZL}	Closed
t _{PZH}	Open

- (1) The pulse generator (PG) has the following characteristics (10%~90%) : t_r=3ns, t_f=3ns
- (2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

OCTAL 3-STATE INVERTING AND NONINVERTING BUS TRANSCEIVER

TIMING DIAGRAM

